National Semiconductor

CLC417
Dual Low-Power, Programmable Gain Buffer

General Description

The CLC417 is a dual, low-cost, high-speed (120MHz) buffer which features user-programmable gains of +2, +1, and -1V/V. The CLC417's high 60mA output current, coupled with its ultra-low 39mW per channel power consumption makes it the ideal choice for demanding applications that are sensitive to both power and cost.

Utilizing National's proven architectures, this dual current feedback amplifier surpasses the performance of alternate solutions with a closed-loop design that produces new standards for buffers in gain accuracy, input impedance, and input bias currents. The CLC417's internal feedback network provides an excellent gain accuracy of 0.1%. High source impedance applications will benefit from the CLC417's 6MΩ input impedance along with its exceptionally low 100nA input bias current.

With exceptional gain flatness and low differential gain and phase errors, the CLC417 is very useful for professional video processing and distribution. A 120MHz -3dB bandwidth coupled with a 400V/µs slew rate also make the CLC417 a perfect choice in cost-sensitive applications such as video monitors, fax machines, copiers, and CATV systems. Back-terminated video applications will be enhanced by a gain of +2 configuration which requires no external gain components reducing costs and board space.

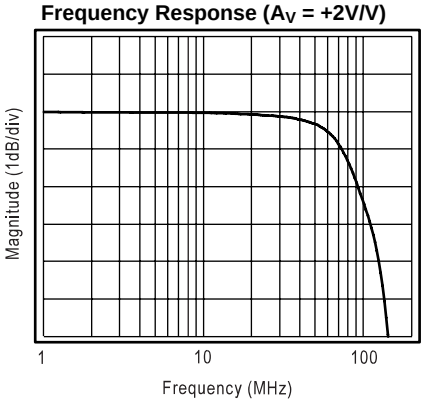
Features

- 0.01%, 0.03° D_G, $D\phi$
- High output current: 60mA
- High input impedance: 6MΩ
- Gains of ±1, +2 with no external components
- Low power
- Very low input bias currents: 100nA
- Excellent gain accuracy: 0.1%
- High speed: 120MHz -3dB BW
- Low-cost

Applications

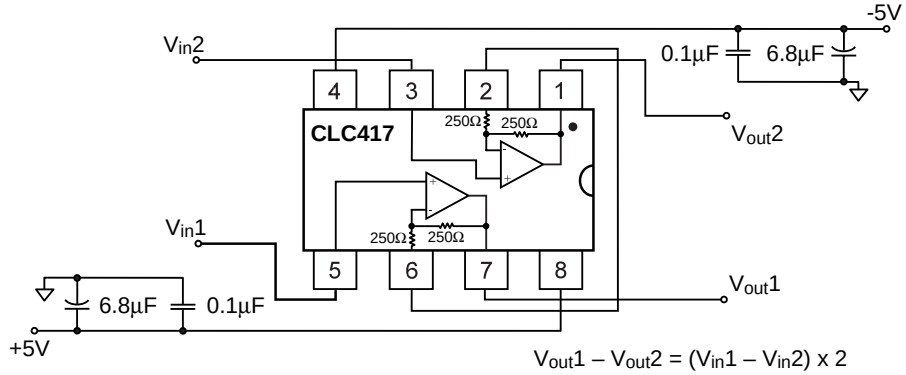
- Desktop video systems
- Video distribution
- Flash A/D driver
- High-speed line driver
- High-source impedance applications
- Professional video processing
- High resolution monitors

Frequency Response (A_V = +2V/V)



Typical Application

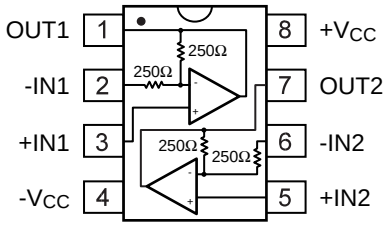
Differential Input/Differential Output Amplifier



$V_{out}1 - V_{out}2 = (V_{in}1 - V_{in}2) \times 2$

Pinout

DIP & SOIC



Printed in the U.S.A.

CLC417 Electrical Characteristics (A_V = +2, V_{cc} = ± 5V, R_L = 100Ω unless specified)

PARAMETERS	CONDITIONS	TYP	MIN/MAX RATINGS			UNITS	NOTES
Ambient Temperature	CLC417AJ	+25°C	+25°C	0 to 70°C	-40 to 85°C		
FREQUENCY DOMAIN RESPONSE							
-3dB bandwidth	V_{out} < 1.0V_{pp}	120	85	65	60	MHz	
	V_{out} < 5.0V_{pp}	52	40	36	35	MHz	1
±0.1dB bandwidth	V_{out} < 1.0V_{pp}	50	15			MHz	
gain flatness	V_{out} < 1.0V_{pp}						
peaking	DC to 200MHz	0	0.5	0.6	0.8	dB	
rolloff	<30MHz	0.05	0.5	0.65	0.7	dB	
linear phase deviation	<20MHz	0.3	0.6	0.7	0.7	deg	
differential gain	4.43MHz, R_L=150Ω	0.01	0.04	0.04	0.04	%	
differential phase	4.43MHz, R_L=150Ω	0.03	0.08	0.11	0.12	deg	
TIME DOMAIN RESPONSE							
rise and fall time	2V step	4.3	6.5	7.2	7.4	ns	
settling time to 0.05%	2V step	22	30	38	41	ns	
overshoot	2V step	3	12	12	12	%	
slew rate A_V = +2	2V step	400	300	260	250	V/µs	
A_V = -1	1V step	700				V/µs	
DISTORTION AND NOISE RESPONSE							
2nd harmonic distortion	2V_{pp}, 1MHz	-80				dBc	
3rd harmonic distortion	2V_{pp}, 1MHz	-80				dBc	
2nd harmonic distortion	2V_{pp}, 10MHz	-66	-55	-50	-47	dBc	
3rd harmonic distortion	2V_{pp}, 10MHz	-57	-50	-47	-46	dBc	
equivalent input noise							
voltage	>1MHz	5	6.3	6.6	6.7	nV/√Hz	
inverting current	>1MHz	12	15	16	17	pA/√Hz	
non-inverting current	>1MHz	3	3.8	4.0	4.2	pA/√Hz	
crosstalk, input referred	2V_{pp}, 10MHz	72	66	66	66	dB	
STATIC DC PERFORMANCE							
input offset voltage		1	5	7	8	mV	A
average drift		30		50	50	µV/°C	
input bias current	non-inverting	100	900	1600	2800	nA	A
average drift		3		8	11	nA/°C	
input bias current	inverting	1	5	6	8	µA	A
average drift		17		40	45	nA/°C	
output offset voltage		2.5	13.3	17.6	19.6	mV	A,2
amplifier gain error		±0.1%	±1.5%	±1.5%	±1.5%	V/V	A
internal resistors (R_f, R_g)		250Ω	±20%				
power supply rejection ratio	DC	52	47	47	45	dB	
common-mode rejection ratio	DC	50	45	45	43	dB	
supply current per channel	R_L= ∞	3.9	4.5	4.6	4.9	mA	A
MISCELLANEOUS PERFORMANCE							
input resistance	non-inverting	6	3	2.4	1	MΩ	
input capacitance	non-inverting	1	2	2	2	pF	
common mode input range		±2.2	±1.8	±1.7	±1.5	V	
output voltage range	R_L= ∞	+4.0,-3.4	+3.9,-3.3	+3.8,-3.2	+3.7,-2.8	V	
output voltage range	R_L= 100Ω	+3.5,-2.9	+3.1,-2.8	+2.9,-2.7	+2.4,-1.7	V	
output current		60	44	38	20	mA	
output resistance, closed loop		0.06	0.2	0.25	0.4	Ω	

Recommended gain range ±1, +2 V/V — Transistor count = 110

Min/max ratings are based on product characterization and simulation. Individual parameters are tested as noted. Outgoing quality levels are determined from tested parameters.

Absolute Maximum Ratings

supply voltage	±7V
I_{out} is short circuit protected to ground	
common-mode input voltage	±Vcc
maximum junction temperature	+175°C
storage temperature range	65°C to +150°C
lead temperature (soldering 10 sec)	+300°C
ESD rating (human body model)	2000V

Notes

1) At temps < 0°C, spec is guaranteed for R_L = 500Ω.
2) Source impedance 1kΩ.
A) J-level: spec is 100% tested at +25°C.

Ordering Information

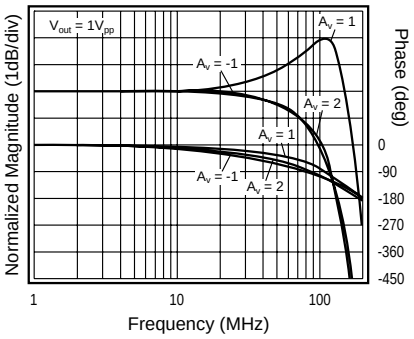
Model	Temperature Range	Description
CLC417AJP	-40°C to +85°C	8-pin PDIP
CLC417AJE	-40°C to +85°C	8-pin SOIC

Package Thermal Resistance

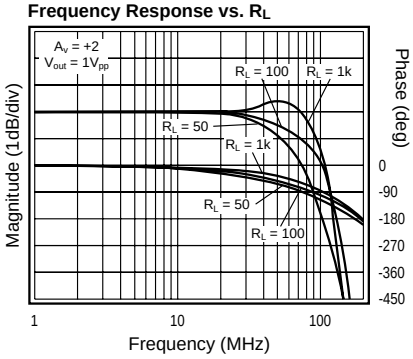
Package	θ_{JC}	θ_{JA}
Plastic (AJP)	80°C/W	95°C/W
Surface Mount (AJE)	95°C/W	115°C/W

CLC417 Typical Performance Characteristics (V_{cc} = ±5V, A_V = +2, R_L = 100Ω; unless specified)

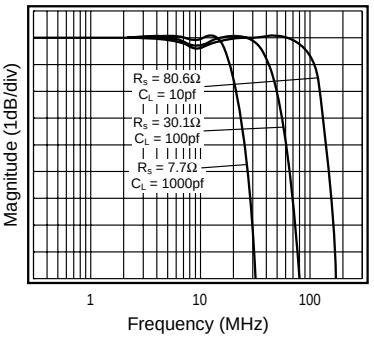
Frequency Response



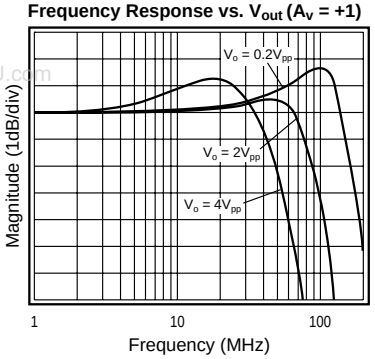
Frequency Response vs. R_L



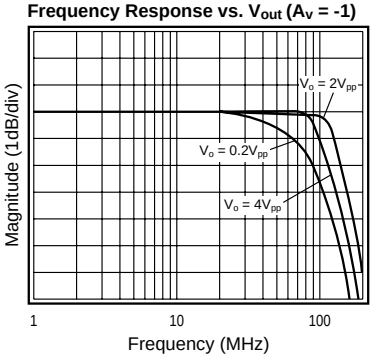
Frequency Response vs. C_L



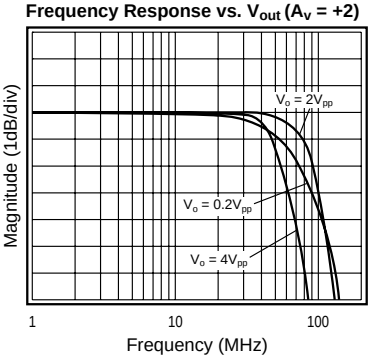
Frequency Response vs. V_{out} (A_V = +1)



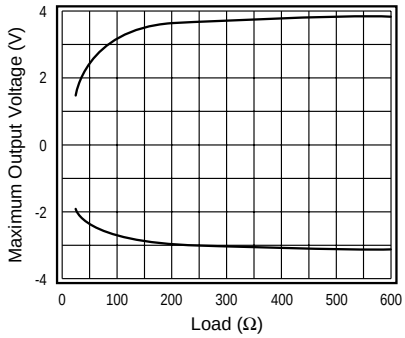
Frequency Response vs. V_{out} (A_V = -1)



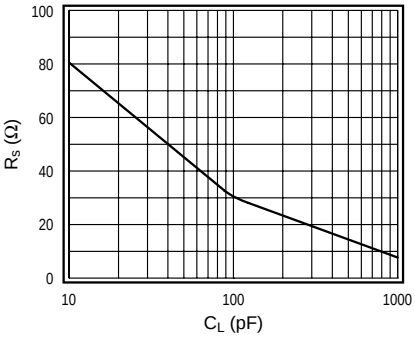
Frequency Response vs. V_{out} (A_V = +2)



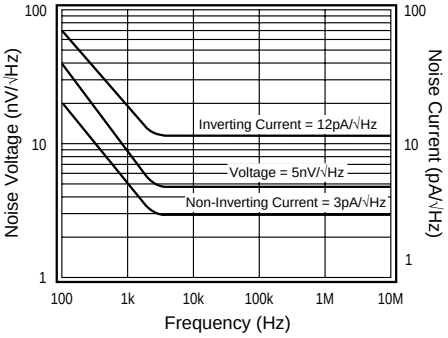
Maximum Output Voltage vs. R_L



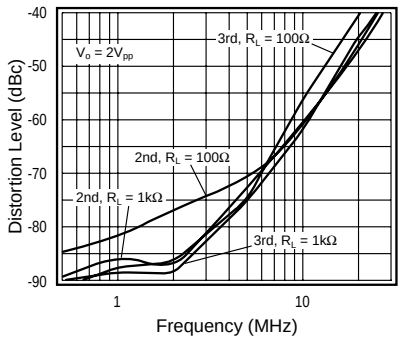
Recommended R_S vs. Capacitive Load



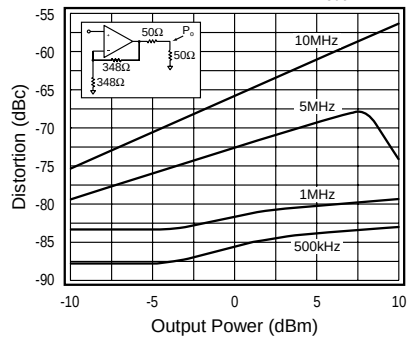
Equivalent Input Noise



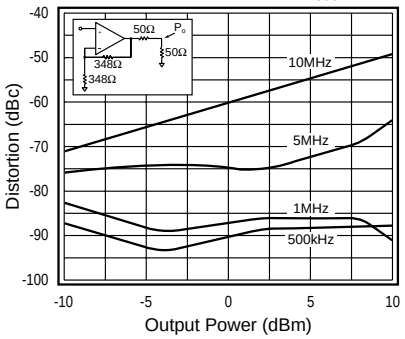
2nd & 3rd Harmonic Distoration



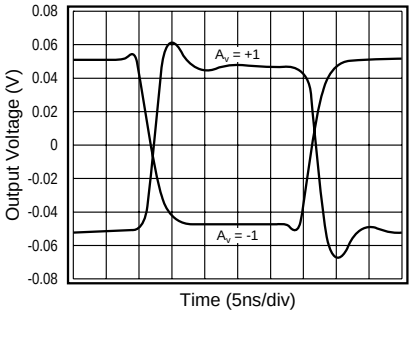
2nd Harmonic Distortion vs. P_{out}



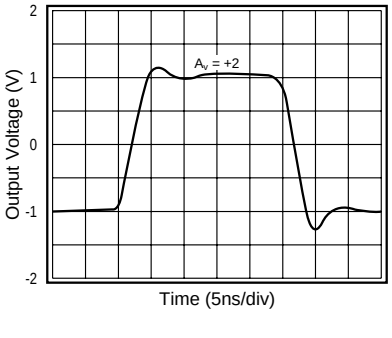
3rd Harmonic Distortion vs. P_{out}



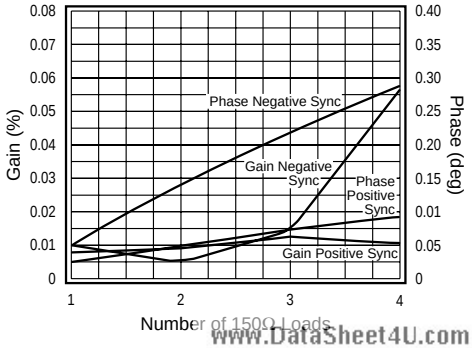
Small Signal Pulse Response



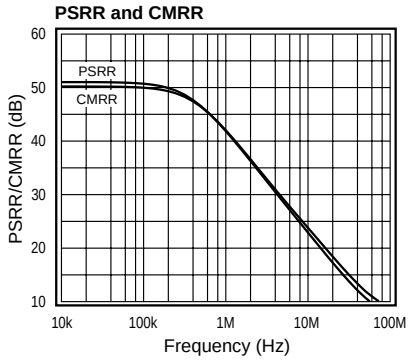
Large Signal Pulse Response

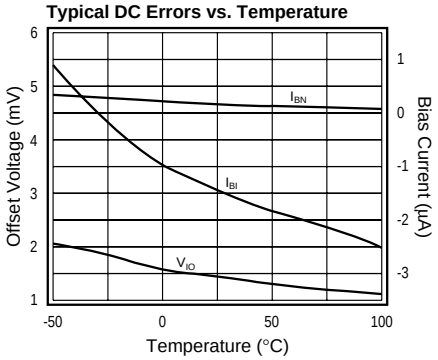


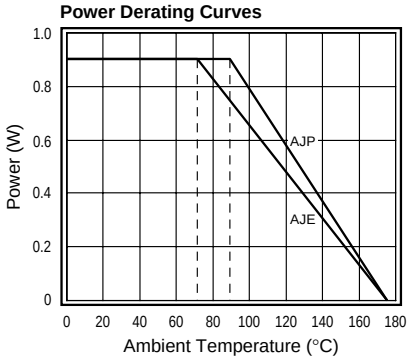
Differential Gain & Phase



CLC417 Typical Performance Characteristics (V_{cc} = ±5V, A_v = +2, R_L = 100Ω; unless specified)







CLC417 OPERATION

Description

The CLC417 is a dual current feedback buffer with the following features:

- Gains of +1, -1, and 2 are achievable without external resistors
- Differential gain and phase errors of 0.01% and 0.03° into a 150Ω load
- Low, 3.9mA, supply current per amplifier

The convenient 8-pin package and internal resistors make common applications, like that seen on the front page, easily feasible in a limited amount of space. The professional video quality differential gain and phase errors and low power capabilities of the CLC417 make this product a good choice for video applications.

If gains other than +1, -1, or +2V/V are required, then the CLC416 can be used. The CLC416 is a dual current feedback amplifier with near identical performance, and allows for external feedback and gain resistors.

Closed Loop Gain Selection

Gains of +1, +2, and -1V/V can be achieved by both of the CLC417's amplifiers. Implement the gain selection by connecting the inverting (-IN) and non-inverting (+IN) pins as described in the table below.

Gain A_v	Input Connections	
	+IN	-IN
-1V/V	ground	input signal
+1V/V	input signal	NC (open)
+2V/V	input signal	ground

The gain accuracy of the CLC417 is excellent and stable over temperature. The internal feedback and gain setting resistors, R_f and R_g, are diffused silicon resistors. R_f and R_g have a process variation of ±20% and a temperature coefficient of ~ 2000ppm/°C. Although the absolute values of R_f and R_g change with processing and temperature, their ratio (R_f/R_g) remains constant. If an external resistor is used in series with R_g, gain accuracy over temperature will be impacted by temperature coefficient differences between internal and external resistors.

Non-Inverting Unity Gain Considerations

Gains of +1V/V are obtained by removing all resistive and capacitive connections between the inverting pins and ground on the CLC417 amplifiers. Too much capacitive coupling between the inverting pin and ground may cause stability problems. Minimize this capacitive coupling by removing the ground plane near the input and output pins. The response labeled ***open*** in Figure 1 is the result of the inverting pin left open and all capacitive coupling removed. A flatter response can be obtained by inserting a resistor between the inverting and non-inverting pins as shown in Figure 2. The two remaining plots in Figure 1 illustrate a 300Ω resistor and a short connected between pins 2 and 3 of the CLC417.

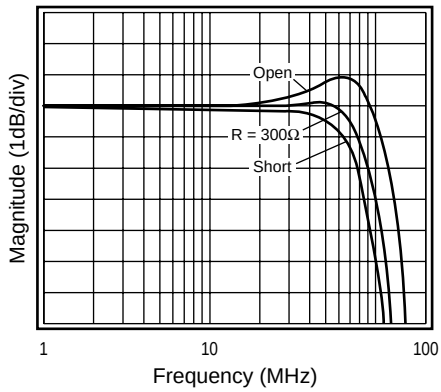
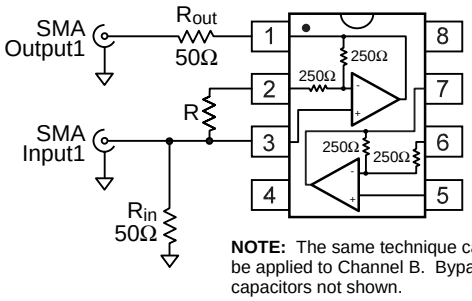


Figure 1: Frequency Response vs. Unity Gain Configuration



NOTE: The same technique can also be applied to Channel B. Bypass capacitors not shown.

Figure 2: Optional Unity Gain Configuration

Channel Matching

Channel matching and crosstalk efficiency are largely dependent on board layout. The layout of National's dual amplifier evaluation boards are optimized to produce maximum channel matching and isolation. Typical channel matching for the CLC417 is shown in Figure 3.

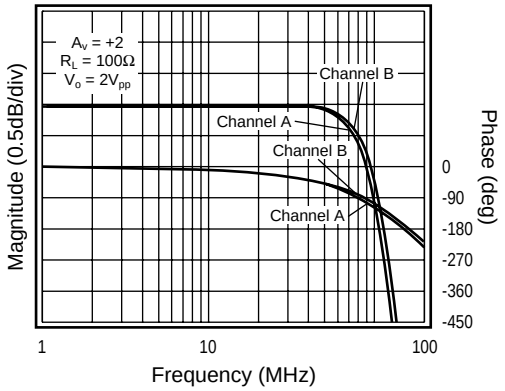


Figure 3: Channel Matching

The CLC417's channel-to-channel isolation is better than 70dB for input frequencies of 4MHz. Input referred crosstalk vs. frequency is illustrated in Figure 4.

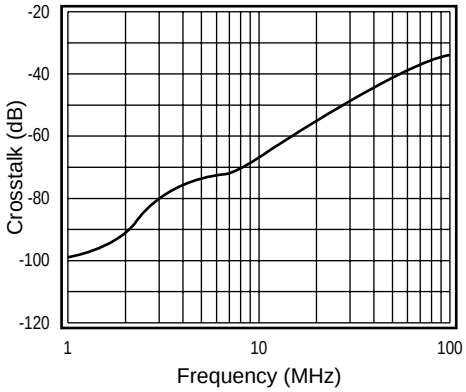


Figure 4: Input Referred Crosstalk vs. Frequency

Driving Cables and Capacitive Loads

When driving cables, double termination is used to prevent reflections. For capacitive load applications, a small series resistor at the output of the CLC417 will improve stability. The ***R_S vs. Capacitive Load*** plot, in the ***Typical Performance*** section, gives the recommended series resistance value for optimum flatness at various capacitive loads.

Power Dissipation

The power dissipation of an amplifier can be described in two conditions:

- Quiescent Power Dissipation - P_Q (No Load Condition)
- Total Power Dissipation - P_T (with Load Condition)

The following steps can be taken to determine the power consumption for each CLC417 amplifier:

1. Determine the quiescent power
   $P_Q = (V_{CC} - V_{EE}) \cdot I_{CC}$
2. Determine the RMS power at the output stage
   $P_O = (V_{CC} - V_{load})\ (I_{load})$, where V_{load} and I_{load} are the RMS voltage and current across the external load.
3. Determine the total RMS power
   $P_T = P_Q + P_O$

Add the total RMS powers for both channels to determine the power dissipated by the dual.

The maximum power that the package can dissipate at a given temperature is illustrated in the ***Power Derating*** curves in the ***Typical Performance*** section. The power derating curve for any package can be derived by utilizing the following equation:

$$P = \frac{(175^\circ - Tamb)}{\theta_{JA}}$$

where: T_{amb} = Ambient temperature (°C)
θ_{JA} = Thermal resistance, from junction to ambient, for a given package (°C/W)

Layout Considerations

A proper printed circuit layout is essential for achieving high frequency performance. National provides evaluation boards for the CLC417 (CLC730038 - DIP, CLC730036 - SOIC) and suggests their use as a guide for high frequency layout and as an aid for device testing and characterization.

Supply bypassing is required for best performance. The bypass capacitors provide a low impedance return current path at the supply pins. They also provide high frequency filtering on the power supply traces. Other layout factors play a major role in high frequency performance. The following are recommended as a basis for high frequency layout:

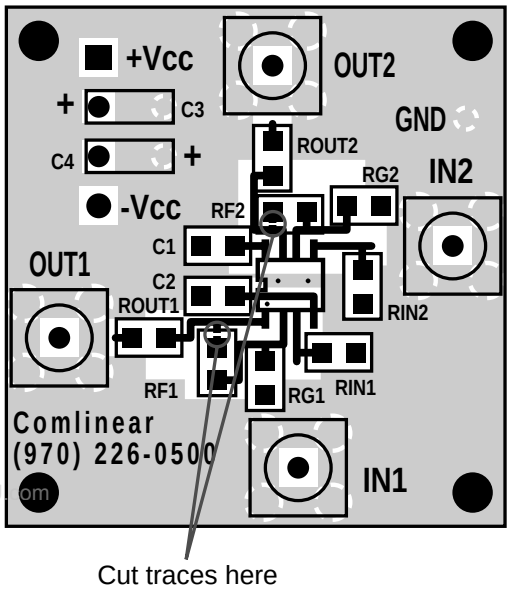
1. Include 6.8µF tantalum and 0.1µF ceramic capacitors on both supplies.
2. Place the 6.8µF capacitors within 0.75 inches of the power pins.
3. Place the 0.1µF capacitors less than 0.1 inches from the power pins.
4. Remove the ground plane near the input and output pins to reduce parasitic capacitance.
5. Minimize all trace lengths to reduce series inductances.

Additional information is included in the evaluation board literature.

Special Evaluation Board Considerations

To optimize off-isolation of the CLC417, cut the R_f trace on both the 730038 and 730036 evaluation boards. This cut minimizes capacitive feedthrough between the input and output. Figure 5 indicates the alterations recommended to improve off-isolation.

730036 Top



730038 Bottom

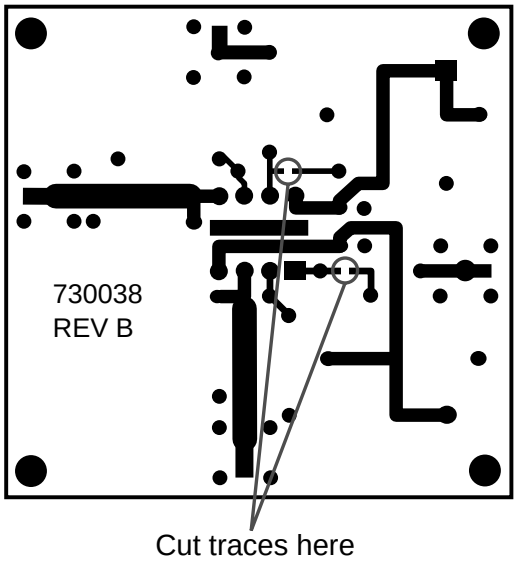


Figure 5: Optional Evaluation Board Alterations

SPICE Models

SPICE models provide a means to evaluate amplifier designs. Free SPICE models are available for National's monolithic amplifiers that:

- Support Berkeley SPICE 2G and its many derivatives
- Reproduce typical DC, AC, Transient, and Noise performance
- Support room temperature simulations

The ***readme*** file that accompanies the diskette lists released models, and provides a list of modeled parameters. The application note OA-18, Simulation SPICE Models for National's Op Amps, contains schematics and a reproduction of the ***readme*** file.

Applications Circuits

Video Cable Driver

The CLC417 was designed to produce exceptional video performance at all three closed-loop gains. A typical cable driving configuration is shown in Figure 6. In this example, the amplifier is configured with a gain of 2.

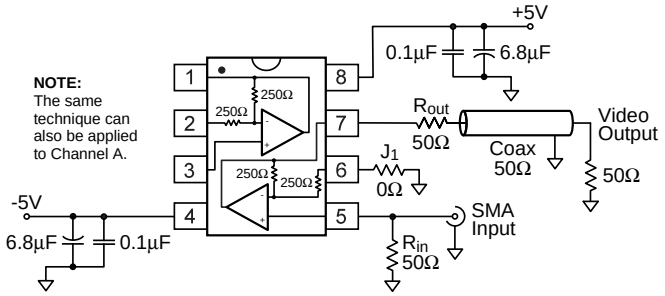


Figure 6: Typical Cable Driver

Single to Differential Line Driver

The topology in Figure 7 accomplishes a single-ended to differential conversion with no external components. With this configuration, the value of Vin is limited to the common mode input range of the CLC417.

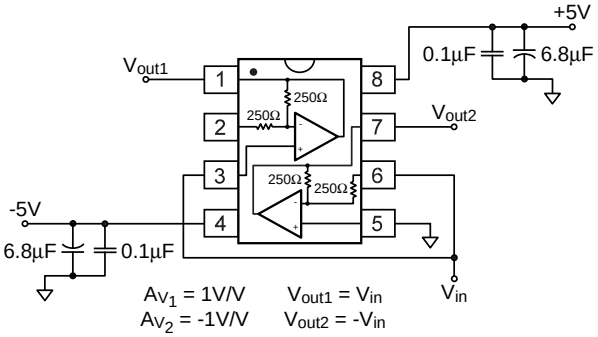


Figure 7: Single to Differential Line Driver

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Customer Design Applications Support

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Life Support Policy

National's products are not authorized for use as critical components in life support devices or systems without the express written approval of the president of National Semiconductor Corporation. As used herein:

1. Life support devices or systems are devices or systems which, a) are intended for surgical implant into the body, or b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.

2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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