

Silicon NPN High-Power Transistor

 \dots designed for general–purpose power amplifier and switching applications.

• Collector-Emitter Sustaining Voltage —

 $V_{CEO(sus)} = 80 \text{ Vdc (Min)}$

• DC Current Gain —

 $h_{FE} = 20 \text{ (Min)} @ I_C = 6.0 \text{ Adc}$

www.DataSheet Low Collector — Emitter Saturation Voltage —

 $V_{CE(sat)} = 1.0 \text{ Vdc (Max)} @ I_C = 7.0 \text{ Adc}$

• High Current — Gain-Bandwidth Product —

 $f_T = 4.0 \text{ MHz (Min)} @ I_C = 1.0 \text{ Adc}$

MAXIMUM RATINGS (1)

Rating	Symbol	Max	Unit
Collector–Emitter Voltage	V _{CEO}	80	Vdc
Collector–Base Voltage	V_{CB}	80	Vdc
Emitter–Base Voltage	V _{EB}	5.0	Vdc
Collector Current — Continuous Peak	Ic	15 30	Adc
Base Current	Ι _Β	5.0	Adc
Total Device Dissipation @ T _C = 25°C Derate above 25°C	P _D	160 0.915	Watts W/°C
Operating and Storage Junction Temperature Range	T _J , T _{stg}	-65 to +200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	1.1	°C/W

(1) Indicates JEDEC registered data. Units and conditions differ on some parameters and re-registration reflecting these changes has been requested. All above values meet or exceed present JEDEC registered data.

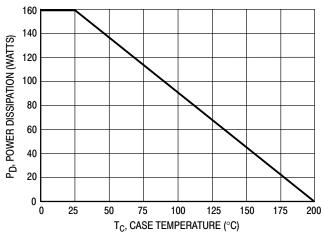


Figure 1. Power Derating

Preferred devices are ON Semiconductor recommended choices for future use and best overall value.

2N5882

ON Semiconductor Preferred Device

15 AMPERE
SILICON
POWER TRANSISTOR
80 VOLTS
160 WATTS

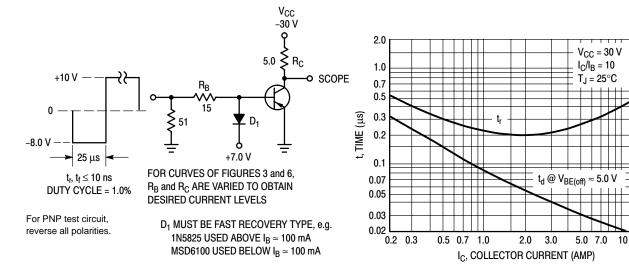


CASE 1-07 TO-204AA (TO-3)

*ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Sustaining Vo (I _C = 200 mAdc, I _B = 0)	oltage (2)	V _{CEO(sus)}	80	_	Vdc
Collector Cutoff Current $(V_{CE} = 40 \text{ Vdc}, I_B = 0)$		ICEO	_	1.0	mAdc
Collector Cutoff Current $(V_{CE} = 80 \text{ Vdc}, V_{BE(off)} = 1.5 \text{ Vdc})$ $(V_{CE} = 80 \text{ Vdc}, V_{BE(off)} = 1.5 \text{ Vdc}, T_{C} = 150^{\circ}\text{C})$		_ _	0.5 5.0	mAdc	
Collector Cutoff Current I_{CBO} $(V_{CB} = 80 \text{ Vdc}, I_E = 0)$		_	0.5	mAdc	
Emitter Cutoff Current (V _{EB} = 5.0 Vdc, I _C = 0)		I _{EBO}		1.0	mAdc
ON CHARACTERISTICS					
DC Current Gain (1) ($I_C = 2.0 \text{ Adc}, V_{CE} = 4.0 \text{ Vdc}$) ($I_C = 6.0 \text{ Adc}, V_{CE} = 4.0 \text{ Vdc}$) ($I_C = 15 \text{ Adc}, V_{CE} = 4.0 \text{ Vdc}$)		h _{FE}	35 20 4.0	— 100 —	_
Collector–Emitter Saturation Vo ($I_C = 7.0$ Adc, $I_B = 0.7$ Adc) ($I_C = 15$ Adc, $I_B = 3.75$ Adc)	Itage (2)	V _{CE(sat)}	_ _	1.0 4.0	Vdc
Base–Emitter Saturation Voltage (1) (I _C = 15 Adc, I _B = 3.75 Adc)		V _{BE(sat)}	_	2.5	Vdc
Base–Emitter On Voltage (2) (I _C = 6.0 Adc, V _{CE} = 4.0 Vdc)		V _{BE(on)}	_	1.5	Vdc
DYNAMIC CHARACTERISTICS					
Current–Gain — Bandwidth Product (3) (I _C = 1.0 Adc, V _{CE} = 10 Vdc, f _{test} = 1.0 MHz)		f _T	4.0	_	MHz
Output Capacitance (V _{CB} = 10 Vdc, I _E = 0, f = 100 kHz)		C _{ob}	_	400	pF
Small–Signal Current Gain (I _C = 2.0 Adc, V _{CE} = 4.0 Vdc, f = 1.0 kHz)		h _{fe}	20	_	_
SWITCHING CHARACTERISTIC	cs				
Rise Time	0/ 00 // 1 00 / 1	t _r	_	0.7	μs
Storage Time	$(V_{CC} = 30 \text{ Vdc}, I_C = 6.0 \text{ Adc},$	t _s	_	1.0	us

Fall Time



 $I_{B1} = I_{B2} = 0.6$ Adc See Figure 2)

Figure 2. Switching Times Test Circuit

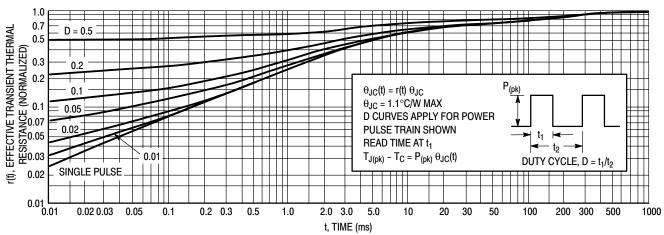
Figure 3. Turn-On Time

8.0

μs

^{*}Indicates JEDEC Registered Data. (2) Pulse Test: Pulse Width $\leq 300 \,\mu\text{s}$, Duty Cycle $\leq 2.0\%$

⁽³⁾ $f_T = |h_{fe}| \cdot f_{test}$.



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Figure 4. Thermal Response

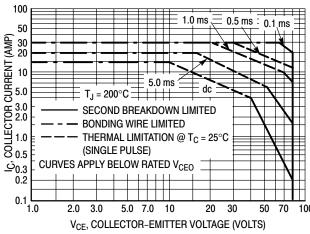


Figure 5. Active-Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 200^{\circ}C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} < 200^{\circ}C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

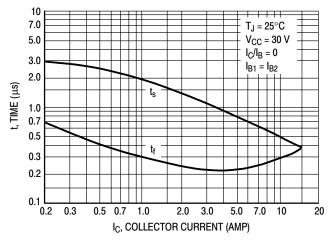


Figure 6. Turn-Off Time

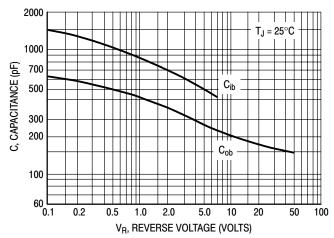
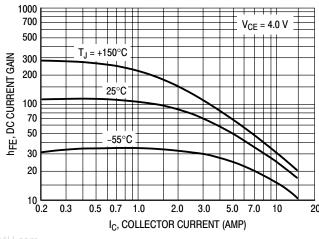
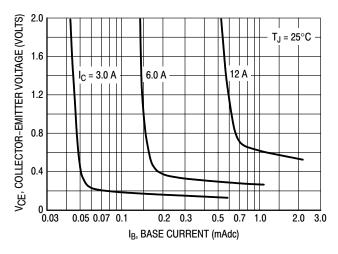


Figure 7. Capacitance





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Figure 8. DC Current Gain

Figure 9. Collector Saturation Region

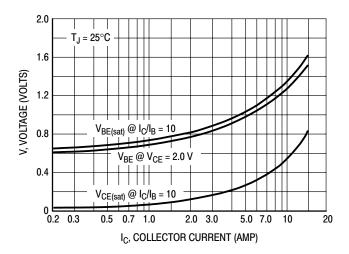
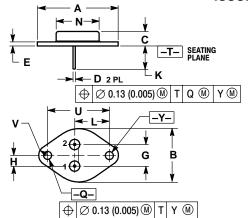


Figure 10. "On" Voltage

PACKAGE DIMENSIONS

CASE 1-07 TO-204AA (TO-3) ISSUE Z



NOTES:

- (OLES: 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982. 2. CONTROLLING DIMENSION: INCH. 3. ALL RULES AND NOTES ASSOCIATED WITH REFERENCED TO-204AA OUTLINE SHALL APPLY.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
Α	1.550 REF		39.37 REF	
В		1.050		26.67
С	0.250	0.335	6.35	8.51
D	0.038	0.043	0.97	1.09
E	0.055	0.070	1.40	1.77
G	0.430 BSC		10.92 BSC	
Н	0.215 BSC		5.46 BSC	
K	0.440	0.480	11.18	12.19
L	0.665 BSC		16.89 BSC	
N		0.830		21.08
Q	0.151	0.165	3.84	4.19
U	1.187 BSC		30.15 BSC	
٧	0.131	0.188	3.33	4.77

STYLE 1: PIN 1. BASE 2. EMITTER CASE: COLLECTOR

Notes

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Notes

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