AK4526A
High Performance Multi-channel Audio CODEC

GENERAL DESCRIPTION

The AK4526A is a single chip CODEC that includes two channels of ADC and six channels of DAC. The ADC outputs 20bit data and the DAC accepts up to 24bit input data. The ADC has an enhanced dual bit architecture with wide dynamic range. The DAC achieves low outband noise and high jitter tolerance by use of SCF(switched capacitor filter) techniques. An auxiliary digital audio input interface maybe used instead of the ADC for passing audio data to the primary audio output port. Control may be set directly by pins or programmed through a separate serial interface.

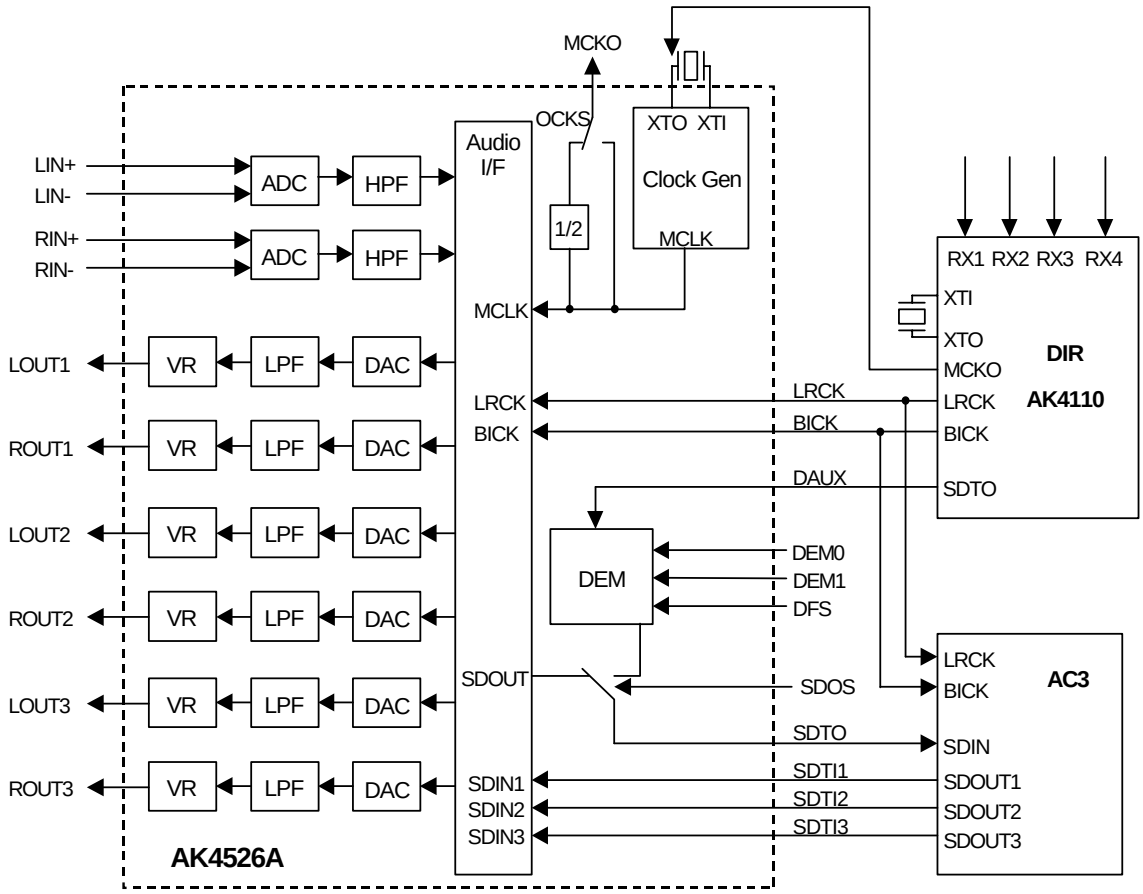
The AK4526A has a dynamic range of 100dB and is well suited for digital surround for home theater and car audio. An AC-3 system can be built with a IEC958(SPDIF) receiver such as the AK4110. The AK4526A is available in a small 44pin LQFP package which will reduce system space.

*AC-3 is a trademark of Dolby Laboratories.

FEATURES

- **2ch ADC with 20bit data output capability**
  - **64x Oversampling**
  - **Sampling Rate up to 48kHz**
  - **Differential Inputs with single-ended use capability**
  - **S/(N+D): 92dB**
  - **Dynamic Range, S/N: 100dB**
  - **Digital HPF for offset cancellation**
  - **I/F format: MSB justified or I^2S**
- **6ch DAC with 24bit data input capability**
  - **128x Oversampling**
  - **Sampling Rate up to 96kHz**
  - **Single-Ended Outputs**
  - **2nd order SCF**
  - **S/(N+D): 90dB**
  - **Dynamic Range: 100dB**
  - **S/N: 100dB, 108dB(Mute)**
  - **I/F format: MSB justified, LSB justified or I^2S**
  - **Individual attenuation control with 21 levels and 1dB step**
- **De-emphasis for 32kHz, 44.1kHz, 48kHz and 96kHz**
- **High Jitter Tolerance**
- **TTL Level Digital I/F**
- **Serial uP I/F for mode setting**
- **Master clock: 256fs, 384fs or 512fs for fs=32kHz to 48kHz**
  128fs, 192fs or 256fs for fs=96kHz
- **Power Supply: 4.5 to 5.5V**
- **Small 44pin LQFP**

■ Block Diagram

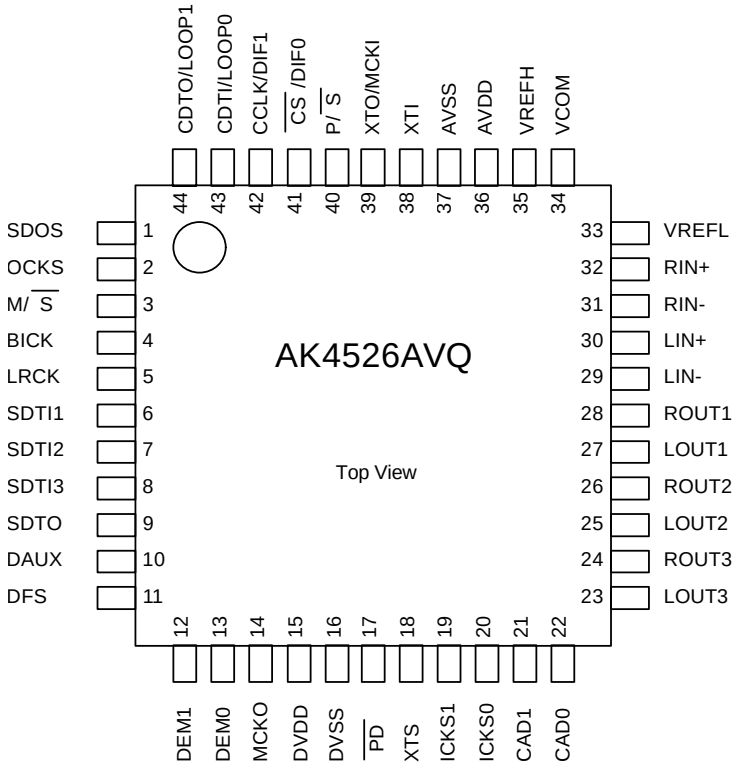


Block Diagram (DIR and AC-3 DSP are external parts)

■ Ordering Guide

AK4526AVQ	-10 ~ +70°C	44pin LQFP (0.8mm pitch)
AKD4526A	Evaluation Board for AK4526A	

■ Pin Layout



PIN/FUNCTION

No.	Pin Name	I/O	Function
1	SDOS	I	SDTO Source Select Pin "L": Internal ADC output, "H": DAUX input ORed with serial control register if P/$\overline{S}$ ="L".
2	OCKS	I	MCKO Clock Frequency Select Pin "L": MCLK, "H": MCLK/2 ORed with serial control register if P/$\overline{S}$ ="L".
3	M/$\overline{S}$	I	Audio Data Master/Slave Mode Select Pin "L": Slave mode, "H": Master mode
4	BICK	I/O	Audio Serial Data Clock Pin
5	LRCK	I/O	Input/Output Channel Clock Pin
6	SDTI1	I	DAC1 Audio Serial Data Input Pin
7	SDTI2	I	DAC2 Audio Serial Data Input Pin
8	SDTI3	I	DAC3 Audio Serial Data Input Pin
9	SDTO	O	Audio Serial Data Output Pin
10	DAUX	I	AUX Audio Serial Data Input Pin
11	DFS	I	Double Speed Sampling Mode Pin "L": Normal Speed, "H": Double Speed, the ADC is powered down. ORed with serial control register if P/$\overline{S}$ ="L".
12	DEM1	I	De-emphasis Pin ORed with serial control register if P/$\overline{S}$ ="L".
13	DEM0	I	De-emphasis Pin ORed with serial control register if P/$\overline{S}$ ="L".
14	MCKO	O	Master Clock Output Pin
15	DVDD	-	Digital Power Supply Pin
16	DVSS	-	Digital Ground Pin
17	$\overline{PD}$	I	Power-Down & Reset Pin When "L", the AK4526A is powered down and the control registers are reset to default state. If the state of P/$\overline{S}$, M/$\overline{S}$, CAD0-1 changes, then the AK4526A must be reset by $\overline{PD}$.
18	XTS	I	X'tal oscillator Select/Test Mode Pin "H": X'tal Oscillator selected "L": External clock source selected
19	ICKS1	I	Input Clock Select 1 Pin
20	ICKS0	I	Input Clock Select 0 Pin
21	CAD1	I	Chip Address Pin Used during the serial control mode.
22	CAD0	I	Chip Address Pin Used during the serial control mode.
23	LOUT3	O	Lch #3 Analog Output Pin
24	ROUT3	O	Rch #3 Analog Output Pin
25	LOUT2	O	Lch #2 Analog Output Pin
26	ROUT2	O	Rch #2 Analog Output Pin
27	LOUT1	O	Lch #1 Analog Output Pin
28	ROUT1	O	Rch #1 Analog Output Pin
29	LIN-	I	Lch Analog Negative Input Pin
30	LIN+	I	Lch Analog Positive Input Pin
31	RIN-	I	Rch Analog Negative Input Pin
32	RIN+	I	Rch Analog Positive Input Pin

No.	Pin Name	I/O	Function
33	VREFL	I	Negative Voltage Reference Input Pin, AVSS
34	VCOM	O	Common Voltage Output Pin, AVDD/2 Large external capacitor is used to reduce power-supply noise.
35	VREFH	I	Positive Voltage Reference Input Pin, AVDD
36	AVDD	-	Analog Power Supply Pin
37	AVSS	-	Analog Ground Pin
38	XTI	I	X'tal Input Pin
39	XTO	O	X'tal Output Pin if XTS="H"
	MCKI	I	External Master Clock Input Pin if XTS="L"
40	P/$\overline{S}$	I	Parallel/Serial Select Pin "L": Serial control mode, "H": Parallel control mode
41	DIF0	I	Audio Data Interface Format Pin in parallel mode
	$\overline{CS}$	I	Chip Select Pin in serial mode
42	DIF1	I	Audio Data Interface Format Pin in parallel mode
	CCLK	I	Control Data Clock Pin in serial mode
43	LOOP0	I	Loopback Mode Pin in parallel mode Enables digital loop-back from ADC to 3 DACs.
	CDTI	I	Control Data Input Pin in serial mode
44	LOOP1	I	Loopback Mode Pin in parallel mode Enables all 3 DAC channels to be input from SDTI1.
	CDTO	O	Control Data Output Pin in serial mode

If pins XTS, ICKS0, ICKS1, $\overline{PD}$, P/$\overline{S}$, DFS, DEM0, DEM1, CAD0, CAD1, M/$\overline{S}$, OCKS, SDOS are not driven, then XTS, ICKS0,ICKS1, CAD0, CAD1 must be tied to either AVSS or AVDD. $\overline{PD}$, P/$\overline{S}$, DFS, DEM0, DEM1, M/$\overline{S}$, OCKS, SDOS must be tied to either DVSS or DVDD.

ABSOLUTE MAXIMUM RATINGS

(AVSS, DVSS=0V; Note 1)

Parameter		Symbol	min	max	Units
Power Supplies	Analog	AVDD	-0.3	6.0	V
	Digital	DVDD	-0.3	6.0	V
	|AVSS-DVSS| (Note 2)	ΔGND	-	0.3	V
Input Current (any pins except for supplies)		IIN	-	±10	mA
Analog Input Voltage		VINA	-0.3	AVDD+0.3	V
Digital Input Voltage		VIND	-0.3	DVDD+0.3	V
Ambient Temperature (power applied)		Ta	-10	70	°C
Storage Temperature		Tstg	-65	150	°C

Note:1. All voltages with respect to ground.
2. AVSS and DVSS must be same voltage level.

WARNING: Operation at or beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS

(AVSS, DVSS=0V; Note 1)

Parameter		Symbol	min	typ	max	Units
Power Supplies	Analog	AVDD	4.5	5.0	5.5	V
(Note 3)	Digital	DVDD	4.5	5.0	5.5	V

Note:1. All voltages with respect to ground.
3. The power up sequence between AVDD and DVDD is not critical.

*AKM assumes no responsibility for the usage beyond the conditions in this datasheet.

ANALOG CHARACTERISTICS

(Ta=25°C; AVDD, DVDD=5V; AVSS, DVSS=0V; VREFH=AVDD, VREFL=AVSS; fs=44.1kHz;
Signal Frequency =1kHz; 20bit Data; Measurement Frequency=10Hz ~ 20kHz; unless otherwise specified)

Parameter		min	typ	max	Units
ADC Analog Input Characteristics: Differential Inputs; Analog Source Impedance=470Ω					
Resolution				20	Bits
S/(N+D) (-0.5dB Input) (Note 4)		84	92		dB
DR (-60dB Input, A-Weighted)		94	100		dB
S/N (A-Weighted) (Note 5)		94	100		dB
Interchannel Isolation		90	110		dB
DC Accuracy					
Interchannel Gain Mismatch			0.2	0.3	dB
Gain Drift			20	-	ppm/°C
Input Voltage AIN=0.6x(VREFH-VREFL) (Note 6)		2.85	3.0	3.15	Vpp
Input Resistance		20	30		kΩ
Power Supply Rejection (Note 7)			50		dB
DAC Analog Output Characteristics:					
Resolution				24	Bits
S/(N+D)	fs=44.1kHz	80	90		dB
	fs=96kHz	78	88		dB
DR (-60dB Output, A-Weighted)	fs=44.1kHz	95	100		dB
	fs=96kHz	94	100		dB
S/N (A-Weighted) (Note 5)	fs=44.1kHz	95	100		dB
(Note 8)	fs=96kHz	94	100		dB
Interchannel Isolation		90	110		dB
DC Accuracy					
Interchannel Gain Mismatch			0.2	0.5	dB
Gain Drift			20	-	ppm/°C
Output Voltage AOUT=0.6x(VREFH-VREFL)		2.75	3.0	3.25	Vpp
Load Resistance		5			kΩ
Power Supply Rejection (Note 7)			50		dB
Output Volume					
Step Size		0	1		dB
Attenuation Control Range		-20		0	dB
Power Supplies					
Power Supply Current (AVDD+DVDD)					
Normal Operation ($\overline{PD}$ ="H")					
DFS="L" (Note 9)			113	157	mA
Power-down mode ($\overline{PD}$ ="L")					
XTS="L" (Note 10)			1	2	mA

Note: 4. In case of single ended input, S/(N+D)=83dB(typ, @AVDD=5V).
5. S/N measured by CCIR-ARM is 96dB at each converter and 94dB at ADC to DAC loopback.
6. Full scale input for each AIN+/- pin is 1.5Vpp in differential mode.
7. PSR is applied to AVDD, DVDD with 1kHz, 50mVpp. VREFH/VREFL pin is held a constant voltage.
8. DR and S/N at BW=40kHz are typically 93dB.
9. Typically, AVDD=90mA, DVDD=23mA. When DFS="H", AVDD=76mA and DVDD=22mA.
10. All digital input pins are held DVDD or DVSS. When XTS="H", typically 15mA.

FILTER CHARACTERISTICS (fs=44.1kHz)

(Ta=25°C; AVDD, DVDD=4.5 ~ 5.5V; DEM=OFF)

Parameter		Symbol	min	typ	max	Units
ADC Digital Filter (Decimation LPF):						
Passband (Note 11)	-0.005dB	PB	0		19.76	kHz
	-0.02dB		0		20.02	kHz
	-0.06dB		0		20.20	kHz
	-6.0dB		0		22.05	kHz
Stopband		SB	24.34			kHz
Passband Ripple		PR			±0.005	dB
Stopband Attenuation		SA	80			dB
Group Delay (Note 12)		GD		29.3		1/fs
Group Delay Distortion		ΔGD		0		us
ADC Digital Filter (HPF):						
Frequency Response (Note 11)	-3dB	FR		0.9		Hz
	-0.5dB			2.7		Hz
	-0.1dB			6.0		Hz
DAC Digital Filter:						
Passband (Note 11)	-0.06dB	PB	0		20.0	kHz
	-6.0dB		0		22.05	kHz
Stopband		SB	24.1			kHz
Passband Ripple		PR			±0.06	dB
Stopband Attenuation		SA	43			dB
Group Delay (Note 12)		GD		14.7		1/fs
DAC Digital Filter + Analog Filter:						
Frequency Response: 0 ~ 20.0kHz		FR	-	±0.2	-	dB

Notes: 11. The passband and stopband frequencies scale with fs.
For example, 20.02kHz at –0.02dB is 0.454 x fs. The reference frequency of these responses is 1kHz.

12. The calculating delay time which occurred by digital filtering. This time is from setting the input of analog signal to setting the 20bit data of both channels to the output register for ADC.
For DAC, this time is from setting the 20/24bit data of both channels on input register to the output of analog signal.

FILTER CHARACTERISTICS (fs=96kHz)

(Ta=25°C; AVDD, DVDD=4.5 ~ 5.5V; DEM=OFF)

Parameter		Symbol	min	typ	max	Units
DAC Digital Filter:						
Passband (Note 13)	-0.06dB	PB	0		43.5	kHz
	-6.0dB		0		48.0	kHz
Stopband		SB	52.5			kHz
Passband Ripple		PR			±0.06	dB
Stopband Attenuation		SA	43			dB
Group Delay (Note 12)		GD		14.7		1/fs
DAC Digital Filter + Analog Filter:						
Frequency Response: 0 ~ 20.0kHz		FR		±0.2		dB
40kHz		FR		-2		dB

Note:13. The passband and stopband frequencies scale with fs.
The reference frequency of these responses is 1kHz.

DIGITAL CHARACTERISTICS

(Ta=25°C; AVDD, DVDD=4.5 ~ 5.5V)

Parameter	Symbol	min	typ	max	Units
High-Level Input Voltage (XTS pin)	VIH1	90%DVDD	-	-	V
(All pins except XTS pin)	VIH2	2.2	-	-	V
Low-Level Input Voltage (XTS pin)	VIL1	-	-	10%DVDD	V
(All pins except XTS pin)	VIL2	-	-	0.8	V
Hight-Level Output Voltage (Iout= -1mA)	VOH	DVDD-0.4	-	-	V
Low-Level Output Voltage (Iout= 1mA)	VOL	-	-	0.4	V
Input Leakage Current	Iin	-	-	±10	uA

SWITCHING CHARACTERISTICS

(Ta=25°C; AVDD, DVDD=4.5 ~ 5.5V; C_L=20pF)

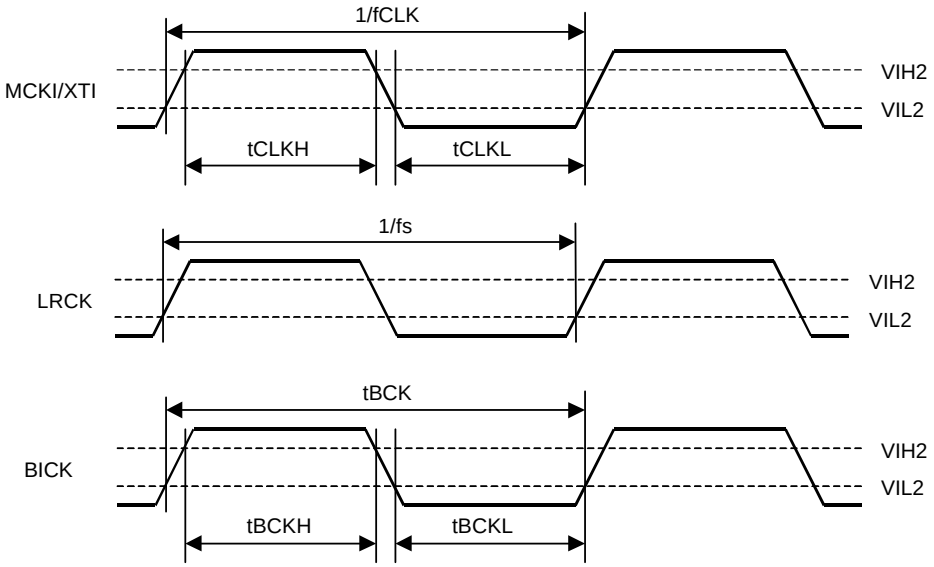
Parameter		Symbol	min	typ	max	Units
Master Clock Input	256fs:	fCLK	8.192		12.288	MHz
	Pulse Width Low	tCLKL	27			ns
	Pulse Width High	tCLKH	27			ns
	384fs:	fCLK	12.288		18.432	MHz
	Pulse Width Low	tCLKL	20			ns
	Pulse Width High	tCLKH	20			ns
	512fs:	fCLK	16.384		24.576	MHz
	Pulse Width Low	tCLKL	15			ns
	Pulse Width High	tCLKH	15			ns
MCKO Output	Frequency	fMCK	4.096		24.576	MHz
	Duty (XTS="H")	dMCK	40	50	60	%
LRCK frequency						
DAC Normal Speed Mode (DFS="0")		fsn	32		48	kHz
DAC Double Speed Mode (DFS="1")		fsd	64		96	kHz
Duty Cycle		Duty	45		55	%
Audio Interface Timing						
Slave mode						
BICK Period		tBCK	160			ns
BICK Pulse Width Low		tBCKL	65			ns
Pulse Width High		tBCKH	65			ns
LRCK Edge to BICK "↑"	(Note 14)	tLRB	45			ns
BICK "↑" to LRCK Edge	(Note 14)	tBLR	45			ns
LRCK to SDTO(MSB)		tLRS			40	ns
BICK "↓" to SDTO		tBSD			50	ns
SDTI Hold Time		tSDH	40			ns
SDTI Setup Time		tSDS	25			ns
Master mode						
BICK Frequency		fBCK		64fs		Hz
BICK Duty		dBCK		50		%
BICK "↓" to LRCK		tMBLR	-20		20	ns
BICK "↓" to SDTO		tBSD			50	ns
SDTI Hold Time		tSDH	40			ns
SDTI Setup Time		tSDS	25			ns

Note 14. BICK rising edge must not occur at the same time as LRCK edge.

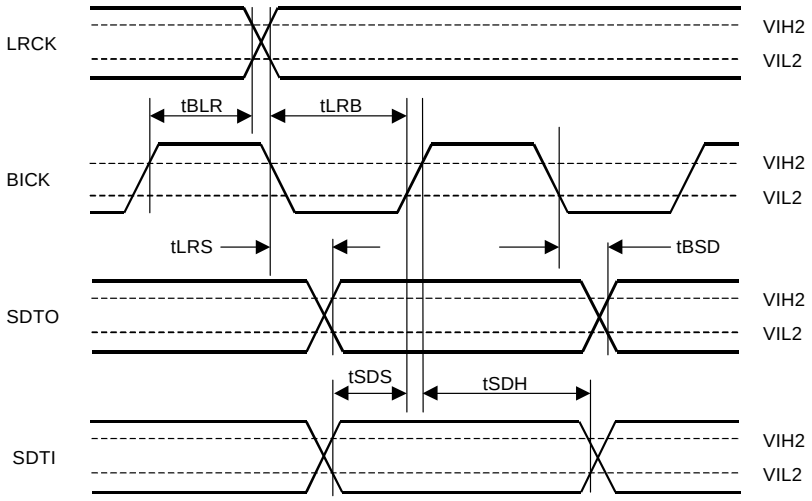
Parameter	Symbol	min	typ	max	Units
Control Interface Timing					
CCLK Period	tCCK	200			ns
CCLK Pulse Width Low	tCCKL	80			ns
Pulse Width High	tCCKH	80			ns
CDTI Setup Time	tCDS	40			ns
CDTI Hold Time	tCDH	40			ns
$\overline{CS}$ "H" Time	tCSW	150			ns
$\overline{CS}$ "↓" to CCLK "↑"	tCSS	50			ns
CCLK "↑" to $\overline{PD}$ "↑"	tCSH	50			ns
CCLK "↓" to CDTO valid	tDCD			45	ns
$\overline{CS}$ "↑" to CDTO Hi-Z	tCCZ			70	ns
Rise Time of $\overline{CS}$	tR1			20	ns
Fall Time of $\overline{CS}$	tF1			20	ns
Rise Time of CCLK	tR2			20	ns
Fall Time of CCLK	tF2			20	ns
Reset Timing					
$\overline{PD}$ Pulse Width (Note 15)	tPD	150			ns
$\overline{PD}$ "↑" to SDTO valid (Note 16)	tPDV		516		1/fs

Note:15. The AK4526A can be reset by bringing $\overline{PD}$ "L" to "H" only upon power-up.
When X'tal mode(XTS="H"), at power-up, $\overline{PD}$ should be held "L" for 5ms to allow the X'tal oscillation to begin.
16. These cycles are the number of LRCK rising from $\overline{PD}$ rising.

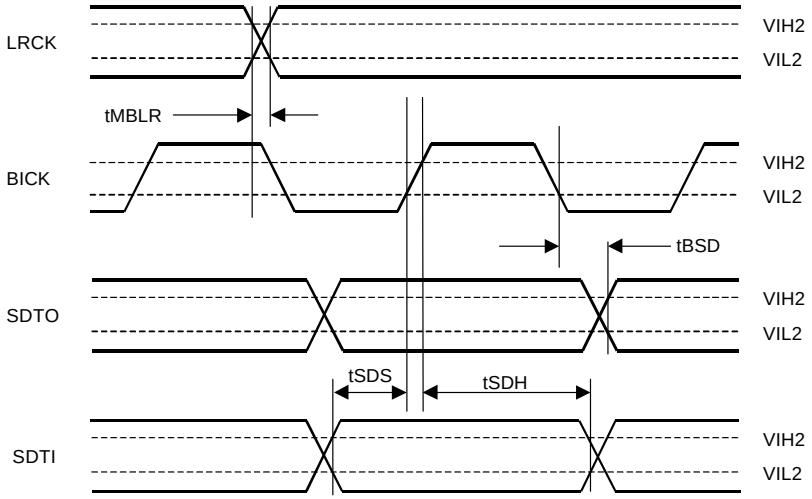
■ Timing Diagram



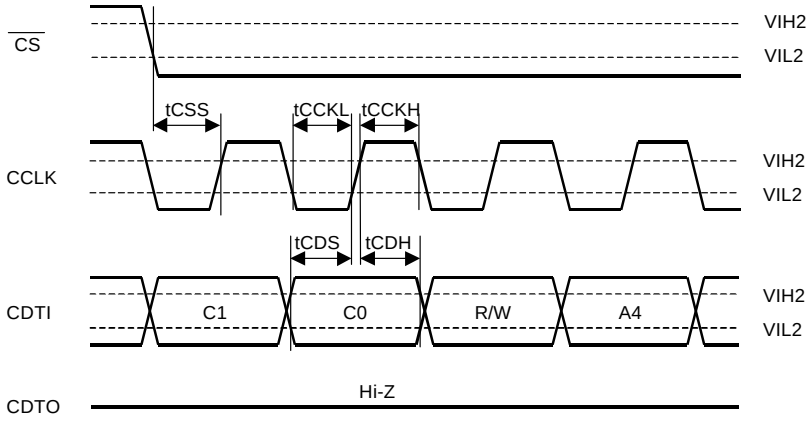
Clock Timing



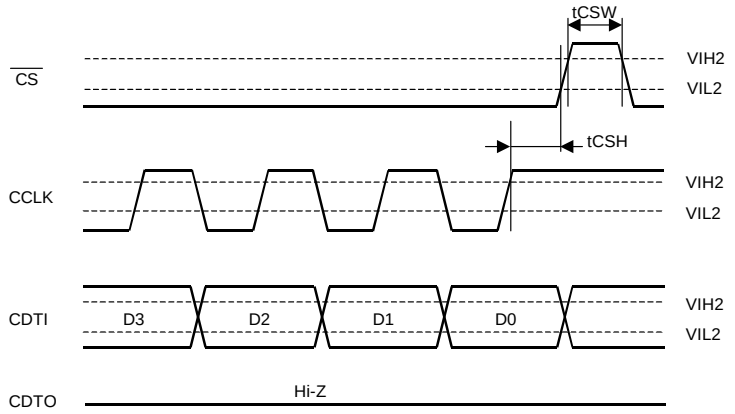
Audio Interface Timing (Slave mode)



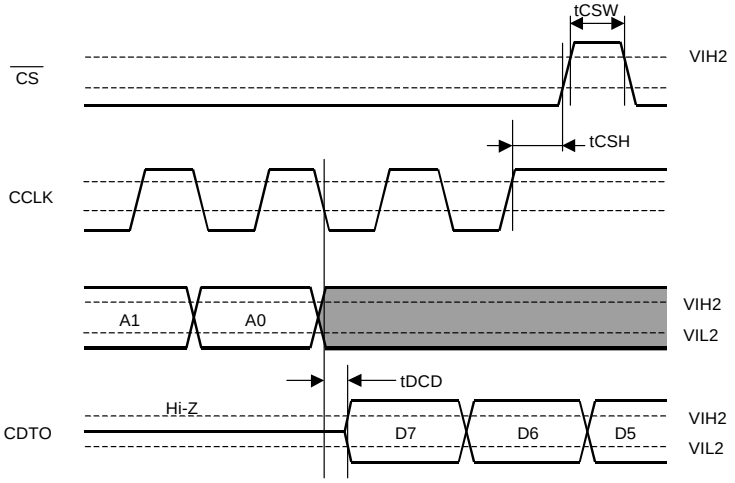
Audio Interface Timing (Master mode)

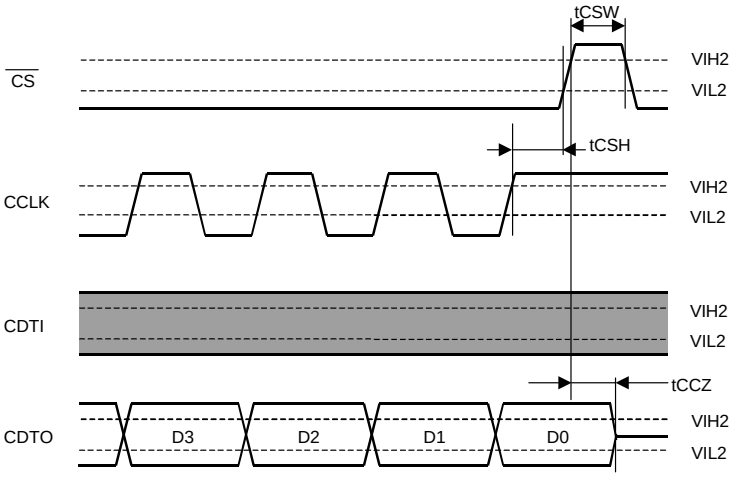


WRITE/READ Command Input Timing

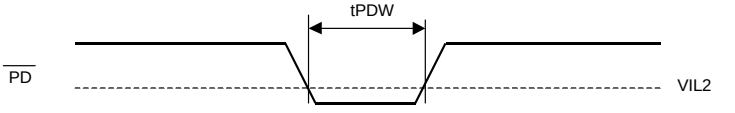


WRITE Data Input Timing





READ Data Output Timing 2



Power Down & Reset Timing

OPERATION OVERVIEW

■ System Clock

The master clock can be either a crystal resonator placed across the XTI and XTO pin (XTS="H"), or external TTL level clock input to the MCKI pin (XTS="L") with the XTI pin left floating. The relationship between the master clock and the desired sample rate is defined in Table 1. The sampling rate corresponds to 32kHz ~ 48kHz at normal speed mode (DFS="0") and 64kHz ~ 96kHz (DFS="1"). The LRCK clock input must be derived from the master clock, and the phase is not critical. Either the same or a half frequency of XTI/MCKI frequency for the master clock output (MCKO) can be selected by OCKS. MCKO may be used as the master clock for the additional ADC or DAC. The ADC is powered down during double speed mode (DFS="1").

In slave mode, MCKI should be synchronized with LRCK but the phase is not critical. External clocks (MCKI, BICK) should always be present whenever the AK4526A is in normal operation mode ($\overline{PD}$ ="H"). If these clocks are not provided, the AK4526A may draw excess current because the device utilizes dynamic refreshed logic internally. If the external clocks are not present, the AK4526A should be in the power-down mode ($\overline{PD}$ ="L"). After exiting reset at power-up etc., the AK4526A is in the power-down mode until MCKI and LRCK are input.

No.	ICKS1	ICKS0	XTI/MCKI		
			DFS="0"	DFS="1"	
0	0	0	256fs	128fs	at reset
1	0	1	384fs	192fs	
2	1	0	512fs	256fs	
3	1	1	256fs	256fs	

Table 1. Master clock frequency select

When changing DFS, some click noise may occur. At that case, the analog outputs should be muted externally or by the internal attenuators.

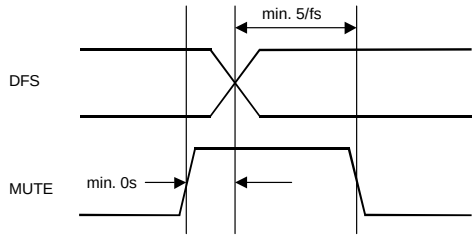


Figure 1. External mute timing at DFS change

When using crystal oscillator, external loading capacitor (~ 40pF to AVSS for XTI/XTO) are required. When X'tal mode (XTS="H"), at power-up, $\overline{PD}$ should be held "L" for 5ms to allow the X'tal oscillation to begin.

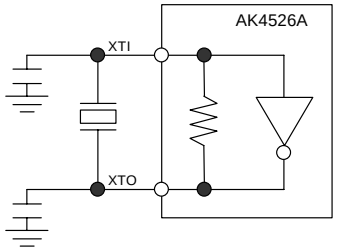


Figure 2. X'tal resonator connection (XTS="H")

■ De-emphasis Filter

The AK4526A includes the digital de-emphasis filter (tc=50/15us) by IIR filter. This filter corresponds to four sampling frequencies (32kHz, 44.1kHz, 48kHz, 96kHz). In parallel control mode (P/$\overline{S}$ ="H"), de-emphasis mode is selected by the DFS, DEM1 & DEM0 pins. In serial control mode (P/$\overline{S}$ ="L"), de-emphasis is set by OR of pins and register.

No.	DFS	DEM1	DEM0	Mode	
0	0	0	0	44.1kHz	
1	0	0	1	OFF	at reset
2	0	1	0	48kHz	
3	0	1	1	32kHz	
4	1	0	0	OFF	
5	1	0	1	OFF	
6	1	1	0	96kHz	
7	1	1	1	OFF	

Table 2. De-emphasis control

■ Digital High Pass Filter

The ADC has a digital high pass filter for DC offset cancel. The cut-off frequency of the HPF is 0.9Hz at fs=44.1kHz and also scales with sampling rate (fs).

■ Analog Volume Control

The DAC outputs include analog volume and may be independently attenuated in 1dB steps. Level changes attenuate the DAC and the internal filter noise with the signal until the residual noise floor is equal to the noise floor of the output buffer. Level changes only occur during zero-crossings to minimize audible artifacts. If these is no zero-crossings, then the level will change after a time-out. The time-out period scales with fs. The periods of 256/fs, 512/fs, 1024/fs and 2048/fs are selectable by TM1-0 bits. For each DAC channel, there is a register status bit that indicates if the level change has occurred. If the attenuation register is written to before the status flag is cleared , the previous level change is made and the timer is reset. Zero-crossing detection may be disabled by serial control.

The on-chip volume can attenuate the DAC output from 0dB to –20dB. Table 3 shows the S/N of the DAC at each attenuation level.

	Output Volume Setting		
	0dB	-10dB	-20dB
A-weight	100dB	96dB	88dB
CCIR-ARM	96dB	92dB	84dB

Table 3. DAC S/N

■ Audio Serial Interface Format

The audio interface corresponds to both master mode and slave mode. LRCK and BICK are inputs in slave mode. For master mode, LRCK outputs fs clock and BICK outputs 64fs clock.

Four serial data modes can be selected by the DIF0 and DIF1 pins as shown in Table 4. In all modes the serial data is MSB-first, 2's compliment format. The SDTO is clocked out on the falling edge of BICK and the SDTI/DAUX are latched on the rising edge of BICK.

Figure 3-5 shows the timing at SDOS="L". In this case, the SDTO outputs the ADC output data. When SDOS="H", the data input to DAUX is converted to SDTO's format and output from SDTO. Mode 2 and mode 3 in SDTI/DAUX input formats can be used for 16-20bit data by zeroing the unused LSBs.

Mode	DIF1	DIF0	SDTO		SDTI, SDTI2, SDTI3, DAUX	LRCK
			ADC SDOS="L"	DAUX SDOS="H"		
0	0	0	20bit, MSB justified	20bit, MSB justified	20bit, LSB justified	H/L
1	0	1	20bit, MSB justified	24bit, MSB justified	24bit, LSB justified	H/L
2	1	0	20bit, MSB justified	24bit, MSB justified	24bit, MSB justified	H/L
3	1	1	20bit, IIS (I2S)	24bit, IIS (I2S)	24bit, IIS (I2S)	L/H

Table 4. Audio data formats

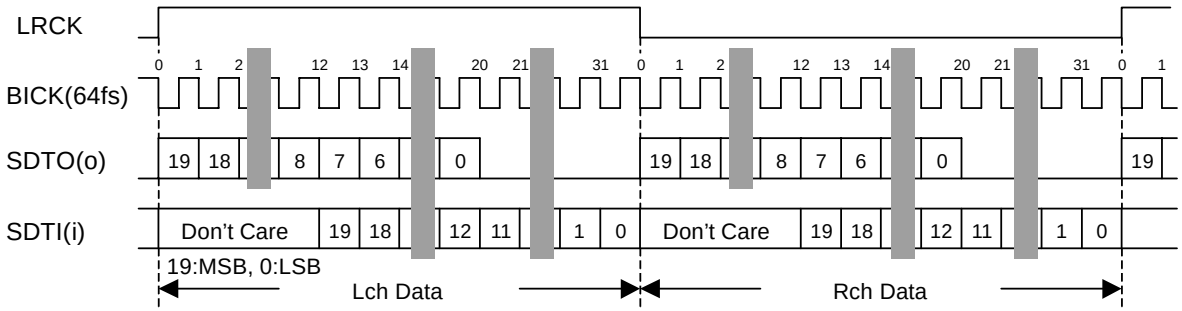


Figure 3. Mode 0 Timing

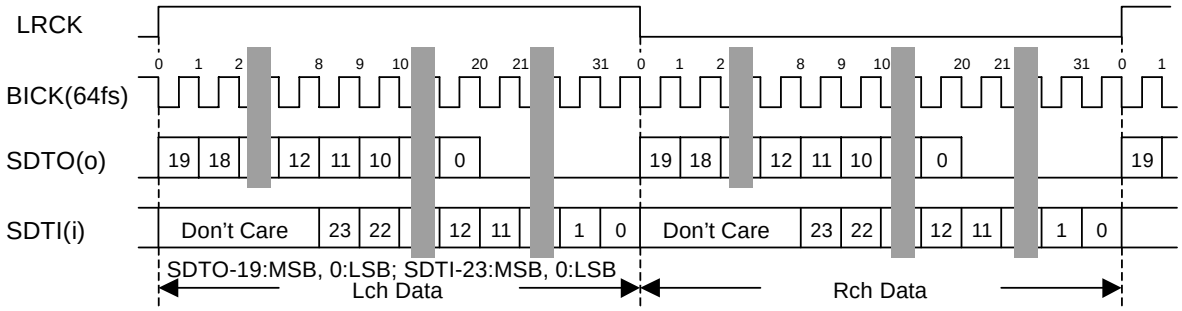


Figure 4. Mode 1 Timing
*When SDOS="H", up to 24bit data is output from SDTO.

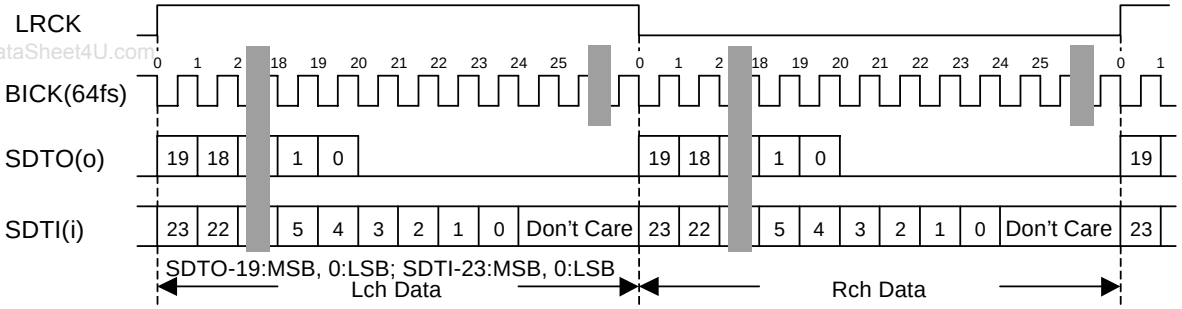


Figure 5. Mode 2 Timing
*When SDOS="H", up to 24bit data is output from SDTO.

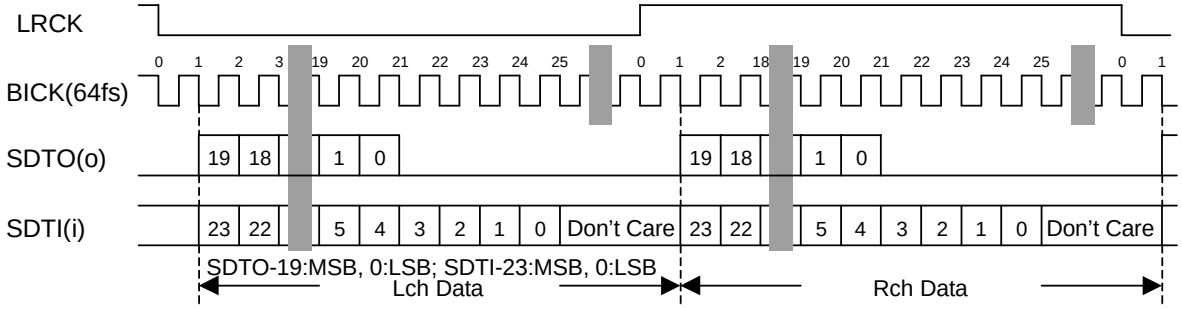
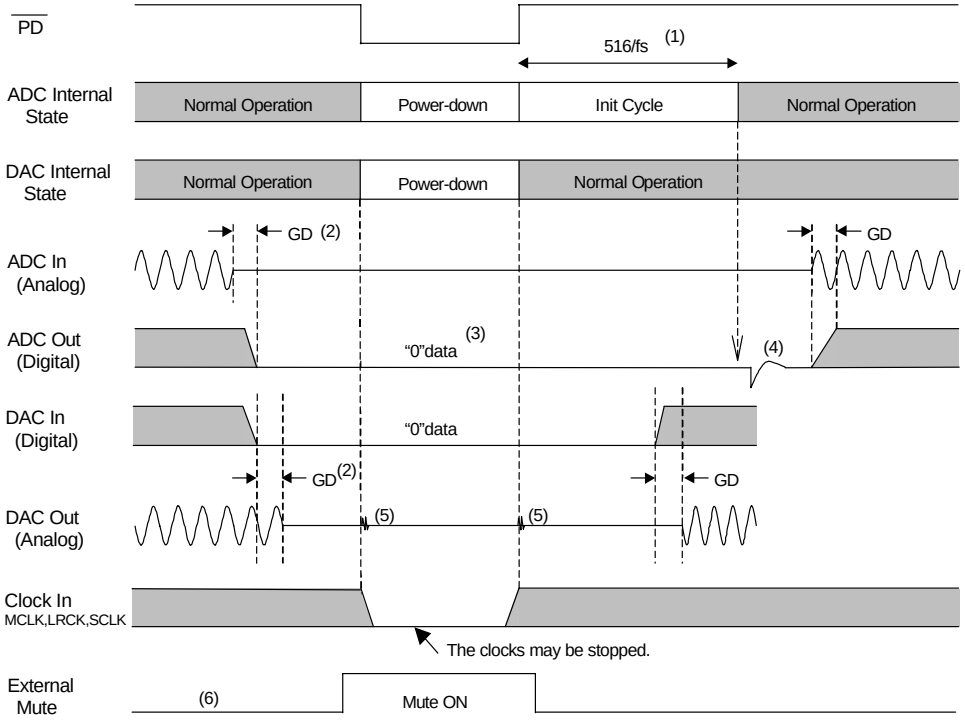


Figure 6. Mode 3 Timing
*When SDOS="H", up to 24 bit data is output from SDTO.

■ Power-Down & Reset

The ADCs and DACs of AK4526A are placed in the power-down mode by bringing $\overline{PD}$ "L" and both digital filters are reset at the same time. $\overline{PD}$ "L" also reset the control registers to their default values. This reset should always be done after power-up. In case of the ADC, an analog initialization cycle starts after exiting the power-down mode. Therefore, the output data, SDTO becomes available after 516 cycles of LRCK clock. This initialization cycle does not affect the DAC operation. Figure 7 shows the power-up sequence.



(1) The analog part of ADC is initialized after exiting the power-down state.
(2) Digital output corresponding to analog input and analog output corresponding to digital input have the group delay (GD).
(3) A/D output is "0" data at the power-down state.
(4) Click noise occurs at the end of initialization of the analog part. Please mute the digital output externally if the click noise influences system application. Required muting time depends on the configuration of the input buffer circuits.

Figure 10: 1s
Figure 11: 200ms

(5) Click noise occurs at the edge of $\overline{PD}$.
(6) Please mute the analog output externally if the click noise (5) influences system application.

Figure 7. Power-up sequence

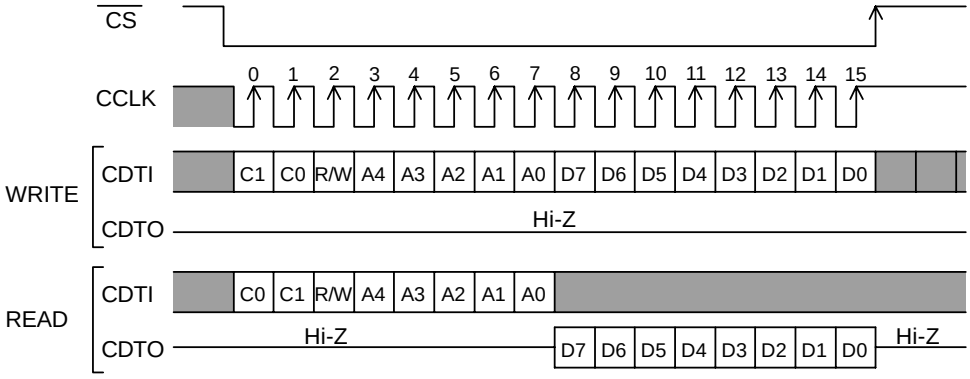
During the power-down mode, the crystal oscillator is left running if XTS="H". The condition of the outputs are as follows.

CDTO = high impedance
SDTO = "L"
MCKO = Clock out
LRCK = "L" (master mode)
BICK = "L" (master mode)
AOUT = VCOM (AVDD/2)

■ Mode Control Interface

Control may be configured directly by pins during the parallel control mode. The serial control interface is enabled by the P/$\overline{S}$ pin = "L". In this mode, internal registers may be either written to or read by the 4 wire uP interface pins: $\overline{CS}$, CCLK, CDTI & CDTO. The data on this interface consists of Chip address (2bits, C0/1) Read/Write (1bit), Register address (MSB first, 5bits) and Control data (MSB first, 8bits). Address and data is clocked in on the rising edge of CCLK and data is clocked out on the falling edge. For write operations, data is latched after the 16th rising edge of CCLK, after a high-to-low transition of $\overline{CS}$. For read operations, the CDTO output goes high impedance after a low-to-high transition of $\overline{CS}$. The operation of the control serial port may be completely asynchronous with the audio sample rate.

The chip address is determined by the state of the CAD0 and CAD1 inputs. $\overline{PD}$ = "L" resets the registers to their default values.



C1-C0: Chip Address (4 address selectable)
R/W READ/WRITE (0:READ, 1:WRITE)
A4-A0: Register Address
D7-D0: Control data

Figure 8. Control I/F Timing

■ Register Map

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Control 1	0	TM1	TM0	ZCD	DIF1	DIF0	OCKS	MUTE
01H	Control 2	0	0	LOOP1	LOOP0	SDOS	DFS	DEM1	DEM0
02H	LOUT1 Volume Control	0	0	0	ATT4	ATT3	ATT2	ATT1	ATT0
03H	ROUT1 Volume Control	0	0	0	ATT4	ATT3	ATT2	ATT1	ATT0
04H	LOUT2 Volume Control	0	0	0	ATT4	ATT3	ATT2	ATT1	ATT0
05H	ROUT2 Volume Control	0	0	0	ATT4	ATT3	ATT2	ATT1	ATT0
06H	LOUT3 Volume Control	0	0	0	ATT4	ATT3	ATT2	ATT1	ATT0
07H	ROUT3 Volume Control	0	0	0	ATT4	ATT3	ATT2	ATT1	ATT0
08H	Volume Status	0	0	R3	L3	R2	L2	R1	L1

Note: For addresses from 09H to 1FH, data is not written and only "0" is read back.
$\overline{PD}$ = "L", resets the registers to their default values.

■ Register Definitions

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Control 1	0	TM1	TM0	ZCD	DIF1	DIF0	OCKS	MUTE
R/W		R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET		0	1	0	0	0	0	0	0

MUTE: DAC mute control
0: Normal operation
1: DAC outputs muted
MUTE causes all DAC outputs to be muted. The registers of each volume setting are preserved during mute and the DAC outputs return to their previous volume setting after MUTE is programmed "L". Muting is done according to the ZCD, TM1 and TM0 register settings.

OCKS: Output Clock Frequency Select
0: MCKO = master clock
1: MCKO = master clock / 2
Register bit is ORed with OCKS pin if P/$\overline{S}$ = "L".

DIF1-0: Audio data interface modes (see Table 4)
00: Mode 0
01: Mode 1
10: Mode 2
11: Mode 3

ZCD: Zero crossing disable
0: DAC attenuation changes occur only on zero-crossing or after timeout.
1: DAC attenuation changes occur immediately.

TM1-0: Zero crossing time out period select
00: 256/fs
01: 512/fs
10: 1024/fs
11: 2048/fs

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
01H	Control 2	0	0	LOOP1	LOOP0	SDOS	DFS	DEM1	DEM0
R/W		R	R	R/W	R/W	R/W	R/W	R/W	R/W
RESET		0	0	0	0	0	0	0	0

DFS, DEM1-0: De-emphasis response

000: 44.1kHz
001: OFF
010: 48kHz
011: 32kHz
100: OFF
101: OFF
110: 96kHz
111: OFF

Register bits are ORed with DFS, DEM1, DEM0 pins if P/$\overline{S}$ = "L".
ADC is poewered down at DFS = "1".

SDOS: SDTO source select

0: ADC → SDTO
1: DAUX/De-emphasis → SDTO

Register bit is ORed with SDOS pin if P/$\overline{S}$ = "L".

LOOP1-0: Loopback mode enable

00: Normal (No loop back)
01: LIN → LOUT1, LOUT2, LOUT3
RIN → ROUT1, ROUT2, ROUT3
The digital ADC output is connected to the digital DAC input. In this mode, SDTO is output by SDOS and the input DAC data to SDTI1-3 is ignored. In 96kHz mode the ADC output to DAC input goes to all "0".
10 SDTI1(L) → SDTI2(L), SDTI3(L)
SDTI1(R) → SDTI2(R), SDTI3(R)
In this mode the input DAC data SDTI2 and SDTI3 is ignored.
11: N/A

When the audio format is set mode 1 at loopback mode, the audio format of SDTO becomes mode 3.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
02H	LOUT1 Volume Control	0	0	0	ATT4	ATT3	ATT2	ATT1	ATT0
03H	ROUT1 Volume Control	0	0	0	ATT4	ATT3	ATT2	ATT1	ATT0
04H	LOUT2 Volume Control	0	0	0	ATT4	ATT3	ATT2	ATT1	ATT0
05H	ROUT2 Volume Control	0	0	0	ATT4	ATT3	ATT2	ATT1	ATT0
06H	LOUT3 Volume Control	0	0	0	ATT4	ATT3	ATT2	ATT1	ATT0
07H	ROUT3 Volume Control	0	0	0	ATT4	ATT3	ATT2	ATT1	ATT0
R/W		R	R	R	R/W	R/W	R/W	R/W	R/W
RESET		0	0	0	0	0	0	0	0

ATT4-0: Attenuation level

00000: 0dB
00001: -1dB
00010: -2dB
↓
10011: -19dB
10100: -20dB
10101: Mute
↓
10111: Mute

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
08H	Volume Status	0	0	R3	L3	R2	L2	R1	L1
R/W		R	R	R	R	R	R	R	R
RESET		0	0	0	0	0	0	0	0

L3-1, R3-1: Attenuation change status

0: Attenuation level changed
1: Waiting for zero-crossing or timeout

SYSTEM DESIGN

Figure 9 shows the system connection diagram. An evaluation board is available which demonstrates application circuits, the optimum layout, power supply arrangements and measurement results.

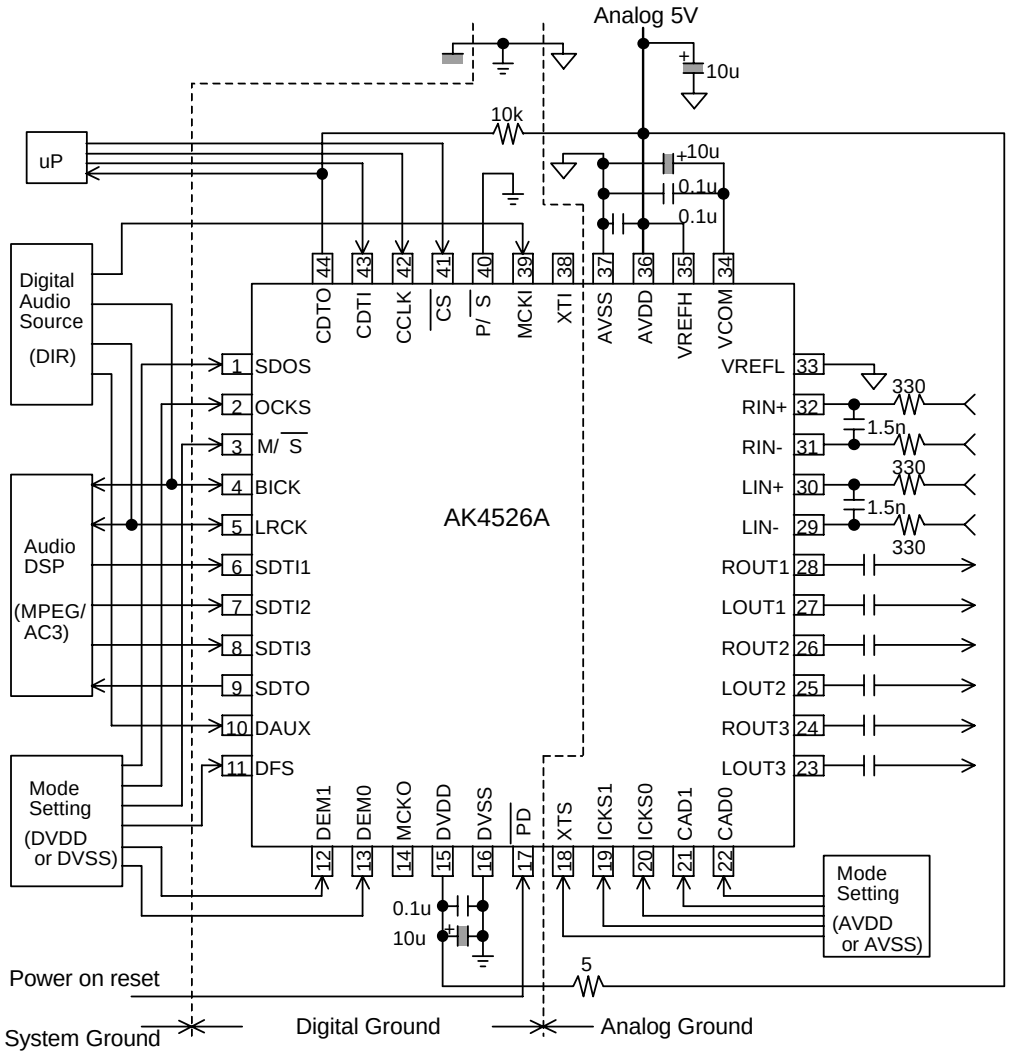


Figure 9. Typical Connection Diagram

If pins XTS, ICKS0, ICKS1, $\overline{PD}$, P/$\overline{S}$, DFS, DEM0, DEM1, CAD0, CAD1, M/$\overline{S}$, OCKS, SDOS are not driven, then XTS, ICKS0, ICKS1, CAD0, CAD1 MUST BE tied either AVSS or AVDD. $\overline{PD}$, P/$\overline{S}$, DFS, DEM0, DEM1, M/$\overline{S}$, OCKS, SDOS must be tied either DVSS or DVDD.

1. Grounding and Power Supply Decoupling

The AK4526A requires careful attention to power supply and grounding arrangements. AVDD and DVDD are usually supplied from analog supply in system. Alternatively if AVDD and DVDD are supplied separately, the power up sequence is not critical. AVSS and DVSS of the AK4526A should be connected to analog ground plane. System analog ground and digital ground should be connected together near to where the supplies are brought onto the printed circuit board. Decoupling capacitors should be as near to the AK4526A as possible, with the small value ceramic capacitor being the nearest.

2. Voltage Reference Inputs

The differential voltage between VREFH and VREFL sets the analog input/output range. VREFH pin is normally connected to AVDD with a 0.1uF ceramic capacitor and VREFL pin is connected to AVSS. VCOM is a signal ground of this chip. An electrolytic capacitor 10uF parallel with a 0.1uF ceramic capacitor attached to VCOM pin eliminates the effects of high frequency noise. No load current may be drawn from VCOM pin. All signals, especially clocks, should be kept away from the VREFH, VREFL and VCOM pins in order to avoid unwanted coupling into the AK4526A.

3. Analog Inputs

The ADC inputs are differential and internally biased to the common voltage (AVDD/2) with 30kΩ (typ) resistance. Figure 10 is a circuit example which analog signal is input by single end. The signal can be input from either positive or negative input and the input signal range scales with the supply voltage and nominally 0.6 x (VREFH-VREFL) Vpp. In case of single ended input, the distortion around full scale degrades compared with differential input. Figure 11 is a circuit example which analog signal is input to both positive and negative input and the input signal range scales with the supply voltage and nominally 0.3 x (VREFH-VREFL) Vpp. The AK4526A can accept input voltages from AVSS to AVDD. The ADC output data format is 2's complement. The output code is 7FFFFH(@20bit) for input above a positive full scale and 80000H(@20bit) for input below a negative fill scale. The ideal code is 00000H(@20bit) with no input signal. The DC offset is removed by the internal HPF.

The AK4526A samples the analog inputs at 64fs. The digital filter rejects noise above the stop band except for multiples of 64fs. A simple RC filter (fc=150kHz) may be used to attenuate any noise around 64fs and most audio signals do not have significant energy at 64fs.

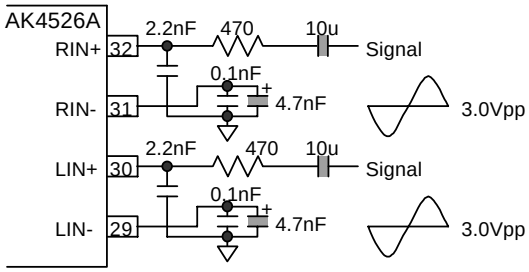


Figure 10. Single End Input Example

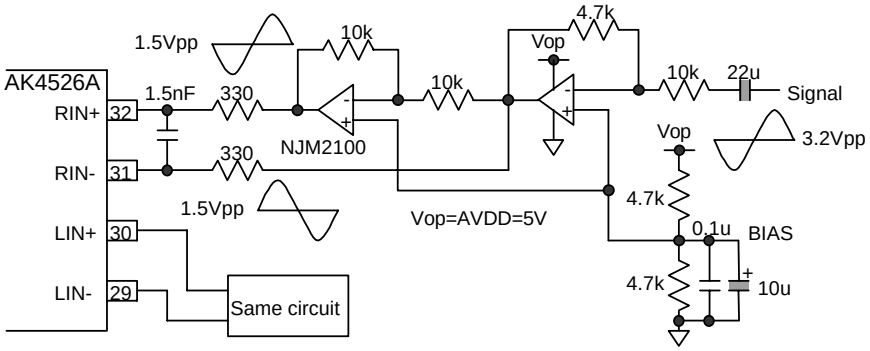


Figure 11. Differential Input Buffer Example

4. Analog Outputs

The analog outputs are also single-ended and centered around the VCOM voltage. The input signal range scales with the supply voltage and nominally 0.6 x (VREFH-VREFL) Vpp. The DAC input data format is 2's complement. The output voltage is a positive full scale for 7FFFFH(@20bit) and a negative full scale for 80000H(@20bit). The ideal output is VCOM voltage for 00000H(@20bit). The internal analog filters remove most of the noise generated by the delta-sigma modulator of DAC beyond the audio passband.

DC offsets on analog outputs are eliminated by AC coupling since DAC outputs have DC offsets of a few mV.

■ Layout Example

Figure 12 shows a layout example in the following condition.

External clock mode, Slave mode and Serial control mode with Address “00”.

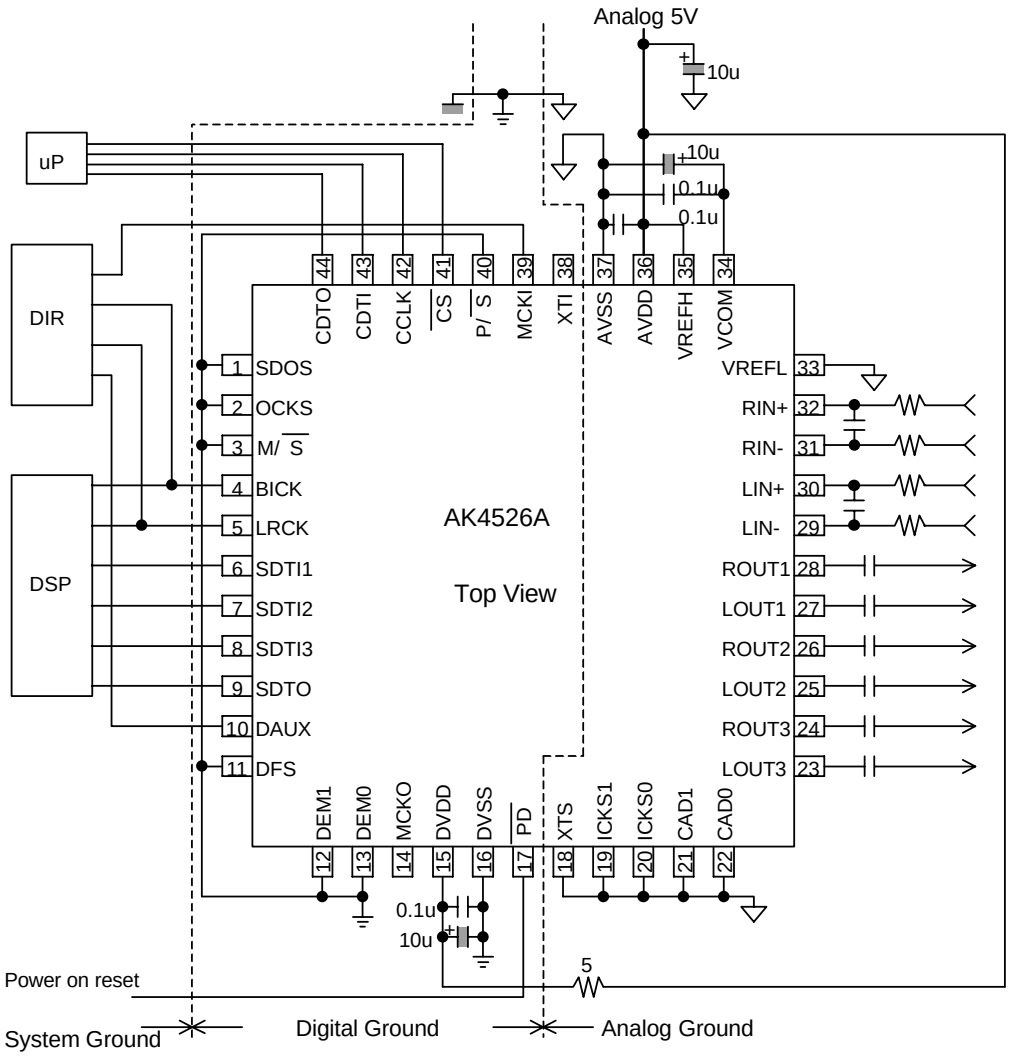


Figure 12. Layout example

■ Peripheral I/F Example

The AK4526A can accept the signal of device with a nominal 3.3V supply because of TTL input. However as the digital output level is 5V, the peripheral device must accept 5V signal when the device operate at a nominal 3.3V supply. Figure 13 shows an example with the mixed system of 3.3V and 5V.

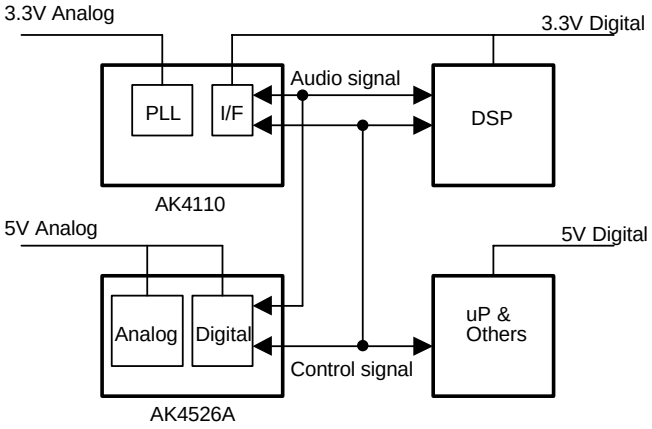
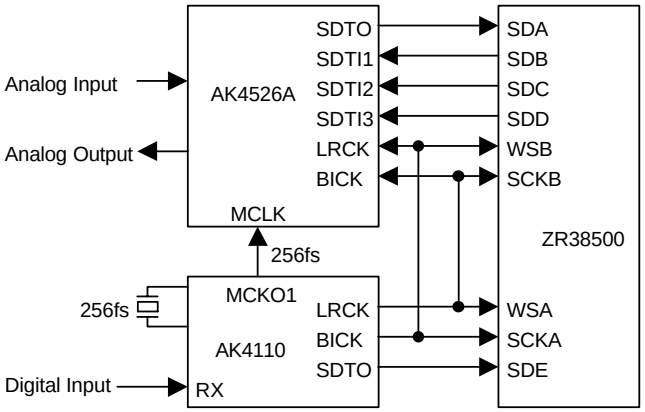


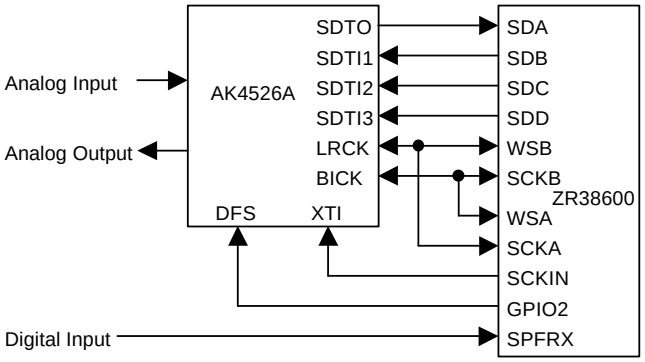
Figure 13. Power supply connection example

■ Applications

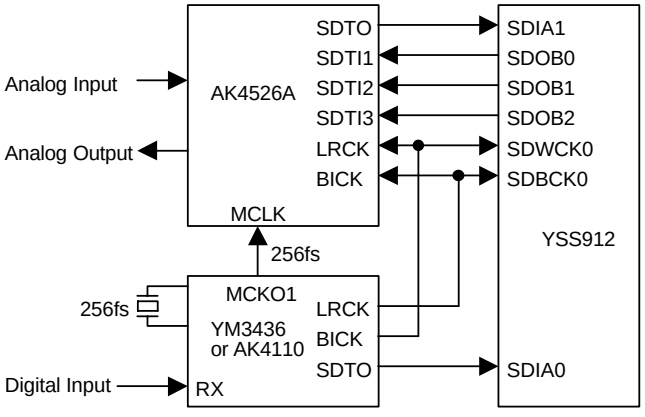
1) Zoran AC3 decoder, ZR38500



2) Zoran AC3 decoder, ZR38600

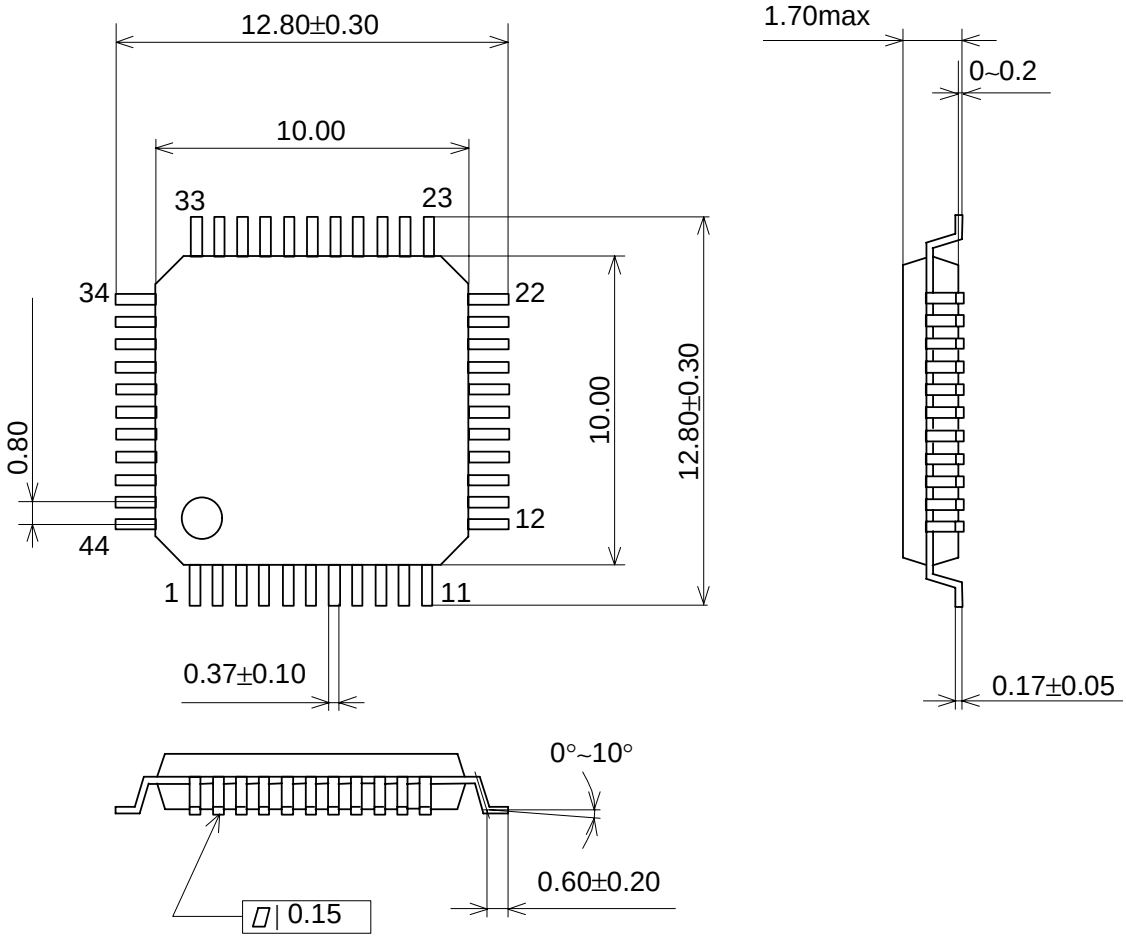


3) Yamaha AC3 decoder, YSS912



PACKAGE

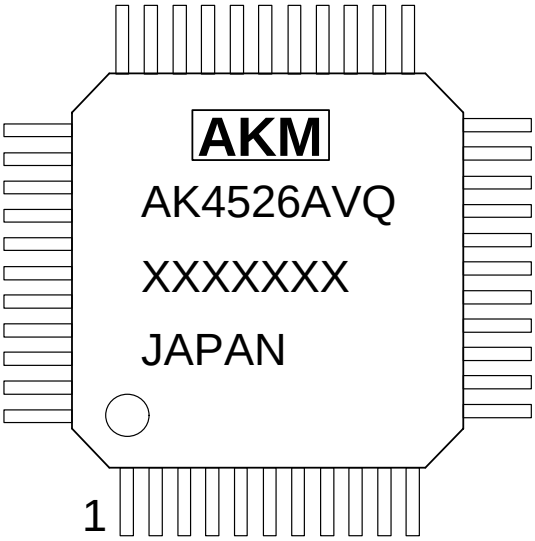
44pin LQFP (Unit: mm)



■ **Package & Lead frame material**

Package molding compound:	Epoxy
Lead frame material:	Cu
Lead frame surface treatment:	Solder plate

MARKING



1) Pin #1 indication
2) Date Code: XXXXXXX(7 digits)
3) Marking Code: AK4526AVQ
4) Country of Origin
5) Asahi Kasei Logo

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