Five-Channel, 300mA Current-Source-Output 16-/12-Bit SoftSpan DACs

FEATURES

- **Per-Channel Programmable Output Ranges: 300mA, 200mA, 100mA, 50mA, 25mA, 12.5mA,6.25mA and 3.125mA**
- **Flexible 2.85V to 33V Supply Voltage**
- **1V Dropout Guaranteed**
- **Separate Voltage Supply per Output Channel**
- **Internal Switches to Optional Negative Supply**
- **Full 16-/12-Bit Resolution at All Ranges**
- Guaranteed Operation –40°C to 125°C
- Precision (10ppm/°C Max) Internal Reference or External Reference Input
- Analog Mux Monitors Voltages and Currents
- A/B Toggle via SPI or Dedicated Pin
- 1.8V to 5V SPI Serial Interface
- 5mm × 5mm 32-Lead QFN Package

APPLICATIONS

- Tunable Lasers
- Semiconductor Optical Amplifiers
- Resistive Heaters
- Current Mode Biasing
- Proportional Solenoid Drive

DESCRIPTION

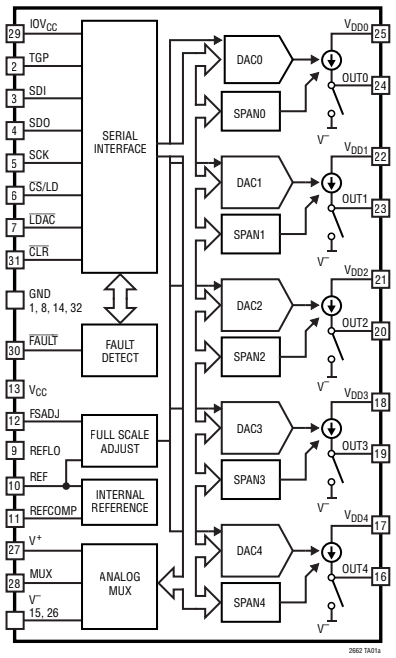
The LTC®2662 is a family of five-channel, 16-/12-bit current-source digital-to-analog converters, providing five high-compliance current source outputs with guaranteed 1V dropout at 200mA. The part supports load voltages of up to 32V. There are eight current ranges, programmable per channel, with full-scale outputs of up to 300mA; and the channels can be paralleled to allow for ultrafine adjustments of large currents, or for combined outputs of up to 1.5A.

A dedicated supply pin is provided for every output channel. Each can be operated from 2.85V to 33V, and internal switches allow any output to be pulled to the optional negative supply.

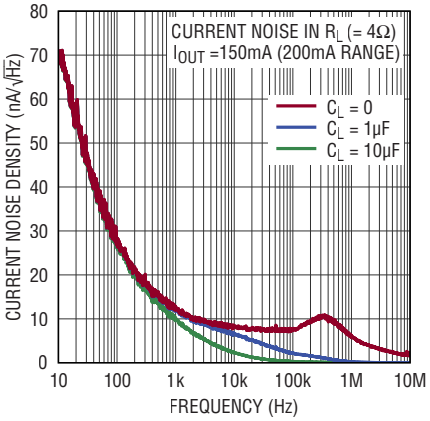
The LTC2662 includes a precision integrated 1.25V reference (10ppm/°C maximum), with the option to use an external reference.

The SPI/Microwire-compatible 3-wire serial interface operates on logic levels as low as 1.71V at clock rates up to 50MHz.

BLOCK DIAGRAM



Current Noise Density vs Frequency



RL AND CL ARE PARALLEL OUTPUT LOADS
NOISE FOR CL = 10µF AND CL = 1µF DERIVED FROM CL = 0 DATA

2662 TA01b

Rev A

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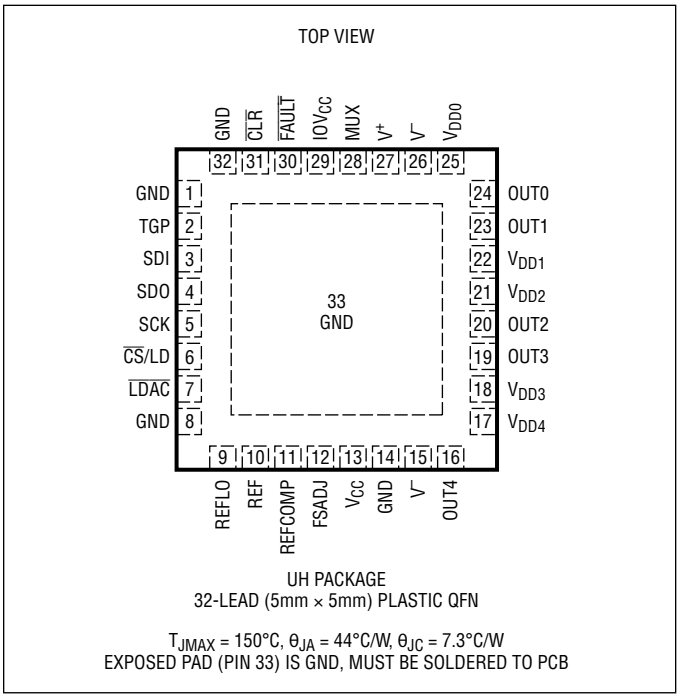
ABSOLUTE MAXIMUM RATINGS

(Note 1)

Analog Supply Voltage (V_{CC}) ..... –0.3V to 6V
Digital I/O Voltage (IOV_{CC}) ..... –0.3V to 6V
Negative Supply Voltage (V^-) ..... –16.5V to 0.3V
Positive Supply Voltage (V^+) ..... –0.3V to (V^- + 36V)
Output Supply Voltages
(V_{DD0}, V_{DD1}, V_{DD2}, V_{DD3}, V_{DD4}) ..... –0.3V to (V^+ + 0.3V)
OUT0, OUT1, OUT2,
OUT3, OUT4 ..... (V^- – 0.3V) to (V_{DDX} + 0.3V)
MUX ..... (V^- – 0.3V) to (V^+ + 0.3V)
REF, REFCOMP, FSADJ .... –0.3V to Min (V_{CC} + 0.3V, 6V)
$\overline{CS}$/LD, SCK, SDI, $\overline{LDAC}$, $\overline{CLR}$, TGP ..... –0.3V to 6V
$\overline{FAULT}$ ..... –0.3V to 6V
SDO ..... –0.3V to Min (I_{OVCC} + 0.3V, 6V)
Operating Junction Temperature (T_J) Range
LTC2662C ..... 0°C to 70°C
LTC2662I ..... –40°C to 85°C
LTC2662H ..... –40°C to 125°C
Maximum Junction Temperature..... 150°C
Storage Temperature Range ..... –65°C to 150°C

PIN CONFIGURATION



UH PACKAGE
32-LEAD (5mm × 5mm) PLASTIC QFN

T_{JMAX} = 150°C, θ_{JA} = 44°C/W, θ_{JC} = 7.3°C/W
EXPOSED PAD (PIN 33) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LTC2662 C UH 16 #TR PBF

LEAD FREE DESIGNATOR
PBF = Lead Free

TAPE AND REEL
TR = 2500-Piece Tape and Reel

RESOLUTION
16 = 16-Bit
12 = 12-Bit

PACKAGE TYPE
UH = 32-Lead QFN

TEMPERATURE GRADE
C = Commercial Temperature Range (0°C to 70°C)
I = Industrial Temperature Range (–40°C to 85°C)
H = Automotive Temperature Range (–40°C to 125°C)

PRODUCT PART NUMBER

Contact the factory for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

Tape and reel specifications. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

PRODUCT SELECTION GUIDE

LEAD FREE FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC2662CUH-16#PBF	LTC2662CUH-16#TRPBF	266216	32-Lead (5mm × 5mm) QFN	0°C to 70°C
LTC2662IUH-16#PBF	LTC2662IUH-16#TRPBF	266216	32-Lead (5mm × 5mm) QFN	–40°C to 85°C
LTC2662HUH-16#PBF	LTC2662HUH-16#TRPBF	266216	32-Lead (5mm × 5mm) QFN	–40°C to 125°C
LTC2662CUH-12#PBF	LTC2662CUH-12#TRPBF	266212	32-Lead (5mm × 5mm) QFN	0°C to 70°C
LTC2662IUH-12#PBF	LTC2662IUH-12#TRPBF	266212	32-Lead (5mm × 5mm) QFN	–40°C to 85°C
LTC2662HUH-12#PBF	LTC2662HUH-12#TRPBF	266212	32-Lead (5mm × 5mm) QFN	–40°C to 125°C

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating junction temperature range, otherwise specifications are at T_J = 25°C. V_{CC} = IOV_{CC} = 5V; V^- = –5V; $V_{DD0/1/2/3/4}$ = 5V, V^+ = 5V, FSADJ = V_{CC}, $V_{(REF)}$ = 1.25V external unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		LTC2662-12 MIN	LTC2662-12 TYP	LTC2662-12 MAX	LTC2662-16 MIN	LTC2662-16 TYP	LTC2662-16 MAX	UNITS
DC Performance All Ranges (Note 4)										
	Resolution		●	12			16			Bits
	Monotonicity	(Note 3)	●	12			16			Bits
DNL	Differential Nonlinearity	(Note 3)	●			±0.5		±0.2	±1	LSB
INL	Integral Nonlinearity	(Note 3)	●			±4		±12	±64	LSB
I_{OS}	Offset Error Current	(Note 3)	●			±0.4		±0.1	±0.4	%FSR
	V_{OS} Temperature Coefficient				±10			±10		ppm/°C
GE	Gain Error (Note 4)	300mA, 200mA, 100mA Ranges 50mA, 25mA Ranges 12.5mA, 6.25mA, 3.125mA Ranges	● ● ●			±0.9 ±1.2 ±1.5		±0.3 ±0.4 ±0.7	±0.9 ±1.2 ±1.5	%FSR %FSR %FSR
	Gain Temperature Coefficient	FSADJ = V_{CC}			±30			30		ppm/°C
TUE	Total Unadjusted Error (Note 4)	300mA, 200mA, 100mA Ranges 50mA, 25mA Ranges 12.5mA, 6.25mA, 3.125mA Range	● ● ●			±1.4 ±1.7 ±2		±0.4 ±0.5 ±0.8	±1.4 ±1.7 ±2	%FSR %FSR %FSR
PSRR	Power Supply Rejection Ratio	Range = 100mA; I_{OUT} = 50mA V_{CC}: 4.75V to 5.25V V_{DDX}: 2.85V to 3.15V V_{DDX}: 4.75V to 5.25V V^+: 4.75V to 5.25V V^-: –5.25V to –4.75V			 ±0.15 ±0.05 ±0.25 ±0.01 ±0.001			 ±2.2 ±0.6 ±3.7 ±0.09 ±0.01		 LSB LSB LSB LSB LSB
	DC Crosstalk (Note 5)	Due to 200mW Change in Dissipated Power			±1			±14		LSB

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
DC Performance							
$V_{DROPOUT}$	Dropout Voltage (V_{DDX} – V_{OUTX})	200mA Range; (V_{DDX} – V^-) = 4.75V 200mA Range; (V_{DDX} – V^-) = 2.85V 200mA Range; (V_{DDX} – V^-) = 33V 300mA Range; (V_{DDX} – V^-) = 4.75V 300mA Range; (V_{DDX} – V^-) = 2.85V	● ● ●		0.72 0.85 0.76 1.13 1.15	1 1.1 1.75	V V V V V
	Hi-Z Output Leakage Current	I_{OUTX} = Hi-Z, 2.85V ≤ (V_{DDX} – V^-) ≤ 33V	●		0.1	1	µA
$R_{PULLDOWN}$	OUTX Switch-to-V^- Resistance to V^- Supply	Span Code = 1000b, Sinking 80mA	●		8	12	Ω
$I_{PULLDOWN}$	OUTX Switch-to-V^- Current	Maximum Allowable DC Current				80	mA
AC Performance							
t_{SET}	Settling Time, Full-Scale Step 3.125mA Range	±0.024% (±1LSB at 12b) (Notes 9, 12) ±0.0015% (±1LSB at 16b) (Notes 9, 12)			6.1 19.2		µs µs
	Settling Time, 145mA-155mA Step 200mA Range	±0.024% (±1LSB at 12b) (Notes 9, 12) ±0.0015% (±1LSB at 16b) (Notes 9, 12)			3.5 7.7		µs µs
	Settling Time, Full-Scale Step 200mA Range	±0.024% (±1LSB at 12b) (Notes 9, 12) ±0.0015% (±1LSB at 16b) (Notes 9, 12)			4.5 8.7		µs ms
	Glitch Impulse	At Mid-Scale Transition, 200mA Range, R_{LOAD} = 4Ω			180		pA•s
	DAC-to-DAC Crosstalk (Note 6)	100mA to 200mA Step, R_{LOAD} = 15Ω			150		pA•s
i_{noise}	Output Current Noise Density Internal Reference, I_{OUT} = 150mA, R_{LOAD} = 4Ω, C_{LOAD} = 10µF	f = 1kHz f = 10kHz f = 100kHz f = 1MHz			12 5 0.5 0.05		nA/√Hz nA/√Hz nA/√Hz nA/√Hz

REFERENCE CHARACTERISTICS

The ● denotes the specifications which apply over the full operating junction temperature range, otherwise specifications are at T_J = 25°C. V_{CC} = IOV_{CC} = 5V; V^- = –5V; $V_{DD0/1/2/3/4}$ = 5V, V^+ = 5V, FSADJ = V_{CC} unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{REF}	Reference Output Voltage			1.248	1.25	1.252	V
	V_{REF} Temperature Coefficient	(Note 7)			±3	±10	ppm/°C
	V_{REF} Line Regulation	V_{CC} = 5V ±10%			50		µV/V
	V_{REF} Short-Circuit Current	V_{CC} = 5.5V, Forcing Output to GND			2.5		mA
	REFCOMP Pin Short-Circuit Current	V_{CC} = 5.5V, Forcing Output to GND			65		µA
	V_{REF} Load Regulation	V_{CC} = 5V ±10%, I_{REF} = 100µA Sourcing			140		mV/mA
	V_{REF} Output Voltage Noise Density	$C_{REFCOMP}$ = C_{REF} = 0.1µF, at f = 10kHz			32		nV/√Hz
	V_{REF} Input Voltage Range	External Reference Mode	●	1.225		1.275	V
	V_{REF} Input Current	External Reference Mode	●		0.001	1	µA
	V_{REF} Input Capacitance	(Note 8)			40		pF
R_{FSADJ}	External Full-Scale Adjust Gain Resistor	R_{FSADJ} to GND	●	19	20	50	kΩ

DIGITAL INPUTS AND DIGITAL OUTPUTS

The ● denotes the specifications which apply over the full operating junction temperature range, otherwise specifications are at T_J = 25°C. V_{CC} = IOV_{CC} = 5V; V^- = –5V; $V_{DD0/1/2/3/4}$ = 5V, V^+ = 5V, FSADJ = V_{CC} unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Digital I/O							
V_{OH}	Digital Output High Voltage	SDO Pin, Load Current = –100µA	●	IOV_{CC} – 0.2			V
V_{OL}	Digital Output Low Voltage	SDO Pin, Load Current = 100µA $\overline{FAULT}$ Pin, Load Current = 100µA	● ●			0.2 0.2	V V
	Digital Hi-Z Output Leakage Current	SDO Pin Leakage Current ($\overline{CS}$/LD High) $\overline{FAULT}$ Pin Leakage Current (Not Asserted)	● ●			±1 1	µA µA
	Digital Input Current	V_{IN} = GND to IOV_{CC}	●			±1	µA
C_{IN}	Digital Input Capacitance	(Note 8)	●			8	pF
IOV_{CC} = 2.85 to V_{CC}							
V_{IH}	High Level Input Voltage		●	0.8 • IOV_{CC}			V
V_{IL}	Low Level Input Voltage		●			0.5	V
IOV_{CC} = 1.71V to 2.85V							
V_{IH}	High Level Input Voltage		●	0.8 • IOV_{CC}			V
V_{IL}	Low Level Input Voltage		●			0.5	V

POWER REQUIREMENTS

The ● denotes the specifications which apply over the full operating junction temperature range, otherwise specifications are at T_J = 25°C. V_{CC} = IOV_{CC} = 5V; V^- = –5V; $V_{DD0/1/2/3/4}$ = 5V, V^+ = 5V, FSADJ = V_{CC}, $V_{(REF)}$ = 1.25V external unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{CC}	Analog Supply Voltage	V_{CC} Must Not Exceed V^+	●	2.85		5.5	V
IOV_{CC}	Digital I/O Supply Voltage		●	1.71		V_{CC}	V
V^-	Negative Supply Voltage		●	–15.75		0	V
V^+	Positive Supply Voltage		●	2.85		V^- + 33	V
V_{DD0} to V_{DD4}	Output Supply Voltages		●	2.85		V^+	V
	Supply Current V_{CC}	All Ranges (Code = 0, All Channels)	●		2.6	3.8	mA
	Supply Current IOV_{CC}	All Ranges (Code = 0, All Channels)	●		0.01	1	µA
	Supply Current V^+	All Ranges (Code = 0, All Channels)	●		385	500	µA
	Supply Current V^-	All Ranges (Code = 0, All Channels)	●		2.3	3.2	mA
	Supply Current $V_{DD0/1/2/3/4}$	All Ranges (Code = 0, per Channel) 25mA Range (Code = Full-Scale, per Channel), (Note 10) 200mA Range (Code = Full-Scale, per Channel), (Note 10)	● ● ●		0.7 26.5 204	1.2 27.6 207	mA mA mA
I_{SLEEP}	Shutdown Current V_{CC}	(Note 11)	●		1	10	µA
	Shutdown Current IOV_{CC}	(Note 11)	●		0.01	1	µA
	Shutdown Current V^+	(Note 11)	●		20	36	µA
	Shutdown Current V^-	(Note 11)	●		30	59	µA
	Shutdown Current $V_{DD0/1/2/3/4}$	(Note 11) per Channel	●		4.2	8.1	µA
Monitor Mux							
	DC Output Impedance				15		kΩ
	Leakage Current	Monitor Mux Disabled (High Impedance)	●		0.1	1	µA
	Output Voltage Range	Monitor Mux Selected to I_{OUT0-4} Pin Voltage	●	V^-		V^+	V
	Continuous Current (Note 8)	Maximum Allowable Current	●			±1	mA

TIMING CHARACTERISTICS

The ● denotes the specifications which apply over the full operating junction temperature range, otherwise specifications are at T_J = 25°C. Digital input low and high voltages are 0V and IOV_{CC}, respectively.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V^+ = V_{DDX} = V_{CC} = 2.85V to 5.5V, IOV_{CC} = 2.85V to V_{CC}							
t_1	SDI Valid to SCK Setup		●	6			ns
t_2	SDI Valid to SCK Hold		●	6			ns
t_3	SCK HIGH Time		●	9			ns
t_4	SCK LOW Time		●	9			ns
t_5	$\overline{CS}$/LD Pulse Width		●	10			ns
t_6	LSB SCK High to $\overline{CS}$/LD High		●	19			ns
t_7	$\overline{CS}$/LD Low to SCK High		●	7			ns
t_8	SDO Propagation Delay From SCK Falling Edge C_{LOAD} = 10pF	4.5V ≤ IOV_{CC} ≤ V_{CC} 2.85V ≤ IOV_{CC} < 4.5V	● ●			20 30	ns ns

TIMING CHARACTERISTICS

The ● denotes the specifications which apply over the full operating junction temperature range, otherwise specifications are at T_J = 25°C. Digital input low and high voltages are 0V and IOV_{CC}, respectively.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
t_9	CLR Pulse Width		●	20			ns
t_{10}	$\overline{CS}$/LD High to SCK Positive Edge		●	7			ns
t_{12}	LDAC Pulse Width		●	15			ns
t_{13}	$\overline{CS}$/LD High to LDAC High or Low Transition		●	15			ns
	SCK Frequency	50% Duty Cycle	●			50	MHz
t_{14}	TGP High Time	(Note 8)	●	1			µs
t_{15}	TGP Low Time	(Note 8)	●	1			µs
$V^+ = V_{DDX} = V_{CC}$ = 2.85V to 5.5V, 1.71V ≤ IOV_{CC} < 2.85V							
t_1	SDI Valid to SCK Setup		●	7			ns
t_2	SDI Valid to SCK Hold		●	7			ns
t_3	SCK HIGH Time		●	30			ns
t_4	SCK LOW Time		●	30			ns
t_5	$\overline{CS}$/LD Pulse Width		●	15			ns
t_6	LSB SCK High to $\overline{CS}$/LD High		●	19			ns
t_7	$\overline{CS}$/LD Low to SCK High		●	7			ns
t_8	SDO Propagation Delay From SCK Falling Edge	C_{LOAD} = 10pF	●			60	ns
t_9	CLR Pulse Width		●	30			ns
t_{10}	$\overline{CS}$/LD High to SCK Positive Edge		●	7			ns
t_{12}	LDAC Pulse Width		●	15			ns
t_{13}	$\overline{CS}$/LD High to LDAC High or Low Transition		●	15			ns
	SCK Frequency	50% Duty Cycle	●			15	MHz
t_{14}	TGP High Time	(Note 8)	●	1			µs
t_{15}	TGP Low Time	(Note 8)	●	1			µs

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: All voltage values are with respect to GND.

Note 3: Offset current is measured at code 384 for LTC2662-16 and at code 24 for LTC2662-12. Linearity is defined from code 384 to code 65,535 for LTC2662-16; and from code 24 to code 4095 for LTC2662-12.

Note 4: For I_{FS} = 300mA, R_{LOAD} = 10Ω; I_{FS} = 200mA, R_{LOAD} = 15Ω; I_{FS} = 100mA, R_{LOAD} = 30Ω; I_{FS} = 50mA, R_{LOAD} = 50Ω; I_{FS} = 25mA, R_{LOAD} = 100Ω; I_{FS} = 12.5mA, R_{LOAD} = 200Ω; I_{FS} = 6.25mA, R_{LOAD} = 400Ω; I_{FS} = 3.125mA, R_{LOAD} = 800Ω

Note 5: I_{FS} = 200mA, R_{LOAD} = 15Ω; DC crosstalk is measured with a 100mA to 200mA current step on all 4 aggressor channels. Total Power Dissipation change is 4 × 50mW = 200mW. Monitor channel is held at 3/4 *I_{FS} or 150mA.

Note 6: DAC-to-DAC crosstalk is the glitch that appears at the output of one DAC due to a 100mA to 200mA step change in an adjacent DAC channel. The measured DAC is at mid-scale (100mA). 200mA range, internal reference, V_{DDX} = 5V, V^- = –5V.

Note 7: Temperature coefficient is calculated by first computing the ratio of the maximum change in output voltage to the nominal output voltage. The ratio is then divided by the specified temperature range.

Note 8: Guaranteed by design and not production tested.

Note 9: V_{DDX} = 5V (3.125mA range); V_{DDX} = 4V (200mA range); V^- = –5V for all ranges. For large current output steps, internal thermal effects result in a final settling tail. In most cases the tail is too small to affect settling to ±0.024%, but several milliseconds may be needed for full settling to the ±0.0015% level. For best results, always solder the exposed pad (pin 33) to a solid GND plane, and set V_{DDX} as low as practicable for each channel to reduce power dissipation in the part. The listed results were obtained using a DC2692 demo circuit with no additional heatsinks.

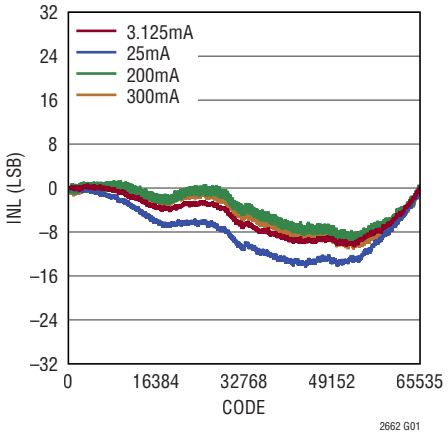
Note 10: Single Channel at Specified Output.

Note 11: Digital Inputs at 0V or IOV_{CC}.

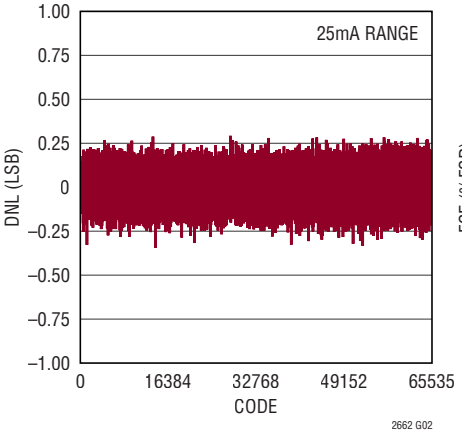
Note 12: Internal reference mode. Load is 15Ω (200mA range) or 800Ω (3.125mA range) in parallel with 100pF terminated to GND.

TYPICAL PERFORMANCE CHARACTERISTICS

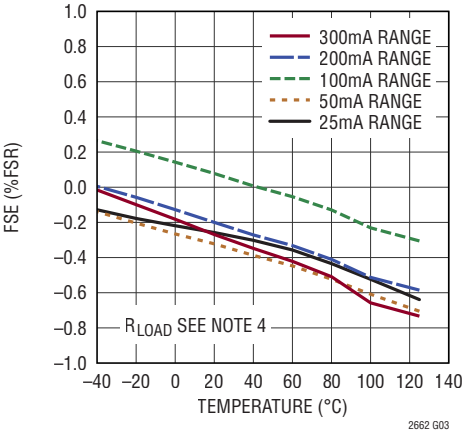
LTC2662-16
Integral Nonlinearity (INL)



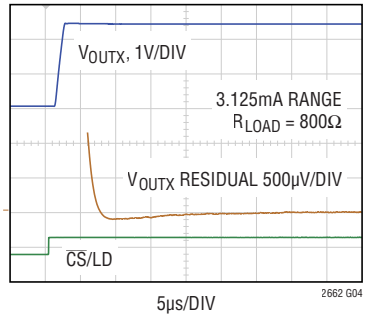
LTC2662-16
Differential Nonlinearity (DNL)



Full–Scale Current Error
vs Temperature

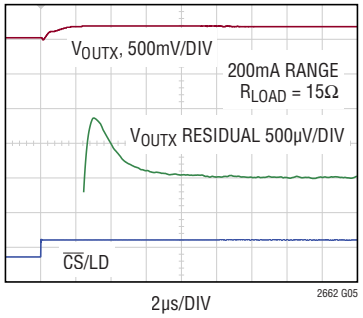


Settling 0 to 3.125mA Step



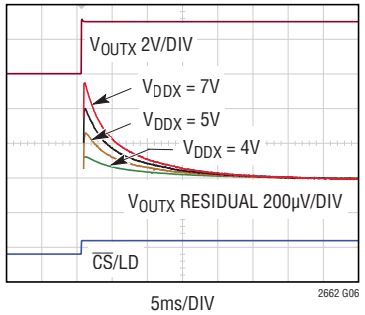
t_{SETTLE} = 6.1µs TO ±0.024%, 19.2µs TO ±0.0015%
AVERAGE OF 8192 EVENTS

Settling 145mA to 155mA Step



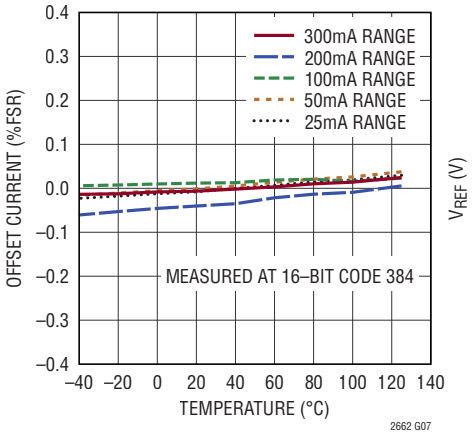
t_{SETTLE} = 3.5µs TO ±0.024%, 7.7µs TO ±0.0015%
AVERAGE OF 1024 EVENTS

Settling 0 to 200mA Step

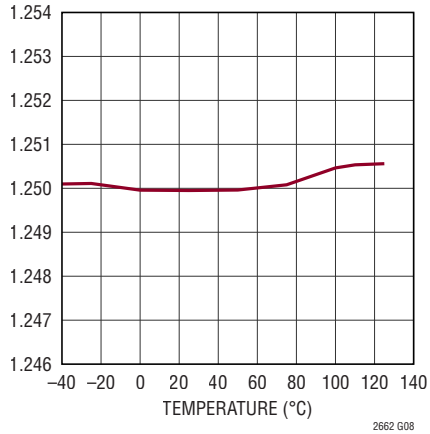


200mA RANGE; R_{LOAD} = 15Ω
t_{SETTLE} = 4.5µs TO ±0.024%, 8.7ms TO ±0.0015%
t_{SETTLE} MEASURED AT V_{DDX} = 4V TO MINIMIZE
THERMAL SETTLING TAILS

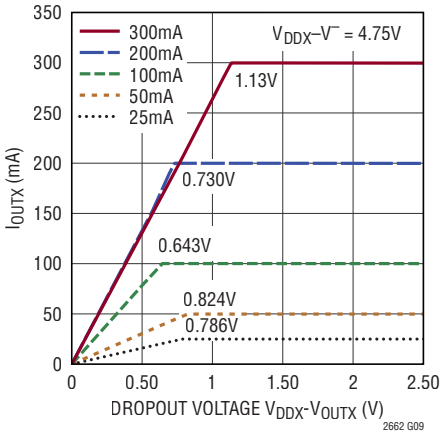
Offset Current Error
vs Temperature



Reference Output vs Temperature

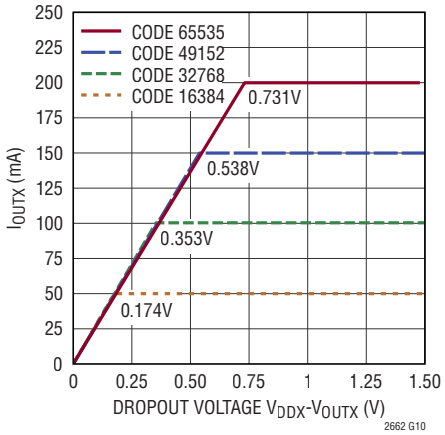


Dropout Voltage vs Current Range

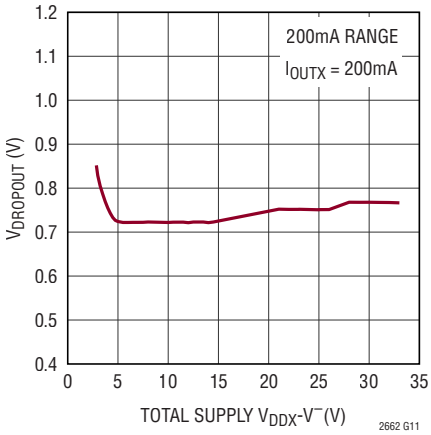


TYPICAL PERFORMANCE CHARACTERISTICS

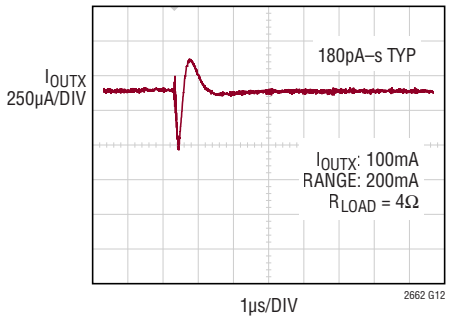
Dropout Voltage vs Code, 200mA Range



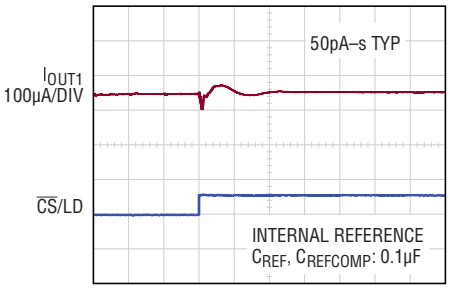
Dropout vs Total Supply Voltage



Mid–Scale Glitch

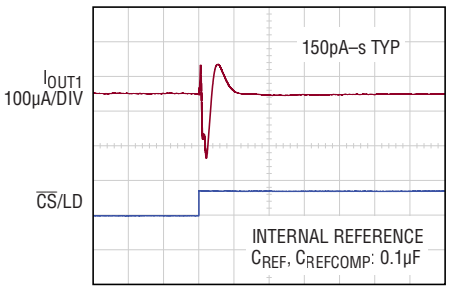


DAC–to–DAC Crosstalk (Falling)



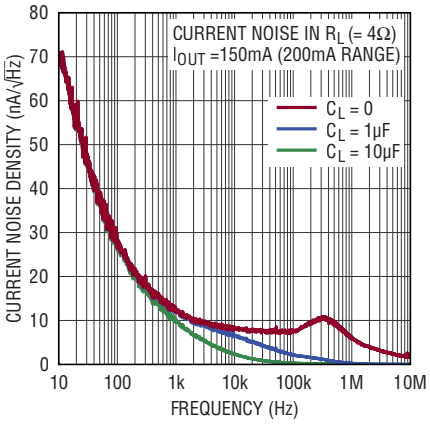
CH1: 200mA RANGE, I_{OUT1} = 100mA
CH0: 200mA RANGE, 200mA TO 100mA STEP
[FALLING TRANSITION]
ALL CHANNELS R_{LOAD}=15Ω, C_{LOAD}=0

DAC–to–DAC Crosstalk (Rising)



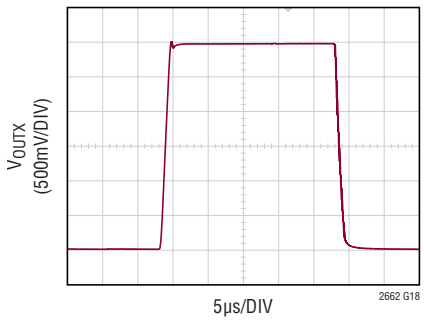
CH1: 200mA RANGE, I_{OUT1} = 100mA
CH0: 200mA RANGE, 100mA TO 200mA STEP
[RISING TRANSITION]
ALL CHANNELS R_{LOAD} = 15Ω, C_{LOAD} = 0

Current Noise Density vs Frequency



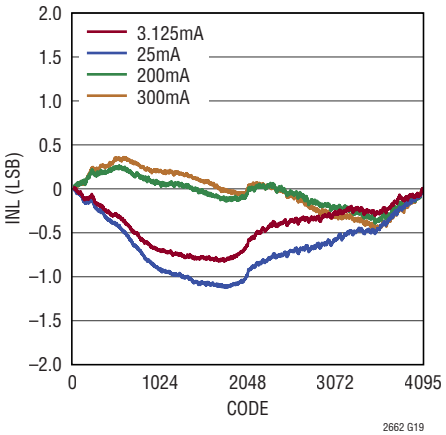
R_L AND C_L ARE PARALLEL OUTPUT LOADS
NOISE FOR C_L = 10µF AND C_L = 1µF DERIVED
FROM C_L = 0 DATA

Large Signal Response

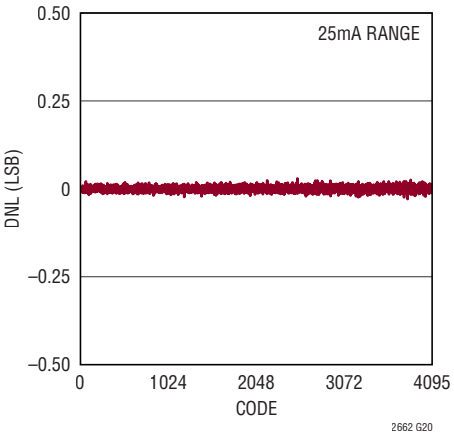


200mA RANGE; RLOAD = 15Ω

LTC2662-12 Integral Nonlinearity (INL)



LTC2662-12 Differential Nonlinearity (DNL)



Rev A

PIN FUNCTIONS

GND (Pins 1, 8, 14, 32): Ground. These pins and the exposed pad (pin 33) must be tied directly to a solid ground plane.

TGP (Pin 2): Asynchronous Toggle Pin. A falling edge updates the DAC register with data from input register A. A rising edge updates the DAC register with data from input register B. Toggle operations only affect those DAC channels with their toggle select bit (Tx) set to 1. Tie the TGP pin to IOV_{CC} if toggle operations are to be done through software. Tie the TGP pin to GND if not using toggle operations. Logic levels are determined by IOV_{CC}.

SDI (Pin 3): Serial Data Input. Data on SDI is clocked into the DAC on the rising edge of SCK. The LTC2662 accepts input word lengths of 24, 32 or multiples of 32 bits. Logic levels are determined by IOV_{CC}.

SDO (Pin 4): Serial Data Output. The serial output of the 32-bit shift register appears at the SDO pin. The data transferred to the device via the SDI pin is delayed 32 SCK rising edges before being output at the next falling edge. Can be used for data echo readback or daisy-chain operation. The SDO pin becomes high impedance when $\overline{CS}$/LD is high. Logic levels are determined by IOV_{CC}.

SCK (Pin 5): Serial Clock Input. Logic levels are determined by IOV_{CC}.

$\overline{CS}$/LD (Pin 6): Serial Interface Chip Select/Load Input. When $\overline{CS}$/LD is low, SCK is enabled for shifting SDI data into the register. In addition, SDO is enabled when $\overline{CS}$/LD is low. When $\overline{CS}$/LD is taken high, SDO and SCK are disabled and the specified command (see Table 1) is executed. Logic levels are determined by IOV_{CC}.

$\overline{LDAC}$ (Pin 7): Active Low Asynchronous DAC Update Pin. This pin allows updates independent of SPI timing. If $\overline{CS}$/LD is high, a falling edge on $\overline{LDAC}$ updates all DAC registers with the contents of the input registers. $\overline{LDAC}$ is gated by $\overline{CS}$/LD and has no effect if $\overline{CS}$/LD is low. Logic levels are determined by IOV_{CC}.

If not used, tie $\overline{LDAC}$ to IOV_{CC}.

REFLO (Pin 9): Reference Low. Signal ground for the reference. Tie directly to GND.

REF (Pin 10): Reference Input/Output. The voltage at the REF pin proportionally scales the full-scale output current of each DAC output channel. By default, the internal 1.25V reference is routed to this pin. This pin must be buffered when driving external DC load currents. If the reference is disabled (see Reference Modes in the Operation section), its output is disconnected and the REF pin becomes a high impedance input which will accept a precision external reference. For low noise and reference stability, tie a capacitor from this pin to GND. The value must be less than $C_{REFCOMP}$, where $C_{REFCOMP}$ is the capacitance tied to the REFCOMP pin. The allowable external reference input range is 1.225V to 1.275V.

REFCOMP (Pin 11): Internal Reference Compensation Pin. For low noise and reference stability, tie a 0.1µF capacitor from this pin to GND. Tying REFCOMP to GND causes the part to power up with the internal reference disabled, allowing the use of an external reference at start-up.

FSADJ (Pin 12): Full-Scale current Adjust pin. This pin can be used in one of two ways to produce either nominal, internally-calibrated output ranges, or incrementally-tunable ranges. In either case, the reference voltage V_{REF} is forced across a resistor R_{FSADJ} to define a reference current that scales the outputs for all ranges and channels. Full-scale currents are proportional to the voltage at REF (pin 10) and inversely proportional to R_{FSADJ}.

If FSADJ is tied to V_{CC}, an internal R_{FSADJ} (20k) is selected, resulting in nominal output ranges. An external resistor of 19k to 41k can be used instead by simply connecting the resistor between FSADJ and GND. In this case the external resistor controls the scaling of ranges, and the internal resistor is automatically disconnected. See Table 3 for details.

When using an external resistor, FSADJ is sensitive to stray capacitance; the pin should be compensated with a snubber network consisting of a series combination of 1k and 1µF, connected in parallel to R_{FSADJ}. With the recommended compensation, the pin is stable driving stray capacitance of up to 50pF.

PIN FUNCTIONS

V_{CC} (Pin 13): Analog Supply Voltage. 2.85V ≤ V_{CC} ≤ 5.5V. Bypass to GND with a 1µF capacitor.

V^- (Pins 15, 26): Negative Supply Voltage. –15.75V ≤ V^- ≤ GND. Bypass to GND with a 1µF capacitor unless V^- is connected to GND.

OUT0 to OUT4 (Pins 24, 23, 20, 19, 16): DAC Analog Current Outputs. Each current output pin has a dedicated analog supply pin V_{DD0} to V_{DD4}. The operational voltage level range at these pins is $V^- \le V_{OUTX} \le V_{DDX}$.

V_{DD0} to V_{DD4} (Pins 25, 22, 21, 18, 17): Output Supply Voltages. 2.85V ≤ $V_{DD0/1/2/3/4}$ ≤ V^+. These five positive supply inputs provide independent supplies for each of the five DAC current output pins OUT0 to OUT4 respectively. Bypass each supply input to GND separately with a 1µF capacitor.

V^+ (Pin 27): Positive Supply Voltage. 2.85V ≤ V^+ ≤ V^- + 33V. V^+ must always be greater than or equal to the largest of the five DAC positive supply voltages V_{DD0} to V_{DD4} and V_{CC}. The supply voltage difference ($V^+ – V^-$) can-not exceed 33V maximum. Bypass to GND with a 1µF capacitor.

MUX (Pin 28): Analog Multiplexer Output. Pin voltages and currents can be monitored by measuring the voltage at the MUX pin. When the mux is disabled, this pin becomes high impedance. The available mux selections are given in Table 4.

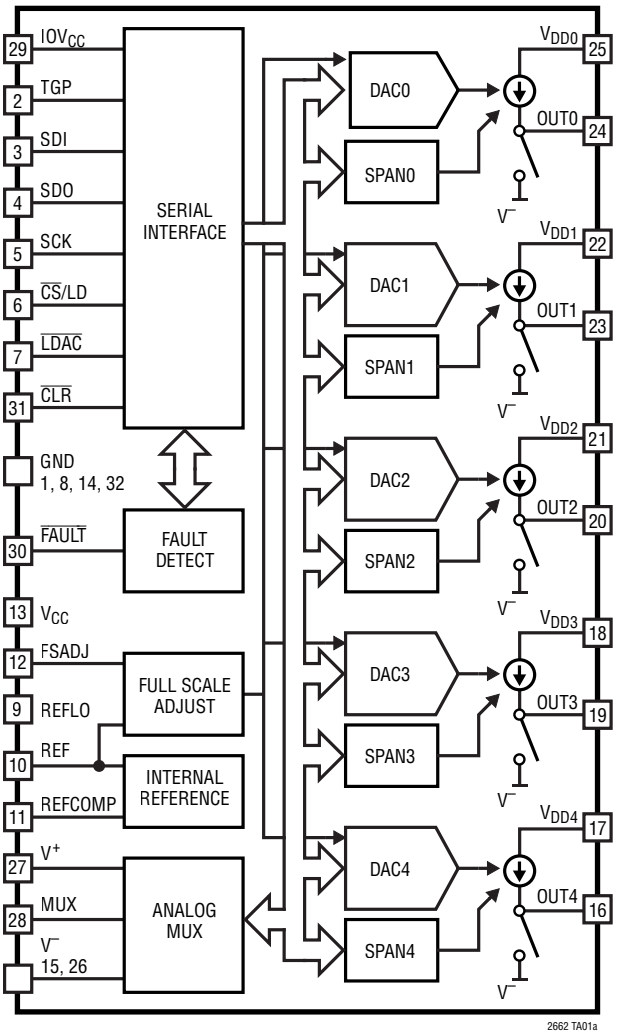
IOV_{CC} (Pin 29): Digital Input/Output Supply Voltage. 1.71V ≤ IOV_{CC} ≤ V_{CC} + 0.3V. Bypass to GND with a 0.1µF capacitor.

$\overline{\text{FAULT}}$ (Pin 30): Active-Low Fault Detection Pin. This open-drain N-channel output pulls low when any valid fault condition is detected. This pin is released on the next $\overline{CS}$/LD rising edge. A pull-up resistor is required.

$\overline{\text{CLR}}$ (Pin 31): Active-Low Asynchronous Clear Input. A logic low at this level-triggered input clears the part to the default reset code and output range which is zero-scale and high impedance (Hi-Z) outputs. The control registers are cleared to zero. Logic levels are determined by IOV_{CC}.

EXPOSED PAD (Pin 33): Ground. Solder this pad directly to the analog ground plane.

BLOCK DIAGRAM



TIMING DIAGRAMS

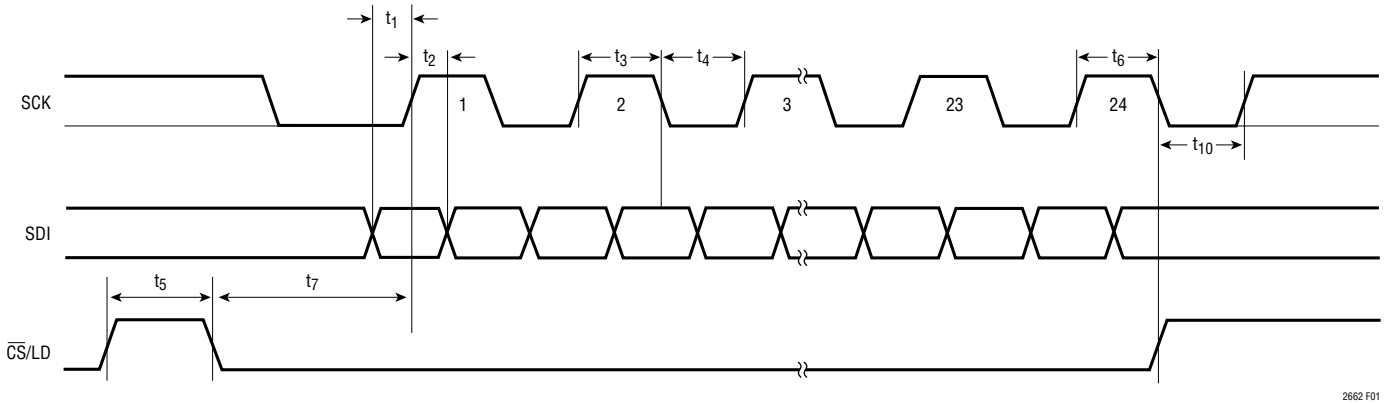


Figure 1. Serial Interface Timing

TIMING DIAGRAMS

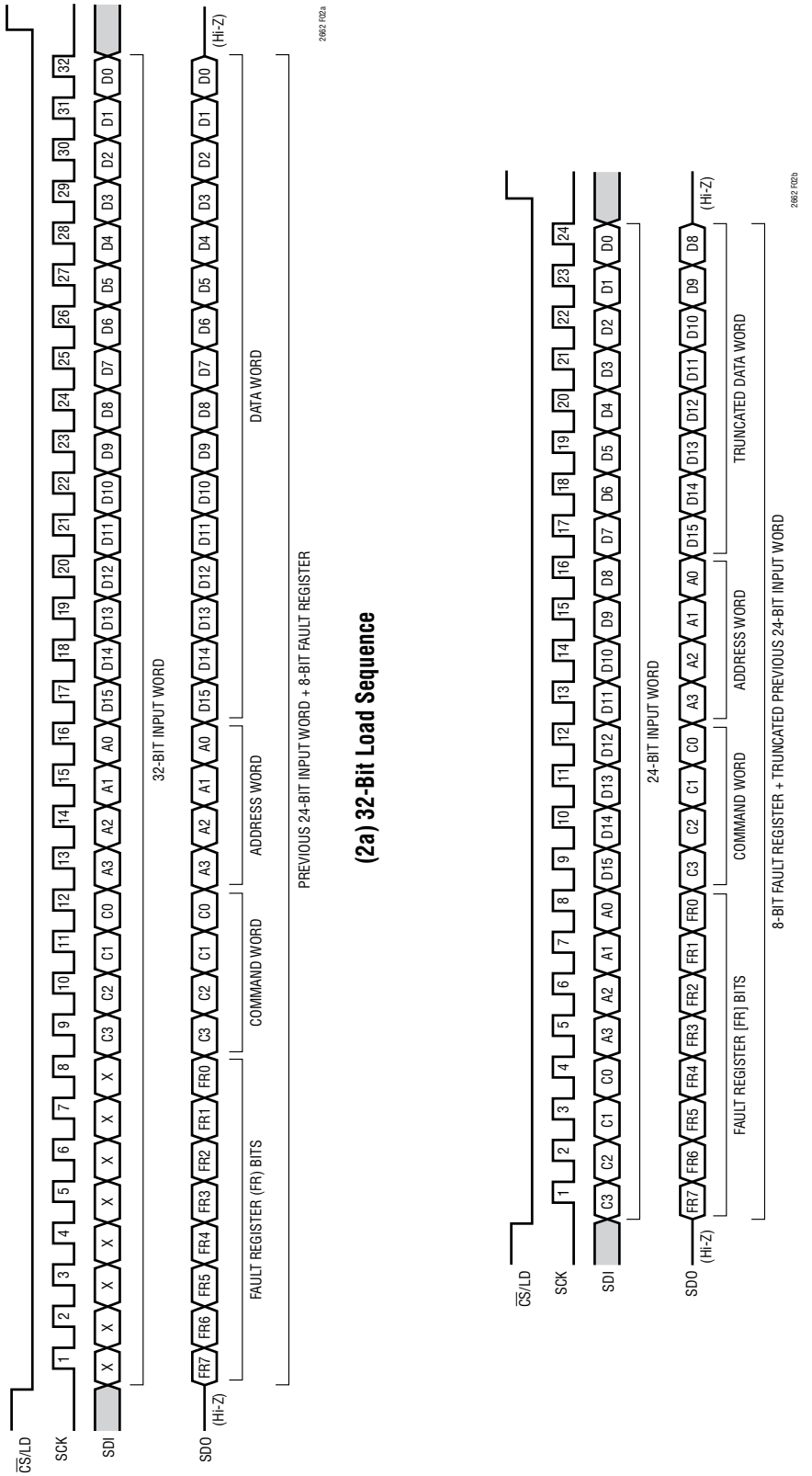


Figure 2. LTC2662-16 Load Sequences

OPERATION

The LTC2662 is a family of five-channel, current source output digital-to-analog converters (DACs) with selectable output ranges, precision reference and a high-voltage multiplexer (MUX) for surveying the channel output voltages and currents. Each output draws its current from a separate dedicated positive supply pin that accepts voltages of 2.85V to 33V, allowing optimization of power dissipation and headroom for a wide range of loads. Internal 12Ω switches allow any output pin to be connected to an optional negative V^- supply voltage and sink up to 80mA.

Power-On-Reset

The outputs reset to a high-impedance state on power up, making system initialization consistent and repeatable. After power-on initialization, select the output range via SPI bus using Tables 1, 2 and 3.

Power Supply Sequencing and Start-Up

The supplies (V_{CC}, IOV_{CC}, V^+, V^- and V_{DD0} to V_{DD4}) may be powered up in any convenient order. If an external reference is used, do not allow the input voltage at REF to rise above V_{CC} + 0.3V during supply turn-on and turn-off sequences (see the Absolute Maximum Ratings section).

After start-up, IOV_{CC} should be within V_{CC}; and no supply should exceed V^+. DC reference voltages of 1.225V to 1.275V are acceptable.

Supply bypassing is critical to achieving the best possible performance. Use at least 1µF of low-ESR capacitance to ground on all supply pins and locate as close to the device as possible. A 0.1µF capacitor may be used for IOV_{CC}.

Table 1. Command Codes

COMMAND				
C3	**C2**	**C1**	**C0**	
0	0	0	0	Write Code to *n*
1	0	0	0	Write Code to All
0	1	1	0	Write Span to n
1	1	1	0	Write Span to All
0	0	0	1	Update *n* (Power Up)
1	0	0	1	Update All (Power Up)
0	0	1	1	Write Code to *n*, Update *n* (Power Up)
0	0	1	0	Write Code to *n*, Update All (Power Up)
1	0	1	0	Write Code to All, Update All (Power Up)
0	1	0	0	Power Down *n*
0	1	0	1	Power Down Chip
1	0	1	1	Monitor Mux
1	1	0	0	Toggle Select
1	1	0	1	Global Toggle
0	1	1	1	Config Command
1	1	1	1	No Operation

Table 2. DAC Addresses, n

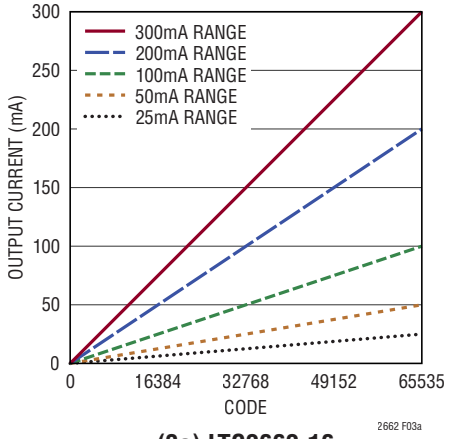
ADDRESS				
A3	**A2**	**A1**	**A0**	
0	0	0	0	DAC 0
0	0	0	1	DAC 1
0	0	1	0	DAC 2
0	0	1	1	DAC 3
0	1	0	0	DAC 4

Note: Any DAC address code used other than the codes given above in Table 2 will cause the command to be ignored.

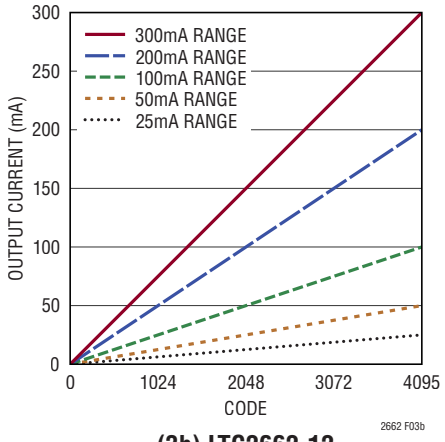
Data Transfer Functions

The DAC input-to-output transfer functions for all resolutions and output ranges greater than or equal to 25mA are shown in Figure 3. The input code is in straight binary format for all ranges.

OPERATION



(3a) LTC2662-16



(3b) LTC2662-12

Figure 3. Transfer Function

Serial Interface

When the $\overline{CS}$/LD pin is taken low, the data on the SDI pin is loaded into the shift register on the rising edge of the clock (SCK pin). The 4-bit command, C3-C0, is loaded first, followed by the 4-bit DAC address, A3-A0, and finally the 16-bit data word in straight binary format. For the LTC2662-16, the data word comprises the 16-bit input code, ordered MSB-to-LSB. For the LTC2662-12, the data word comprises the 12-bit input code, ordered MSB-to-LSB, followed by four don't-care bits. Data can only be transferred to the LTC2662 when the $\overline{CS}$/LD signal is low. The rising edge of $\overline{CS}$/LD ends the data transfer and causes the device to carry out the action specified in the 24-bit input word.

While the minimum input word is 24 bits, it may optionally be extended to 32 bits. To use the 32-bit word width, 8 don't-care bits must be transferred to the device first, followed by the 24-bit word, as just described. The 32-bit word is required for daisy-chain operation. It also provides accommodation for processors that have a minimum word width of 16 or more bits. The complete 24-bit and 32-bit sequences are shown in Figure 2a and Figure 2b. Note that the Fault Register outputs appear on the SDO pin for either word width.

Input and DAC Registers

The LTC2662 has five internal registers for each DAC, in addition to the main shift register. Each DAC channel has two sets of double-buffered registers: one set for the code data, and one set for the span (output range) of the DAC. Double buffering provides the capability to simultaneously update the span and code, which allows smooth current transitions when changing output ranges. It also permits the simultaneous updating of multiple DACs.

Each set of double-buffered registers comprises an input register and a DAC register:

- Input Register: The write operation shifts data from the SDI pin into a chosen register. The input registers are holding buffers; write operations do not affect the DAC outputs

  In the code data path, there are two input registers, A and B, for each DAC register. Register B is an alternate register used only in the toggle operation, while register A is the default input register

- DAC Register: The update operation copies the contents of an input register to its associated DAC register. The content of a DAC register directly controls the DAC output current or range. The update operation also powers up the selected DAC if it had been in power-down mode.

Note that updates always refresh both code and span data, but the values held in the DAC registers remain unchanged unless the associated input register values have been changed via a write operation. For example, if a new code is written and the channel is updated, the code is updated while the span is refreshed unchanged. A channel update can come from a serial update command, an LDAC negative pulse or a toggle operation.

OPERATION

Output Ranges and SoftSpan Operation

The LTC2662 is a five-channel current DAC with selectable output ranges. The full set of current output ranges is only available through SPI programming.

Figure 5 shows a simplified diagram of a single channel of the LTC2662. The full-scale current range of the LTC2662 is selected via four control bits S(3:0) on a per channel basis. Also provided is the ability to provide an external reference or to use a precision external resistor at pin FSADJ to reduce the overall gain drift over temperature of the LTC2662.

The LTC2662 initializes at power-on with all channel outputs (OUT0 to OUT4) at Hi-Z. The range and code of each channel are then fully programmable through SoftSpan as given in Table 3.

Each channel has a set of double-buffered registers for range information. Program the span input register using the *write span n* or *write span all* commands (0110b and 1110b, respectively). Figure 4 shows the syntax, and Table 3 shows the span codes and ranges.

As with the double-buffered code registers, update operations copy the span input registers to the associated span DAC registers.

Table 3. Span Codes

				OUTPUT RANGE	
S3	S2	S1	S0	External R_{FSADJ}	FSADJ = V_{CC}
0	0	0	0	(Hi-Z)	
0	0	0	1	$50 \cdot V_{REF}/R_{FSADJ}$	3.125mA
0	0	1	0	$100 \cdot V_{REF}/R_{FSADJ}$	6.25mA
0	0	1	1	$200 \cdot V_{REF}/R_{FSADJ}$	12.5mA
0	1	0	0	$400 \cdot V_{REF}/R_{FSADJ}$	25mA
0	1	0	1	$800 \cdot V_{REF}/R_{FSADJ}$	50mA
0	1	1	0	$1600 \cdot V_{REF}/R_{FSADJ}$	100mA
0	1	1	1	$3200 \cdot V_{REF}/R_{FSADJ}$	200mA
1	1	1	1	$4800 \cdot V_{REF}/R_{FSADJ}$	300mA
1	0	0	0	(Switch to V^-)	

As shown in Table 3, there are two additional selections (code 0000 and code 1000) which place the output(s) in a high impedance (Hi-Z) mode or in a mode where a low on-resistance (≤12Ω) NMOS device shunts the DAC output to the negative supply V^-. When the NMOS device is enabled, the OUTX pin driver is disabled for that channel(s). Span codes not listed in Table 3 default to the Hi-Z output range.

Monitor Mux

The LTC2662 includes a high voltage multiplexer (mux) for monitoring both the voltages and currents at the five current output pins (OUT0 to OUT4). Additionally, the output supply voltages (V_{DD0} to V_{DD4}), the positive/negative supplies V^+/V^-, core supply V_{CC}, reference voltage V_{REF} and die temperature can all be monitored.

The MUX pin is intended for use with high impedance inputs only; the impedance at the pin is typically 15kΩ. Continuous DC output current at the MUX pin must be limited to ±1mA to avoid damaging internal circuitry.

The operating range of the mux extends rail-to-rail from V^- to V^+; its output is disabled (high impedance) at power-up.

The syntax and codes for the *mux* command are shown in Figure 6 and Table 4.

Current Measurement Using the Mux

Measure the current of any output pin by using the *mux* command (1011b) along with one of the mux current measurement codes from Table 4. The mux responds by outputting a voltage proportional to the actual output current. The proportionality factor is given by the following equation:

$$I_{OUTX} = I_{FS} \cdot V_{MUX}/V_{REF} \quad (1)$$

The V_{MUX} pin voltage has the same excellent linearity as the current outputs, but calibrating for slope error (±15% FSR) is necessary for accurate results. ±1% FSR accuracy is easily achievable with a one- or two-point calibration.

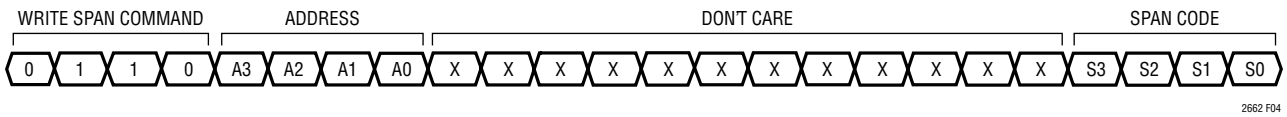


Figure 4. Write Span Syntax

OPERATION

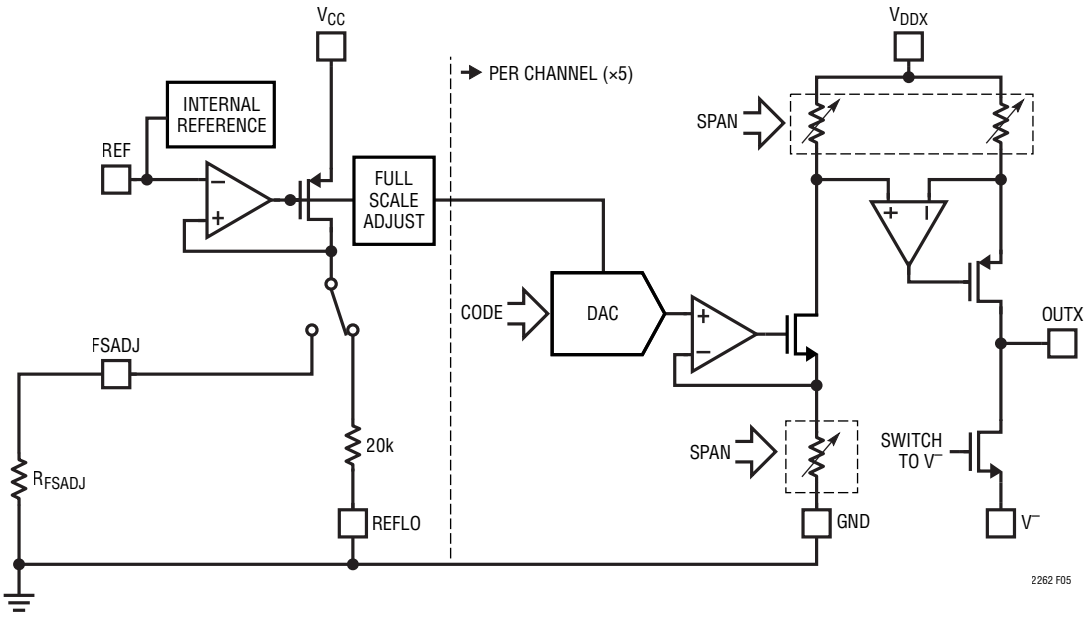


Figure 5. LTC2662 Single Channel Simplified Diagram

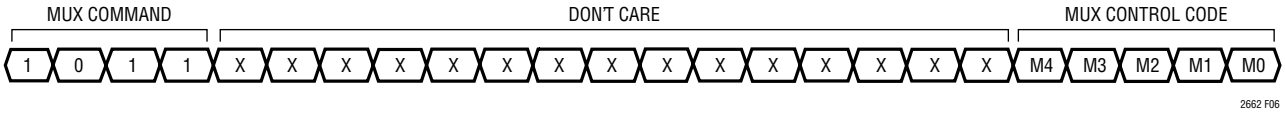


Figure 6. Mux Command

Note that for a given V_{REF} and DAC code, V_{MUX} is constant and does not vary by range; but full-scale current I_{FS} has a different value for each output range. If the channel's range is set to Hi-Z or Short-to-V^-, or if it is in dropout (flagged by fault register bits FR0 to FR4), the voltage is not representative of the pin current.

Die Temperature Measurement Using the Mux

Measure the die temperature by using the *mux* command along with mux control code 01010b. The V_{MUX} pin voltage in this case is linearly related to the die temperature by a temperature coefficient of –3.7mV/°C. The measured junction temperature T_J is then

$$T_J = 25°C + (1.4V – V_{MUX})/(3.7mV/°C)$$

If needed, the temp monitor can be calibrated by measuring the initial temperature and voltage, and then substituting these values for 25°C and 1.4V, respectively, in the equation.

Monitor Mux Pre-Charge Considerations

The analog multiplexer in the LTC2662 is unbuffered. This obviates error terms from amplifier offsets; but without buffers, the high-impedance current outputs could be disturbed due to charge transfer at the moment when the MUX pin is connected. The LTC2662 contains circuitry that suppresses charging glitches on the output pins (OUT0 to OUT4) by pre-charging the MUX pin before connecting it to the output.

OPERATION

Table 4. Monitor Mux Control Codes

M4	M3	M2	M1	M0	MUX PIN OUTPUT	NOTES:
0	0	0	0	0	Disabled (Hi-Z)	
0	0	0	0	1	OUT0 Current Measurement	$I_{OUT0} = I_{FS} \bullet V_{MUX}/V_{REF}$
0	0	0	1	0	OUT1 Current Measurement	$I_{OUT1} = I_{FS} \bullet V_{MUX}/V_{REF}$
0	0	0	1	1	OUT2 Current Measurement	$I_{OUT2} = I_{FS} \bullet V_{MUX}/V_{REF}$
0	0	1	0	0	OUT3 Current Measurement	$I_{OUT3} = I_{FS} \bullet V_{MUX}/V_{REF}$
0	0	1	0	1	OUT4 Current Measurement	$I_{OUT4} = I_{FS} \bullet V_{MUX}/V_{REF}$
0	0	1	1	0	V_{CC}	
0	1	0	0	0	V_{REF}	
0	1	0	0	1	V_{REFLO}	DAC Reference GND
0	1	0	1	0	Die Temperature, T	$T = 25°C + (1.4V – V_{MUX})/(0.0037V/°C)$
1	0	0	0	0	V_{DD0}	
1	0	0	0	1	V_{DD1}	
1	0	0	1	0	V_{DD2}	
1	0	0	1	1	V_{DD3}	
1	0	1	0	0	V_{DD4}	
1	0	1	0	1	V^+	
1	0	1	1	0	$V^–$	
1	0	1	1	1	GND	
1	1	0	0	0	OUT0 Pin Voltage	
1	1	0	0	1	OUT1 Pin Voltage	
1	1	0	1	0	OUT2 Pin Voltage	
1	1	0	1	1	OUT3 Pin Voltage	
1	1	1	0	0	OUT4 Pin Voltage	

Due to the pre-charge behavior, the mux output becomes valid approximately 7µs after the Mux command is given ($\overline{CS}$/LD rising). Residual charging transients can be further reduced by adding capacitance to the output pins if needed. Do not add capacitance to the MUX pin, as this potentially increases the disturbance to the outputs during mux switching. Up to 100pF on the MUX pin is allowable.

Toggle Operations

Some systems require that the DAC outputs switch repetitively between two output levels (i.e. switching between an 'on' and 'off' state). The LTC2662 toggle function facilitates these kinds of operations by providing two input registers (A and B) per DAC channel.

Toggling between A and B is controlled by three signals. The first of these is the *toggle select* command, which acts on the data field of 5 bits, each of which controls a single channel (see Figure 7). The second is the *global toggle* command, which controls all selected channels using the global toggle bit TGB (see Figure 8). Finally, the TGP pin allows the use of an external clock or logic signal to toggle the DAC outputs between A and B. The signals from these controls are combined as shown in Figure 9.

If the toggle function is not needed, tie TGP (Pin 2) to ground and leave the toggle select register in its power-on reset state (cleared to zero). Input registers A then function as the sole input registers, and registers B are not used.

OPERATION

Toggle Select Register (TSR)

The *toggle select* command (1100b) syntax is shown in Figure 7. Each bit in the 5-bit TSR data field controls the DAC channel of the same name: T0 controls channel 0, T1 channel 1… and T4 controls channel 4.

The toggle select bits (T0, T1… T4) have a dual function. First, each toggle select bit controls which input register (A or B) receives data from a write-code operation. When the toggle select bit of a given channel is high, write-code operations are directed to input register B of the addressed channel. When the bit is low, write-code operations are directed to input register A. Secondly, each toggle select bit enables the corresponding channel for a toggle operation.

Writing to Input Registers A and B

Having chosen channels to toggle, write the desired codes to input registers A for the chosen channels; then set the channels' toggle select bits using the *toggle select* command; and finally, write the desired codes to input registers B. Once these steps are completed, the channels are ready to toggle. For example, to set up channel 3 to toggle between codes 4096 and 4200:

1) *Write code* channel 3 (code = 4096) to register A

   00000011 00010000 00000000

2) *Toggle select* (set bit T3)

   11000000 00000000 00001000

3) *Write code* channel 3 (code = 4200) to register B

   00000011 00010000 01101000

The *write code* of step (3) is directed to register B because in step (2), bit T3 was set to 1. Channel 3 now has input registers A and B holding the two desired codes, and is prepared for the toggle operation.

Note: After writing to register B, the code for register A can still be changed. The state of the Toggle Select bit determines to which register (A or B) a write is directed.

First, toggle select bit T3 has to be reset to 0:

11000000 00000000 00000000

Then write the new register A code. Let's say the new code is 4300, so the instruction would be:

00000011 00010000 11001100

After that, set toggle select bit T3 to 1 again [step 2 above]. It is not necessary to write to register B again; channel 3 is ready for the toggle operation.

Toggling Between Registers A and B

Once input registers A and B have been written to for all desired channels and the corresponding toggle-select bits are set high, as in the previous example, the channels are ready for toggling.

The LTC2662 supports three types of toggle operations: a first in which all selected channels are toggled together using the SPI port; a second in which all selected channels are toggled together using an external clock or logic signal; and a third in which any combination of channels can be instructed to update from either input register A or B.

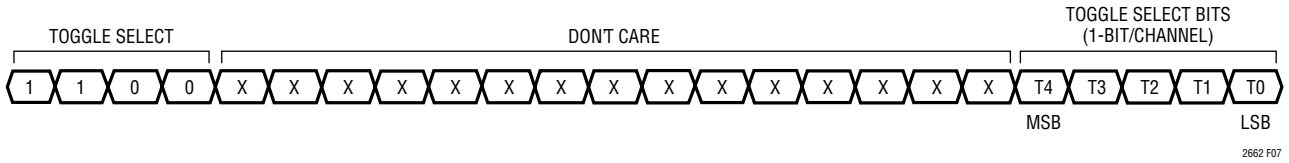


Figure 7. Toggle Select Syntax

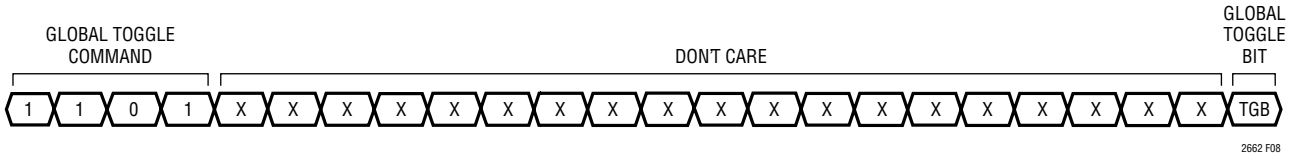


Figure 8. Global Toggle Syntax

OPERATION

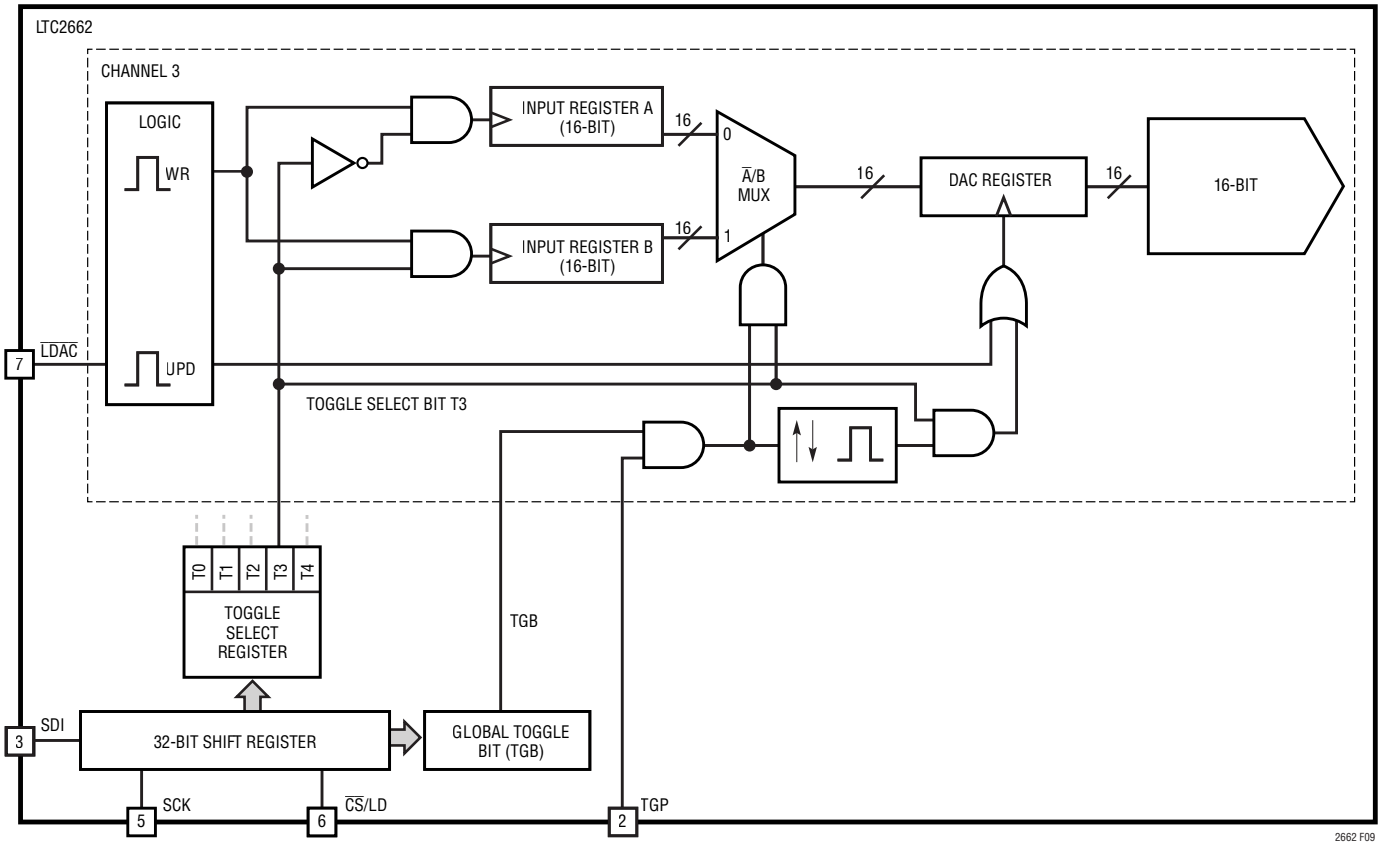


Figure 9. Conceptual Block Diagram—Toggle Functionality

The internal toggle-update circuit is edge triggered, so only transitions (of TGB or TGP) trigger an update from the respective input register.

To toggle all selected channels together using the SPI port, ensure the TGP pin is high and that the bits in the toggle select register corresponding to the desired channels are also high. Use the global command (1101b) to alternate codes, sequentially changing the global toggle bit TGB (see Figure 8). Changing TGB from 1 to 0 updates the DAC registers from their respective input registers A. Changing TGB from 0 to 1 updates the DAC registers from their respective input registers B. Note that in this way up to 5 channels may be toggled with just one serial command.

To toggle all selected channels using an external logic signal, ensure that the TGB bit in the global toggle register is high and that in the toggle select register, the bits corresponding to the desired channels are also high. Apply a clock or logic signal to the TGP pin to alternate codes. TGP falling edges update the DAC registers from their associated input registers A. TGP rising edges update the DAC registers from their associated input registers B. Note that once the input registers are set up, all toggling is triggered by the signal applied to the TGP pin, with no further SPI instructions needed.

To cause any combination of channels to update from either input register A or B, ensure the TGP pin is high and that the TGB bit in the global toggle register is also high. Using the *toggle select* command set the toggle

OPERATION

select bits as needed to select the input register (A or B) with which each channel is to be updated. Then update all channels, either by using the serial command (1001b) or by applying a negative pulse to the LDAC pin. Any channels whose toggle select bits are 0 update from input register A, while channels whose toggle select bits are 1 update from input register B (see Figure 9). By alternating toggle select and update operations, up to 5 channels can be simultaneously switched to A or B as needed.

Daisy-Chain Operation

The serial output of the shift register appears at the SDO pin. Data transferred to the device from the SDI input is delayed 32 SCK rising edges before being output at the next SCK falling edge, suitable for clocking into the microprocessor on the next 32 SCK rising edges.

The SDO output can be used to facilitate control of multiple serial devices from a single 3-wire serial port (i.e. SCK, SDI and $\overline{CS}$/LD). Such a daisy-chain series is configured by connecting the SDO of each upstream device to the SDI of the next device in the chain. The shift registers of the devices are thus connected in series, effectively forming a single input shift register which extends through the entire chain. Because of this, the devices can be addressed and controlled individually by simply concatenating their input words; the first instruction addresses the last device in the chain and so forth. The SCK and $\overline{CS}$/LD signals are common to all devices in the series.

In use, $\overline{CS}$/LD is first taken low. Then, the concatenated input data is transferred to the chain, using the SDI of the first device as the data input. When the data transfer is complete, $\overline{CS}$/LD is taken high, completing the instruction sequence for all devices simultaneously. A single device can be controlled by using the *no-operation* command (1111b) for all other devices in the chain. When $\overline{CS}$/LD is taken high, the SDO pin presents a high impedance output, so a pull-up resistor is required at the SDO of each device (except the last) for daisy-chain operation.

Echo Readback

The SDO pin can be used to verify data transfer to the device. During each 32-bit instruction cycle, SDO outputs the previous 32-bit instruction for verification. The 8-bit "don't-care" prefix is replaced by 8 Fault Register status bits, followed by the 4-bit command and address words and the full 16-bit data word (see Figure 2a). The SDO sequence for a 24-bit instruction cycle is the same, except that the data word is truncated to 8 bits (see Figure 2b). When $\overline{CS}$/LD is high, SDO presents a high impedance output, releasing the bus for use by other SPI devices.

Fault Register (FR)

The LTC2662 provides notifications of operational fault conditions. The fault register (FR) status bits comprise the first data byte (8 bits) of each 24- or 32-bit SDO word, outputted to the SDO pin during every SPI transaction. See Figure 2 for sequences.

An FR bit is set when its trigger condition is detected, and clocked to SDO during the next SPI transaction. FR information is updated with each SPI transaction. Note that if a fault condition is corrected by the action of an SPI instruction, the cleared FR flag for that condition is observable at SDO on the next SPI transaction.

Table 5 lists the Fault Register bits and their associated trigger conditions.

Table 5. Fault Register (FR)

FR Bit	Fault Condition
FR0	Open-Circuit condition detected on OUT0
FR1	Open-Circuit condition detected on OUT1
FR2	Open-Circuit condition detected on OUT2
FR3	Open-Circuit condition detected on OUT3
FR4	Open-Circuit condition detected on OUT4
FR5	Overtemperature. If die temperature $T_J > 175°C$, FR5 is set and thermal protection is activated. Can be disabled using the Config command (0111b).
FR6	Power Limit. If $V_{DDX} - V_{OUTX} > 10V$ and the current range is ≥ 200mA, FR6 is set and the range for that channel is reduced to 100mA. Can be disabled using the *Config* command (0111b).
FR7	Invalid SPI sequence length. Valid sequence lengths are 24, 32 and multiples of 32 bits. For all other lengths, FR7 is set and the SPI instruction is ignored.

OPERATION

Fault Indicator Pin ($\overline{\text{FAULT}}$, Pin 30)

The $\overline{\text{FAULT}}$ pin is an open-drain N-channel output that pulls low when a fault condition is detected. It is released on the next rising $\overline{\text{CS}}$/LD edge. The pin is an open-drain output suitable for wired-OR connection to an interrupt bus; a pull-up resistor on the bus is required.

Fault Conditions and Thermal Overload Protection

There are four types of fault conditions that cause the $\overline{\text{FAULT}}$ pin to pull low. First, FR0 to FR4 flag an open-circuit (OC) condition on any of the output pins (OUT0 to OUT4, respectively) when an output channel enters dropout due to insufficient voltage from V_{DDX} to OUTx. Independent open-circuit detection is provided for each of the five DAC current output pins.

FR5 provides a detection flag which is set when the die temperature exceeds 175°C. The overtemperature condition also forces all five DAC channels to power down and the open-drain $\overline{\text{FAULT}}$ pin to pull low. FR5 remains set and the device stays in shutdown until the die cools. Below approximately 150°C the DAC channels can be returned to normal operation. Note that a $\overline{\text{CS}}$/LD rising edge releases the $\overline{\text{FAULT}}$ pin regardless of the die temperature.

Since any DAC channel can source up to 300mA, die heating potential of the system design should be evaluated carefully. FR6, a power-limit protection flag, is provided to help prevent accidental damage to the current output device(s). The power-limit fault condition is triggered for the 200mA and 300mA full-scale current spans when the voltage difference between an output supply pin (V_{DDX}) and its current output pin (OUTX) is ≥10V.

Finally, FR7 is provided to flag invalid SPI word lengths. Valid word lengths are 24 bits, 32 bits, and integer multiples of 32 bits; any other length causes FR7 to set, the $\overline{\text{FAULT}}$ pin to assert, and the instruction itself to be ignored.

Config Command

The Config command has four arguments—OC, PL, TS and RD (see Figure 10).

Setting the OC bit disables open-circuit detection (FR0 to FR4). Likewise, the PL bit disables power-limit protection (FR6); and the TS bit disables thermal protection (FR5). Use these options with caution, particularly PL and TS.

The RD bit is used to select external-reference operation. The REFCOMP pin must be grounded for external reference use whether the RD bit is set or not.

Power-Down Mode

For power-constrained applications, power-down mode can be used to reduce the supply current whenever less than five DAC outputs are needed. When in power-down, the voltage-to-current output drivers and reference buffers are disabled. The current DAC outputs are put into a high impedance state. Register contents are not disturbed during power-down.

Any channel or combination of channels can be put into power-down mode by using command 0100b in combination with the appropriate DAC address. In addition, all the DAC channels and the integrated reference together can be put into power-down using the Power-Down Chip command, 0101b. The 16-bit data word is ignored for all power-down commands.

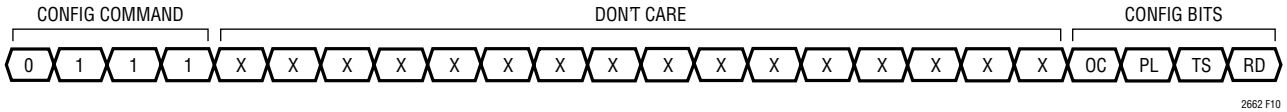


Figure 10. Config Command Syntax: Open-Circuit Detection Disable (OC), Power Limit Protection Disable (PL), Thermal Shutdown Disable (TS) and Reference Disable (RD)

OPERATION

Normal operation resumes by executing any command which includes a DAC update—either in software, as shown in Table 1 or by toggling (see the Types of Toggle Operations section). The selected DAC channel is powered up as it is updated with the new code value. When updating a powered-down DAC, add wait time to accommodate the extra pow-er-up delay. If the channels have been powered down (command 0100b) prior to the update command, the power-up delay time is 30µs. If, alternatively the chip has been powered down (command 0101b), the power-up delay time is 35µs.

Valid Supply Ranges

The valid supply ranges for the LTC2662 have several restrictions as described in the Electrical Characteristics table (Power Requirements) and the Pin Functions section. The voltage at V^+ (Pin 27) must be greater than or equal to all other supply voltages. V^+ is allowed to be up to 33V above $V^–$. The five output supplies (V_{DD0} to V_{DD4}) may be independently set between 2.85V and V^+. The negative supply, $V^–$, may be any voltage between –15.75V and GND, but note again that V^+ must be no more than 33V above $V^–$.

Current Outputs

The LTC2662 incorporates a high-gain voltage-to-current converter at each current output pin. INL and DNL are guaranteed for all ranges from 3.125mA to 300mA if the minimum dropout voltage ($V_{DDX} – V_{OUTX}$) is met for all DAC codes.

If sufficient dropout voltage is maintained, the DC output impedances of the current outputs (OUT0 to OUT4) are very high. Each current output has a dedicated positive supply pin, V_{DD0} to V_{DD4}, to allow the tailoring of each channel's current compliance and power dissipation.

Switch-to-$V^–$ Mode

Span code 1000b can be used to pull outputs below GND. In Switch-to-$V^–$ mode, the output current is turned off for the addressed channel(s), and the channel voltage V_{OUTX} pulls to $V^–$. The pulldown switch can sink up to 80mA at an effective resistance of 12Ω max.

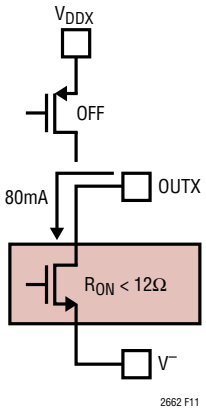


Figure 11. Switch-to-$V^–$ Mode

Switch-to-$V^–$ mode can be invoked with the *write span to all* or *write span to n* command and the desired address. Span codes are shown in Table 3; a diagram of an output in Switch-to-$V^–$ mode is shown in Figure 11.

Gain Adjustment Using the FSADJ Pin

The full-scale output currents are proportional to the reference voltage, and inversely proportional to the resistance associated with FSADJ. That is:

$$I_{OUTFS} \sim V_{REF}/R_{FSADJ}.$$

If the FSADJ pin is tied to V_{CC}, the LTC2662 uses an internal R_{FSADJ} = 20k. Optionally, FSADJ can instead be connected to a grounded external resistor to tune the default current ranges to the application, or for the best possible temperature coefficient using an appropriately-specified precision resistor. Values from 19k to 41k are supported. The new current ranges can easily be calculated using the 'External R_{FSADJ}' column of Table 3. The internal resistor is automatically disconnected when using an external resistor.

When using an external resistor, FSADJ is sensitive to stray capacitance; the pin should be compensated with a snubber network consisting of a series combination of 1k and 1µF, connected in parallel to R_{FSADJ}. With the recommended compensation, the pin is stable driving stray capacitance of up to 50pF.

OPERATION

Offset Current and Code Zero

The offset current error of the LTC2662 is guaranteed ±0.4%FSR maximum. If the offset of a given channel is positive, some nonzero current flows at code zero; if negative, the current is zero (leakage only) for a range of codes close to zero. Offset and linearity endpoints are measured at code 384 (LTC2662-16) or 24 (LTC2662-12), guaranteeing that the DAC is operating with a measurable output current at the point of measurement.

A channel with a positive offset error may not completely turn off, even at code zero. To turn an output completely off, set the range to "Hi-Z" (span code 0000b from Table 3), and update the channel.

Reference Modes

The LTC2662 can be used with either an internal or external reference. As with voltage DACs, the reference voltage scales the outputs, so that the outputs reflect any errors in the reference. Full scale output currents are limited to 300mA maximum per channel regardless of reference voltage.

The internal 1.25V reference has a typical temperature drift of ±2ppm/°C and an initial output tolerance of ±2mV max. It is trimmed, tested and characterized independent of the DACs; and the DACs are tested and characterized with an "ideal" external reference.

To use the internal reference, the REFCOMP pin should be left floating, with no DC path to GND. In addition, the RD bit in the Config register must have a value of 0. This value is reset to 0 at power-up, or it can be reset using the *config* command, 0111b. Figure 9 shows the command syntax.

For reference stability and low noise, a 0.1µF capacitor should be tied between REFCOMP and GND. In this configuration, the internal reference can drive up to 0.1µF with excellent stability. To ensure stable operation, the capacitive load on the REF pin should not exceed that on the REFCOMP pin. A buffer is needed if the internal reference is to drive external circuitry.

To use an external reference, tie the REFCOMP pin to GND. This disables the output of the internal reference at start-up, so that the REF pin becomes a high-impedance input. Apply the reference voltage at the REF pin after powering up. Set the RD bit to 1 using the *config* command, 0111b. The REF input voltage range is 1.225V to 1.275V.

Board Layout

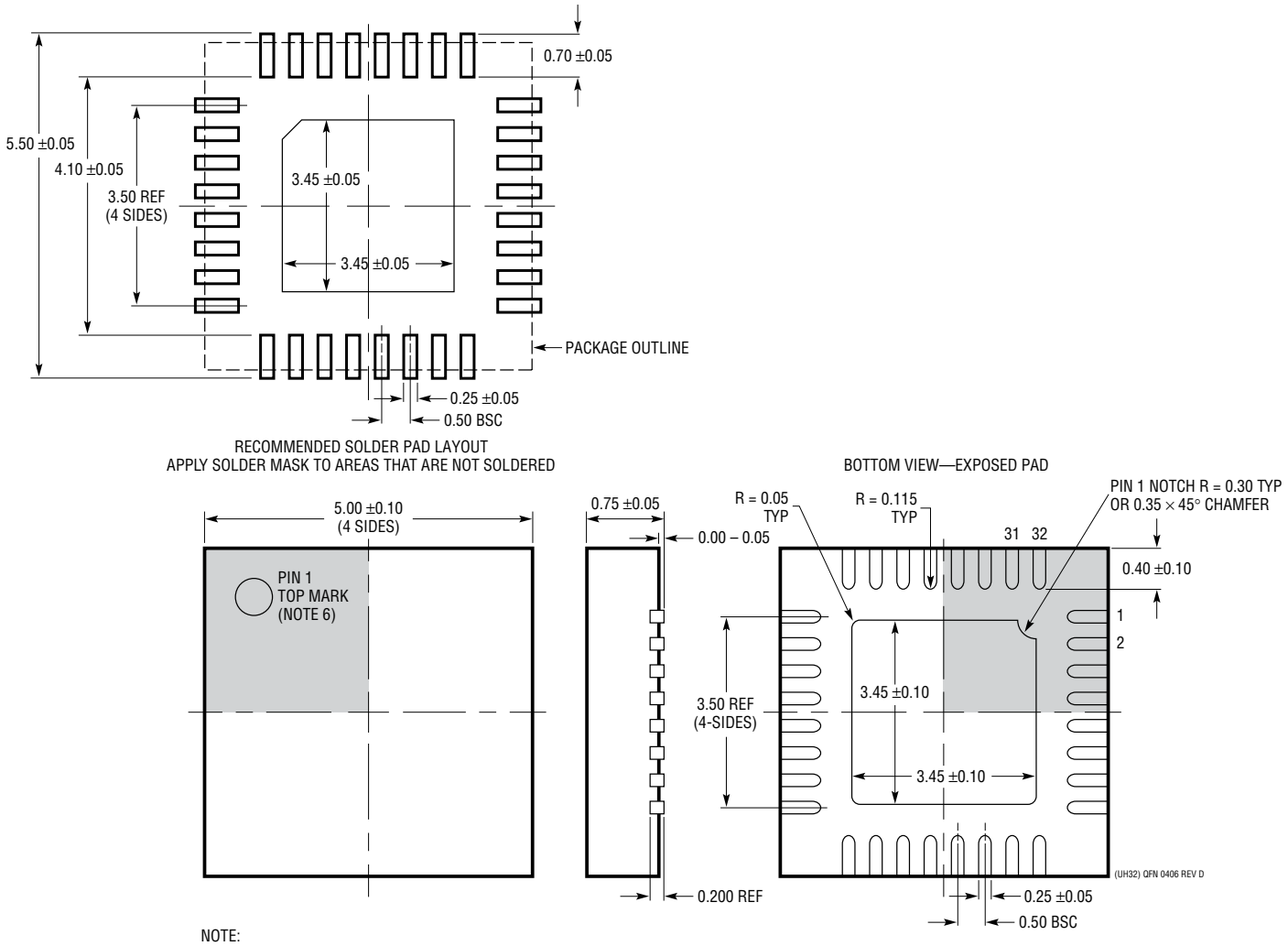
The excellent load regulation and DC crosstalk performance of these devices is achieved in part by minimizing common-mode resistance of signal and power grounds.

As with any high resolution converter, clean board grounding is important. A low impedance analog ground plane is necessary, as are star-grounding techniques. Keep the board layer used for star-ground continuous to minimize ground resistances; that is, use the star-ground concept without using separate star traces. Resistance from the REFLO pin to the star point should be as low as possible. The exposed pad (Pin 33) is recommended as the star ground point.

For best performance, stitch the ground plane with arrays of vias on 150 to 200 mil centers connecting it with the ground pours from the other board layers. This reduces the overall ground resistance and minimizes ground loop area.

PACKAGE DESCRIPTION

UH Package
32-Lead Plastic QFN (5mm × 5mm)
(Reference LTC DWG # 05-08-1693 Rev D)

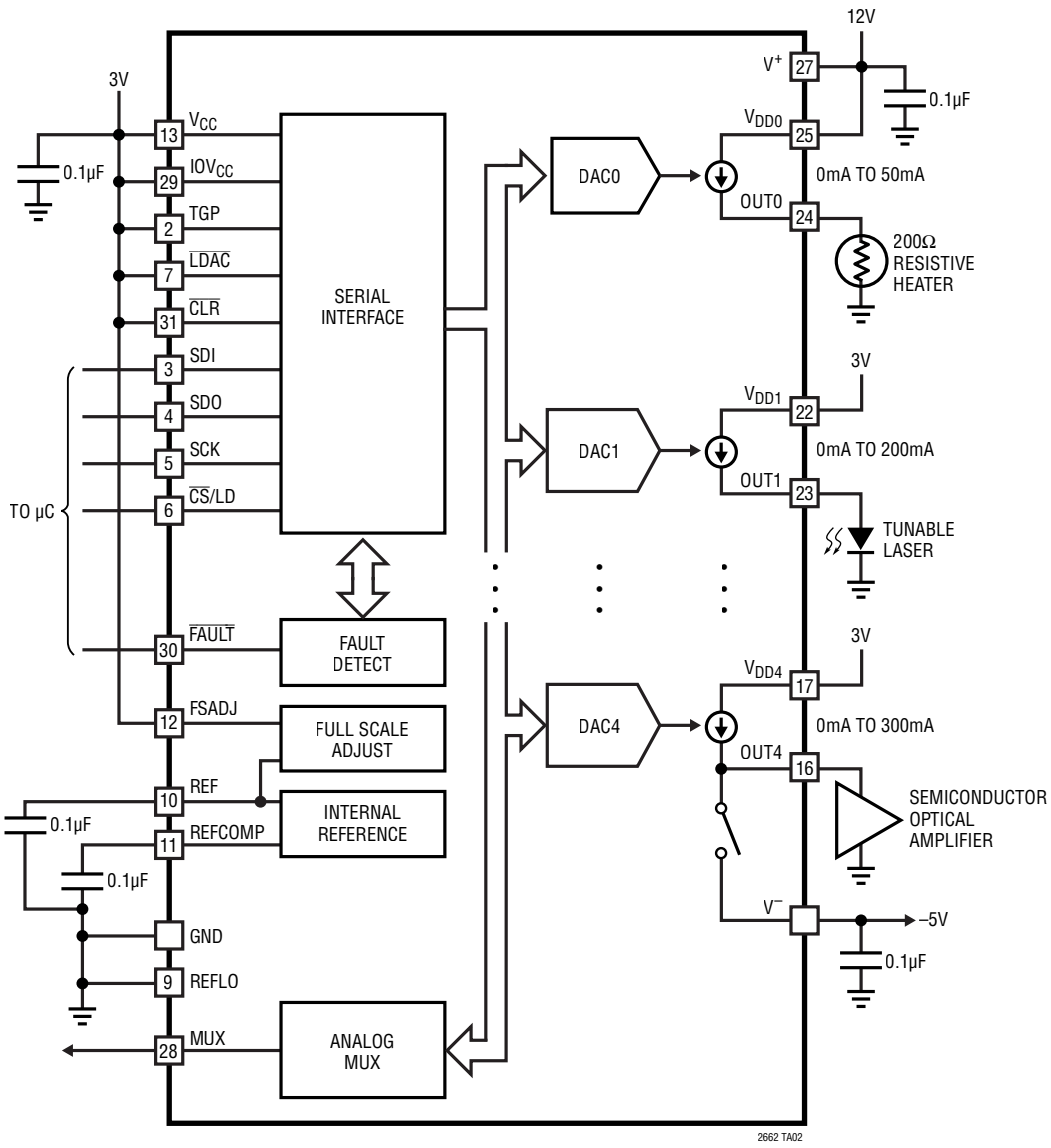


NOTE:
1. DRAWING PROPOSED TO BE A JEDEC PACKAGE OUTLINE
   M0-220 VARIATION WHHD-(X) (TO BE APPROVED)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE
   MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.20mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION
   ON THE TOP AND BOTTOM OF PACKAGE

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	01/19	Add LTC2662-12	1, 4-12, 16-17, 23-26, 28

TYPICAL APPLICATION



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC2668	16-Channel Serial 16-/12-Bit V_{OUT} SoftSpan DACs with ±10ppm/°C Reference	Software-Programmable Output Ranges Up to ±10V, 6mm × 6mm QFN Package
LTC2666	Octal Serial 16-/12-Bit V_{OUT} SoftSpan DACs with ±10ppm/°C Reference	Software-Programmable Output Ranges Up to ±10V, 5mm × 5mm QFN Package
LTC2664	Quad Serial 16-/12-Bit V_{OUT} SoftSpan DACs with ±10ppm/°C Reference	Software-Programmable Output Ranges Up to ±10V, 5mm × 5mm QFN Package
References		
LTC6655	Low Drift Precision Buffered Reference	0.025% Max Tolerance 2ppm/°C Max, 0.25ppm$_{P-P}$ 0.1Hz to 10Hz Noise