LM10010 VID Voltage Programmer for Point of Load Regulator

Check for Samples: LM10010

FEATURES

- **Output Current Accuracy (-40°C to +125°C)**
- **Input Voltage Range: 3V to 5.5V**
- **6-Bit Current DAC That Connects Directly to the Feedback Node of an External Regulator to Provide Output Voltage Control**
- **Precision Enable to Support Custom UVLO**
- **WSON-10 3 mm x 3 mm Footprint, 0.5 mm Pitch**
- **Compatible With the TMS320C66XX DSP Smart Reflex Technology**

APPLICATIONS

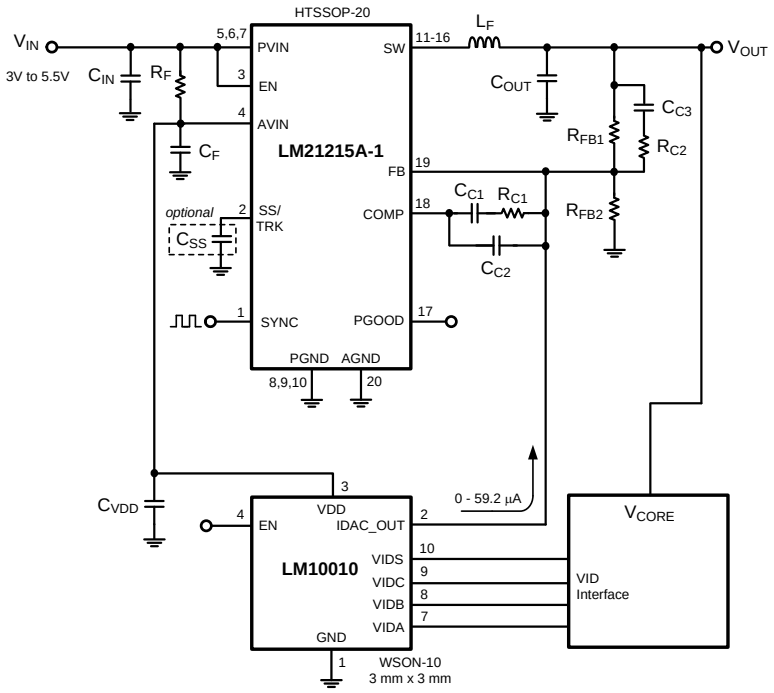
- **Broadband, Networking, and Wireless Communications**
- **Notebook and Palmtop Computers, PDAs**
- **Portable Instruments**
- **Battery-Powered Equipment**
- **Powering Digital Loads With a 6-Bit, 4 Pin VID Interface**

DESCRIPTION

The LM10010 is a precision, digitally programmed device used to control the output voltage of a DC/DC converter. The LM10010 outputs a DC current inversely proportional to a 6-bit input word. This current DAC output connects to the feedback pin of a regulator in order to adjust its output voltage to a desired range and resolution set by the user. As the 6-bit word counts up, the output voltage is adjusted higher based on the setting of the feedback resistors in the converter.

The LM10010 is designed to program point of load regulators with adjustable resistor feedback networks for VID (Voltage Identification).

Typical Application Circuit



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Connection Diagram

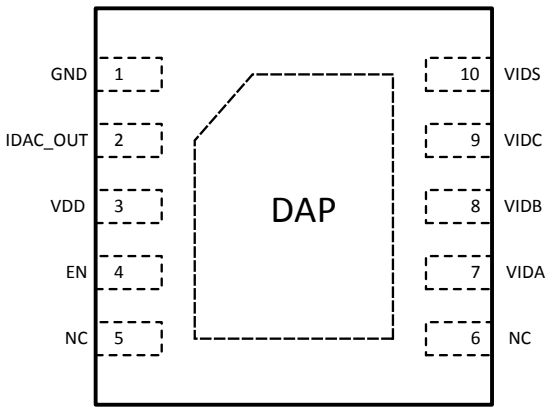


Figure 1. Top View
WSON-10 3mm x 3mm
0.5mm pitch

Pin Descriptions

Pin No.	Name	Description
1	GND	Ground.
2	IDAC_OUT	Output current DAC that connects to the feedback node of the regulator.
3	VDD	Positive supply input.
4	EN	Precision enable input.
5	NC	No Connect.
6	NC	No Connect.
7	VIDA	VID digital input: Bit 0 when VIDS transitions low; Bit 3 when VID transitions high.
8	VIDB	VID digital input: Bit 1 when VIDS transitions low; Bit 4 when VID transitions high.
9	VIDC	VID digital input: Bit 2 when VIDS transitions low; Bit 5 when VID transitions high.
10	VIDS	VID select line: Transition low selects lower 3 bits, Transition high selects upper 3 bits.
DAP	DAP	Die Attach Pad. Not electrically connected to device, connect to system ground plane for reduced thermal resistance.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings (1)(2)

VDD, EN, IDAC_OUT		-0.3V to 6V
VIDA, VIDB, VIDC, VIDS		-0.3V to 6V
ESD Rating(3)	Human Body Model	2 kV
Storage Temperature		-65°C to +150°C
Junction Temperature		+150°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not ensure specific performance limits. For ensured specifications and conditions, see the Electrical Characteristics.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
(3) The human body model is a 100 pF capacitor discharged through a 1.5 kΩ resistor into each pin.

Operating Ratings

VDD	3.0V to 5.5V
IDAC_OUT	-0.3V to VDD-1.75V
VIDA, VIDB, VIDC, VIDS	-0.3V to 5.5V
EN	-0.3V to 5.5V
Junction Temperature	−40°C to +125°C
Ambient Temperature	−40°C to +125°C
WSON-10 Thermal Resistance (θ_{JA})(1)	40°C/W

(1) Junction to ambient thermal resistance is highly application and board layout dependent. Specified thermal resistance values for the package specified is based on a 4-layer, 4"x3", 2/1/1/2 oz. Cu board as per JEDEC standards is used.

Electrical Characteristics

Limits in standard type are for T_J = 25°C only. Limits appearing in **boldface** type apply over the full operating junction temperature range (-40°C < T_J < +125°C). Unless otherwise noted, specifications apply to the Typical Application Circuit. See (1).

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
Supply, UVLO, and Enable						
I_Q	Quiescent current	VDD=5.0V, V_{EN}=2.0V		250	**280**	µA
		VDD=5.0V, V_{EN}=2.0V, I_{FS}		340		µA
		VDD=5.0V, V_{EN}=0.0V		45	**70**	µA
UVLO	Under voltage rising threshold			2.65	**2.95**	V
	Under voltage falling threshold		**2.2**	2.45		V
	Hysteresis		**100**	200	**300**	mV
V_{EN}	Enable rising threshold		**1.20**	1.34	**1.45**	V
	Enable hysteresis		**50**	100	**180**	mV
I_{EN}	Enable pullup current			2		µA
IDAC						
ACC	Accuracy	Measured at full scale	**2**		**-2**	%
LSB	DAC step size	I_{FS} /(2^6-1)		940		nA
Default	Output code	At startup		46d		Code
	Output current	At startup		16		µA
I_{FS}	Full-scale output current	VID[5:0] = 000000b		59.2		µA
INL	Integral non-linearity		**-1**	0.15	**1**	LSB

(1) All limits are ensured. All electrical characteristics having room temperature limits are tested during production at T_A = 25°C. All hot and cold limits are specified by correlating the electrical characteristics to process and temperature variations and applying statistical process control.

Electrical Characteristics (continued)

Limits in standard type are for T_J = 25°C only. Limits appearing in **boldface** type apply over the full operating junction temperature range (-40°C < T_J < +125°C). Unless otherwise noted, specifications apply to the Typical Application Circuit. See [(1)].

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
DNL	Differential non-linearity		**-0.25**	0.06	**0.25**	LSB
Offset	Offset current	VID[5:0] = 111111b		60		nA
V_{OUT_MAX}	Output compliance	VDD-V_{IDAC_OUT}, VDD=3V		1.3	**1.75**	V
VID Logic Inputs [(2)]						
V_{IL}	Input voltage low				**0.4**	V
V_{IH}	Input voltage high		**1.1**			V
I_{IL}	Input current low		**-5**			µA
I_{IH}	Input current high				**5**	µA
$t_{DEGLITCH}$	Input deglitch time			3.4		µs
t_1	VIDS delay time to VID latch	VIDS rising edge	**1**			µs
t_2	Input hold time VIDA, VIDB, VIDC valid	VIDS edge	**20**			µs
t_3	VIDS delay time to VID latch	VIDS falling edge	**1**			µs
t_4	Input hold time VIDA, VIDB, VIDC valid	VIDS edge	**20**			µs
t_5	Delay to beginning of IDAC_OUT transition	Measured from VIDS rising edge		10	**17**	µs
t_6	IDAC_OUT transition time	Time constant for exponential rise		40		µs

(2) For VID timing, see Figure 2

Timing Diagram

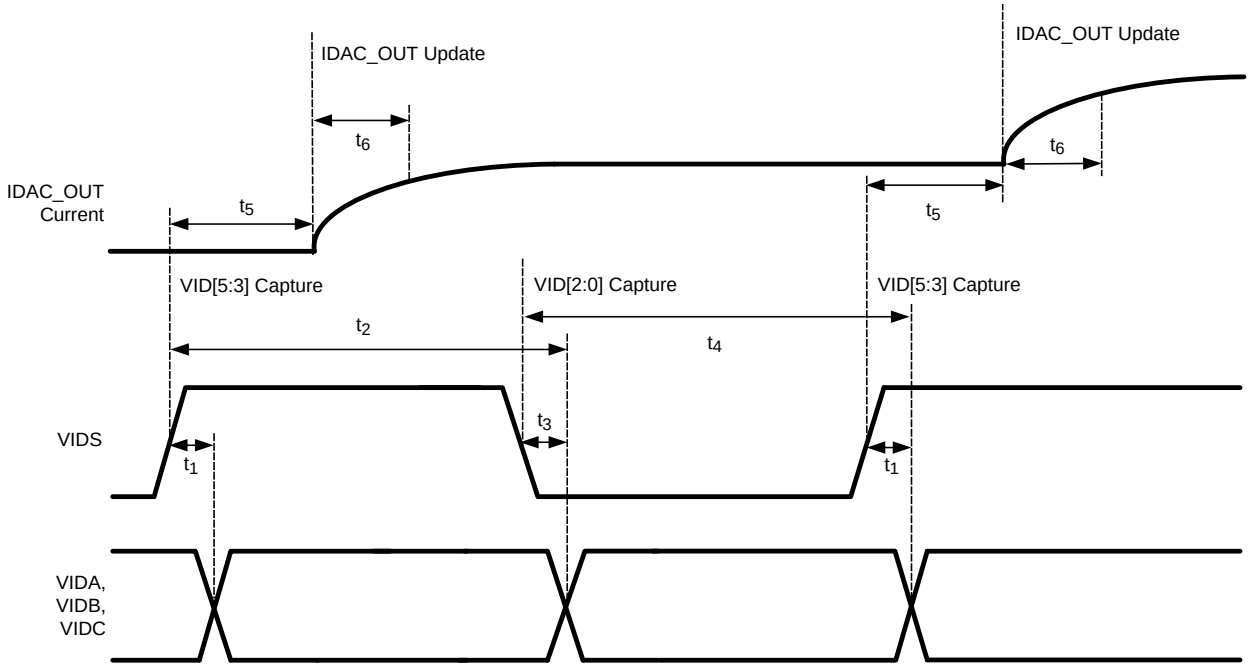


Figure 2. Timing Diagram for LM10010 Communications

Typical Performance Characteristics

Unless otherwise specified, the following conditions apply: T_J = 25°C, VDD = 5V. All graphs show junction temperature.

Supply Current (Default Startup)

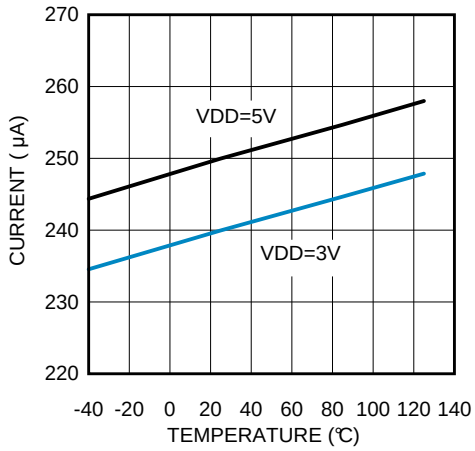


Figure 3.

Supply Current (Max IDAC Current)

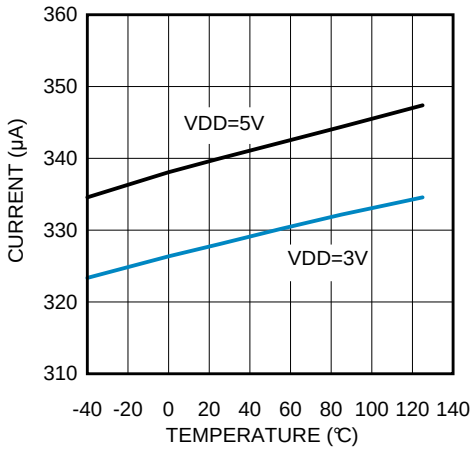


Figure 4.

Supply Current (EN Low)

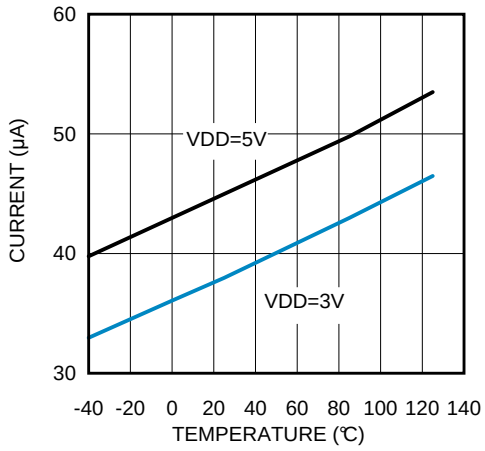


Figure 5.

Output Compliance to Positive Rail (VDD-V_{IDAC_OUT})

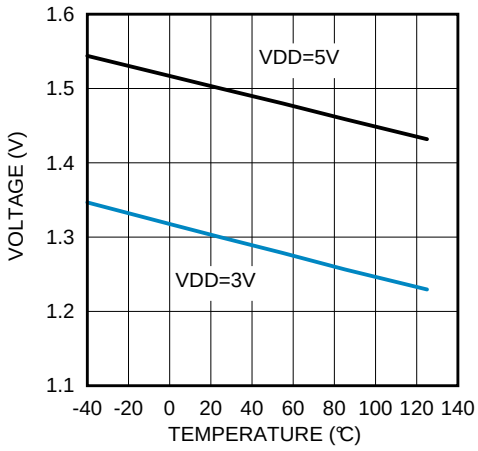


Figure 6.

Gain Error

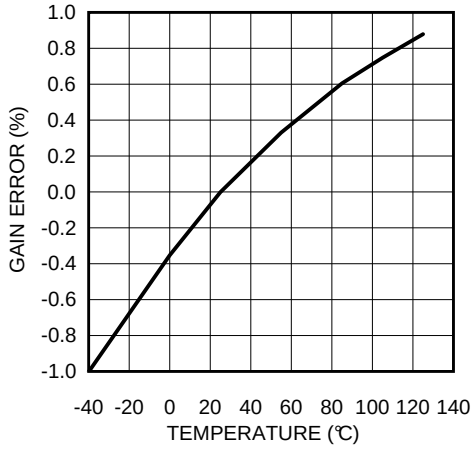


Figure 7.

IDAC Offset Current

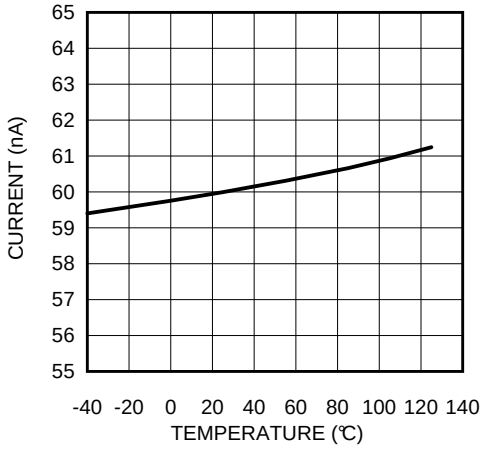


Figure 8.

Typical Performance Characteristics (continued)

Unless otherwise specified, the following conditions apply: T_J = 25°C, VDD = 5V. All graphs show junction temperature.

UVLO Thresholds

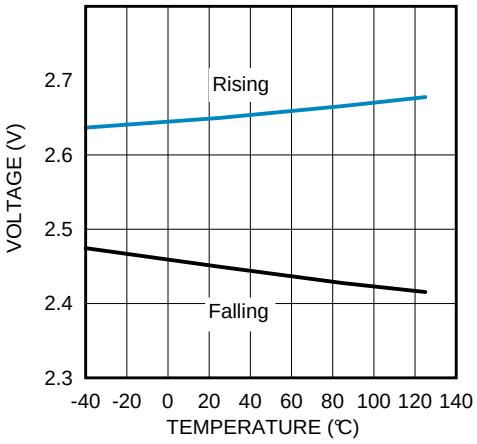


Figure 9.

EN (Enable) Threshold

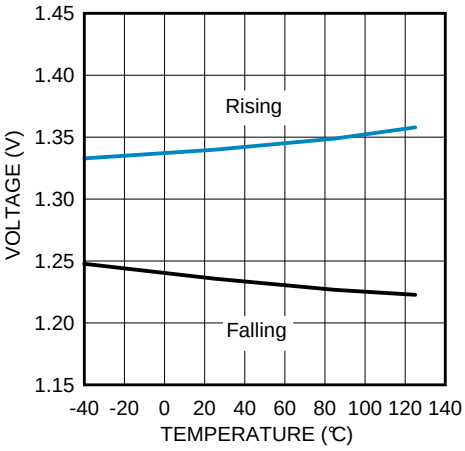


Figure 10.

Integral Non-Linearity

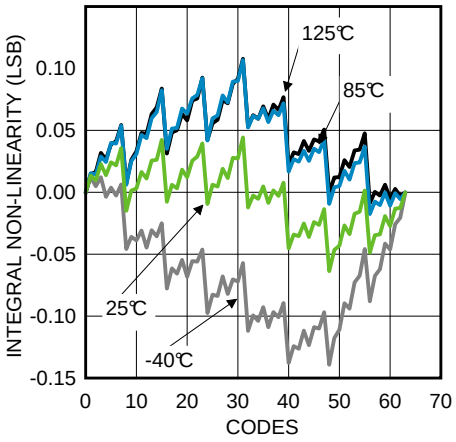


Figure 11.

Differential Non-Linearity

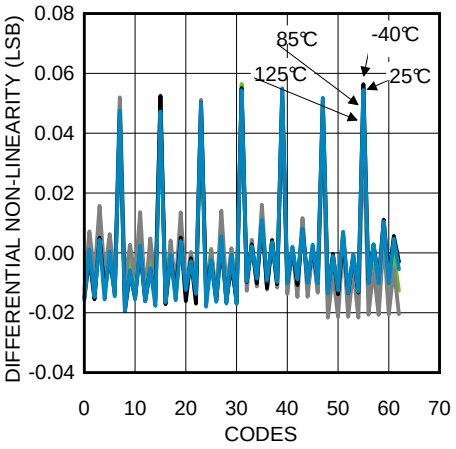


Figure 12.

BLOCK DIAGRAM

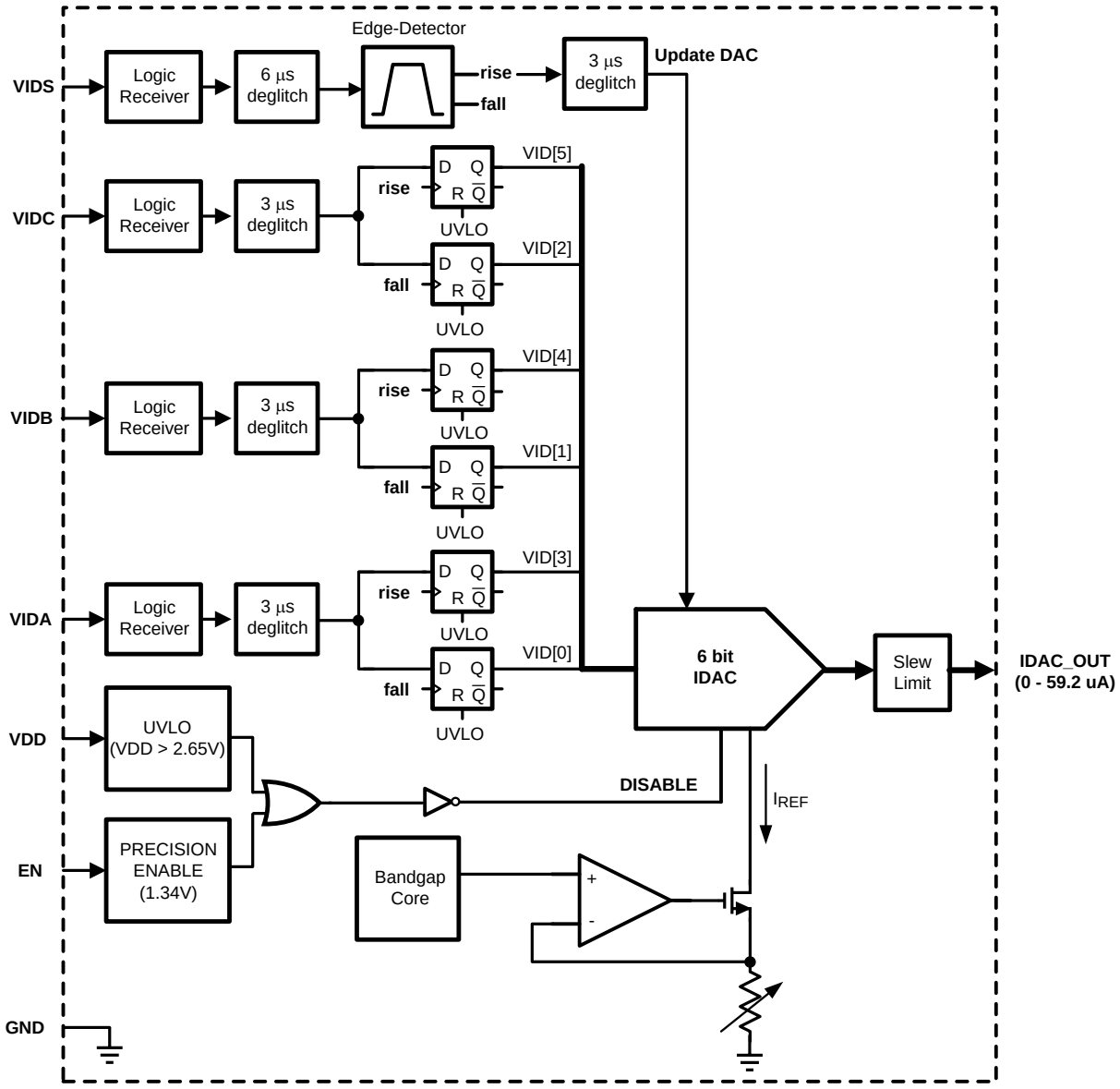


Figure 13. LM10010 Block Diagram

FUNCTIONAL DESCRIPTION

General

The LM10010 is a precision current DAC used for controlling any point of load regulator with an adjustable resistor feedback network. Four communication lines are used to write to a 6-bit IDAC value. The output of the IDAC is used to send current to the feedback node of a regulator, adjusting the output voltage. With this method, it is possible to precisely control the output voltage of the regulator.

An enable pin (EN) is provided to allow for a reduced quiescent current when not in use. Also, the VDD line is monitored so that an under-voltage event will shut down the device.

The device is available in a 10-pad No-Pullback Leadless Leadframe Package (WSON-10). The LM10010 can be used in numerous applications with regulators from 3.0V to 5.5V supplies. A block diagram of the LM10010 is shown in Figure 13 above.

Theory of Operation

The LM10010 can be thought of as a D/A converter, converting the VID communication to analog outputs. In this device, the output is a current DAC (IDAC_OUT), which is connected to the feedback node of a slave regulator. Therefore, all VID data words are decoded into a 6-bit current DAC output. The impedance of the feedback node at DC appears as the top feedback resistor. This is because the control loop of the slave regulator effectively maintains a constant current/voltage across the bottom feedback resistor, and creates low impedance at the VOUT node. Therefore, as more current is sourced into the feedback node, the more the output voltage is reduced. See Figure 14.

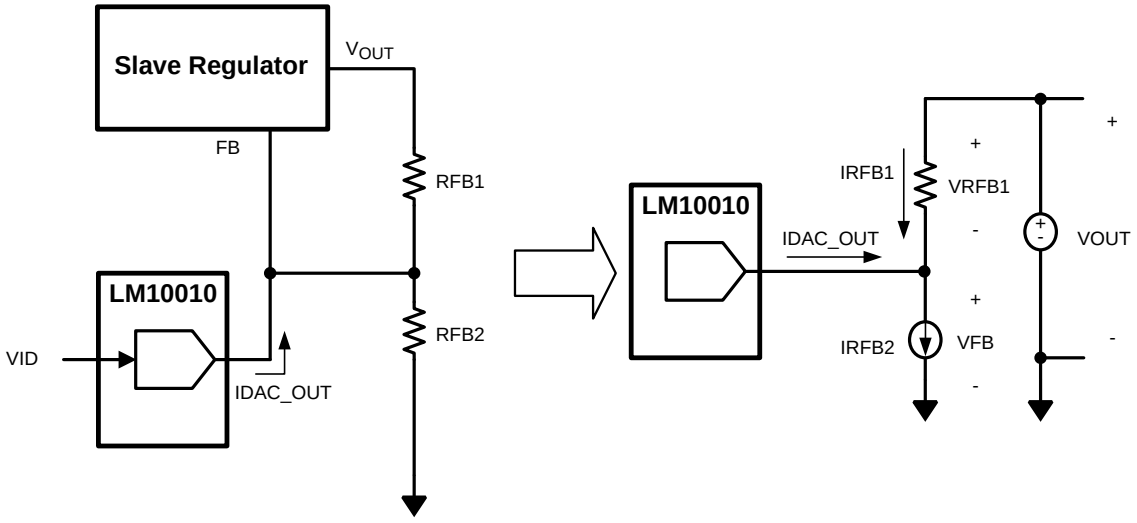


Figure 14. Output voltage is controlled via current injection into the feedback node

Current DAC

The LM10010 current DAC is based on a low voltage bandgap reference setting a current through a precision adjustable resistor. This bandgap is trimmed for precision and gives excellent performance over temperature. The output current has a maximum full-scale range of 59.2 µA and is adjustable with the 6-bit VID word. This allows for 64 settings, with a resolution of 940 nA. The current DAC also has a slew limit to prevent abrupt changes in the output. As the VID data lines are set for the output voltage for the regulator, deglitch filters provide a small delay and the output current rises with a $1\text{-}e^{-t}$ function that can be identified by a time constant.

VID Programming

Four pins are used to communicate with the LM10010. VIDC, VIDB, and VIDA are data lines, while VIDS is a latching strobe that programs in the LM10010 data. As shown in the Timing Diagram in Figure 2, the falling edge of VIDS latches in the data from VIDC, VIDB, and VIDA as the lower three LSB of the IDAC value. After a minimum hold time, the rising edge of VIDS latches in the data from VIDC, VIDB, and VIDA as the upper three LSB of the IDAC value. Internally, a delay on VIDS allows for the setting of all VID lines simultaneously.

The VID data word is set so that the lowest output current is seen at the highest VID data word (59.2 µA at a code of 0d). Conversely, the lowest current is seen at the highest VID data word (0 µA at 63d). During VID operation with the regulator, this will translate to the lowest output voltage with the lowest VID word, and the highest output voltage with the highest VID word. The communications pins can be used with a low voltage microcontroller, with a maximum V_{IL} of 0.4V and a minimum V_{IH} of 1.1V.

Upon startup, the IDAC is set at a code of 46d, which translates to approximately 16 µA. This default startup value is trimmed at final test. For applications with a different default output current at startup, please contact Texas Instruments.

Deglitch Time

The four digital input pins all have deglitch filters which prevent transient noise from affecting the operation of the LM10010. These filters will also impart a small delay to the digital signal. On the VIDS latching signal, there is an additional delay. As mentioned previously, this allows for the VID data lines and the VIDS strobe to be set simultaneously without the need for setup time.

Enable Pin and UVLO

The enable (EN) pin allows the output of the device to be enabled or disabled with an external control signal. This pin is a precision analog input that enables the device when the voltage exceeds 1.34V (typical). The EN pin has 100 mV of hysteresis and will disable the output when the enable voltage falls below 1.24V (typical). If EN is not used, it can be left open, and will be pulled high by an internal 2 µA current source. Since the enable pin has a precise turn-on threshold it can be used along with an external resistor divider network from VIN to configure the device to turn-on at a precise input voltage.

The LM10010 has a built-in under-voltage lockout (UVLO) protection circuit that keeps the device from operating until the input voltage reaches 2.65V (typical). The UVLO threshold has 200 mV of hysteresis that keeps the device from responding to power-on glitches during startup. Note that the enable and the UVLO are functionally the same as a reset. Bringing the device back from a low enable setting or from a VDD under-voltage event will reset the device back to its startup default setting.

APPLICATION INFORMATION

Design Example

In this example, an LM21215A-1 is used as the buck regulator to provide CVDD to the TMS320C6670 or TMS320C6678 from 0.7V to 1.1V and an output current of up to 15A. The LM10010 in conjunction with VID control from the DSP, provides control of the output voltage within this range with 6 bits of resolution. For this example, the 400 mV of voltage range translates to a 6.4 mV resolution in the control of the regulator output voltage. In this calculation, 1% resistor values are used. A schematic for this example is shown in the circuit of Figure 15.

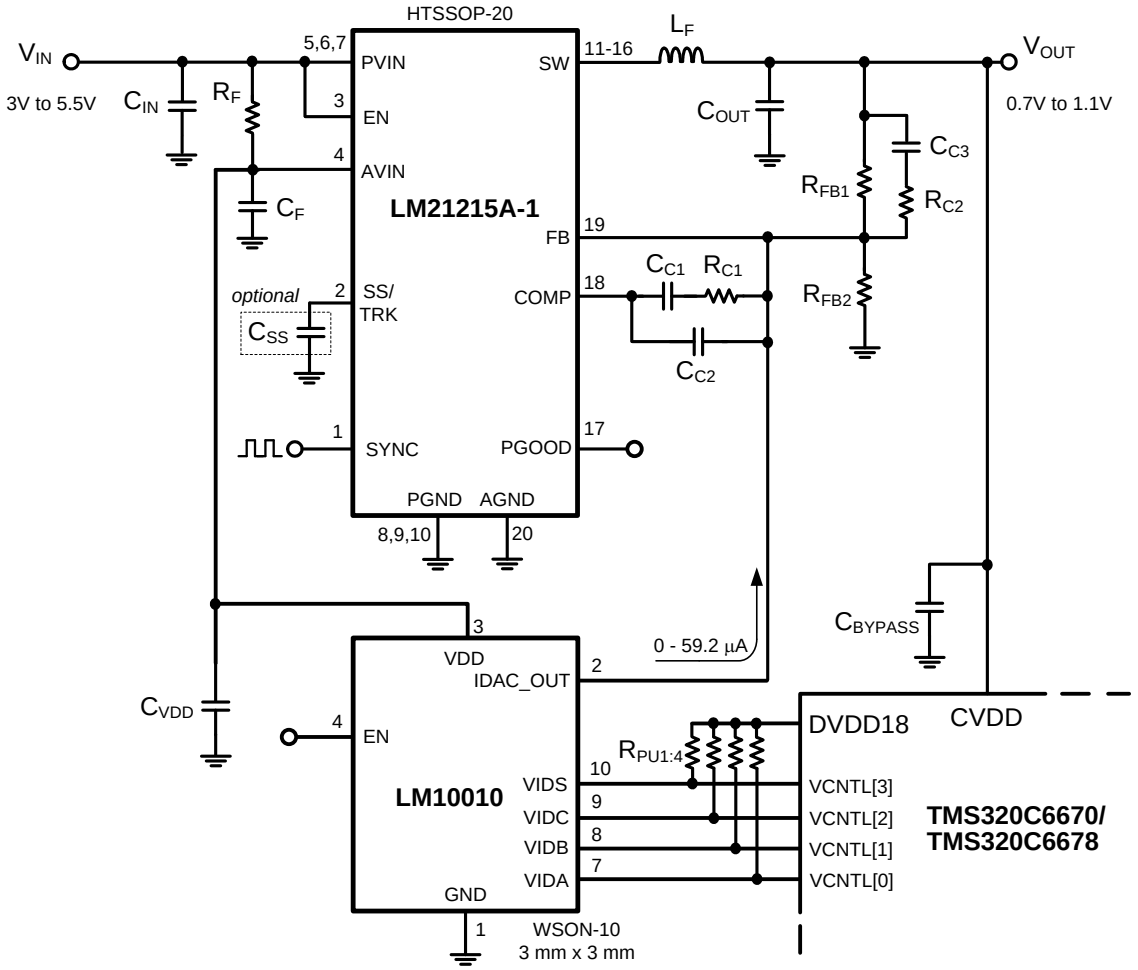


Figure 15. Typical Application Circuit

Setting the V_{OUT} Range and LSB

Looking at the Typical Application Circuit in Figure 15, the following equation defines V_{OUT} of a given regulator (valid for $V_{OUT} > V_{FB}$):

$$V_{OUT} = V_{FB} \cdot \left(1 + \frac{R_{FB1}}{R_{FB2}}\right) - I_{DAC\_OUT} \cdot R_{FB1} \quad (1)$$

Here, the output voltage is a function of the resistor divider from R_{FB1} and R_{FB2}. Additionally, there is a current supplied by the LM10010 that helps drive the feedback resistor R_{FB2}, thus lowering the necessary current supplied through R_{FB1}, and lowering V_{OUT}.

The change in the output voltage can be analyzed based on the resolution of the current DAC from the LM10010 compared to the desired resolution of the output swing of the regulator. R_{FB1} is designed to provide the desired LSB for V_{OUT} with the equation:

$$V_{OUT,LSB} = I_{DAC\_OUT,LSB} \cdot R_{FB1} \quad (2)$$

Based on the desired default V_{OUT} (with IDAC_OUT = 0 µA), R_{FB2} can be solved from Eq. 1 above.

Example Solution

Assuming a 400 mV output range, 64 VID codes, and an IDAC LSB of 0.940 µA, it is desired to have a V_{OUT} with an LSB of 6.4 mV and a default value of 1.1V using an LM21215A-1 regulator:

$$6.4\,mV = 0.940\,\mu A \cdot R_{FB1} \quad (3)$$

$$R_{FB1} = 6.8\,k\Omega \quad (4)$$

$$1.103V = 0.6V \cdot \left(1 + \frac{6.8\,k\Omega}{R_{FB2}}\right) - 0V \quad (5)$$

$$R_{FB2} = 8.1\,k\Omega \quad (6)$$

Using 1% resistor values, R_{FB1} can be set to 6.81 kΩ and R_{FB2} can be set to 8.06 kΩ. This will yield a regulator output range of 0.704V to 1.107V. At startup, the code of the LM10010 will be 46d (101110b) and will output a 15.97 µA. This will give an output voltage of approximately 1.0V (0.998V) when power is applied and both the LM10010 and the LM21215A-1 come out of UVLO. Of course, values calculated here will be dependent on the accuracy of the regulator, the LM10010 IDAC, and the resistor values used in the circuit.

Table 1 shows the codes and some of the resultant values of the IDAC current and the corresponding regulator output voltage for the previous example.

Table 1. VID Codes with IDAC Current and Regulator Voltage for the Example

VID Code	IDAC Current (µA)	Regulator Voltage (V)
000000b	59.20	0.7038
000001b	58.26	0.7102
000010b	57.32	0.7166
000011b	56.38	0.7230
...		
111100b	2.82	1.0878
111101b	1.88	1.0941
111110b	0.94	1.1005
111111b	0.00	1.1069

PC Board Guidelines

The following guidelines should be followed when designing the PC board for the LM10010:

- Place the LM10010 close to the regulator feedback pin to minimize the FB trace length.
- Place a small capacitor, C_{VDD}, (1 nF) directly adjacent to the VDD and GND pins of the LM10010 to help minimize transients which may occur on the input supply line.
- The high current path from the board's input to the load and the return path should be parallel and close to each other to minimize loop inductance.
- The ground connections for the various components around the LM10010 should be connected directly to each other, and to the LM10010's GND pins, and then connected to the system ground at one point. Do not connect the various component grounds to each other through the high current ground line.
- For additional information about the operation of the regulator, please consult the respective datasheet and application notes on the respective evaluation boards.

REVISION HISTORY

Changes from Revision B (March 2013) to Revision C	Page
• Changed layout of National Data Sheet to TI format	11

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM10010SD/NOPB	ACTIVE	WSON	DSC	10	1000	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 125	L254B	Samples
LM10010SDX/NOPB	ACTIVE	WSON	DSC	10	4500	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 125	L254B	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

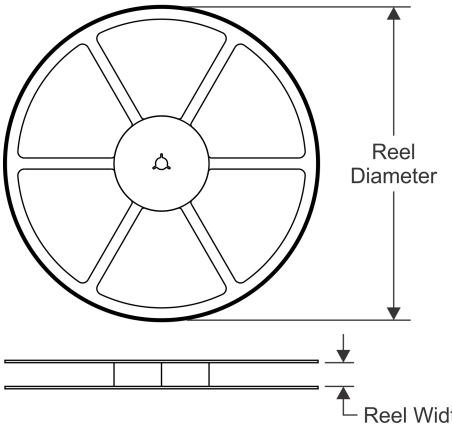
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

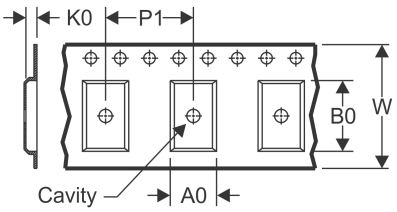
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

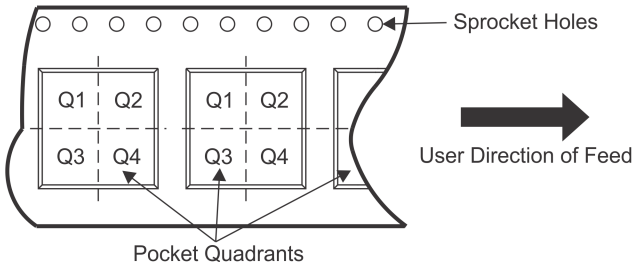


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

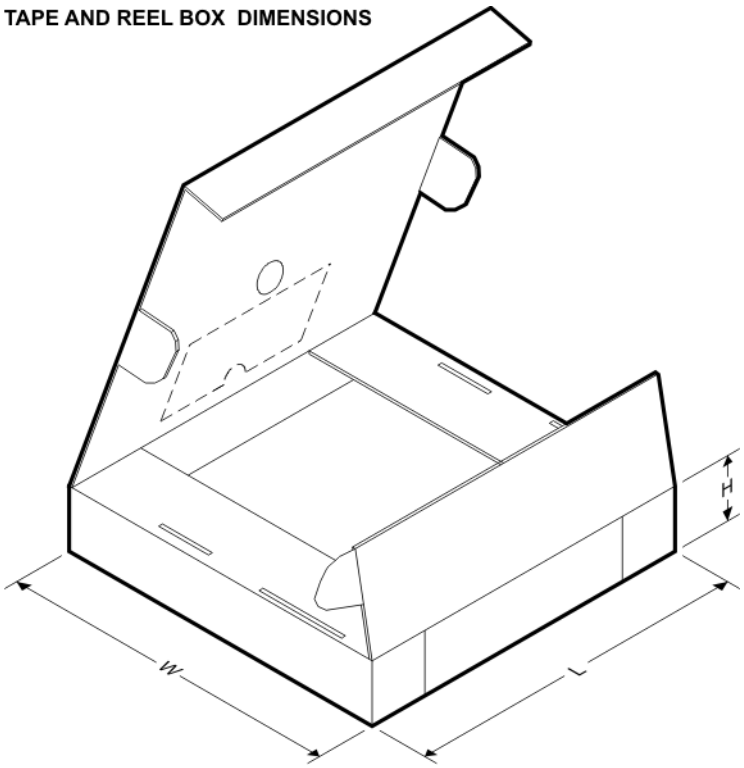
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM10010SD/NOPB	WSON	DSC	10	1000	178.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1
LM10010SDX/NOPB	WSON	DSC	10	4500	330.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1

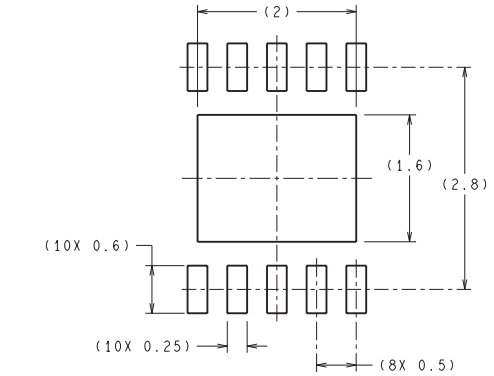
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

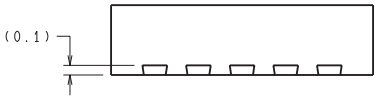
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM10010SD/NOPB	WSON	DSC	10	1000	210.0	185.0	35.0
LM10010SDX/NOPB	WSON	DSC	10	4500	367.0	367.0	35.0

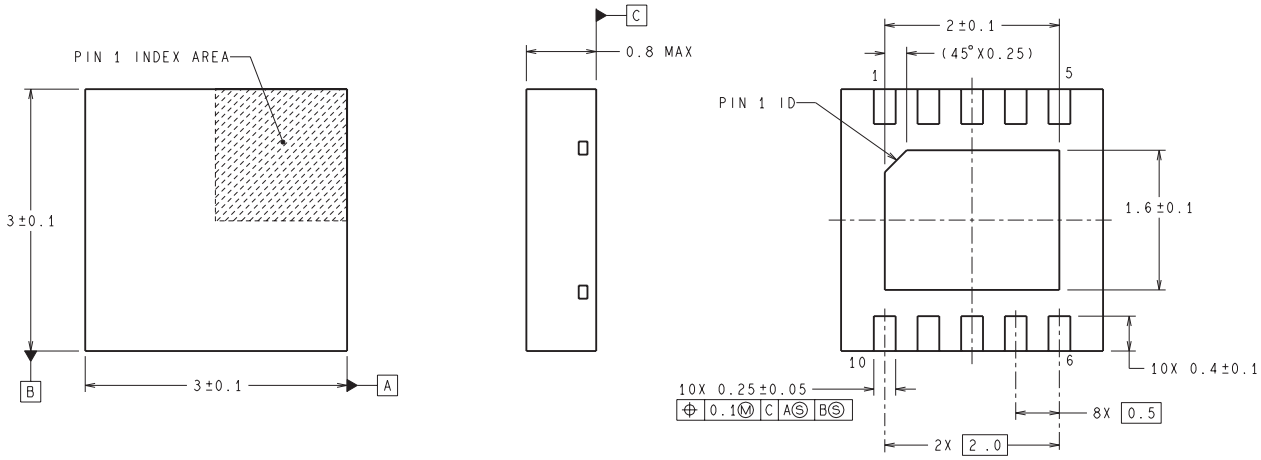
DSC0010A



RECOMMENDED LAND PATTERN

DIMENSIONS ARE IN MILLIMETERS
DIMENSIONS IN ( ) FOR REFERENCE ONLY





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