DS9638QML RS-422 Dual High Speed Differential Line Driver

Check for Samples: DS9638QML

FEATURES

- **Single 5V Supply**
- **Schottky Technology**
- **TTL and CMOS Compatible Inputs**
- **Output Short Circuit Protection**
- **Input Clamp Diodes**
- **Complementary Outputs**
- **Minimum Output Skew (<1.0 ns Typical)**
- **50 mA Output Drive Capability for 50Ω Transmission Lines**
- **Meets EIA RS-422 Specifications**
- **Propagation Delay of Less than 10 ns**
- **"Glitchless" Differential Output**
- **Delay Time Stable with V_{CC} and Temperature Variations (<2.0 ns typical) (Figure 4)**
- **Extended Temperature Range**

DESCRIPTION

The DS9638 is a Schottky, TTL compatible, dual differential line driver designed specifically to meet the EIA Standard RS-422 specifications. It is designed to provide unipolar differential drive to twisted pair or parallel wire transmission lines. The inputs are TTL compatible. The outputs are similar to totem pole TTL outputs, with active pull-up and pull-down. The device features a short circuit protected active pull-up with low output impedance and is specified to drive 50Ω transmission lines at high speed. The mini-CDIP provides high package density.

Connection Diagram

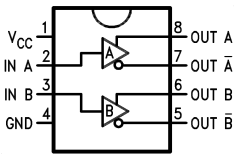


Figure 1. 8-Lead CDIP, Top View

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings(1)

Storage Temperature Range	Ceramic DIP	−65°C to +175°C
Lead Temperature	Ceramic DIP (Soldering, 60 sec.)	300°C
Maximum Power Dissipation at 25°C(2)	Cavity Package	1300 mW
V_{CC} Lead Potential to Ground		−5V to 7V
Input Voltage		−0.5V to +7V

(1) "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be ensured. They are not meant to imply that the devices should be operated at these limits. The tables of "Electrical Characteristics provide conditions for actual device operation.
(2) Derate cavity package 8.7 mW/°C above 25°C.

Recommended Operating Conditions

DS9638J/883	Min	Max	Units
Supply Voltage (V_{CC})	4.5	5.5	V
Output Current HIGH (I_{OH})		−50	mA
Output Current LOW (I_{OL})		50	mA
Operating Temperature (T_A)	−55	125	°C

Quality Conformance Inspection

MIL-STD-883, Method 5005 - Group A

Subgroup	Description	Temp (°C)
1	Static tests at	+25°C
2	Static tests at	+125°C
3	Static tests at	-55°C
4	Dynamic tests at	+25°C
5	Dynamic tests at	+125°C
6	Dynamic tests at	-55°C
7	Functional tests at	+25°C
8A	Functional tests at	+125°C
8B	Functional tests at	-55°C
9	Switching tests at	+25°C
10	Switching tests at	+125°C
11	Switching tests at	-55°C
12	Setting time at	+25°C
13	Setting time at	+125°C
14	Setting time at	-55°C

DS9638J/883 Electrical Characteristics DC Parameters

Over recommended operating temperature and supply voltage ranges, unless otherwise specified

Symbol	Parameter	Conditions	Notes	Min	Max	Units	Sub-Groups
V_{OL}	Output Voltage Low	V_{CC} = 4.5V, F_{IOL} = 30mA for temp, F_{IOL} = 35mA for room	See (1)		0.5	V	1, 2, 3
VFCD	Input Clamped Voltage	V_{CC} = 4.5V, FIFCD = -18mA		-1.2		V	1, 2, 3
V_{OHQVT}	V_T, $\overline{V}_T$ Terminated Output Voltage	V_{CC} = 5.5V, R_O = 100 Ω		2		V	1, 2, 3
V_{OH}	Logical "1" Output Voltage	V_{CC} = 4.5V, F_{IOH} = -10mA		2.5		V	1
				2.0			2, 3
V_{OHQ}	Logical "1" Output Voltage	V_{CC} = 4.5V, F_{IOHQ} = -40mA		2.0		V	1
				1.0			2, 3
V_{OHQBAL}	V_T- $\overline{V}_T$ Output Balance	V_{CC} = 5.5V, R_O = 100 Ω		-0.4	0.4	V	1, 2, 3
I_{IL}	Logical "0" Input Current	V_{CC} = 5.5V, F_{VIIL}= 0.5V		-200		µA	1, 2, 3
I_{IH}	Logical "1" Input Current	V_{CC} = 5.5V, F_{VIIH} = 2.7V			25	µA	1, 2, 3
I_{IHQH}	Logical "1" Input Current	V_{CC} = 5.5V, FV_{IIHQH} = 5.5V			50	µA	1, 2, 3
I_{OS}	Output Short Circuit Current	V_{CC} = 5.5V, FV_{IOS} = 0V		-150	-50	mA	1
				-150	-40		2, 3
I_{CC}	Supply Current	V_{CC} = 5.5V, FV_{CCH} = 5.5V			65	mA	1
					75	mA	2, 3
I_{OHC}	I_O (off) Output Leakage	V_{CC} = 5.5V, FV_{OH} = 5.5V			200	µA	1
V_{OS}, $\overline{V}_{OS}$	Output Offset Voltage		See (2)		3	V	1, 2, 3
V_{OS}- $\overline{V}_{OS}$	Output Offset Balance		See (3)		.4	V	1, 2, 3
V_{IH}	Input High Voltage		See (4)	2		V	1, 2, 3
V_{IL}	Input Low Voltage		See (4)		0.5	V	1, 2, 3
V_{HB}	I_X Output Leakage	V_{CC} = 0.0V, FIOHBQI = 150 µA		5.55		V	1
I_{CEX}	Output Leakage Current	V_{CC} = 0.0V, FVCEX = 5.5V			150	µA	2, 3
I_{CEXQI}	Output Leakage Current	V_{CC} = 0.0V, FVICEXQ2 = -0.25V		-150		µA	2, 3

(1) 35mA is more stringent than 30mA.
(2) Specified by design.
(3) Specified by Vt- $\overline{V}_T$ test.
(4) Specified by V_{OH} & V_{OL} tests.

DS9638J/883 Electrical Characteristics AC Parameters

Over recommended operating temperature and supply voltage ranges, unless otherwise specified

Symbol	Parameter	Conditions	Notes	Min	Max	Units	Sub-Groups
t_{PLH}	Propagation Delay to High Level	V_{CC} = 5V, R_O = 100 Ω, C_L = 15_{PF}			20	nS	9
t_{PHL}	Propagation Delay to Low Level	V_{CC} = 5V, R_O = 100 Ω, C_L = 15_{PF}			20	nS	9
t_F	Fall Time	V_{CC} = 5V, 90% - 10%			20	nS	9
t_R	Rise Time	V_{CC} = 5V, 10% - 90%			20	nS	9

Equivalent Circuit

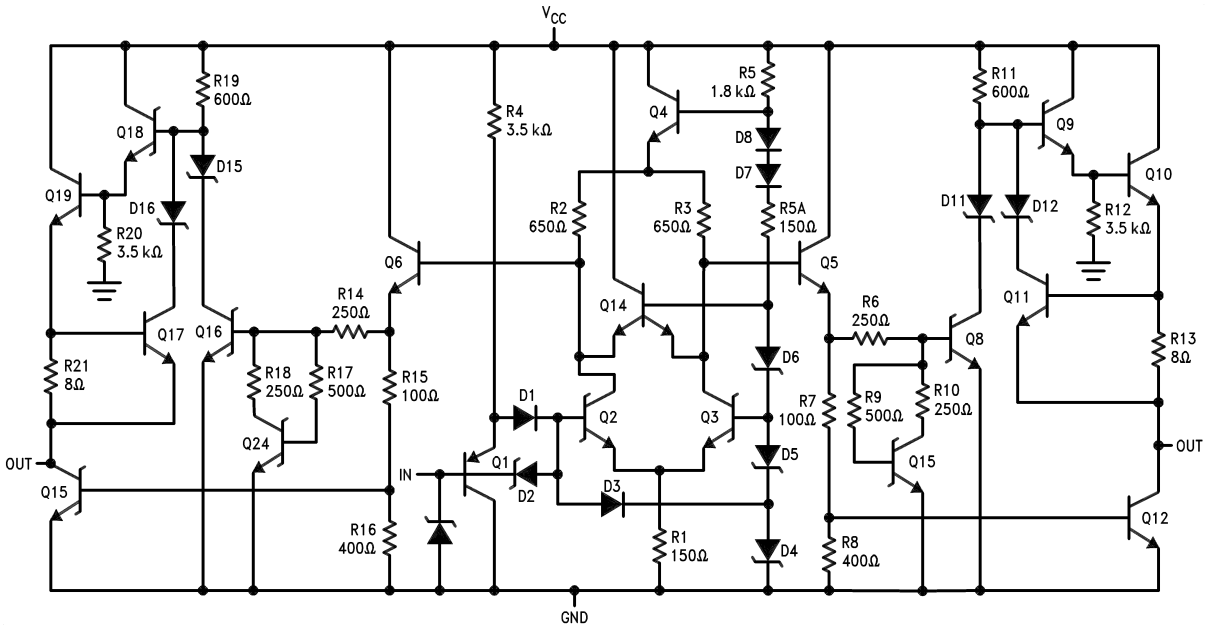


Figure 2.

DC Test Circuit

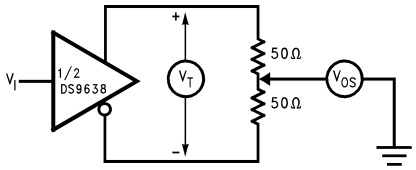
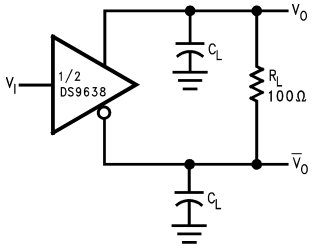


Figure 3. Terminated Output Voltage and Output Balance



The pulse generator has the following characteristics:
C_L includes probe and jig capacitance.
PRR = 500 kHz, t_W = 100 ns,
$t_r \le 5.0$ ns, $Z_O = 50\Omega$.

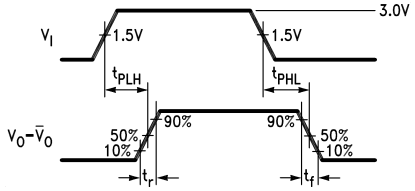


Figure 4. AC Test Circuit and Voltage Waveform

Typical Delay Characteristics

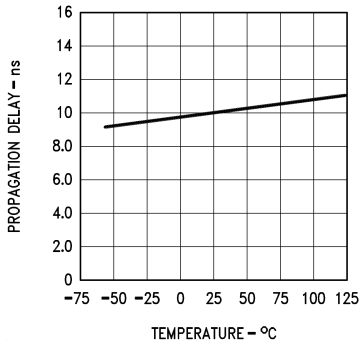


Figure 5.

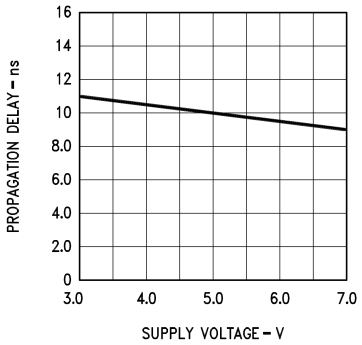


Figure 6.

REVISION HISTORY

Date Released	Revision	Section	Originator	Changes
05/27/08	A	New Release, Corporate Format, Change to DC Electrical Section	Bill Petcher	1 MDS data sheet converted into one Corp. data sheet format. Change made to V_{OH}, V_{OHQ} and I_{OS}. MNDS9638-X, Rev. 0AL data sheet will be Archived.

Changes from Original (April 2013) to Revision A **Page**

- Changed layout of National Data Sheet to TI format 5

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-8754601PA	ACTIVE	CDIP	NAB	8	40	TBD	Call TI	Call TI	-55 to 125	DS9638J/883 5962-87546 01PA Q ACO 01PA Q >T	Samples
DS9638J/883	ACTIVE	CDIP	NAB	8	40	TBD	Call TI	Call TI	-55 to 125	DS9638J/883 5962-87546 01PA Q ACO 01PA Q >T	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

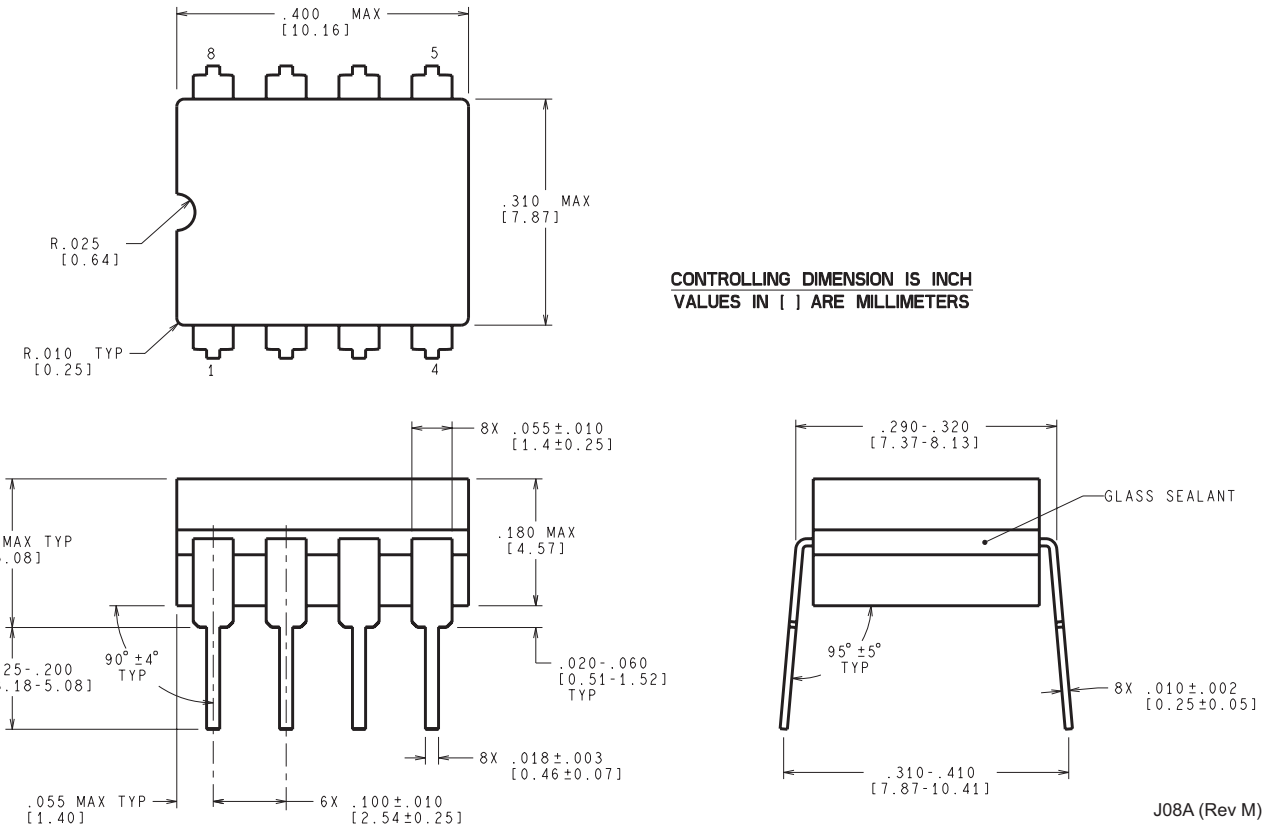
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

NAB0008A


.400 MAX
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5
.310 MAX
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R.025
[0.64]
R.010 TYP
[0.25]
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4
CONTROLLING DIMENSION IS INCH
VALUES IN [ ] ARE MILLIMETERS
8X .055±.010
[1.4±0.25]
.200 MAX TYP
[5.08]
.180 MAX
[4.57]
8X .125-.200
[3.18-5.08]
90° ±4°
TYP
.020-.060
[0.51-1.52]
TYP
8X .018±.003
[0.46±0.07]
.055 MAX TYP
[1.40]
6X .100±.010
[2.54±0.25]
.290-.320
[7.37-8.13]
GLASS SEALANT
95° ±5°
TYP
8X .010±.002
[0.25±0.05]
.310-.410
[7.87-10.41]
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