

## DS90LV027AQ Automotive LVDS Dual Differential Driver

 Check for Samples: [DS90LV027AQ](#)

### FEATURES

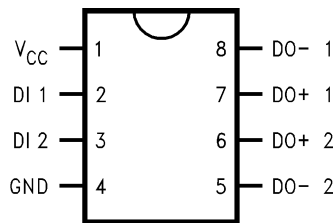
- AECQ-100 Grade 1
- >600 Mbps (300MHz) Switching Rates
- 0.3 ns Typical Differential Skew
- 0.7 ns Maximum Differential Skew
- 3.3V Power Supply Design
- Low Power Dissipation (46 mW @ 3.3V Static)
- Flow-Through Design Simplifies PCB Layout
- Power Off Protection (Outputs in High Impedance)
- Conforms to TIA/EIA-644 Standard
- 8-Lead SOIC Package Saves Space

### DESCRIPTION

The DS90LV027AQ is a dual LVDS driver device optimized for high data rate and low power applications. The device is designed to support data rates in excess of 600Mbps (300MHz) utilizing Low Voltage Differential Signaling (LVDS) technology. The DS90LV027AQ is a current mode driver allowing power dissipation to remain low even at high frequency. In addition, the short circuit fault current is also minimized.

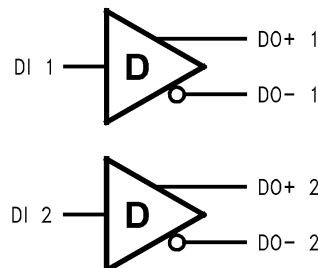
The device is in a 8-lead SOIC package. The DS90LV027AQ has a flow-through design for easy PCB layout. The differential driver outputs provides low EMI with its typical low output swing of 360 mV. It is perfect for high speed transfer of clock and data. The DS90LV027AQ can be paired with its companion dual line receiver, the DS90LV028AQ, or with any of TI's LVDS receivers, to provide a high-speed point-to-point LVDS interface.

### Connection Diagram



**Figure 1. Dual-In-Line**  
See Package Number D0008A

### Functional Diagram



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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### Absolute Maximum Ratings<sup>(1)(2)</sup>

Supply Voltage ( $V_{CC}$ )	-0.3V to +4V
Input Voltage (DI)	-0.3V to ( $V_{CC} + 0.3V$ )
Output Voltage (DO±)	-0.3V to +3.9V
Maximum Package Power Dissipation @ +25°C	
D Package	1068 mW
Derate D Package	9.71 mW/°C above +25°C
Package Thermal Resistance (4-Layer, 2 oz. Cu, JEDEC)	
$\theta_{JA}$	103.0°C/W
$\theta_{JC}$	50.0°C/W
Storage Temperature Range	-65°C to +150°C
Lead Temperature Range Soldering	
(4 sec.)	+260°C
Maximum Junction Temperature	+135°C
ESD Ratings	
HBM <sup>(3)</sup>	≥ 8kV
MM <sup>(4)</sup>	≥ 250V
CDM <sup>(5)</sup>	≥ 1250V

- (1) Absolute Maximum Ratings are those values beyond which the safety of the device cannot be ensured. They are not meant to imply that the devices should be operated at these limits. Electrical Characteristics specifies conditions of device operation.
- (2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
- (3) Human Body Model, applicable std. JESD22-A114C
- (4) Machine Model, applicable std. JESD22-A115-A
- (5) Field Induced Charge Device Model, applicable std. JESD22-C101-C

### Recommended Operating Conditions

	Min	Typ	Max	Units
Supply Voltage ( $V_{CC}$ )	3.0	3.3	3.6	V
Temperature ( $T_A$ )	-40	25	+125	°C

### Electrical Characteristics

Over Supply Voltage and Operating Temperature ranges, unless otherwise specified.<sup>(1)(2)(3)</sup>

Symbol	Parameter	Conditions	Pin	Min	Typ	Max	Units	
<b>DIFFERENTIAL DRIVER CHARACTERISTICS</b>								
$V_{OD}$	Output Differential Voltage	$R_L = 100\Omega$ (Figure 2)	DO+, DO-	250	360	450	mV	
$\Delta V_{OD}$	$V_{OD}$ Magnitude Change				1	35	mV	
$V_{OH}$	Output High Voltage				1.4	1.6	V	
$V_{OL}$	Output Low Voltage				0.9	1.1	V	
$V_{OS}$	Offset Voltage				1.125	1.2	1.375	V
$\Delta V_{OS}$	Offset Magnitude Change				0	3	25	mV
$I_{OXD}$	Power-off Leakage	$V_{OUT} = V_{CC}$ or GND, $V_{CC} = 0V$			±1	±10	µA	
$I_{OSD}$	Output Short Circuit Current				-5.7	-8	mA	

- (1) Current into device pins is defined as positive. Current out of device pins is defined as negative. All voltages are referenced to ground except  $V_{OD}$ .
- (2) All typicals are given for:  $V_{CC} = +3.3V$  and  $T_A = +25^\circ C$ .
- (3) The DS90LV027AQ is a current mode device and only function with datasheet specification when a resistive load is applied to the drivers outputs.

## Electrical Characteristics (continued)

Over Supply Voltage and Operating Temperature ranges, unless otherwise specified. <sup>(1)(2)(3)</sup>

Symbol	Parameter	Conditions	Pin	Min	Typ	Max	Units
<b>DIFFERENTIAL DRIVER CHARACTERISTICS</b>							
$V_{IH}$	Input High Voltage		DI	2.0		$V_{CC}$	V
$V_{IL}$	Input Low Voltage			GND		0.8	V
$I_{IH}$	Input High Current	$V_{IN} = 3.3V$ or $2.4V$			$\pm 2$	$\pm 10$	$\mu A$
$I_{IL}$	Input Low Current	$V_{IN} = GND$ or $0.5V$			$\pm 1$	$\pm 10$	$\mu A$
$V_{CL}$	Input Clamp Voltage	$I_{CL} = -18$ mA			-1.5	-0.6	V
$I_{CC}$	Power Supply Current	No Load	$V_{IN} = V_{CC}$ or GND	$V_{CC}$	8	14	mA
		$R_L = 100\Omega$			14	20	mA

## Switching Characteristics

Over Supply Voltage and Operating Temperature Ranges, unless otherwise specified. <sup>(1)(2)(3)(4)</sup>

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>DIFFERENTIAL DRIVER CHARACTERISTICS</b>						
$t_{PHLD}$	Differential Propagation Delay High to Low	$R_L = 100\Omega$ , $C_L = 15$ pF (Figure 3 and Figure 4)	0.3	0.8	2.0	ns
$t_{PLHD}$	Differential Propagation Delay Low to High		0.3	1.1	2.0	ns
$t_{SKD1}$	Differential Pulse Skew $ t_{PHLD} - t_{PLHD} $ <sup>(5)</sup>		0	0.3	0.7	ns
$t_{SKD2}$	Channel to Channel Skew <sup>(6)</sup>		0	0.4	0.8	ns
$t_{SKD3}$	Differential Part to Part Skew <sup>(7)</sup>		0		1.0	ns
$t_{SKD4}$	Differential Part to Part Skew <sup>(8)</sup>		0		1.7	ns
$t_{TLH}$	Transition Low to High Time		0.2	0.5	1.0	ns
$t_{THL}$	Transition High to Low Time		0.2	0.5	1.0	ns
$f_{MAX}$	Maximum Operating Frequency <sup>(9)</sup>				350	

- All typicals are given for:  $V_{CC} = +3.3V$  and  $T_A = +25^\circ C$ .
- These parameters are ensured by design. The limits are based on statistical analysis of the device over PVT (process, voltage, temperature) ranges.
- $C_L$  includes probe and fixture capacitance.
- Generator waveform for all tests unless otherwise specified:  $f = 1$  MHz,  $Z_O = 50\Omega$ ,  $t_r \leq 1$  ns,  $t_f \leq 1$  ns (10%-90%).
- $t_{SKD1}$ ,  $|t_{PHLD} - t_{PLHD}|$ , is the magnitude difference in differential propagation delay time between the positive going edge and the negative going edge of the same channel.
- $t_{SKD2}$  is the Differential Channel to Channel Skew of any event on the same device.
- $t_{SKD3}$ , Differential Part to Part Skew, is defined as the difference between the minimum and maximum specified differential propagation delays. This specification applies to devices at the same  $V_{CC}$  and within  $5^\circ C$  of each other within the operating temperature range.
- $t_{SKD4}$ , part to part skew, is the differential channel to channel skew of any event between devices. This specification applies to devices over recommended operating temperature and voltage ranges, and across process distribution.  $t_{SKD4}$  is defined as  $|Max - Min|$  differential propagation delay.
- $f_{MAX}$  generator input conditions:  $t_r = t_f < 1$  ns (0% to 100%), 50% duty cycle, 0V to 3V. Output criteria: duty cycle = 45%/55%,  $V_{OD} > 250mV$ , all channels switching.

### Parameter Measurement Information

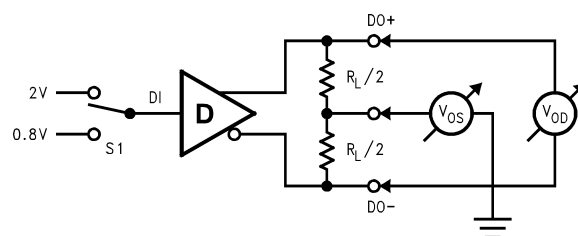
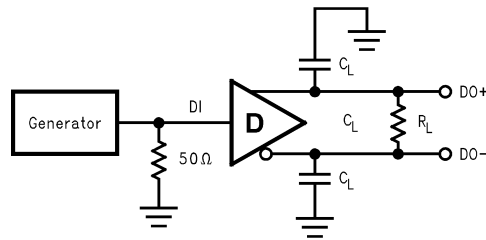
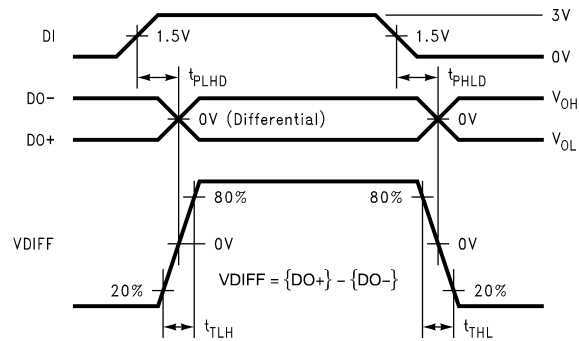


Figure 2. Differential Driver DC Test Circuit

### Parameter Measurement Information (continued)



**Figure 3. Differential Driver Propagation Delay and Transition Time Test Circuit**



**Figure 4. Differential Driver Propagation Delay and Transition Time Waveforms**

## APPLICATION INFORMATION

### DEVICE PIN DESCRIPTIONS

Pin #	Name	Description
2, 3	DI	TTL/CMOS driver input pins
6, 7	DO+	Non-inverting driver output pin
5, 8	DO-	Inverting driver output pin
4	GND	Ground pin
1	V <sub>CC</sub>	Positive power supply pin, +3.3V ± 0.3V

Typical Performance Curves

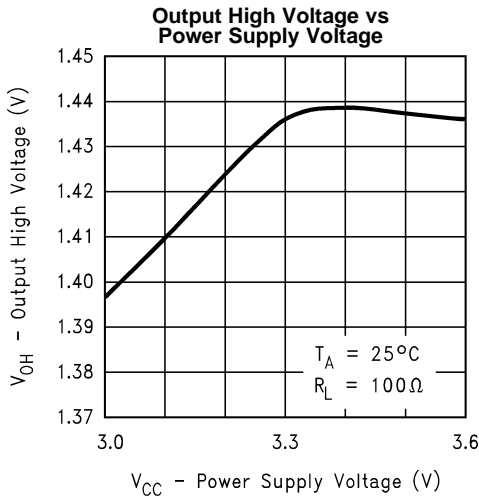


Figure 5.

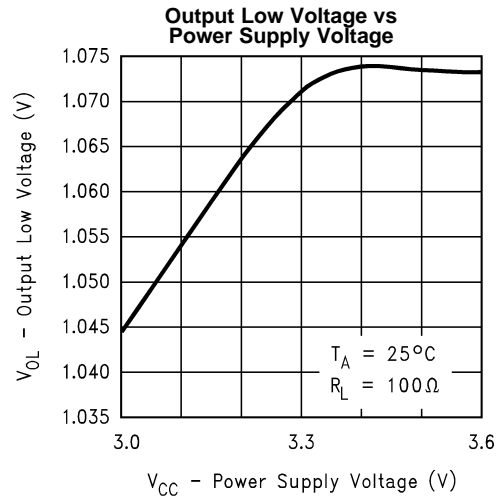


Figure 6.

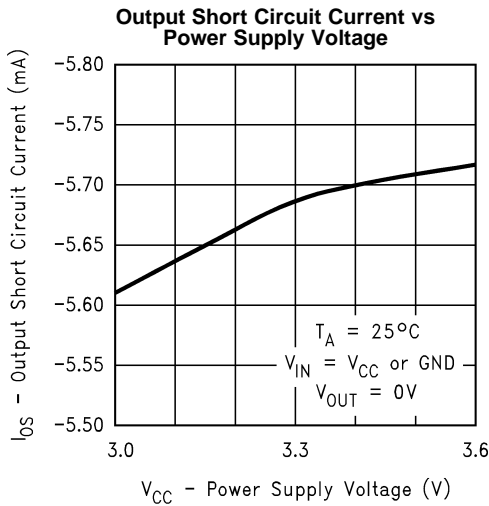


Figure 7.

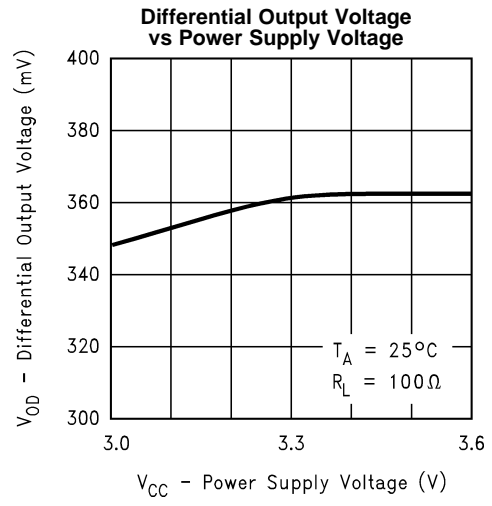


Figure 8.

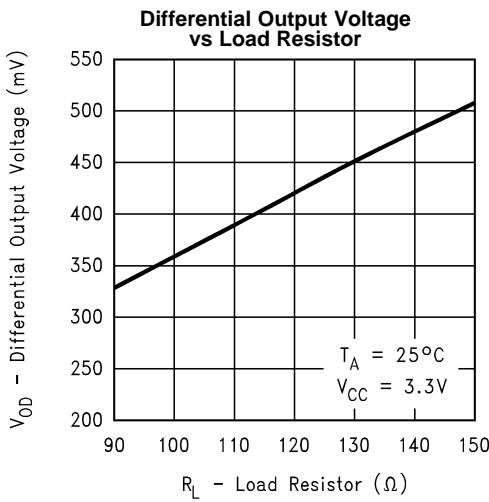


Figure 9.

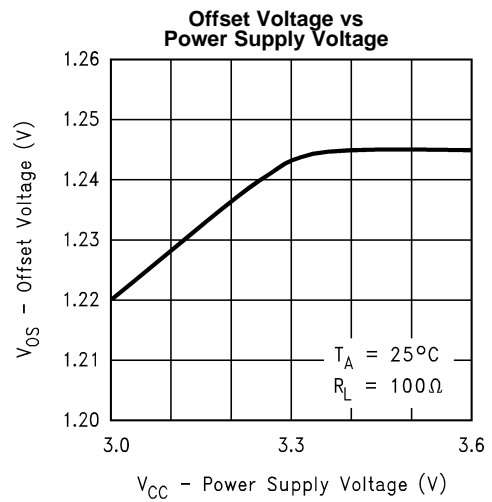


Figure 10.

Typical Performance Curves (continued)

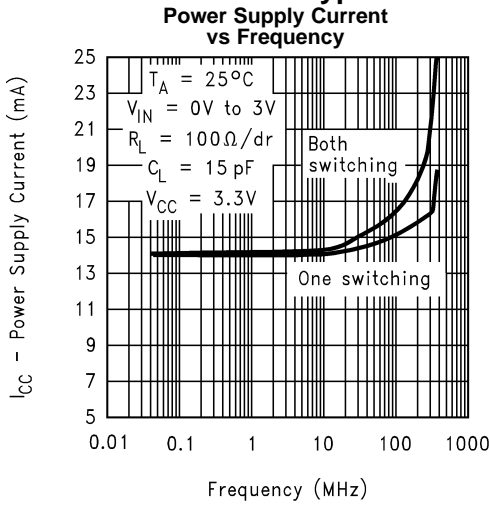


Figure 11.

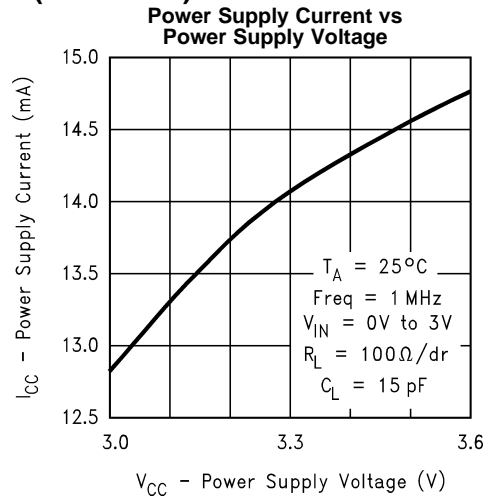


Figure 12.

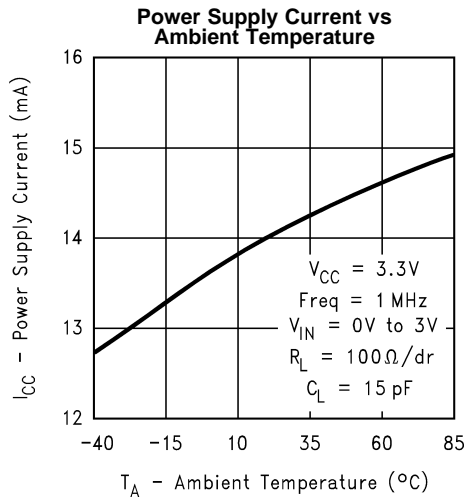


Figure 13.

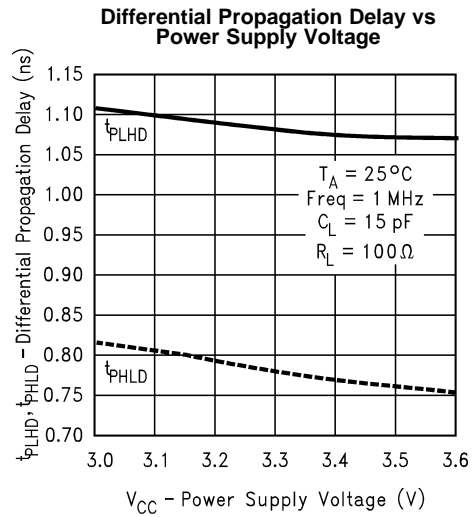


Figure 14.

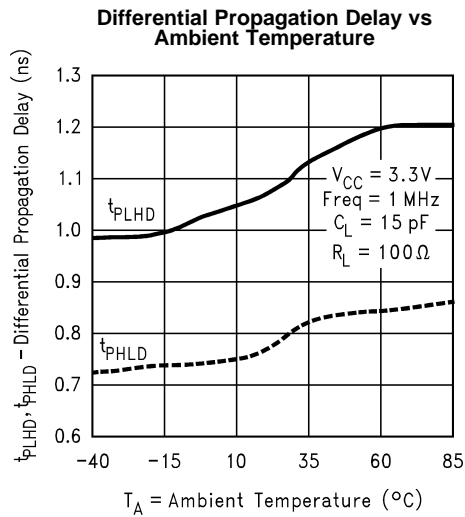


Figure 15.

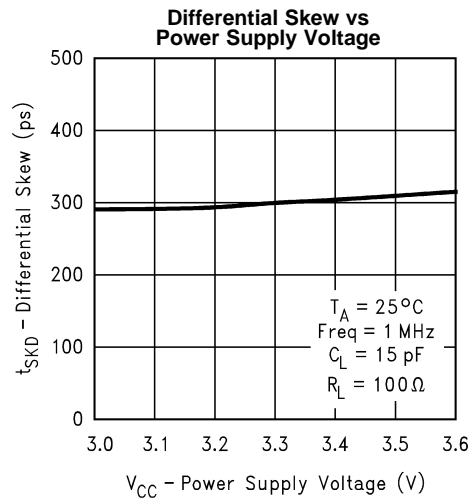


Figure 16.

Typical Performance Curves (continued)

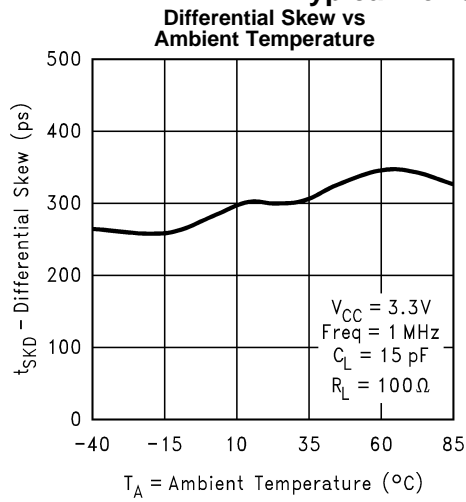


Figure 17.

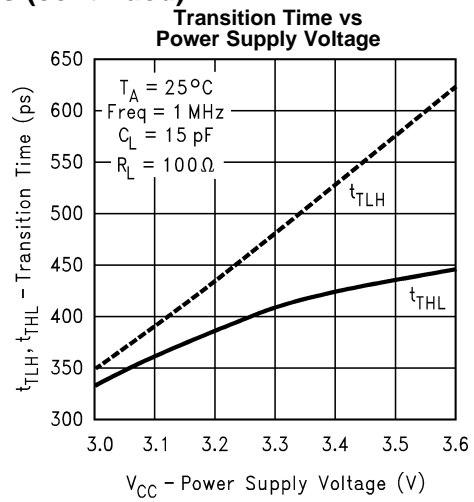


Figure 18.

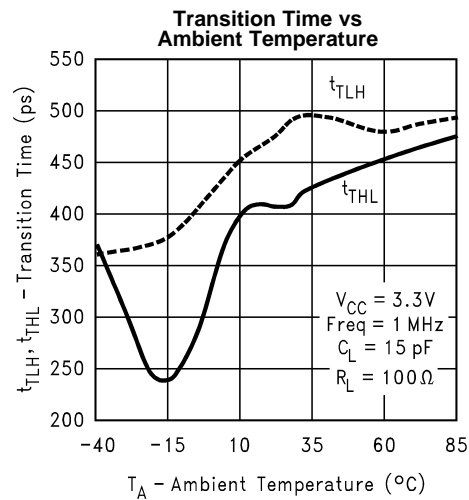


Figure 19.

### REVISION HISTORY

Changes from Revision C (April 2013) to Revision D	Page
• Changed layout of National Data Sheet to TI format .....	<a href="#">7</a>

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DS90LV027AQMA/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 125	90LV0 27AQM	<a href="#">Samples</a>
DS90LV027AQMAX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 125	90LV0 27AQM	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DS90LV027AQMXX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DS90LV027AQMAX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0



D0008A

# PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

## NOTES:

- Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed  $.006$  [0.15] per side.
- This dimension does not include interlead flash.
- Reference JEDEC registration MS-012, variation AA.

# EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
 EXPOSED METAL SHOWN  
 SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON .005 INCH [0.125 MM] THICK STENCIL  
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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