DM383 DaVinci™ Digital Media Processor

Check for Samples: DM383

1 High-Performance System-on-Chip (SoC)

1.1 Features

- High-Performance DaVinci Digital Media Processors
  - Up to 1000-MHz ARM® Cortex™-A8 RISC Processor
  - Up to 2000 ARM Cortex-A8 MIPS
- ARM Cortex-A8 Core
  - ARMv7 Architecture
    - In-Order, Dual-Issue, Superscalar Processor Core
    - NEON™ Multimedia Architecture
    - Supports Integer and Floating Point
    - Jazelle® RCT Execution Environment
- ARM Cortex-A8 Memory Architecture
  - 32KB of Instruction and Data Caches
  - 256KB of L2 Cache with ECC
  - 64KB of RAM, 48KB of Boot ROM
- 256KB of On-Chip Memory Controller (OCMC) RAM
- Imaging Subsystem (ISS)
  - Camera Sensor Connection
    - Parallel Connection for Raw (up to 16-Bit) and BT.656/BT.1120 (8- or 16-Bit)
    - CSI2 Serial Connection
  - Image Sensor Interface (ISIF) for Handling Image and Video Data From the Camera Sensor
  - Image Pipe Interface (IPIPEIF) for Image and Video Data Connection Between Camera Sensor, ISIF, IPIPE, and DRAM
  - Image Pipe (IPIPE) for Real-Time Image and Video Processing
  - Resizer
    - Resizing Image and Video From 1/16x to 8x
    - Generating Two Different Resizing Outputs Concurrently
    - Hardware 3A Engine (H3A) for Generating Key Statistics for 3A (AE, AWB, and AF) Control
- Face Detect (FD) Engine
  - Hardware Face Detection for up to 35 Faces Per Frame
- Programmable High-Definition Video Image Coprocessing (HDVICP v2) Engine
  - Encode, Decode, Transcode Operations
  - H.264 BP/MP/HP, MPEG-2, VC-1, MPEG-4 SP/ASP, JPEG/MJPEG
- Media Controller
  - Controls the HDVPSS, HDVICP2, and ISS
- Endianness
  - ARM Instructions and Data – Little Endian
- HD Video Processing Subsystem (HDVPSS)
  - Two 165-MHz HD Video Capture Inputs
    - One 16- or 24-Bit Input, Splittable Into Dual 8-Bit SD Capture Ports
    - One 8-, 16-, or 24-Bit HD Input and 8-Bit SD Input Capture Port
  - Two 165-MHz HD Video Display Outputs
    - One 16-, 24-, or 30-Bit and One 16- or 24-Bit Output
  - Component HD Analog Output
  - Composite Analog Output
  - Digital HDMI 1.3 Transmitter with Integrated PHY
  - Advanced Video Processing Features Such as Scan, Format, and Rate Conversion
  - Three Graphics Layers and Compositors
- 32-Bit DDR2, DDR3, and DDR3L SDRAM Interface
  - Supports up to 400 MHz for DDR2, 533 MHz for DDR3, and 533 MHz for DDR3L
  - Up to Two x 16 Devices, 2GB of Total Address Space
  - Dynamic Memory Manager (DMM)
    - Programmable Multi-Zone Memory Mapping
    - Enables Efficient 2D Block Accesses
    - Supports Tiled Objects in 0°, 90°, 180°, or 270° Orientation and Mirroring

- General-Purpose Memory Controller (GPMC)
  - 8- or 16-Bit Multiplexed Address and Data Bus
  - 512MB of Total Address Space Divided Among up to 8 Chip Selects
  - Glueless Interface to NOR Flash, NAND Flash (BCH/Hamming Error Code Detection), SRAM and Pseudo-SRAM
  - Error Locator Module (ELM) Outside of GPMC to Provide up to 16-Bit or 512-Byte Hardware ECC for NAND
  - Flexible Asynchronous Protocol Control for Interface to FPGA, CPLD, ASICs, and More
- Enhanced Direct Memory Access (EDMA) Controller
  - Four Transfer Controllers
  - 64 Independent DMA Channels
  - 8 QDMA Channels
- Dual USB 2.0 Ports with Integrated PHYs
  - USB2.0 High- and Full-Speed Clients
  - USB2.0 High-, Full-, and Low-Speed Hosts
  - Supports End Points 0-15
- Eight 32-Bit General-Purpose Timers (Timer1–8)
- One System Watchdog Timer (WDT0)
- Three Configurable UART/IrDA/CIR Modules
  - UART0 with Modem Control Signals
  - Supports up to 3.6864 Mbps
  - SIR, MIR, FIR (4.0 MBAUD), and CIR
- Four Serial Peripheral Interfaces (SPIs) (up to 48 MHz)
  - Each with Four Chip Selects
- Three MMC/SD/SDIO Serial Interfaces (up to 48 MHz)
  - Supporting up to 1-, 4-, or 8-Bit Modes
- Dual Controller Area Network (DCAN) Module
  - CAN Version 2 Part A, B
- Four Inter-Integrated Circuit (I^2C Bus™) Ports
- Two Multichannel Audio Serial Ports (McASP)
  - Six Serializer Transmit and Receive Ports
  - Two Serializer Transmit and Receive Ports
  - DIT-Capable For S/PDIF (All Ports)
- Serial ATA (SATA) 3.0 Gbps Controller with Integrated PHY
  - Direct Interface to 1 Hard Disk Drive
  - Hardware-Assisted Native Command Queuing (NCQ) from up to 32 Entries
  - Supports Port Multiplier and Command-Based Switching
- Real-Time Clock (RTC)
  - One-Time or Periodic Interrupt Generation
- Up to 125 General-Purpose I/O (GPIO) Pins
- One Spin Lock Module with up to 128 Hardware Semaphores
- One Mailbox Module with 12 Mailboxes
- On-Chip ARM ROM Bootloader (RBL)
- Power, Reset, and Clock Management
  - SmartReflex™ Technology (Level 2b)
  - Multiple Independent Core Power Domains
  - Multiple Independent Core Voltage Domains
  - Support for Multiple Operating Points per Voltage Domain
  - Clock Enable and Disable Control for Subsystems and Peripherals
- 32KB of Embedded Trace Buffer™ (ETB™) and 5-pin Trace Interface for Debug
- IEEE 1149.1 (JTAG) Compatible
- 609-Pin Pb-Free BGA Package (AAR Suffix), 0.8-mm Effective Pitch with Via Channel Technology to Reduce PCB Cost (0.5-mm Ball Spacing)
- 45-nm CMOS Technology
- 1.8- and 3.3-V Dual Voltage Buffers for General I/O

1.2 Applications

- **Car Black Box Digital Video Recorder**
- **Portable Digital Video Recorder**
- **Intrusion Control Panels with Video**
- **Access Control Panels with Video**

1.3 Description

DM383 DaVinci Digital Media Processors are a highly integrated, cost-effective, low-power, programmable platform that leverages TI's DaVinci processor technology to meet the processing needs of Car Black Box Digital Video Recorders, Portable Digital Video Recorders, and similar devices in SD and HD resolutions. The Programmable High-Definition Video Image Processor of the device supports 1080p60 of real time H.264BP/MP/HP video encode or decode. The included best-in-class H.264 encoder provides high-quality video encode for the lowest possible bit rate under all conditions, reducing valuable storage space to a minimum. In addition, the device also supports other video codecs such as MJPEG, MPEG-2, and MPEG-4. The device provides a full set of video preprocessing and postprocessing functions to ensure the best video quality. The low power consumption and high performance of the device makes it particularly suitable for portable and automotive applications.

The device enables original-design manufacturers (ODMs) and after-market manufacturers to quickly bring to market devices featuring robust operating systems support, rich user interfaces, and high processing performance through the maximum flexibility of a fully integrated mixed processor solution. The device also combines programmable video and audio processing with a highly integrated peripheral set.

The device processors include a high-definition video and imaging coprocessor 2 (HDVICP2), to off-load many video and imaging processing tasks for common video and imaging algorithms. Programmability is provided by an ARM Cortex-A8 RISC CPU with NEON extension and high-definition video and imaging coprocessors. The ARM lets developers separate control functions from A/V algorithms programmed on coprocessors, thus reducing the complexity of the system software. The ARM Cortex-A8 32-bit RISC processor with NEON floating-point extension includes: 32KB of instruction cache; 32KB of data cache; 256KB of L2 cache with ECC; 48KB of boot ROM; and 64KB of RAM.

The rich peripheral set provides the ability to control external peripheral devices and communicate with external processors. For details on each peripheral, see the related sections in this document and the associated peripheral reference guides. The peripheral set includes: HD Video Processing Subsystem; two USB ports with integrated 2.0 PHY; two serializer McASP audio serial ports (with DIT mode); three UARTs with IrDA and CIR support; four SPI serial interfaces; a CSI2 serial connection; three MMC/SD/SDIO serial interfaces; four I^2C master and slave interfaces; a parallel camera interface (CAM); up to 125 general-purpose I/Os (GPIOs); eight 32-bit general-purpose timers; system watchdog timer; DDR2/DDR3/DDR3L SDRAM interface; flexible 8- or 16-bit asynchronous memory interface; two Controller Area Network (DCAN) modules; Serial ATA (SATA) 3.0 Gbps controller with integrated PHY; a Spin Lock; and Mailbox.

Additionally, TI provides a complete set of development tools for the ARM which include C compilers and a Microsoft® Windows® debugger interface for visibility into source code execution.

1.4 Functional Block Diagram

Figure 1-1 shows the functional block diagram of the device.

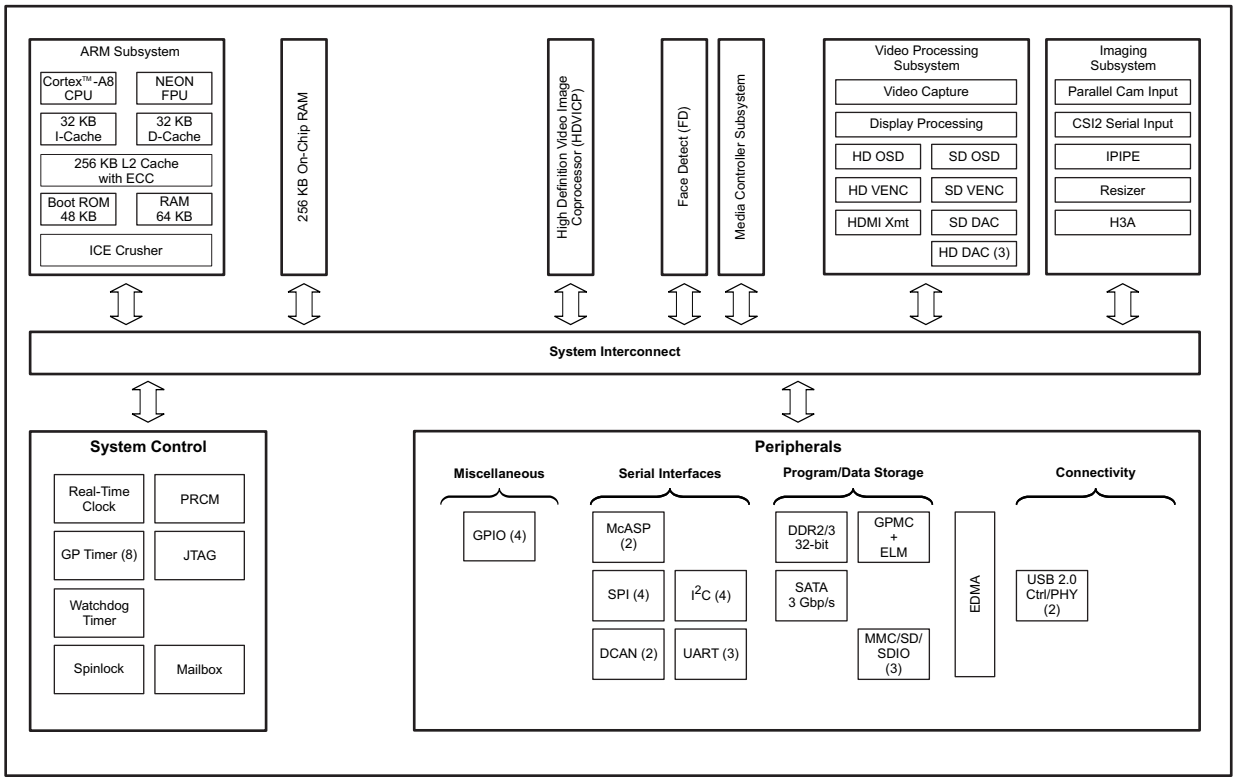


Figure 1-1. Functional Block Diagram

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Revision History

SEE	ADDITIONS/MODIFICATIONS/DELETIONS
Global	Added support for OPP100 to: • Section 6.2, *Recommended Operating Conditions* • Section 6.3, *Reliability Data* • Table 7-3, *Device Operating Points (OPPs)* • Table 7-4, *Supported OPP Combinations*
Power, Reset, Clocking, and Interrupts	Changed OPP100 speed from 500 to 600 MHz for ARM Cortex-A8 in Table 7-3, *Device Operating Points (OPPs)*.
	Removed requirement that the maximum voltage difference between CVDD and any other CVDD_x voltage domain must be < 150 mV. • Table 7-4, *Supported OPP Combinations*

2 Device Overview

2.1 Device Comparison

2.2 Device Characteristics

Table 2-1 provides an overview of the DM383 DaVinci™ Digital Media Processors,, which includes significant features of the device, including the capacity of on-chip RAM, peripherals, and the package type with pin count.

Table 2-1. Characteristics of the Processor

HARDWARE FEATURES		DM383
Peripherals Not all peripherals pins are available at the same time (for more details, see the Device Configurations section).	HD Video Processing Subsystem (HDVPSS)	1 16-/24-bit HD Capture Port ***or*** 2 8-bit SD Capture Ports ***and*** 1 8/16/24-bit HD Input Port ***and*** 1 8-bit SD Input Port ***and*** 1 16-/24-/30-bit HD Display Port or 1 HDMI 1.3 Transmitter ***and*** 1 16-/24-bit HD Display Port ***and*** 1 SD Video DAC ***and*** 3 HD Video DACs
	Imaging Subsystem (ISS)	1 Parallel Camera Input for Raw (up to 16-bit) and BT.656/BT.1120 (8/16-bit) and 1 CSI2 Serial Input
	DDR2/3 Memory Controller	16-/32-bit Bus Width
	GPMC + ELM	Asynchronous (8-/16-bit bus width) RAM, NOR, NAND
	EDMA	64 Independent Channels 8 QDMA Channels
	USB 2.0	2 (Supports High- and Full-Speed as a Device and High-, Full-, and Low-Speed as a Host)
	Timers	8 (32-bit General purpose) ***and*** 1 (System Watchdog)
	UART	3 (with SIR, MIR, FIR, CIR support and RTS/CTS flow control) (UART0 Supports Modem Interface)
	SPI	4 (Each supporting up to 4 slave devices)
	MMC/SD/SDIO	1 (1-bit or 4-bit or 8-bit modes) ***and*** 1 (8-bit mode) ***or*** 2 (1-bit or 4-bit modes)
	I2C	4 Master or Slave
	Media Controller	Controls HDVPSS, HDVICP2, and ISS
	McASP	2 (6/2 Serializers, each with Transmit/Receive and DIT capability)
	Controller Area Network (DCAN)	2
	Serial ATA (SATA) 3.0 Gbps	1 (Supports 1 Hard Disk Drive)
	RTC	1
	GPIO	Up to 125 pins

Table 2-1. Characteristics of the Processor (continued)

HARDWARE FEATURES			DM383
	Spinlock Module		1 (up to 128 H/W Semaphores)
	Mailbox Module		1 (with 12 Mailboxes)
On-Chip Memory	Size (Bytes)		640KB RAM, 48KB ROM
	Organization		**ARM** 32KB I-cache 32KB D-cache 256KB L2 Cache with ECC 64KB RAM 48KB Boot ROM
			ADDITIONAL SHARED MEMORY 256KB On-chip RAM
JTAG BSDL ID	DEVICE_ID Register (address location: 0x4814 0600)		see Section 8.5.3.1, JTAG ID (JTAGID) Register Description
CPU Frequency	MHz		ARM® Cortex™-A8 up to 1000 MHz
Cycle Time	ns		ARM® Cortex™ -A8 1.0 ns
Voltage	Core Logic (V)	DEEP SLEEP, OPP100, OPP120, Turbo, Nitro	0.83 V – 1.35 V
	I/O (V)		1.35 V, 1.5 V, 1.8 V, 3.3 V
Package	16 x 16 mm		609-Pin BGA (AAR) [with Via Channel™ Technology]
Process Technology	µm		0.045 µm
Product Status	Product Preview (PP), Advance Information (AI), or Production Data (PD)		PD

2.3 Device Compatibility

2.4 ARM® Cortex™-A8 Microprocessor Unit (Processor) Subsystem Overview

The ARM® Cortex™-A8 Subsystem is designed to allow the ARM Cortex-A8 master control of the device. In general, the ARM Cortex-A8 is responsible for configuration and control of the various subsystems, peripherals, and external memories.

The ARM Cortex-A8 Subsystem includes the following features:

- ARM Cortex-A8 RISC processor:
  - ARMv7 ISA plus Thumb2™, JazelleX™, and Media Extensions
  - NEON™ Floating-Point Unit
  - Enhanced Memory Management Unit (MMU)
  - Little Endian
  - 32KB L1 Instruction Cache
  - 32KB L1 Data Cache
  - 256KB L2 Cache with Error Correction Code (ECC)
- CoreSight Embedded Trace Module (ETM)
- ARM Cortex-A8 Interrupt Controller (AINTC)
- Embedded PLL Controller (PLL_ARM)
- 64KB Internal RAM
- 48KB Internal Public ROM

Figure 2-1 shows the ARM Cortex-A8 Subsystem for the device.

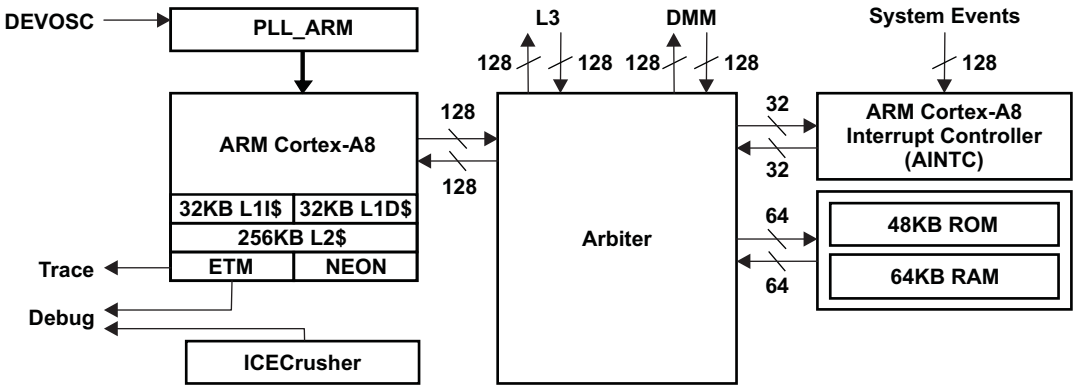


Figure 2-1. ARM Cortex-A8 Subsystem

2.4.1 ARM Cortex-A8 RISC Processor

The ARM Cortex-A8 processor is a member of ARM Cortex family of general-purpose microprocessors. This processor is targeted at multi-tasking applications where full memory management, high performance, low die size, and low power are all important. The ARM Cortex-A8 processor supports the ARM debug architecture and includes logic to assist in both hardware and software debug. The ARM Cortex-A8 processor has a Harvard architecture and provides a complete high-performance subsystem, including:

- ARM Cortex-A8 Integer Core
- Superscalar ARMv7 Instruction Set
- Thumb-2 Instruction Set
- Jazelle RCT Acceleration
- CP14 Debug Coprocessor

- CP15 System Control Coprocessor
- NEON 64-/128-bit Hybrid SIMD Engine for Multimedia
- Enhanced VFPv3 Floating-Point Coprocessor
- Enhanced Memory Management Unit (MMU)
- Separate Level-1 Instruction and Data Caches
- Integrated Level-2 Cache with ECC Support
- 128-bit Interconnect with Level 3 Fast (L3) System Memories and Peripherals
- Embedded Trace Module (ETM).

2.4.2 Embedded Trace Module (ETM)

To support real-time trace, the ARM Cortex-A8 processor provides an interface to enable connection of an embedded trace module (ETM). The ETM consists of two parts:

- The Trace port which provides real-time trace capability for the ARM Cortex-A8.
- Triggering facilities that provide trigger resources, which include address and data comparators, counter, and sequencers.

The ARM Cortex-A8 trace port is not pinned out and is, instead, only connected to the system-level Embedded Trace Buffer (ETB). The ETB has a 32KB buffer memory. ETB enabled debug tools are required to read/interpret the captured trace data.

2.4.3 ARM Cortex-A8 Interrupt Controller (AINTC)

The ARM Cortex-A8 subsystem contains an interrupt controller (AINTC) that prioritizes all service requests from the system peripherals and generates either IRQ or FIQ to the ARM Cortex-A8 processor.

2.4.4 ARM Cortex-A8 PLL (PLL_ARM)

The ARM Cortex-A8 subsystem contains an embedded PLL Controller (PLL_ARM) for generating the subsystem's clocks from the device Clock input.

2.4.5 ARM Processor Interconnect

The ARM Cortex-A8 processor is connected through the arbiter to the L3 interconnect port. The L3 interconnect port is 128-bits wide and provides access to the other device modules.

2.5 Media Controller Overview

The Media Controller has the responsibility of managing the HDVPSS, HDVICP2, and ISS modules.

2.6 HDVICP2 Overview

The HDVICP2 is a Video Encoder/Decoder hardware accelerator supporting a range of encode, decode, and transcode operations for most major video codec standards. The main video Codec standards supported in hardware are MPEG1/2/4 ASP/SP, H.264 BL/MP/HP, VC-1 SP/MP/AP, RV9/10, AVS-1.0, and ON2 VP6.2/VP7.

The HDVICP2 hardware accelerator is composed of the following elements:

- Motion estimation acceleration engine
- Loop filter acceleration engine
- Sequencer, including its memories and an interrupt controller
- Intra-prediction estimation engine
- Calculation engine
- Motion compensation engine
- Entropy coder/decoder
- Video Direct Memory Access (DMA)
- Synchronization boxes
- Shared L2 controller
- Local interconnect

2.7 Face Detect (FD) Overview

The device Face Detection (FD) module performs face detection and tracking within a picture stored in memory. This module is typically used for video encoding, face-based priority auto-focusing, or red-eye removal. The FD module supports QVGA resolution inputs stored in DRR memory in 8-bit Luma format. In addition, it uses 51.25KB of DDR for its working memory.

The FD module supports the following features:

- Input image:
  - QVGA Input Image Size (H x V = 320 x 240)
  - 8-bit Gray Scale Data (0x00 = Black and 0xFF = White)

- Detection Capabilities:
  - Face Inclination of ±45°
  - Face Direction:
    - Up/Down: ±30°
    - Left/Right: ±60°
  - Supported Detection Directions:
    - 0° Faces are Vertical
    - +90° Faces are Rotated Right by 90°
    - -90° Faces are Rotated Left by 90°
    - Supported Minimum Face Sizes of 20, 25, 32 or 40 Pixels
  - Supported Detection Start Positions:
    - X = 0 to 160
    - Y = 0 to 120
  - Supported Detection Area Sizes:
    - X = 160 to 320
    - Y = 120 to 240
  - Provides Size, Position, Angle, and Confidence Level for Each Face

2.8 Spinlock Module Overview

The Spinlock module provides hardware assistance for synchronizing the processes running on multiple processors in the device:

- ARM Cortex-A8 processor
- Media Controller

The Spinlock module implements 128 spinlocks (or hardware semaphores) that provide an efficient way to perform a lock operation of a device resource using a single read-access, avoiding the need for a read-modify-write bus transfer of which the programmable cores are not capable.

2.9 Mailbox Module Overview

The device Mailbox module facilitates communication between the ARM Cortex-A8 and the Media Controller. It consists of twelve mailboxes, each supporting a 1-way communication between two of the above processors. The sender sends information to the receiver by writing a message to the mailbox registers. Interrupt signaling is used to notify the receiver that a message has been queued or to notify the sender about an overflow situation.

The Mailbox module supports the following features (see Figure 2-2):

- 12 mailboxes
- Flexible mailbox-to-processor assignment scheme
- Four-message FIFO depth for each message queue
- 32-bit message width
- Message reception and queue-not-full notification using interrupts
- Three interrupts (one to ARM Cortex-A8 and two to Media Controller)

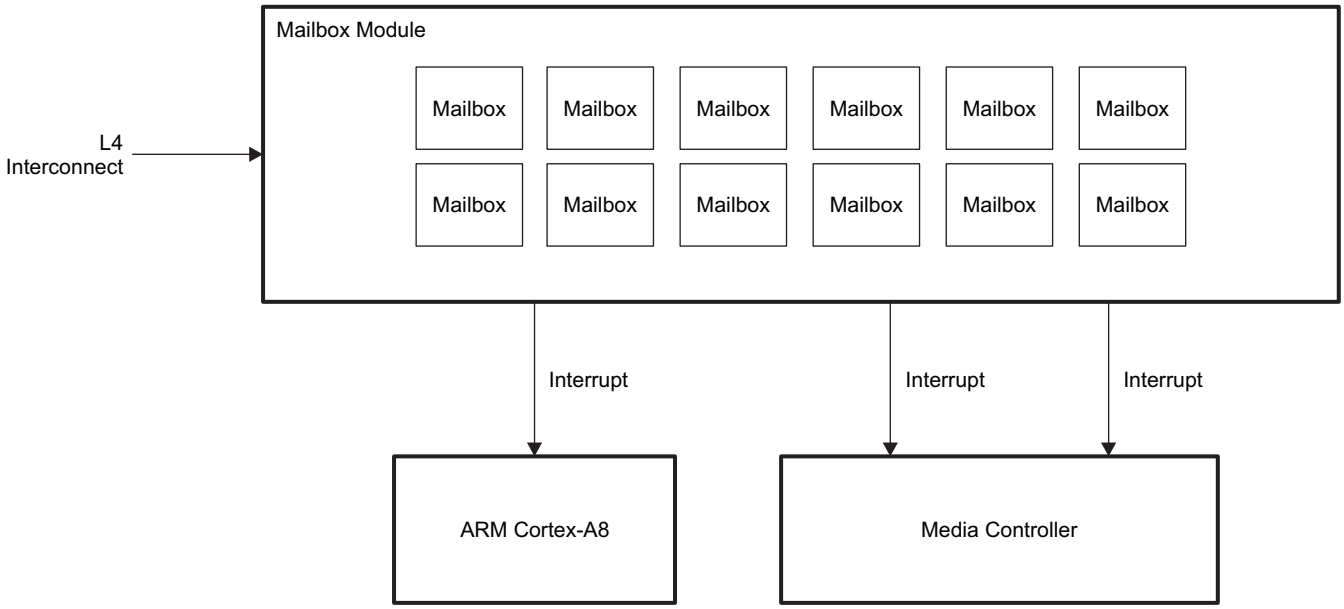


Figure 2-2. Mailbox Module Block Diagram

2.10 Memory Map Summary

The device has multiple on-chip memories associated with its processor and subsystems. To help simplify software development a unified memory map is used where possible to maintain a consistent view of device resources across all bus masters.

2.10.1 L3 Memory Map

Table 2-2 shows the L3 memory map for all system masters (including Cortex-A8).

For more details on the interconnect topology and connectivity across the L3 and L4 interconnects, see Section 5.

Table 2-2. L3 Memory Map

START ADDRESS (HEX)	END ADDRESS (HEX)	SIZE	DESCRIPTION
0x0000_0000	0x00FF_FFFF	16MB	Reserved (BOOTROM)
0x1000_0000	0x1FFF_FFFF	496MB	General Purpose Memory Controller (GPMC) External Memory Space
0x2000_0000	0x2FFF_FFFF	256MB	Reserved
0x3000_0000	0x3FFF_FFFF	256MB	Reserved
0x4000_0000	0x4001_FFFF	128KB	Reserved
0x4002_0000	0x4002_BFFF	48KB	ARM Cortex-A8 ROM (Accessible by ARM Cortex-A8 *only*)
0x4002_C000	0x402E_FFFF	2832KB	Reserved
0x402F_0000	0x402F_03FF	1KB	Reserved
0x402F_0400	0x402F_FFFF	64KB - 1KB	ARM Cortex-A8 RAM (Accessible by ARM Cortex-A8 *only*)
0x4030_0000	0x4033_FFFF	256KB	OCMC SRAM
0x4034_0000	0x407F_FFFF	4864KB	Reserved
0x4080_0000	0x4083_FFFF	256KB	Reserved
0x4084_0000	0x40DF_FFFF	5888KB	Reserved
0x40E0_0000	0x40E0_7FFF	32KB	Reserved
0x40E0_8000	0x40EF_FFFF	992KB	Reserved
0x40F0_0000	0x40F0_7FFF	32KB	Reserved
0x40F0_8000	0x40FF_FFFF	992KB	Reserved
0x4100_0000	0x41FF_FFFF	16MB	Reserved
0x4200_0000	0x43FF_FFFF	32MB	Reserved
0x4400_0000	0x443F_FFFF	4MB	L3 Fast configuration registers
0x4440_0000	0x447F_FFFF	4MB	L3 Mid configuration registers
0x4480_0000	0x44BF_FFFF	4MB	L3 Slow configuration registers
0x44C0_0000	0x45FF_FFFF	20MB	Reserved
0x4600_0000	0x463F_FFFF	4MB	McASP0 Data Peripheral Registers
0x4640_0000	0x467F_FFFF	4MB	McASP1 Data Peripheral Registers
0x4680_0000	0x46BF_FFFF	4MB	Reserved
0x46C0_0000	0x46FF_FFFF	4MB	HDMI
0x4700_0000	0x473F_FFFF	4MB	Reserved
0x4740_0000	0x477F_FFFF	4MB	USB
0x4780_0000	0x4780_FFFF	64KB	Reserved
0x4781_0000	0x4781_1FFF	8KB	MMC/SD/SDIO2 Peripheral Registers
0x4781_2000	0x47BF_FFFF	4MB - 72KB	Reserved
0x47C0_0000	0x47FF FFFF	4MB	Reserved
0x47C0_0000	0x47C0_BFFF	48KB	Reserved

Table 2-2. L3 Memory Map (continued)

START ADDRESS (HEX)	END ADDRESS (HEX)	SIZE	DESCRIPTION
0x47C0_C000	0x47C0_C3FF	1KB	Reserved
0x47C0_C400	0x47C0_C7FF	1KB	DDR PHY Registers
0x47C0_C800	0x47C0_CBFF	1KB	Reserved
0x47C0_CC00	0x47C0_CFFF	1KB	Reserved
0x47C0_D000	0x47FF FFFF	4052KB	Reserved
0x4800_0000	0x48FF_FFFF	16MB	L4 Slow Peripheral Domain (see Table 2-4)
0x4900_0000	0x490F_FFFF	1MB	EDMA TPCC Registers
0x4910_0000	0x497F_FFFF	7MB	Reserved
0x4980_0000	0x498F_FFFF	1MB	EDMA TPTC0 Registers
0x4990_0000	0x499F_FFFF	1MB	EDMA TPTC1 Registers
0x49A0_0000	0x49AF_FFFF	1MB	EDMA TPTC2 Registers
0x49B0_0000	0x49BF_FFFF	1MB	EDMA TPTC3 Registers
0x49C0_0000	0x49FF_FFFF	4MB	Reserved
0x4A00_0000	0x4AFF_FFFF	16MB	L4 Fast Peripheral Domain (see Table 2-3)
0x4B00_0000	0x4BFF_FFFF	16MB	Emulation Subsystem
0x4C00_0000	0x4CFF_FFFF	16MB	DDR Registers
0x4D00_0000	0x4DFF_FFFF	16MB	Reserved
0x4E00_0000	0x4FFF_FFFF	32MB	DDR DMM Registers
0x5000_0000	0x50FF_FFFF	16MB	GPMC Registers
0x5100_0000	0x51FF_FFFF	16MB	Reserved
0x5200_0000	0x54FF_FFFF	48MB	Reserved
0x5500_0000	0x55FF_FFFF	16MB	Media Controller
0x5600_0000	0x56FF_FFFF	16MB	Reserved
0x5700_0000	0x57FF_FFFF	16MB	Reserved
0x5800_0000	0x58FF_FFFF	16MB	HDVICP2 Configuration
0x5900_0000	0x59FF_FFFF	16MB	HDVICP2 SL2
0x5A00_0000	0x5BFF_FFFF	32MB	Reserved
0x5C00_0000	0x5DFF_FFFF	32MB	ISS
0x5E00_0000	0x5FFF_FFFF	32MB	Reserved
0x6000_0000	0x7FFF_FFFF	512MB	DDR DMM Tiler Window (see Table 2-5)
0x8000_0000	0xFFFF_FFFF	2GB	DDR
0x1 0000 0000	0x1 FFFF FFFF	4GB	DDR DMM Tiler Extended Address Map (ISS and HDVPSS only) [see Table 2-5]

2.10.2 L4 Memory Map

The L4 Fast Peripheral Domain and L4 Slow Peripheral Domain regions of the memory maps above are broken out into Table 2-3 and Table 2-4.

For more details on the interconnect topology and connectivity across the L3 and L4 interconnects, see , *System Interconnect*.

2.10.2.1 L4 Fast Peripheral Memory Map

Table 2-3. L4 Fast Peripheral Memory Map

Cortex-A8 and L3 Masters		SIZE	DEVICE NAME
START ADDRESS (HEX)	END ADDRESS (HEX)		
0x4A00_0000	0x4A00_07FF	2KB	L4 Fast Configuration - Address/Protection (AP)
0x4A00_0800	0x4A00_0FFF	2KB	L4 Fast Configuration - Link Agent (LA)
0x4A00_1000	0x4A00_13FF	1KB	L4 Fast Configuration - Initiator Port (IP0)
0x4A00_1400	0x4A00_17FF	1KB	L4 Fast Configuration - Initiator Port (IP1)
0x4A00_1800	0x4A00_1FFF	2KB	Reserved
0x4A00_2000	0x4A07_FFFF	504KB	Reserved
0x4A08_0000	0x4A09_FFFF	128KB	Reserved
0x4A0A_0000	0x4A0A_0FFF	4KB	Reserved
0x4A0A_E000	0x4A0F_FFFF	380KB	Reserved
0x4A10_0000	0x4A10_7FFF	32KB	Reserved
0x4A10_8000	0x4A10_8FFF	4KB	Reserved
0x4A14_0000	0x4A14_FFFF	64KB	SATA0 Peripheral Registers
0x4A15_0000	0x4A15_0FFF	4KB	SATA0 Interconnect Registers
0x4A15_1000	0x4A17_FFFF	188KB	Reserved
0x4A18_0000	0x4A1A_1FFF	136KB	Reserved
0x4A1A_2000	0x4A1A_3FFF	8KB	Reserved
0x4A1A_4000	0x4A1A_4FFF	4KB	Reserved
0x4A1A_5000	0x4A1A_5FFF	4KB	Reserved
0x4A1A_6000	0x4A1A_6FFF	4KB	Reserved
0x4A1A_7000	0x4A1A_7FFF	4KB	Reserved
0x4A1A_8000	0x4A1A_9FFF	8KB	Reserved
0x4A1A_A000	0x4A1A_AFFF	4KB	Reserved
0x4A1A_B000	0x4A1A_BFFF	4KB	Reserved
0x4A1A_C000	0x4A1A_CFFF	4KB	Reserved
0x4A1A_D000	0x4A1A_DFFF	4KB	Reserved
0x4A1A_E000	0x4A1A_FFFF	8KB	Reserved
0x4A1B_0000	0x4A1B_0FFF	4KB	Reserved
0x4A1B_1000	0x4A1B_1FFF	4KB	Reserved
0x4A1B_2000	0x4A1B_2FFF	4KB	Reserved
0x4A1B_6000	0x4A1B_6FFF	4KB	Reserved
0x4A1B_4000	0x4AFF_FFFF	14632KB	Reserved

2.10.2.2 L4 Slow Peripheral Memory Map

Table 2-4. L4 Slow Peripheral Memory Map

Cortex-A8 and L3 Masters		SIZE	DEVICE NAME
START ADDRESS (HEX)	END ADDRESS (HEX)		
0x4800_0000	0x4800_07FF	2KB	L4 Slow Configuration – Address/Protection (AP)
0x4800_0800	0x4800_0FFF	2KB	L4 Slow Configuration – Link Agent (LA)
0x4800_1000	0x4800_13FF	1KB	L4 Slow Configuration – Initiator Port (IP0)
0x4800_1400	0x4800_17FF	1KB	L4 Slow Configuration – Initiator Port (IP1)
0x4800_1800	0x4800_1FFF	2KB	Reserved
0x4800_2000	0x4800_7FFF	24KB	Reserved
0x4800_8000	0x4800_8FFF	32KB	Reserved
0x4801_0000	0x4801_0FFF	4KB	Reserved
0x4801_1000	0x4801_1FFF	4KB	Reserved
0x4801_2000	0x4801_FFFF	56KB	Reserved
0x4802_0000	0x4802_0FFF	4KB	UART0 Peripheral Registers
0x4802_1000	0x4802_1FFF	4KB	UART0 Interconnect Registers
0x4802_2000	0x4802_2FFF	4KB	UART1 Peripheral Registers
0x4802_3000	0x4802_3FFF	4KB	UART1 Interconnect Registers
0x4802_4000	0x4802_4FFF	4KB	UART2 Peripheral Registers
0x4802_5000	0x4802_5FFF	4KB	UART2 Interconnect Registers
0x4802_6000	0x4802_7FFF	8KB	Reserved
0x4802_8000	0x4802_8FFF	4KB	I2C0 Peripheral Registers
0x4802_9000	0x4802_9FFF	4KB	I2C0 Interconnect Registers
0x4802_A000	0x4802_AFFF	4KB	I2C1 Peripheral Registers
0x4802_B000	0x4802_BFFF	4KB	I2C1 Interconnect Registers
0x4802_C000	0x4802_DFFF	8KB	Reserved
0x4802_E000	0x4802_EFFF	4KB	TIMER1 Peripheral Registers
0x4802_F000	0x4802_FFFF	4KB	TIMER1 Interconnect Registers
0x4803_0000	0x4803_0FFF	4KB	SPI0 Peripheral Registers
0x4803_1000	0x4803_1FFF	4KB	SPI0 Interconnect Registers
0x4803_2000	0x4803_2FFF	4KB	GPIO0 Peripheral Registers
0x4803_3000	0x4803_3FFF	4KB	GPIO0 Interconnect Registers
0x4803_4000	0x4803_7FFF	16KB	Reserved
0x4803_8000	0x4803_9FFF	8KB	McASP0 CFG Peripheral Registers
0x4803_A000	0x4803_AFFF	4KB	McASP0 CFG Interconnect Registers
0x4803_B000	0x4803_BFFF	4KB	Reserved
0x4803_C000	0x4803_DFFF	8KB	McASP1 CFG Peripheral Registers
0x4803_E000	0x4803_EFFF	4KB	McASP1 CFG Interconnect Registers
0x4803_F000	0x4803_FFFF	4KB	Reserved
0x4804_0000	0x4804_0FFF	4KB	TIMER2 Peripheral Registers
0x4804_1000	0x4804_1FFF	4KB	TIMER2 Interconnect Registers
0x4804_2000	0x4804_2FFF	4KB	TIMER3 Peripheral Registers
0x4804_3000	0x4804_3FFF	4KB	TIMER3 Interconnect Registers
0x4804_4000	0x4804_4FFF	4KB	TIMER4 Peripheral Registers
0x4804_5000	0x4804_5FFF	4KB	TIMER4 Interconnect Registers
0x4804_6000	0x4804_6FFF	4KB	TIMER5 Peripheral Registers
0x4804_7000	0x4804_7FFF	4KB	TIMER5 Interconnect Registers

Table 2-4. L4 Slow Peripheral Memory Map (continued)

Cortex-A8 and L3 Masters		SIZE	DEVICE NAME
START ADDRESS (HEX)	END ADDRESS (HEX)		
0x4804_8000	0x4804_8FFF	4KB	TIMER6 Peripheral Registers
0x4804_9000	0x4804_9FFF	4KB	TIMER6 Interconnect Registers
0x4804_A000	0x4804_AFFF	4KB	TIMER7 Peripheral Registers
0x4804_B000	0x4804_BFFF	4KB	TIMER7 Interconnect Registers
0x4804_C000	0x4804_CFFF	4KB	GPIO1 Peripheral Registers
0x4804_D000	0x4804_DFFF	4KB	GPIO1 Interconnect Registers
0x4804_E000	0x4804_FFFF	8KB	Reserved
0x4805_0000	0x4805_1FFF	8KB	Reserved
0x4805_2000	0x4805_2FFF	4KB	Reserved
0x4805_3000	0x4805_FFFF	52KB	Reserved
0x4806_0000	0x4806_FFFF	64KB	MMC/SD/SDIO0 Peripheral Registers
0x4807_0000	0x4807_0FFF	4KB	MMC/SD/SDIO0 Interconnect Registers
0x4807_1000	0x4807_FFFF	60KB	Reserved
0x4808_0000	0x4808_FFFF	64KB	ELM Peripheral Registers
0x4809_0000	0x4809_0FFF	4KB	ELM Interconnect Registers
0x4809_1000	0x4809_FFFF	60KB	Reserved
0x480A_0000	0x480A_FFFF	64KB	Reserved
0x480B_0000	0x480B_0FFF	4KB	Reserved
0x480B_1000	0x480B_FFFF	60KB	Reserved
0x480C_0000	0x480C_0FFF	4KB	RTC Peripheral Registers
0x480C_1000	0x480C_1FFF	4KB	RTC Interconnect Registers
0x480C_2000	0x480C_3FFF	8KB	Reserved
0x480C_4000	0x480C_7FFF	16KB	Reserved
0x480C_8000	0x480C_8FFF	4KB	Mailbox Peripheral Registers
0x480C_9000	0x480C_9FFF	4KB	Mailbox Interconnect Registers
0x480C_A000	0x480C_AFFF	4KB	Spinlock Peripheral Registers
0x480C_B000	0x480C_BFFF	4KB	Spinlock Interconnect Registers
0x480C_C000	0x480F_FFFF	208KB	Reserved
0x4810_0000	0x4811_FFFF	128KB	HDVPSS Peripheral Registers
0x4812_0000	0x4812_0FFF	4KB	HDVPSS Interconnect Registers
0x4812_1000	0x4812_1FFF	4KB	Reserved
0x4812_2000	0x4812_2FFF	4KB	HDMI Peripheral Registers
0x4812_3000	0x4812_3FFF	4KB	HDMI Interconnect Registers
0x4812_4000	0x4813_FFFF	112KB	Reserved
0x4814_0000	0x4815_FFFF	128KB	Control Module Peripheral Registers
0x4816_0000	0x4816_0FFF	4KB	Control Module Interconnect Registers
0x4816_1000	0x4817_FFFF	124KB	Reserved
0x4818_0000	0x4818_2FFF	12KB	PRCM Peripheral Registers
0x4818_3000	0x4818_3FFF	4KB	PRCM Interconnect Registers
0x4818_4000	0x4818_7FFF	16KB	Reserved
0x4818_8000	0x4818_8FFF	4KB	SmartReflex0 Peripheral Registers
0x4818_9000	0x4818_9FFF	4KB	SmartReflex0 Interconnect Registers
0x4818_A000	0x4818_AFFF	4KB	SmartReflex1 Peripheral Registers
0x4818_B000	0x4818_BFFF	4KB	SmartReflex1 Interconnect Registers
0x4818_C000	0x4818_CFFF	4KB	OCP Watchpoint Peripheral Registers
0x4818_D000	0x4818_DFFF	4KB	OCP Watchpoint Interconnect Registers

Table 2-4. L4 Slow Peripheral Memory Map (continued)

Cortex-A8 and L3 Masters		SIZE	DEVICE NAME
START ADDRESS (HEX)	END ADDRESS (HEX)		
0x4818_E000	0x4818_EFFF	4KB	Reserved
0x4818_F000	0x4818_FFFF	4KB	Reserved
0x4819_0000	0x4819_3FFF	16KB	Reserved
0x4819_4000	0x4819_BFFF	32KB	Reserved
0x4819_C000	0x481F_FFFF	400KB	Reserved
0x4819_C000	0x4819_CFFF	4KB	I2C2 Peripheral Registers
0x4819_D000	0x4819_DFFF	4KB	I2C2 Interconnect Registers
0x4819_E000	0x4819_EFFF	4KB	I2C3 Peripheral Registers
0x4819_F000	0x4819_FFFF	4KB	I2C3 Interconnect Registers
0x481A_0000	0x481A_0FFF	4KB	SPI1 Peripheral Registers
0x481A_1000	0x481A_1FFF	4KB	SPI1 Interconnect Registers
0x481A_2000	0x481A_2FFF	4KB	SPI2 Peripheral Registers
0x481A_3000	0x481A_3FFF	4KB	SPI2 Interconnect Registers
0x481A_4000	0x481A_4FFF	4KB	SPI3 Peripheral Registers
0x481A_5000	0x481A_5FFF	4KB	SPI3 Interconnect Registers
0x481A_6000	0x481A_6FFF	4KB	Reserved
0x481A_7000	0x481A_7FFF	4KB	Reserved
0x481A_8000	0x481A_8FFF	4KB	Reserved
0x481A_9000	0x481A_9FFF	4KB	Reserved
0x481A_A000	0x481A_AFFF	4KB	Reserved
0x481A_B000	0x481A_BFFF	4KB	Reserved
0x481A_C000	0x481A_CFFF	4KB	GPIO2 Peripheral Registers
0x481A_D000	0x481A_DFFF	4KB	GPIO2 Interconnect Registers
0x481A_E000	0x481A_EFFF	4KB	GPIO3 Peripheral Registers
0x481A_F000	0x481A_FFFF	4KB	GPIO3 Interconnect Registers
0x481B_0000	0x481B_FFFF	64KB	Reserved
0x481C_0000	0x481C_0FFF	4KB	Reserved
0x481C_1000	0x481C_1FFF	4KB	TIMER8 Peripheral Registers
0x481C_2000	0x481C_2FFF	4KB	TIMER8 Interconnect Registers
0x481C_3000	0x481C_3FFF	4KB	SYNCTIMER32K Peripheral Registers
0x481C_4000	0x481C_4FFF	4KB	SYNCTIMER32K Interconnect Registers
0x481C_5000	0x481C_5FFF	4KB	PLLSS Peripheral Registers
0x481C_6000	0x481C_6FFF	4KB	PLLSS Interconnect Registers
0x481C_7000	0x481C_7FFF	4KB	WDT0 Peripheral Registers
0x481C_8000	0x481C_8FFF	4KB	WDT0 Interconnect Registers
0x481C_9000	0x481C_9FFF	8KB	Reserved
0x481C_A000	0x481C_BFFF	8KB	Reserved
0x481C_C000	0x481C_DFFF	8KB	DCAN0 Peripheral Registers
0x481C_E000	0x481C_FFFF	8KB	DCAN0 Interconnect Registers
0x481D_0000	0x481D_1FFF	8KB	DCAN1 Peripheral Registers
0x481D_2000	0x481D_3FFF	8KB	DCAN1 Interconnect Registers
0x481D_4000	0x481D_5FFF	8KB	Reserved
0x481D_6000	0x481D_6FFF	4KB	Reserved
0x481D_7000	0x481D_7FFF	4KB	Reserved
0x481D_8000	0x481E_7FFF	64KB	MMC/SD/SDIO1 Peripheral Registers
0x481E_8000	0x481E_8FFF	4KB	MMC/SD/SDIO1 Interconnect Registers

Table 2-4. L4 Slow Peripheral Memory Map (continued)

Cortex-A8 and L3 Masters		SIZE	DEVICE NAME
START ADDRESS (HEX)	END ADDRESS (HEX)		
0x481E_9000	0x481F_FFFF	52KB	Reserved
0x4820_0000	0x4820_0FFF	4KB	Interrupt controller(1)
0x4820_1000	0x4823_FFFF	252KB	Reserved(1)
0x4824_0000	0x4824_0FFF	4KB	MPUSS config register(1)
0x4824_1000	0x4827_FFFF	252KB	Reserved(1)
0x4828_0000	0x4828_0FFF	4KB	SSM(1)
0x4828_1000	0x482F_FFFF	508KB	Reserved(1)
0x4830_0000	0x48FF_FFFF	13MB	Reserved

(1) These regions decoded internally by the Cortex™-A8 Subsystem and are not physically part of the L4 Slow. They are included here only for reference when considering the Cortex™-A8 Memory Map. For Masters other than the Cortex-A8 these regions are reserved.

2.10.3 DDR DMM TILER Extended Addressing Map

The Tiler includes an additional 4-GBytes of addressing range, enabled by a 33rd address bit, to access the frame buffer in rotated and mirrored views. shows the details of the Tiler Extended Address Mapping. This entirety of this additional range is only accessible to the HDVPSS and ISS subsystems. However, other masters can access any one single view through the 512-MB Tiler region in the base 4GByte address memory map.

Table 2-5. DDR DMM TILER Extended Address Mapping

BLOCK NAME	START ADDRESS (HEX)	END ADDRESS (HEX)	SIZE	DESCRIPTION
Tiler View 0	0x1 0000_0000	0x1 1FFF_FFFF	512MB	Natural 0° View
Tiler View 1	0x1 2000_0000	0x1 3FFF_FFFF	512MB	0° with Vertical Mirror View
Tiler View 2	0x1 4000_0000	0x1 5FFF_FFFF	512MB	0° with Horizontal Mirror View
Tiler View 3	0x1 6000_0000	0x1 7FFF_FFFF	512MB	180° View
Tiler View 4	0x1 8000_0000	0x1 9FFF_FFFF	512MB	90° with Vertical Mirror View
Tiler View 5	0x1 A000_0000	0x1 BFFF_FFFF	512MB	270° View
Tiler View 6	0x1 C000_0000	0x1 DFFF_FFFF	512MB	90° View
Tiler View 7	0x1 E000_0000	0x1 FFFF_FFFF	512MB	90° with Horizontal Mirror View

3 Device Pins

3.1 Pin Maps

The following tables show the top view of the package pin assignments in eight pin maps.

Table 3-1. AAR Ball Map [Section Top_Left - Top View]

	A	B	C	D	E	F
31	VSS	VOUT[0]_R_CR[9]	No Ball	UART0_RTS	UART0_DCD	No Ball
30	VOUT[0]_R_CR[8]	VOUT[0]_R_CR[7]	VOUT[0]_R_CR[6]	UART0_CTS	UART0_DTR	DEVOSC_MXI
29	VOUT[0]_R_CR[5]	VOUT[0]_R_CR[4]	No Ball	No Ball	UART0_DSR	No Ball
28	No Ball	VOUT[0]_R_CR[3]	VOUT[0]_R_CR[2]	No Ball	UART0_TXD	No Ball
27	VOUT[0]_G_Y_YC[9]	VOUT[0]_G_Y_YC[8]	No Ball	No Ball	No Ball	No Ball
26	VOUT[0]_G_Y_YC[6]	VOUT[0]_G_Y_YC[5]	VOUT[0]_G_Y_YC[3]	No Ball	VOUT[0]_G_Y_YC[4]	No Ball
25	No Ball	VOUT[0]_G_Y_YC[7]	VOUT[0]_G_Y_YC[2]	VSS	VSS	VSS
24	USB1_ID	USB1_VBUSIN	VOUT[0]_B_CB_C[9]	VOUT[0]_B_CB_C[8]	VOUT[0]_B_CB_C[7]	VOUT[0]_B_CB_C[2]
23	USB1_DP	USB1_DM	No Ball	No Ball	No Ball	No Ball
22	No Ball	USB0_VBUSIN	No Ball	No Ball	No Ball	No Ball
21	USB0_DP	USB0_DM	USB1_CE	VOUT[0]_B_CB_C[3]	VSS	VOUT[0]_HSYNC
20	USB0_ID	USB0_CE	VOUT[0]_AVID	VSSA_USB	VOUT[0]_VSYNC	VSS
19	No Ball	EMU1	No Ball	No Ball	No Ball	No Ball
18	EMU0	VIN[0]A_D[0]	No Ball	No Ball	No Ball	No Ball
17	VIN[0]A_D[1]	VIN[0]A_D[2]	VIN[0]A_D[3]	VIN[0]A_D[4]	DVDD	VIN[0]A_D[5]
16	No Ball	VIN[0]A_D[8]_BD[0]	VIN[0]A_D[9]_BD[1]	DVDD	VIN[0]A_D[10]_BD[2]	DVDD

Ball Map Position

1	2	3	4	5
6	7	8	9	10

Table 3-2. AAR Ball Map [Section Top_Left_Middle - Top View]

	G	H	J	K	L	M
31	DEVOSC_MXO	SERDES_CLKN	No Ball	RSV26	RSV36	No Ball
30	VSSA_DEVOSC	SERDES_CLKP	RSV24	RSV25	SATA0_RXN0	SATA0_RXP0
29	$\overline{\text{SPI[0]\_SCS[0]}}$	RSV40	$\overline{\text{SPI[1]\_SCS[0]}}$	No Ball	No Ball	SPI[1]_SCLK
28	$\overline{\text{SPI[0]\_SCS[1]}}$	RSV3	SPI[0]_D[0]	No Ball	No Ball	RSV54
27	VSS	RSV1	SPI[0]_D[1]	No Ball	No Ball	SPI[1]_D[1]
26	VSS	VSS	UART0_RXD	No Ball	No Ball	RSV53
25	VSS	RSV39	RSV0	No Ball	No Ball	VDDA_1P8
24	VSS	RSV2	VOUT[0]_B_CB_C[6]	No Ball	No Ball	LDOCAP_SERDESCLK
23	VSS	VOUT[0]_B_CB_C[5]	VOUT[0]_B_CB_C[4]	USB0_DRVVBUS	No Ball	No Ball
22	No Ball	No Ball	No Ball	VOUT[0]_CLK	UART2_RXD	No Ball
21	No Ball	No Ball	No Ball	No Ball	No Ball	UART2_TXD
20	VSS	VIN[0]A_D[7]	No Ball	LDOCAP_ARMRAM	VIN[0]A_D[6]	VDDA_USB_3P3
19	No Ball	No Ball	LDOCAP_ARM	VDDA_USB0_1P8	VDDA_ARMPLL_1P8	VDDA_USB_3P3
18	No Ball	No Ball	No Ball	No Ball	CVDD_ARM	No Ball
17	RSV4	VIN[0]A_D[11]_BD[3]	VDDA_USB1_1P8	CVDD_ARM	CVDD_ARM	CVDD_ARM
16	RSV5	VIN[0]A_D[13]_BD[5]	VIN[0]A_D[12]_BD[4]	VDDA_HDDAC_1P1	VSS	VSS

Ball Map Position

1	2	3	4	5
6	7	8	9	10

Table 3-3. AAR Ball Map [Section Top_Middle_Middle - Top View]

	N	P	R	T	U	V
31	SATA0_TXP0	RSV31	No Ball	TMS	AUXOSC_MXO	No Ball
30	SATA0_TXN0	RSV43	RSV32	RSV33	VSSA_AUXOSC	AUXOSC_MXI
29	RTCK	No Ball	No Ball	TCLK	SD1_DAT[2]_SDRW	No Ball
28	TDI	No Ball	No Ball	DVDD	DEVOSC_WAKE	No Ball
27	VDDA_SATA0_1P8	No Ball	No Ball	I2C[0]_SCL	DVDD	No Ball
26	UART0_RIN	No Ball	No Ball	DVDD	TDO	No Ball
25	VDDA_1P8	No Ball	No Ball	DVDD_SD	DVDD_SD	No Ball
24	SPI[0]_SCLK	No Ball	No Ball	I2C[0]_SDA	TRST	No Ball
23	SPI[1]_D[0]	VDDA_1P8	No Ball	VDDA_HDVICPPLL_1P8	VSS	No Ball
22	VDDA_1P8	No Ball	No Ball	LDOCAP_RAM1	No Ball	No Ball
21	No Ball	VDDS_OSC0_1P8	VSS	VSS	CVDD_HDVICP	CVDD_HDVICP
20	VSSA_USB	VDDS_OSC1_1P8	VSS	VSS	CVDD_HDVICP	CVDD_HDVICP
19	VSSA_USB	No Ball	No Ball	VSS	No Ball	No Ball
18	No Ball	VSS	VSS	CVDD	VSS	VSS
17	VSS	CVDD	CVDD	CVDD	CVDD	CVDD
16	VSS	No Ball	No Ball	VSS	No Ball	No Ball

Ball Map Position

1	2	3	4	5
6	7	8	9	10

Table 3-4. AAR Ball Map [Section Top_Right_Middle - Top View]

	W	Y	AA	AB	AC	AD
31	SD1_DAT[0]	SD0_DAT[2]_SDRW	No Ball	SD0_DAT[6]	MCA[0]_AXR[3]	No Ball
30	SD1_CLK	SD0_DAT[3]	SD1_DAT[1]_SDIRQ	SD0_CLK	SD0_DAT[7]	MCA[0]_ACLKR
29	No Ball	SD1_CMD	SD0_CMD	No Ball	No Ball	MCA[1]_ACLKR
28	No Ball	VSS	SD0_DAT[0]	No Ball	No Ball	MCA[0]_ACLKX
27	No Ball	SD1_DAT[3]	VSS	No Ball	No Ball	MCA[0]_AXR[5]
26	No Ball	VSS	SD0_DAT[1]_SDIRQ	No Ball	No Ball	MCA[0]_AXR[4]
25	No Ball	VSS	No Ball	No Ball	VSS	VSS
24	No Ball	LDOCAP_HDVICPRAM	No Ball	No Ball	MCA[1]_AFSR	VSS
23	LDOCAP_HDVICP	No Ball	No Ball	No Ball	MCA[1]_ACLKX	DDR[0]_A[10]
22	CVDD_HDVICP	MCA[1]_AXR[0]	No Ball	MCA[1]_AFSX	DDR[0]_A[1]	No Ball
21	No Ball	MCA[1]_AXR[1]	No Ball	DDR[0]_CS[0]	No Ball	No Ball
20	CVDD	CVDD	DDR[0]_RST	No Ball	No Ball	DDR[0]_CKE
19	CVDD	CVDD	VDDA_DDRPLL_1P8	No Ball	DDR[0]_D[29]	DDR[0]_D[28]
18	No Ball	No Ball	VSS	DVDD_DDR[0]	DVDD_DDR[0]	No Ball
17	VSS	VSS	VSS	DVDD_DDR[0]	DVDD_DDR[0]	No Ball
16	VSS	VSS	VSS	No Ball	DDR[0]_D[23]	DDR[0]_D[22]

Ball Map Position

1	2	3	4	5
6	7	8	9	10

Table 3-5. AAR Ball Map [Section Top_Right - Top View]

	AE	AF	AG	AH	AJ	AK	AL
31	MCA[0]_AXR[1]	AUD_CLKIN0	No Ball	$\overline{\text{NMI}}$	CLKIN32	No Ball	VSS
30	MCA[0]_AXR[2]	MCA[0]_AFSR	AUD_CLKIN2	$\overline{\text{POR}}$	$\overline{\text{RSTOUT\_WD\_OUT}}$	DDR[0]_A[6]	DDR[0]_VTP
29	MCA[0]_AFSX	MCA[0]_AXR[0]	No Ball	$\overline{\text{RESET}}$	No Ball	DDR[0]_A[9]	DDR[0]_A[8]
28	VSS	No Ball	No Ball	No Ball	No Ball	DDR[0]_A[4]	No Ball
27	VSS	AUD_CLKIN1	No Ball	DDR[0]_A[5]	DDR[0]_A[3]	$\overline{\text{DDR[0]\_CLK}}$	DDR[0]_CLK
26	VSS	No Ball	No Ball	No Ball	No Ball	DDR[0]_BA[0]	$\overline{\text{DDR[0]\_WE}}$
25	VSS	VSS	VSS	DDR[0]_BA[2]	$\overline{\text{DDR[0]\_RAS}}$	$\overline{\text{DDR[0]\_CAS}}$	No Ball
24	VSS	VSS	VSS	RSV34	RSV35	DDR[0]_A[11]	DDR[0]_A[0]
23	VSS	DDR[0]_BA[1]	DDR[0]_A[7]	DDR[0]_A[12]	DDR[0]_A[2]	DDR[0]_A[13]	DDR[0]_A[14]
22	No Ball	No Ball	No Ball	No Ball	No Ball	DDR[0]_A[15]	No Ball
21	No Ball	No Ball	No Ball	No Ball	No Ball	RSV42	DDR[0]_ODT[0]
20	VSS	VSS	DDR[0]_D[31]	VSS	DDR[0]_D[30]	$\overline{\text{DDR[0]\_DQS[3]}}$	DDR[0]_DQS[3]
19	VSS	DDR[0]_D[27]	VSS	DDR[0]_D[26]	DDR[0]_D[25]	DDR[0]_D[24]	No Ball
18	No Ball	No Ball	No Ball	No Ball	No Ball	DDR[0]_DQM[3]	VREFSSTL_DDR[0]
17	No Ball	No Ball	No Ball	No Ball	No Ball	$\overline{\text{DDR[0]\_DQS[2]}}$	DDR[0]_DQS[2]
16	DVDD_DDR[0]	DVDD_DDR[0]	DDR[0]_D[21]	DVDD_DDR[0]	DDR[0]_D[20]	DDR[0]_D[19]	No Ball

Ball Map Position

1	2	3	4	5
6	7	8	9	10

Table 3-6. AAR Ball Map [Section Bottom_Left - Top View]

	A	B	C	D	E	F
15	HDMI_CLKP	HDMI_CLKN	No Ball	No Ball	No Ball	No Ball
14	HDMI_DN0	HDMI_DP0	No Ball	No Ball	No Ball	No Ball
13	No Ball	HDMI_DN1	VIN[0]A_VSYNC	VIN[0]A_HSYNC	DVDD_C	VIN[0]A_D[14]_BD[6]
12	HDMI_DN2	HDMI_DP1	VIN[0]A_DE	DVDD_C	VIN[0]A_D[17]	DVDD_C
11	HDMI_DP2	TV_RSET	No Ball	No Ball	No Ball	No Ball
10	No Ball	TV_VFB0	No Ball	No Ball	No Ball	No Ball
9	HDDAC_A	TV_OUT0	VIN[0]A_CLK	HDDAC_VSYNC	HDDAC_HSYNC	VIN[0]A_D[20]
8	HDDAC_B	HDDAC_C	VSSA_VDAC	VSS	VSS	VSS
7	No Ball	HDDAC_VREF	VIN[0]A_D[21]	VIN[0]A_D[19]	VSS	VSS
6	VIN[0]A_D[22]	HDDAC_IREF	No Ball	No Ball	No Ball	No Ball
5	VIN[0]A_D[23]	VIN[0]A_DE	VIN[0]B_DE	VOUT[1]_B_CB_C[1]	No Ball	VOUT[1]_VSYNC
4	No Ball	VIN[0]A_FLD	No Ball	No Ball	No Ball	No Ball
3	VIN[0]B_FLD	VOUT[0]_FLD	No Ball	VOUT[1]_CLK	No Ball	VOUT[1]_B_CB_C[4]
2	VOUT[1]_G_Y_YC[1]	VOUT[1]_G_Y_YC[0]	VOUT[1]_R_CR[0]	I2C[1]_SCL	VOUT[1]_HSYNC	VOUT[1]_B_CB_C[3]
1	VSS	No Ball	VOUT[1]_R_CR[1]	I2C[1]_SDA	No Ball	VOUT[1]_AVID

Ball Map Position

1	2	3	4	5
6	7	8	9	10

Table 3-7. AAR Ball Map [Section Bottom_Left_Middle - Top View]

	G	H	J	K	L	M
15	No Ball	No Ball	No Ball	No Ball	VDDA_HDDACREF_1P8	No Ball
14	No Ball	No Ball	VDDA_VDAC_1P8	VDDA_HDMI_1P8	VDDA_HDDAC_1P8	CVDD_ARM
13	DVDD_C	VIN[0]A_D[15]_BD[7]	VIN[0]A_FLD	No Ball	VDDA_VIDPLL_1P8	CVDD_ARM
12	DVDD_C	VIN[0]B_CLK	No Ball	No Ball	VOUT[1]_R_CR[6]	No Ball
11	No Ball	No Ball	No Ball	VIN[0]A_D[16]	No Ball	VOUT[1]_R_CR[5]
10	No Ball	No Ball	VOUT[1]_FLD	VIN[0]A_D[18]	No Ball	VOUT[1]_R_CR[7]
9	VSSA_HDMI	VOUT[1]_B_CB_C[0]	VOUT[1]_G_Y_YC[7]	No Ball	No Ball	No Ball
8	VSS	VSSA_HDMI	VOUT[1]_G_Y_YC[4]	No Ball	No Ball	VOUT[1]_B_CB_C[2]
7	VSS	VSS	VSS	No Ball	No Ball	DVDD
6	VSS	VOUT[1]_G_Y_YC[3]	No Ball	No Ball	VOUT[1]_R_CR[2]	DVDD
5	VSS	VOUT[1]_B_CB_C[9]	No Ball	No Ball	DVDD	GPMC_A[19]
4	VSS	VOUT[1]_G_Y_YC[6]	No Ball	No Ball	VOUT[1]_R_CR[3]	DVDD
3	VOUT[1]_B_CB_C[8]	VOUT[1]_B_CB_C[7]	No Ball	No Ball	VOUT[1]_G_Y_YC[8]	GPMC_A[18]
2	VOUT[1]_B_CB_C[6]	VOUT[1]_R_CR[4]	VOUT[1]_R_CR[8]	VOUT[1]_R_CR[9]	VOUT[1]_G_Y_YC[2]	GPMC_A[17]
1	VOUT[1]_B_CB_C[5]	No Ball	VOUT[1]_G_Y_YC[5]	VOUT[1]_G_Y_YC[9]	No Ball	GPMC_A[16]

Ball Map Position

1	2	3	4	5
6	7	8	9	10

Table 3-8. AAR Ball Map [Section Bottom_Middle_Middle - Top View]

	N	P	R	T	U	V
15	No Ball	CVDD	CVDD	VSS	CVDD	CVDD
14	VSS	VSS	VSS	VSS	VSS	VSSA_CSI2
13	VSS	No Ball	No Ball	CVDD	No Ball	No Ball
12	No Ball	VSS	VSS	VSS	CVDD	CVDD
11	DVDD	VSS	VSS	VSS	CVDD	CVDD
10	DVDD	No Ball	No Ball	VDDA_1P8	No Ball	No Ball
9	GPMC_A[20]	No Ball	VDDA_1P8	VDDA_1P8	LDOCAP_RAM0	VDDA_AUDIOPLL_1P8
8	No Ball	No Ball	GPMC_A[23]	GPMC_D[9]	No Ball	No Ball
7	No Ball	No Ball	DVDD_GPMC	DVDD_GPMC	No Ball	No Ball
6	No Ball	No Ball	GPMC_D[10]	DVDD_GPMC	No Ball	No Ball
5	No Ball	No Ball	DVDD_GPMC	GPMC_D[5]	No Ball	No Ball
4	No Ball	No Ball	GPMC_D[11]	DVDD_GPMC	No Ball	No Ball
3	No Ball	No Ball	GPMC_D[12]	GPMC_D[6]	No Ball	No Ball
2	GPMC_A[22]	GPMC_D[15]	GPMC_D[13]	GPMC_D[7]	GPMC_D[3]	CSI2_DY[4]
1	GPMC_A[21]	No Ball	GPMC_D[14]	GPMC_D[8]	No Ball	CSI2_DX[4]

Ball Map Position

1	2	3	4	5
6	7	8	9	10

Table 3-9. AAR Ball Map [Section Bottom_Right_Middle - Top View]

	W	Y	AA	AB	AC	AD
15	No Ball	No Ball	VSS	DVDD_DDR[0]	DVDD_DDR[0]	DDR[0]_D[18]
14	CVDD	CVDD	VSS	DVDD_DDR[0]	No Ball	No Ball
13	CVDD	CVDD	VSS	No Ball	DDR[0]_D[13]	No Ball
12	No Ball	No Ball	GPMC_CS[1]	DDR[0]_D[11]	No Ball	DDR[0]_D[10]
11	VDDA_L3L4_1P8	GPMC_BE[1]	No Ball	No Ball	No Ball	No Ball
10	VDDA_CSI2_1P8	No Ball	GPMC_ADV _ALE	LDOCAP_RAM2	No Ball	No Ball
9	GPMC_D[4]	No Ball	No Ball	GPMC_CLK	GPMC_CS[0]	DDR[0]_D[5]
8	GPMC_WAIT[0]	GPMC_OE_RE	No Ball	No Ball	SD2_DAT[2]_SDRW	RSV41
7	DVDD_RGMII	DVDD_RGMII	No Ball	No Ball	VSSA_CSI2	VSS
6	GPMC_D[0]	DVDD_RGMII	No Ball	No Ball	SD2_SCLK	VSS
5	DVDD_RGMII	GPMC_WE	No Ball	No Ball	SD2_DAT[1]_SDIRQ	VSS
4	GPMC_D[1]	DVDD_RGMII	No Ball	No Ball	SD2_DAT[0]	VSS
3	GPMC_D[2]	GPMC_BE[0] _CLE	No Ball	No Ball	GPMC_CS[2]	VSS
2	CSI2_DX[3]	CSI2_DY[2]	CSI2_DX[2]	CSI2_DX[0]	CSI2_DY[0]	SD2_DAT[4]
1	CSI2_DY[3]	No Ball	CSI2_DX[1]	CSI2_DY[1]	No Ball	SD2_DAT[3]

Ball Map Position

1	2	3	4	5
6	7	8	9	10

Table 3-10. AAR Ball Map [Section Bottom_Right - Top View]

	AE	AF	AG	AH	AJ	AK	AL
15	DVDD_DDR[0]	DDR[0]_D[17]	DVDD_DDR[0]	DDR[0]_D[16]	DDR[0]_DQM[2]	$\overline{\text{DDR[0]\_DQS[1]}}$	DDR[0]_DQS[1]
14	No Ball	No Ball	No Ball	No Ball	No Ball	DDR[0]_D[15]	DDR[0]_D[14]
13	No Ball	No Ball	No Ball	No Ball	No Ball	DDR[0]_D[12]	No Ball
12	VSS	VSS	DDR[0]_D[9]	VSS	DDR[0]_D[8]	DDR[0]_DQM[1]	DDR[0]_D[7]
11	No Ball	DDR[0]_D[6]	VSS	DDR[0]_D[4]	DDR[0]_D[3]	$\overline{\text{DDR[0]\_DQS[0]}}$	DDR[0]_DQS[0]
10	No Ball	No Ball	No Ball	No Ball	No Ball	DDR[0]_D[2]	No Ball
9	VSS	No Ball	No Ball	No Ball	No Ball	DDR[0]_D[1]	DDR[0]_D[0]
8	VSS	GPMC_A[15]	GPMC_A[14]	GPMC_A[13]	GPMC_A[12]	GPMC_A[11]	DDR[0]_DQM[0]
7	VSS	VSS	VSS	VSS	GPMC_A[8]	GPMC_A[9]	No Ball
6	VSS	No Ball	$\overline{\text{GPMC\_CS[4]}}$	No Ball	GPMC_A[5]	GPMC_A[7]	GPMC_A[6]
5	VSS	No Ball	No Ball	No Ball	No Ball	GPMC_A[4]	GPMC_A[3]
4	GPMC_A[10]	No Ball	VIN[1]B_D[0]	No Ball	GPMC_A[2]	GPMC_A[1]	No Ball
3	SD2_DAT[7]	No Ball	GP1[12]	No Ball	No Ball	GPMC_A[27]	VIN[1]B_D[7]
2	SD2_DAT[6]	$\overline{\text{GPMC\_CS[3]}}$	GP1[11]	VIN[1]B_D[2]	VIN[1]B_D[3]	VIN[1]B_D[5]	VIN[1]B_D[6]
1	SD2_DAT[5]	No Ball	TIM2_IO	VIN[1]B_D[1]	No Ball	VIN[1]B_D[4]	VSS

Ball Map Position

1	2	3	4	5
6	7	8	9	10

3.2 Pin Assignments

The following table provides a summary of the device signal ball assignments and characteristics.

1. **BALL NUMBER:** Package ball number(s) associated with each signal(s).
2. **BALL NAME:** The name of the package ball or terminal.
   Note: The table does not take into account subsystem terminal multiplexing options.
3. **SIGNAL NAME**: The signal name for that ball in the mode being used.
4. **PINCNTL REGISTER NAME AND ADDRESS**: The name and address of the register that controls the pin's internal pull-up/down resistors and multiplexing options.
5. **PINCNTL DEFAULT VALUE**: The default value of the PINCNTL after reset.
6. **MODE:** The setting of the MUXMODE[10:0] bits in the associated PINCNTL register that selects this multiplexed signal option.
7. **TYPE:** Signal direction
   - I = Input
   - O = Output
   - I/O = Input/Output
   - D = Open drain
   - DS = Differential
   - A = Analog
   - PWR = Power
   - GND = Ground
8. **DSIS:** The deselected input state (DSIS) indicates the state driven on the peripheral input (logic "0", logic "1", or "PIN" level) when the peripheral pin function is not selected by any of the PINCNTLx registers.
   - 0: Logic 0 driven on the peripheral's input signal port.
   - 1: Logic 1 driven on the peripheral's input signal port.
   - PIN: The value on the pin is driven to the peripheral's input signal port.
9. **BALL RESET STATE:** The state of the ball during device reset.
   - 0: The buffer drives V_{OL} (pulldown/pullup resistor not activated)
     0(PD): The buffer drives V_{OL} with an active pulldown resistor
   - 1: The buffer drives V_{OH} (pulldown/pullup resistor not activated)
     1(PU): The buffer drives V_{OH} with an active pullup resistor
   - Z: High-impedance.
   - L: High-impedance with an active pulldown resistor
   - H : High-impedance with an active pullup resistor
10. **BALL RESET REL. STATE:** The state of the ball following the device coming out of reset.
    - 0: The buffer drives V_{OL} (pulldown/pullup resistor not activated)
      0(PD): The buffer drives V_{OL} with an active pulldown resistor
    - 1: The buffer drives V_{OH} (pulldown/pullup resistor not activated)
      1(PU): The buffer drives V_{OH} with an active pullup resistor
    - Z: High-impedance.
    - L: High-impedance with an active pulldown resistor
    - H : High-impedance with an active pullup resistor
11. **POWER:** The voltage supply that powers the terminal's I/O buffers.
12. **HYS:** Indicates if the input buffer is with hysteresis.
13. **BUFFER TYPE:** Drive strength of the associated output buffer.

Table 3-11. Ball Characteristics (AAR Package)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	PINCNTL REGISTER NAME AND ADDRESS[4]	PINCNTL DEFAULT VALUE[5]	MODE [6]	TYPE [7]	DSIS [8]	BALL RESET STATE [9]	BALL RESET REL. STATE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]
AF31	AUD_CLKIN0	AUD_CLKIN0	PINCNTL14 / 0x4814 0834	0x000C 0000	0x01	I	PIN	L	L	DVDD		
		MCA[0]_AHCLKX			0x04	I/O	PIN					
		USB1_DRVVBUS			0x80	O	PIN					
AF27	AUD_CLKIN1	AUD_CLKIN1	PINCNTL15 / 0x4814 0838	0x000C 0000	0x01	I	PIN	L	L	DVDD		
		MCA[1]_AHCLKX			0x04	I/O	PIN					
		EDMA_EVT3			0x20	I	PIN					
		TIM2_IO			0x40	I/O	PIN					
		GP0[8]			0x80	I/O	PIN					
AG30	AUD_CLKIN2	AUD_CLKIN2	PINCNTL16 / 0x4814 083C	0x000C 0000	0x01	I	PIN	L	L	DVDD		
		EDMA_EVT2			0x20	I	PIN					
		TIM3_IO			0x40	I/O	PIN					
		GP0[9]			0x80	I/O	PIN					
V30	AUXOSC_MXI	AUXOSC_MXI	NA / NA	NA	0x01	I	NA	NA	NA	VDDS_OSC1_1P8		
U31	AUXOSC_MXO	AUXOSC_MXO	NA / NA	NA	0x01	O	NA	NA	NA	VDDS_OSC1_1P8		
AJ31	CLKIN32	CLKIN32	PINCNTL259 / 0x4814 0C08	0x0004 0000	0x01	I	PIN	L	L	DVDD		
		CLKOUT0			0x04	O	PIN					
		TIM3_IO			0x40	I/O	PIN					
		GP3[31]			0x80	I/O	PIN					
AB2	CSI2_DX[0]	CSI2_DX[0]	NA / NA	NA	0x01	I	NA	NA	NA	VDDA_CSI2_1P8		
AA1	CSI2_DX[1]	CSI2_DX[1]	NA / NA	NA	0x01	I	NA	NA	NA	VDDA_CSI2_1P8		
AA2	CSI2_DX[2]	CSI2_DX[2]	NA / NA	NA	0x01	I	NA	NA	NA	VDDA_CSI2_1P8		
W2	CSI2_DX[3]	CSI2_DX[3]	NA / NA	NA	0x01	I	NA	NA	NA	VDDA_CSI2_1P8		
V1	CSI2_DX[4]	CSI2_DX[4]	NA / NA	NA	0x01	I	NA	NA	NA	VDDA_CSI2_1P8		
AC2	CSI2_DY[0]	CSI2_DY[0]	NA / NA	NA	0x01	I	NA	NA	NA	VDDA_CSI2_1P8		
AB1	CSI2_DY[1]	CSI2_DY[1]	NA / NA	NA	0x01	I	NA	NA	NA	VDDA_CSI2_1P8		
Y2	CSI2_DY[2]	CSI2_DY[2]	NA / NA	NA	0x01	I	NA	NA	NA	VDDA_CSI2_1P8		
W1	CSI2_DY[3]	CSI2_DY[3]	NA / NA	NA	0x01	I	NA	NA	NA	VDDA_CSI2_1P8		
V2	CSI2_DY[4]	CSI2_DY[4]	NA / NA	NA	0x01	I	NA	NA	NA	VDDA_CSI2_1P8		

Table 3-11. Ball Characteristics (AAR Package) (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	PINCNTL REGISTER NAME AND ADDRESS[4]	PINCNTL DEFAULT VALUE[5]	MODE [6]	TYPE [7]	DSIS [8]	BALL RESET STATE [9]	BALL RESET REL. STATE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]
P15, P17, R15, R17, T13, T17, T18, U11, U12, U15, U17, V11, V12, V15, V17, W13, W14, W19, W20, Y13, Y14, Y19, Y20	CVDD	CVDD	NA / NA	NA	NA	PWR	NA	NA	NA	NA		
K17, L17, L18, M13, M14, M17	CVDD_ARM	CVDD_ARM	NA / NA	NA	NA	PWR	NA	NA	NA	NA		
U20, U21, V20, V21, W22	CVDD_HDVICP	CVDD_HDVICP	NA / NA	NA	NA	PWR	NA	NA	NA	NA		
AL24	DDR[0]_A[0]	DDR[0]_A[0]	NA / NA	NA	0x01	O	NA	H	1	DVDD_DDR[0]		
AC22	DDR[0]_A[1]	DDR[0]_A[1]	NA / NA	NA	0x01	O	NA	H	1	DVDD_DDR[0]		
AJ23	DDR[0]_A[2]	DDR[0]_A[2]	NA / NA	NA	0x01	O	NA	H	1	DVDD_DDR[0]		
AJ27	DDR[0]_A[3]	DDR[0]_A[3]	NA / NA	NA	0x01	O	NA	H	1	DVDD_DDR[0]		
AK28	DDR[0]_A[4]	DDR[0]_A[4]	NA / NA	NA	0x01	O	NA	H	1	DVDD_DDR[0]		
AH27	DDR[0]_A[5]	DDR[0]_A[5]	NA / NA	NA	0x01	O	NA	H	1	DVDD_DDR[0]		
AK30	DDR[0]_A[6]	DDR[0]_A[6]	NA / NA	NA	0x01	O	NA	H	1	DVDD_DDR[0]		
AG23	DDR[0]_A[7]	DDR[0]_A[7]	NA / NA	NA	0x01	O	NA	H	1	DVDD_DDR[0]		
AL29	DDR[0]_A[8]	DDR[0]_A[8]	NA / NA	NA	0x01	O	NA	H	1	DVDD_DDR[0]		
AK29	DDR[0]_A[9]	DDR[0]_A[9]	NA / NA	NA	0x01	O	NA	H	1	DVDD_DDR[0]		
AD23	DDR[0]_A[10]	DDR[0]_A[10]	NA / NA	NA	0x01	O	NA	H	1	DVDD_DDR[0]		
AK24	DDR[0]_A[11]	DDR[0]_A[11]	NA / NA	NA	0x01	O	NA	H	1	DVDD_DDR[0]		
AH23	DDR[0]_A[12]	DDR[0]_A[12]	NA / NA	NA	0x01	O	NA	H	1	DVDD_DDR[0]		
AK23	DDR[0]_A[13]	DDR[0]_A[13]	NA / NA	NA	0x01	O	NA	H	1	DVDD_DDR[0]		
AL23	DDR[0]_A[14]	DDR[0]_A[14]	NA / NA	NA	0x01	O	NA	H	1	DVDD_DDR[0]		
AK22	DDR[0]_A[15]	DDR[0]_A[15]	NA / NA	NA	0x01	O	NA	H	1	DVDD_DDR[0]		
AK26	DDR[0]_BA[0]	DDR[0]_BA[0]	NA / NA	NA	0x01	O	NA	H	1	DVDD_DDR[0]		
AF23	DDR[0]_BA[1]	DDR[0]_BA[1]	NA / NA	NA	0x01	O	NA	H	1	DVDD_DDR[0]		

Table 3-11. Ball Characteristics (AAR Package) (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	PINCNTL REGISTER NAME AND ADDRESS[4]	PINCNTL DEFAULT VALUE[5]	MODE [6]	TYPE [7]	DSIS [8]	BALL RESET STATE [9]	BALL RESET REL. STATE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]
AH25	DDR[0]_BA[2]	DDR[0]_BA[2]	NA / NA	NA	0x01	O	NA	H	1	DVDD_DDR[0]		
AK25	$\overline{\text{DDR[0]\_CAS}}$	$\overline{\text{DDR[0]\_CAS}}$	NA / NA	NA	0x01	O	NA	H	1	DVDD_DDR[0]		
AD20	DDR[0]_CKE	DDR[0]_CKE	NA / NA	NA	0x01	O	NA	L	L	DVDD_DDR[0]		
AL27	DDR[0]_CLK	DDR[0]_CLK	NA / NA	NA	0x01	O	NA	L	0	DVDD_DDR[0]		
AK27	$\overline{\text{DDR[0]\_CLK}}$	$\overline{\text{DDR[0]\_CLK}}$	NA / NA	NA	0x01	O	NA	H	1	DVDD_DDR[0]		
AB21	$\overline{\text{DDR[0]\_CS[0]}}$	$\overline{\text{DDR[0]\_CS[0]}}$	NA / NA	NA	0x01	O	NA	H	1	DVDD_DDR[0]		
AL9	DDR[0]_D[0]	DDR[0]_D[0]	NA / NA	NA	0x01	I/O	NA	L	L	DVDD_DDR[0]		
AK9	DDR[0]_D[1]	DDR[0]_D[1]	NA / NA	NA	0x01	I/O	NA	L	L	DVDD_DDR[0]		
AK10	DDR[0]_D[2]	DDR[0]_D[2]	NA / NA	NA	0x01	I/O	NA	L	L	DVDD_DDR[0]		
AJ11	DDR[0]_D[3]	DDR[0]_D[3]	NA / NA	NA	0x01	I/O	NA	L	L	DVDD_DDR[0]		
AH11	DDR[0]_D[4]	DDR[0]_D[4]	NA / NA	NA	0x01	I/O	NA	L	L	DVDD_DDR[0]		
AD9	DDR[0]_D[5]	DDR[0]_D[5]	NA / NA	NA	0x01	I/O	NA	L	L	DVDD_DDR[0]		
AF11	DDR[0]_D[6]	DDR[0]_D[6]	NA / NA	NA	0x01	I/O	NA	L	L	DVDD_DDR[0]		
AL12	DDR[0]_D[7]	DDR[0]_D[7]	NA / NA	NA	0x01	I/O	NA	L	L	DVDD_DDR[0]		
AJ12	DDR[0]_D[8]	DDR[0]_D[8]	NA / NA	NA	0x01	I/O	NA	L	L	DVDD_DDR[0]		
AG12	DDR[0]_D[9]	DDR[0]_D[9]	NA / NA	NA	0x01	I/O	NA	L	L	DVDD_DDR[0]		
AD12	DDR[0]_D[10]	DDR[0]_D[10]	NA / NA	NA	0x01	I/O	NA	L	L	DVDD_DDR[0]		
AB12	DDR[0]_D[11]	DDR[0]_D[11]	NA / NA	NA	0x01	I/O	NA	L	L	DVDD_DDR[0]		
AK13	DDR[0]_D[12]	DDR[0]_D[12]	NA / NA	NA	0x01	I/O	NA	L	L	DVDD_DDR[0]		
AC13	DDR[0]_D[13]	DDR[0]_D[13]	NA / NA	NA	0x01	I/O	NA	L	L	DVDD_DDR[0]		
AL14	DDR[0]_D[14]	DDR[0]_D[14]	NA / NA	NA	0x01	I/O	NA	L	L	DVDD_DDR[0]		
AK14	DDR[0]_D[15]	DDR[0]_D[15]	NA / NA	NA	0x01	I/O	NA	L	L	DVDD_DDR[0]		
AH15	DDR[0]_D[16]	DDR[0]_D[16]	NA / NA	NA	0x01	I/O	NA	L	L	DVDD_DDR[0]		

Table 3-11. Ball Characteristics (AAR Package) (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	PINCNTL REGISTER NAME AND ADDRESS[4]	PINCNTL DEFAULT VALUE[5]	MODE [6]	TYPE [7]	DSIS [8]	BALL RESET STATE [9]	BALL RESET REL. STATE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]
AF15	DDR[0]_D[17]	DDR[0]_D[17]	NA / NA	NA	0x01	I/O	NA	L	L	DVDD_DDR[0]		
AD15	DDR[0]_D[18]	DDR[0]_D[18]	NA / NA	NA	0x01	I/O	NA	L	L	DVDD_DDR[0]		
AK16	DDR[0]_D[19]	DDR[0]_D[19]	NA / NA	NA	0x01	I/O	NA	L	L	DVDD_DDR[0]		
AJ16	DDR[0]_D[20]	DDR[0]_D[20]	NA / NA	NA	0x01	I/O	NA	L	L	DVDD_DDR[0]		
AG16	DDR[0]_D[21]	DDR[0]_D[21]	NA / NA	NA	0x01	I/O	NA	L	L	DVDD_DDR[0]		
AD16	DDR[0]_D[22]	DDR[0]_D[22]	NA / NA	NA	0x01	I/O	NA	L	L	DVDD_DDR[0]		
AC16	DDR[0]_D[23]	DDR[0]_D[23]	NA / NA	NA	0x01	I/O	NA	L	L	DVDD_DDR[0]		
AK19	DDR[0]_D[24]	DDR[0]_D[24]	NA / NA	NA	0x01	I/O	NA	L	L	DVDD_DDR[0]		
AJ19	DDR[0]_D[25]	DDR[0]_D[25]	NA / NA	NA	0x01	I/O	NA	L	L	DVDD_DDR[0]		
AH19	DDR[0]_D[26]	DDR[0]_D[26]	NA / NA	NA	0x01	I/O	NA	L	L	DVDD_DDR[0]		
AF19	DDR[0]_D[27]	DDR[0]_D[27]	NA / NA	NA	0x01	I/O	NA	L	L	DVDD_DDR[0]		
AD19	DDR[0]_D[28]	DDR[0]_D[28]	NA / NA	NA	0x01	I/O	NA	L	L	DVDD_DDR[0]		
AC19	DDR[0]_D[29]	DDR[0]_D[29]	NA / NA	NA	0x01	I/O	NA	L	L	DVDD_DDR[0]		
AJ20	DDR[0]_D[30]	DDR[0]_D[30]	NA / NA	NA	0x01	I/O	NA	L	L	DVDD_DDR[0]		
AG20	DDR[0]_D[31]	DDR[0]_D[31]	NA / NA	NA	0x01	I/O	NA	L	L	DVDD_DDR[0]		
AL8	DDR[0]_DQM[0]	DDR[0]_DQM[0]	NA / NA	NA	0x01	O	NA	H	1	DVDD_DDR[0]		
AK12	DDR[0]_DQM[1]	DDR[0]_DQM[1]	NA / NA	NA	0x01	O	NA	H	1	DVDD_DDR[0]		
AJ15	DDR[0]_DQM[2]	DDR[0]_DQM[2]	NA / NA	NA	0x01	O	NA	H	1	DVDD_DDR[0]		
AK18	DDR[0]_DQM[3]	DDR[0]_DQM[3]	NA / NA	NA	0x01	O	NA	H	1	DVDD_DDR[0]		
AL11	DDR[0]_DQS[0]	DDR[0]_DQS[0]	NA / NA	NA	0x01	I/O	NA	L	0	DVDD_DDR[0]		
AK11	$\overline{\text{DDR[0]\_DQS[0]}}$	$\overline{\text{DDR[0]\_DQS[0]}}$	NA / NA	NA	0x01	I/O	NA	H	1	DVDD_DDR[0]		
AK15	$\overline{\text{DDR[0]\_DQS[1]}}$	$\overline{\text{DDR[0]\_DQS[1]}}$	NA / NA	NA	0x01	I/O	NA	H	1	DVDD_DDR[0]		
AL15	DDR[0]_DQS[1]	DDR[0]_DQS[1]	NA / NA	NA	0x01	I/O	NA	L	0	DVDD_DDR[0]		

Table 3-11. Ball Characteristics (AAR Package) (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	PINCNTL REGISTER NAME AND ADDRESS[4]	PINCNTL DEFAULT VALUE[5]	MODE [6]	TYPE [7]	DSIS [8]	BALL RESET STATE [9]	BALL RESET REL. STATE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]
AL17	DDR[0]_DQS[2]	DDR[0]_DQS[2]	NA / NA	NA	0x01	I/O	NA	L	0	DVDD_DDR[0]		
AK17	$\overline{\text{DDR[0]\_DQS[2]}}$	$\overline{\text{DDR[0]\_DQS[2]}}$	NA / NA	NA	0x01	I/O	NA	H	1	DVDD_DDR[0]		
AK20	$\overline{\text{DDR[0]\_DQS[3]}}$	$\overline{\text{DDR[0]\_DQS[3]}}$	NA / NA	NA	0x01	I/O	NA	H	1	DVDD_DDR[0]		
AL20	DDR[0]_DQS[3]	DDR[0]_DQS[3]	NA / NA	NA	0x01	I/O	NA	L	0	DVDD_DDR[0]		
AL21	DDR[0]_ODT[0]	DDR[0]_ODT[0]	NA / NA	NA	0x01	O	NA	L	0	DVDD_DDR[0]		
AJ25	$\overline{\text{DDR[0]\_RAS}}$	$\overline{\text{DDR[0]\_RAS}}$	NA / NA	NA	0x01	O	NA	H	1	DVDD_DDR[0]		
AA20	DDR[0]_RST	DDR[0]_RST	NA / NA	NA	0x01	O	NA	L	0	DVDD_DDR[0]		
AL30	DDR[0]_VTP	DDR[0]_VTP	NA / NA	NA	0x01	I	NA	NA	NA	DVDD_DDR[0]		
AL26	$\overline{\text{DDR[0]\_WE}}$	$\overline{\text{DDR[0]\_WE}}$	NA / NA	NA	0x01	O	NA	H	1	DVDD_DDR[0]		
F30	DEVOSC_MXI	DEV_CLKIN	NA / NA	NA	0x01	I	NA	NA	NA	VDDS_OSC0_1P8		
		DEVOSC_MXI			0x01	I	NA					
G31	DEVOSC_MXO	DEVOSC_MXO	NA / NA	NA	0x01	O	NA	NA	NA	VDDS_OSC0_1P8		
U28	DEVOSC_WAKE	DEVOSC_WAKE	PINCNTL7 / 0x4814 0818	0x000E 0000	0x01	I	1	H	H	DVDD_SD		
		$\overline{\text{SPI[1]\_SCS[1]}}$			0x02	I/O	1					
		TIM5_IO			0x40	I/O	PIN					
		GP1[7]			0x80	I/O	PIN					
D16, E17, F16, L5, M4, M6, M7, N10, N11, T26, T28, U27	DVDD	DVDD	NA / NA	NA	NA	PWR	NA	NA	NA	NA		
D12, E13, F12, G12, G13	DVDD_C	DVDD_C	NA / NA	NA	NA	PWR	NA	NA	NA	NA		
AB14, AB15, AB17, AB18, AC15, AC17, AC18, AE15, AE16, AF16, AG15, AH16	DVDD_DDR[0]	DVDD_DDR[0]	NA / NA	NA	NA	PWR	NA	NA	NA	NA		
R5, R7, T4, T6, T7	DVDD_GPMC	DVDD_GPMC	NA / NA	NA	NA	PWR	NA	NA	NA	NA		
W5, W7, Y4, Y6, Y7	DVDD_RGMII	DVDD_RGMII	NA / NA	NA	NA	PWR	NA	NA	NA	NA		
T25, U25	DVDD_SD	DVDD_SD	NA / NA	NA	NA	PWR	NA	NA	NA	NA		
A18	EMU0	EMU0	NA / NA	NA	0x01	I/O	NA	H	H	DVDD		
B19	EMU1	EMU1	NA / NA	NA	0x01	I/O	NA	H	H	DVDD		

Table 3-11. Ball Characteristics (AAR Package) (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	PINCNTL REGISTER NAME AND ADDRESS[4]	PINCNTL DEFAULT VALUE[5]	MODE [6]	TYPE [7]	DSIS [8]	BALL RESET STATE [9]	BALL RESET REL. STATE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]
AG2	GP1[11]	GP1[11]	PINCNTL233 / 0x4814 0BA0	0x000E 0000	0x80	I/O	PIN	H	H	DVDD_RGMII		
AG3	GP1[12]	GP1[12]	PINCNTL234 / 0x4814 0BA4	0x000E 0000	0x80	I/O	PIN	H	H	DVDD_RGMII		
AK4	GPMC_A[1]	GPMC_A[1]	PINCNTL244 / 0x4814 0BCC	0x0004 0000	0x10	O	PIN	L	L	DVDD_RGMII		
AJ4	GPMC_A[2]	GPMC_A[2]	PINCNTL245 / 0x4814 0BD0	0x0004 0000	0x10	O	PIN	L	L	DVDD_RGMII		
AL5	GPMC_A[3]	GPMC_A[3]	PINCNTL246 / 0x4814 0BD4	0x0004 0000	0x10	O	PIN	L	L	DVDD_RGMII		
AK5	GPMC_A[4]	GPMC_A[4]	PINCNTL247 / 0x4814 0BD8	0x0004 0000	0x10	O	PIN	L	L	DVDD_RGMII		
		SPI[2]_SCS[3]			0x20	I/O	1					
AJ6	GPMC_A[5]	GPMC_A[5]	PINCNTL248 / 0x4814 0BDC	0x0004 0000	0x10	O	PIN	L	L	DVDD_RGMII		
		SPI[2]_SCLK			0x20	I/O	1					
AL6	GPMC_A[6]	GPMC_A[6]	PINCNTL249 / 0x4814 0BE0	0x0004 0000	0x10	O	PIN	L	L	DVDD_RGMII		
		SPI[2]_D[1]			0x20	I/O	PIN					
AK6	GPMC_A[7]	GPMC_A[7]	PINCNTL250 / 0x4814 0BE4	0x0004 0000	0x10	O	PIN	L	L	DVDD_RGMII		
		SPI[2]_D[0]			0x20	I/O	PIN					
AJ7	GPMC_A[8]	GPMC_A[8]	PINCNTL251 / 0x4814 0BE8	0x0004 0000	0x10	O	PIN	L	L	DVDD_RGMII		
AK7	GPMC_A[9]	GPMC_A[9]	PINCNTL252 / 0x4814 0BEC	0x0004 0000	0x10	O	PIN	L	L	DVDD_RGMII		
AE4	GPMC_A[10]	GPMC_A[10]	PINCNTL253 / 0x4814 0BF0	0x0004 0000	0x10	O	PIN	L	L	DVDD_RGMII		
AK8	GPMC_A[11]	GPMC_A[11]	PINCNTL254 / 0x4814 0BF4	0x0004 0000	0x10	O	PIN	L	L	DVDD_RGMII		
AJ8	GPMC_A[12]	GPMC_A[12]	PINCNTL255 / 0x4814 0BF8	0x0004 0000	0x10	O	PIN	L	L	DVDD_RGMII		
		UART1_RXD			0x20	I	1					
AH8	GPMC_A[13]	GPMC_A[13]	PINCNTL256 / 0x4814 0BFC	0x0004 0000	0x10	O	PIN	L	L	DVDD_RGMII		
		UART1_TXD			0x20	O	PIN					
AG8	GPMC_A[14]	GPMC_A[14]	PINCNTL257 / 0x4814 0C00	0x0004 0000	0x10	O	PIN	L	L	DVDD_RGMII		
		UART1_CTS			0x20	I/O	1					
AF8	GPMC_A[15]	GPMC_A[15]	PINCNTL258 / 0x4814 0C04	0x0004 0000	0x10	O	PIN	L	L	DVDD_RGMII		
		UART1_RTS			0x20	O	PIN					
M1	GPMC_A[16]	GPMC_A[16]	PINCNTL105 / 0x4814 09A0	0x0004 0000	0x01	O	PIN	L	L	DVDD_GPMC		
		GP2[5]			0x80	I/O	PIN					
M2	GPMC_A[17]	GPMC_A[17]	PINCNTL106 / 0x4814 09A4	0x0004 0000	0x01	O	PIN	L	L	DVDD_GPMC		
		GP2[6]			0x80	I/O	PIN					
M3	GPMC_A[18]	GPMC_A[18]	PINCNTL107 / 0x4814 09A8	0x0004 0000	0x01	O	PIN	L	L	DVDD_GPMC		
		TIM2_IO			0x40	I/O	PIN					
		GP1[13]			0x80	I/O	PIN					

Table 3-11. Ball Characteristics (AAR Package) (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	PINCNTL REGISTER NAME AND ADDRESS[4]	PINCNTL DEFAULT VALUE[5]	MODE [6]	TYPE [7]	DSIS [8]	BALL RESET STATE [9]	BALL RESET REL. STATE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]
M5	GPMC_A[19]	GPMC_A[19]	PINCNTL108 / 0x4814 09AC	0x0004 0000	0x01	O	PIN	L	L	DVDD_GPMC		
		TIM3_IO			0x40	I/O	PIN					
		GP1[14]			0x80	I/O	PIN					
N9	GPMC_A[20]	GPMC_A[20]	PINCNTL109 / 0x4814 09B0	0x0006 0000	0x01	O	PIN	H	H	DVDD_GPMC		
		$\overline{\text{SPI[2]\_SCS[1]}}$			0x04	I/O	1					
		GP1[15]			0x80	I/O	PIN					
N1	GPMC_A[21]	GPMC_A[21]	PINCNTL110 / 0x4814 09B4	0x0004 0000	0x01	O	PIN	L	L	DVDD_GPMC		
		SPI[2]_D[0]			0x04	I/O	PIN					
		GP1[16]			0x80	I/O	PIN					
N2	GPMC_A[22]	GPMC_A[22]	PINCNTL111 / 0x4814 09B8	0x0006 0000	0x01	O	PIN	H	H	DVDD_GPMC		
		SPI[2]_D[1]			0x04	I/O	PIN					
		HDMI_CEC			0x10	I/O	1					
		TIM4_IO			0x40	I/O	PIN					
		GP1[17]			0x80	I/O	PIN					
R8	GPMC_A[23]	GPMC_A[23]	PINCNTL112 / 0x4814 09BC	0x0004 0000	0x01	O	PIN	L	L	DVDD_GPMC		
		SPI[2]_SCLK			0x04	I/O	1					
		HDMI_HPDET			0x10	I	0					
		TIM5_IO			0x40	I/O	PIN					
		GP1[18]			0x80	I/O	PIN					
AK3	GPMC_A[27]	GPMC_A[27]	PINCNTL243 / 0x4814 0BC8	0x0004 0000	0x04	O	PIN	L	L	DVDD_RGMII		
		GPMC_A[26]			0x08	O	PIN					
		GPMC_A[0]			0x10	O	PIN					
AA10	GPMC_$\overline{\text{ADV}}$_ALE	GPMC_$\overline{\text{ADV}}$_ALE	PINCNTL128 / 0x4814 09FC	0x0006 0000	0x01	O	PIN	H	H	DVDD_GPMC		
		$\overline{\text{GPMC\_CS[6]}}$			0x02	O	PIN					
		TIM5_IO			0x40	I/O	PIN					
		GP1[28]			0x80	I/O	PIN					
Y11	$\overline{\text{GPMC\_BE[1]}}$	$\overline{\text{GPMC\_BE[1]}}$	PINCNTL132 / 0x4814 0A0C	0x0004 0000	0x01	O	PIN	L	L	DVDD_GPMC		
		GPMC_A[24]			0x02	O	PIN					
		EDMA_EVT1			0x20	I	PIN					
		TIM7_IO			0x40	I/O	PIN					
		GP1[30]			0x80	I/O	PIN					
Y3	GPMC_$\overline{\text{BE[0]}}$_CLE	GPMC_$\overline{\text{BE[0]}}$_CLE	PINCNTL131 / 0x4814 0A08	0x0004 0000	0x01	O	PIN	L	L	DVDD_GPMC		
		GPMC_A[25]			0x02	O	PIN					
		EDMA_EVT2			0x20	I	PIN					
		TIM6_IO			0x40	I/O	PIN					
		GP1[29]			0x80	I/O	PIN					

Table 3-11. Ball Characteristics (AAR Package) (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	PINCNTL REGISTER NAME AND ADDRESS[4]	PINCNTL DEFAULT VALUE[5]	MODE [6]	TYPE [7]	DSIS [8]	BALL RESET STATE [9]	BALL RESET REL. STATE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]
AB9	GPMC_CLK	GPMC_CLK	PINCNTL127 / 0x4814 09F8	0x0006 0000	0x01	O	0	H	H	DVDD_GPMC		
		GPMC_CS[5]			0x02	O	PIN					
		GPMC_WAIT[1]			0x08	I	1					
		CLKOUT1			0x10	O	PIN					
		EDMA_EVT3			0x20	I	PIN					
		TIM4_IO			0x40	I/O	PIN					
		GP1[27]			0x80	I/O	PIN					
AC9	GPMC_CS[0]	GPMC_CS[0]	PINCNTL122 / 0x4814 09E4	0x0006 0000	0x01	O	PIN	H	H	DVDD_GPMC		
		GP1[23]			0x80	I/O	PIN					
AA12	GPMC_CS[1]	GPMC_CS[1]	PINCNTL123 / 0x4814 09E8	0x0006 0000	0x01	O	PIN	H	H	DVDD_GPMC		
		GPMC_A[25]			0x02	O	PIN					
		GP1[24]			0x80	I/O	PIN					
AC3	GPMC_CS[2]	GPMC_CS[2]	PINCNTL124 / 0x4814 09EC	0x0006 0000	0x01	O	PIN	H	H	DVDD_RGMII		
		GPMC_A[24]			0x02	O	PIN					
		GP1[25]			0x80	I/O	PIN					
AF2	GPMC_CS[3]	GPMC_CS[3]	PINCNTL125 / 0x4814 09F0	0x0006 0000	0x01	O	PIN	H	H	DVDD_RGMII		
		VIN[1]B_CLK			0x02	I	0					
		SPI[2]_SCS[0]			0x04	I/O	1					
		GP1[26]			0x80	I/O	PIN					
AG6	GPMC_CS[4]	GPMC_CS[4]	PINCNTL126 / 0x4814 09F4	0x0006 0000	0x01	O	PIN	H	H	DVDD_RGMII		
		SD2_CMD			0x02	O	1					
		GP1[8]			0x80	I/O	PIN					
W6	GPMC_D[0]	GPMC_D[0]	PINCNTL89 / 0x4814 0960	0x0005 0000	0x01	I/O	PIN	Z	Z	DVDD_GPMC		
		BTMODE[0]			0x80	I	PIN					
W4	GPMC_D[1]	GPMC_D[1]	PINCNTL90 / 0x4814 0964	0x0005 0000	0x01	I/O	PIN	Z	Z	DVDD_GPMC		
		BTMODE[1]			0x80	I	PIN					
W3	GPMC_D[2]	GPMC_D[2]	PINCNTL91 / 0x4814 0968	0x0005 0000	0x01	I/O	PIN	Z	Z	DVDD_GPMC		
		BTMODE[2]			0x80	I	PIN					
U2	GPMC_D[3]	GPMC_D[3]	PINCNTL92 / 0x4814 096C	0x0005 0000	0x01	I/O	PIN	Z	Z	DVDD_GPMC		
		BTMODE[3]			0x80	I	PIN					
W9	GPMC_D[4]	GPMC_D[4]	PINCNTL93 / 0x4814 0970	0x0005 0000	0x01	I/O	PIN	Z	Z	DVDD_GPMC		
		BTMODE[4]			0x80	I	PIN					
T5	GPMC_D[5]	GPMC_D[5]	PINCNTL94 / 0x4814 0974	0x0005 0000	0x01	I/O	PIN	Z	Z	DVDD_GPMC		
		BTMODE[5]			0x80	I	PIN					
T3	GPMC_D[6]	GPMC_D[6]	PINCNTL95 / 0x4814 0978	0x0005 0000	0x01	I/O	PIN	Z	Z	DVDD_GPMC		
		BTMODE[6]			0x80	I	PIN					
T2	GPMC_D[7]	GPMC_D[7]	PINCNTL96 / 0x4814 097C	0x0005 0000	0x01	I/O	PIN	Z	Z	DVDD_GPMC		
		BTMODE[7]			0x80	I	PIN					

Table 3-11. Ball Characteristics (AAR Package) (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	PINCNTL REGISTER NAME AND ADDRESS[4]	PINCNTL DEFAULT VALUE[5]	MODE [6]	TYPE [7]	DSIS [8]	BALL RESET STATE [9]	BALL RESET REL. STATE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]
T1	GPMC_D[8]	GPMC_D[8]	PINCNTL97 / 0x4814 0980	0x0005 0000	0x01	I/O	PIN	Z	Z	DVDD_GPMC		
		BTMODE[8]			0x80	I	PIN					
T8	GPMC_D[9]	GPMC_D[9]	PINCNTL98 / 0x4814 0984	0x0005 0000	0x01	I/O	PIN	Z	Z	DVDD_GPMC		
		BTMODE[9]			0x80	I	PIN					
R6	GPMC_D[10]	GPMC_D[10]	PINCNTL99 / 0x4814 0988	0x0005 0000	0x01	I/O	PIN	Z	Z	DVDD_GPMC		
		BTMODE[10]			0x80	I	PIN					
R4	GPMC_D[11]	GPMC_D[11]	PINCNTL100 / 0x4814 098C	0x0005 0000	0x01	I/O	PIN	Z	Z	DVDD_GPMC		
		BTMODE[11]			0x80	I	PIN					
R3	GPMC_D[12]	GPMC_D[12]	PINCNTL101 / 0x4814 0990	0x0005 0000	0x01	I/O	PIN	Z	Z	DVDD_GPMC		
		BTMODE[12]			0x80	I	PIN					
R2	GPMC_D[13]	GPMC_D[13]	PINCNTL102 / 0x4814 0994	0x0005 0000	0x01	I/O	PIN	Z	Z	DVDD_GPMC		
		BTMODE[13]			0x80	I	PIN					
R1	GPMC_D[14]	GPMC_D[14]	PINCNTL103 / 0x4814 0998	0x0005 0000	0x01	I/O	PIN	Z	Z	DVDD_GPMC		
		BTMODE[14]			0x80	I	PIN					
P2	GPMC_D[15]	GPMC_D[15]	PINCNTL104 / 0x4814 099C	0x0005 0000	0x01	I/O	PIN	Z	Z	DVDD_GPMC		
		BTMODE[15]			0x80	I	PIN					
Y8	$\overline{\text{GPMC\_OE\_RE}}$	$\overline{\text{GPMC\_OE\_RE}}$	PINCNTL129 / 0x4814 0A00	0x0006 0000	0x01	O	PIN	H	H	DVDD_GPMC		
W8	GPMC_WAIT[0]	GPMC_WAIT[0]	PINCNTL133 / 0x4814 0A10	0x0006 0000	0x01	I	1	H	H	DVDD_GPMC		
		GPMC_A[26]			0x02	O	PIN					
		EDMA_EVT0			0x20	I	PIN					
		GP1[31]			0x80	I/O	PIN					
Y5	$\overline{\text{GPMC\_WE}}$	$\overline{\text{GPMC\_WE}}$	PINCNTL130 / 0x4814 0A04	0x0006 0000	0x01	O	PIN	H	H	DVDD_GPMC		
A9	HDDAC_A	HDDAC_A	NA / NA	NA	0x01	O	NA	NA	NA	VDDA_VDAC_1P8		
A8	HDDAC_B	HDDAC_B	NA / NA	NA	0x01	O	NA	NA	NA	VDDA_VDAC_1P8		
B8	HDDAC_C	HDDAC_C	NA / NA	NA	0x01	O	NA	NA	NA	VDDA_VDAC_1P8		
E9	HDDAC_HSYNC	HDDAC_HSYNC	NA / NA	NA	0x01	O	NA	L	L	DVDD		
B6	HDDAC_IREF	HDDAC_IREF	NA / NA	NA	0x01	I/O	NA	NA	NA	VDDA_VDAC_1P8		
B7	HDDAC_VREF	HDDAC_VREF	NA / NA	NA	0x01	I	NA	NA	NA	VDDA_VDAC_1P8		
D9	HDDAC_VSYNC	HDDAC_VSYNC	NA / NA	NA	0x01	O	NA	L	L	DVDD		
B15	HDMI_CLKN	HDMI_CLKN	NA / NA	NA	0x01	O	NA	NA	NA	VDDA_HDMI_1P8		
A15	HDMI_CLKP	HDMI_CLKP	NA / NA	NA	0x01	O	NA	NA	NA	VDDA_HDMI_1P8		

Table 3-11. Ball Characteristics (AAR Package) (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	PINCNTL REGISTER NAME AND ADDRESS[4]	PINCNTL DEFAULT VALUE[5]	MODE [6]	TYPE [7]	DSIS [8]	BALL RESET STATE [9]	BALL RESET REL. STATE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]
A14	HDMI_DN0	HDMI_DN0	NA / NA	NA	0x01	O	NA	NA	NA	VDDA_HDMI_1P8		
B13	HDMI_DN1	HDMI_DN1	NA / NA	NA	0x01	O	NA	NA	NA	VDDA_HDMI_1P8		
A12	HDMI_DN2	HDMI_DN2	NA / NA	NA	0x01	O	NA	NA	NA	VDDA_HDMI_1P8		
B14	HDMI_DP0	HDMI_DP0	NA / NA	NA	0x01	O	NA	NA	NA	VDDA_HDMI_1P8		
B12	HDMI_DP1	HDMI_DP1	NA / NA	NA	0x01	O	NA	NA	NA	VDDA_HDMI_1P8		
A11	HDMI_DP2	HDMI_DP2	NA / NA	NA	0x01	O	NA	NA	NA	VDDA_HDMI_1P8		
T27	I2C[0]_SCL	I2C[0]_SCL	PINCNTL263 / 0x4814 0C18	0x000C 0000	0x01	I/O	PIN	H	H	DVDD		
T24	I2C[0]_SDA	I2C[0]_SDA	PINCNTL264 / 0x4814 0C1C	0x000C 0000	0x01	I/O	PIN	H	H	DVDD		
D2	I2C[1]_SCL	I2C[1]_SCL	PINCNTL78 / 0x4814 0934	0x000E 0000	0x01	I/O	1	H	H	DVDD		
		HDMI_SCL			0x02	I/O	1					
D1	I2C[1]_SDA	I2C[1]_SDA	PINCNTL79 / 0x4814 0938	0x000E 0000	0x01	I/O	1	H	H	DVDD		
		HDMI_SDA			0x02	I/O	1					
J19	LDOCAP_ARM	LDOCAP_ARM	NA / NA	NA	NA	A	NA	NA	NA	NA		
K20	LDOCAP_ARMRAM	LDOCAP_ARMRAM	NA / NA	NA	NA	A	NA	NA	NA	NA		
W23	LDOCAP_HDVICP	LDOCAP_HDVICP	NA / NA	NA	NA	A	NA	NA	NA	NA		
Y24	LDOCAP_HDVICPRAM	LDOCAP_HDVICPRAM	NA / NA	NA	NA	A	NA	NA	NA	NA		
U9	LDOCAP_RAM0	LDOCAP_RAM0	NA / NA	NA	NA	A	NA	NA	NA	NA		
T22	LDOCAP_RAM1	LDOCAP_RAM1	NA / NA	NA	NA	A	NA	NA	NA	NA		
AB10	LDOCAP_RAM2	LDOCAP_RAM2	NA / NA	NA	NA	A	NA	NA	NA	NA		
M24	LDOCAP_SERDESCLK	LDOCAP_SERDESCLK	NA / NA	NA	NA	A	NA	NA	NA	NA		
AD30	MCA[0]_ACLKR	MCA[0]_ACLKR	PINCNTL19 / 0x4814 0848	0x0004 0000	0x01	I/O	0	L	L	DVDD		
AD28	MCA[0]_ACLKX	MCA[0]_ACLKX	PINCNTL17 / 0x4814 0840	0x0004 0000	0x01	I/O	PIN	L	L	DVDD		
AF30	MCA[0]_AFSR	MCA[0]_AFSR	PINCNTL20 / 0x4814 084C	0x000C 0000	0x01	I/O	0	L	L	DVDD		
AE29	MCA[0]_AFSX	MCA[0]_AFSX	PINCNTL18 / 0x4814 0844	0x000C 0000	0x01	I/O	PIN	L	L	DVDD		
AF29	MCA[0]_AXR[0]	MCA[0]_AXR[0]	PINCNTL21 / 0x4814 0850	0x000C 0000	0x01	I/O	PIN	L	L	DVDD		

Table 3-11. Ball Characteristics (AAR Package) (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	PINCNTL REGISTER NAME AND ADDRESS[4]	PINCNTL DEFAULT VALUE[5]	MODE [6]	TYPE [7]	DSIS [8]	BALL RESET STATE [9]	BALL RESET REL. STATE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]
AE31	MCA[0]_AXR[1]	MCA[0]_AXR[1]	PINCNTL22 / 0x4814 0854	0x000E 0000	0x01	I/O	PIN	H	H	DVDD		
		I2C[3]_SCL			0x20	I/O	1					
AE30	MCA[0]_AXR[2]	MCA[0]_AXR[2]	PINCNTL23 / 0x4814 0858	0x000E 0000	0x01	I/O	PIN	H	H	DVDD		
		I2C[3]_SDA			0x20	I/O	1					
AC31	MCA[0]_AXR[3]	MCA[0]_AXR[3]	PINCNTL24 / 0x4814 085C	0x000C 0000	0x01	I/O	PIN	L	L	DVDD		
AD26	MCA[0]_AXR[4]	MCA[0]_AXR[4]	PINCNTL25 / 0x4814 0860	0x000C 0000	0x01	I/O	PIN	L	L	DVDD		
AD27	MCA[0]_AXR[5]	MCA[0]_AXR[5]	PINCNTL26 / 0x4814 0864	0x000C 0000	0x01	I/O	PIN	L	L	DVDD		
AD29	MCA[1]_ACLKR	MCA[1]_ACLKR	PINCNTL33 / 0x4814 0880	0x0004 0000	0x01	I/O	0	L	L	DVDD		
AC23	MCA[1]_ACLKX	MCA[1]_ACLKX	PINCNTL31 / 0x4814 0878	0x0004 0000	0x01	I/O	PIN	L	L	DVDD		
AC24	MCA[1]_AFSR	MCA[1]_AFSR	PINCNTL34 / 0x4814 0884	0x000C 0000	0x01	I/O	0	L	L	DVDD		
AB22	MCA[1]_AFSX	MCA[1]_AFSX	PINCNTL32 / 0x4814 087C	0x000C 0000	0x01	I/O	PIN	L	L	DVDD		
Y22	MCA[1]_AXR[0]	MCA[1]_AXR[0]	PINCNTL35 / 0x4814 0888	0x000E 0000	0x01	I/O	PIN	H	H	DVDD		
		SD0_DAT[4]			0x02	I/O	PIN					
Y21	MCA[1]_AXR[1]	MCA[1]_AXR[1]	PINCNTL36 / 0x4814 088C	0x000E 0000	0x01	I/O	PIN	H	H	DVDD		
		SD0_DAT[5]			0x02	I/O	PIN					
AH31	$\overline{\text{NMI}}$	$\overline{\text{NMI}}$	PINCNTL261 / 0x4814 0C10	0x000E 0000	0x01	I	PIN	H	H	DVDD		
AH30	$\overline{\text{POR}}$	$\overline{\text{POR}}$	NA / NA	NA	0x01	I	NA	NA	NA	DVDD		
AH29	$\overline{\text{RESET}}$	$\overline{\text{RESET}}$	PINCNTL260 / 0x4814 0C0C	0x000E 0000	0x01	I	PIN	H	H	DVDD		
AJ30	$\overline{\text{RSTOUT\_WD\_OUT}}$	$\overline{\text{RSTOUT\_WD\_OUT}}$	PINCNTL262 / 0x4814 0C14	0x0005 0001	0x01	O	PIN	L	Z	DVDD		
J25	RSV0	RSV0			NA	NA	NA	NA	NA	NA		
H27	RSV1	RSV1	NA / NA	NA	NA	NA	NA	NA	NA	NA		
H24	RSV2	RSV2	NA / NA	NA	NA	NA	NA	NA	NA	NA		
J30	RSV24	RSV24			NA	NA	NA	NA	NA	NA		
K30	RSV25	RSV25	NA / NA	NA	NA	NA	NA	NA	NA	NA		
K31	RSV26	RSV26	NA / NA	NA	NA	NA	NA	NA	NA	NA		
H28	RSV3	RSV3	NA / NA	NA	NA	NA	NA	NA	NA	NA		
P31	RSV31	RSV31	NA / NA	NA	NA	NA	NA	NA	NA	NA		

Table 3-11. Ball Characteristics (AAR Package) (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	PINCNTL REGISTER NAME AND ADDRESS[4]	PINCNTL DEFAULT VALUE[5]	MODE [6]	TYPE [7]	DSIS [8]	BALL RESET STATE [9]	BALL RESET REL. STATE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]
R30	RSV32	RSV32	NA / NA	NA	NA	NA	NA	NA	NA	NA		
T30	RSV33	RSV33	NA / NA	NA	NA	NA	NA	NA	NA	NA		
AH24	RSV34	RSV34	NA / NA	NA	NA	NA	NA	NA	NA	NA		
AJ24	RSV35	RSV35	NA / NA	NA	NA	NA	NA	NA	NA	NA		
L31	RSV36	RSV36	NA / NA	NA	NA	NA	NA	NA	NA	NA		
H25	RSV39	RSV39	NA / NA	NA	NA	NA	NA	NA	NA	NA		
G17	RSV4	RSV4	NA / NA	NA	NA	PWR	NA	NA	NA	NA		
H29	RSV40	RSV40	NA / NA	NA	NA	NA	NA	NA	NA	NA		
AD8	RSV41	RSV41			NA	NA	NA	NA	NA	NA		
AK21	RSV42	RSV42	NA / NA	NA	0x01	O	NA	L	0	NA		
P30	RSV43	RSV43	NA / NA	NA	NA	NA	NA	NA	NA	NA		
G16	RSV5	RSV5	NA / NA	NA	NA	PWR	NA	NA	NA	NA		
M26	RSV53	RSV53	NA / NA	NA	NA	PWR	NA	NA	NA	NA		
M28	RSV54	RSV54	NA / NA	NA	NA	PWR	NA	NA	NA	NA		
N29	RTCK	RTCK	NA / NA	NA	0x01	O	NA	H	Z	DVDD		
L30	SATA0_RXN0	SATA0_RXN0	NA / NA	NA	0x01	I	NA	NA	NA	VDDA_SATA0_1P8		
M30	SATA0_RXP0	SATA0_RXP0	NA / NA	NA	0x01	I	NA	NA	NA	VDDA_SATA0_1P8		
N30	SATA0_TXN0	SATA0_TXN0	NA / NA	NA	0x01	O	NA	NA	NA	VDDA_SATA0_1P8		
N31	SATA0_TXP0	SATA0_TXP0	NA / NA	NA	0x01	O	NA	NA	NA	VDDA_SATA0_1P8		
AB30	SD0_CLK	SD0_CLK	PINCNTL8 / 0x4814 081C	0x0006 0000	0x01	O	1	H	H	DVDD_SD		
		GP0[1]			0x80	I/O	PIN					
AA29	SD0_CMD	SD0_CMD	PINCNTL9 / 0x4814 0820	0x000E 0000	0x01	O	1	H	H	DVDD_SD		
		SD1_CMD			0x02	O	1					
		GP0[2]			0x80	I/O	PIN					

Table 3-11. Ball Characteristics (AAR Package) (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	PINCNTL REGISTER NAME AND ADDRESS[4]	PINCNTL DEFAULT VALUE[5]	MODE [6]	TYPE [7]	DSIS [8]	BALL RESET STATE [9]	BALL RESET REL. STATE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]
AA28	SD0_DAT[0]	SD0_DAT[0]	PINCNTL10 / 0x4814 0824	0x000E 0000	0x01	I/O	PIN	H	H	DVDD_SD		
		SD1_DAT[4]			0x02	I/O	PIN					
		GP0[3]			0x80	I/O	PIN					
Y30	SD0_DAT[3]	SD0_DAT[3]	PINCNTL13 / 0x4814 0830	0x000E 0000	0x01	I/O	PIN	H	H	DVDD_SD		
		SD1_DAT[7]			0x02	I/O	PIN					
		GP0[6]			0x80	I/O	PIN					
AB31	SD0_DAT[6]	SD0_DAT[6]	PINCNTL41 / 0x4814 08A0	0x000E 0000	0x02	I/O	PIN	H	H	DVDD_SD		
		GP0[12]			0x80	I/O	PIN					
AC30	SD0_DAT[7]	SD0_DAT[7]	PINCNTL42 / 0x4814 08A4	0x000E 0000	0x02	I/O	PIN	H	H	DVDD_SD		
		GP0[13]			0x80	I/O	PIN					
AA26	SD0_DAT[1]_SDIRQ	SD0_DAT[1]_SDIRQ	PINCNTL11 / 0x4814 0828	0x000E 0000	0x01	I/O	PIN	H	H	DVDD_SD		
		SD1_DAT[5]			0x02	I/O	PIN					
		GP0[4]			0x80	I/O	PIN					
Y31	SD0_DAT[2]_SDRW	SD0_DAT[2]_SDRW	PINCNTL12 / 0x4814 082C	0x000E 0000	0x01	I/O	PIN	H	H	DVDD_SD		
		SD1_DAT[6]			0x02	I/O	PIN					
		GP0[5]			0x80	I/O	PIN					
W30	SD1_CLK	SD1_CLK	PINCNTL1 / 0x4814 0800	0x0006 0000	0x01	O	PIN	H	H	DVDD_SD		
Y29	SD1_CMD	SD1_CMD	PINCNTL2 / 0x4814 0804	0x000E 0000	0x01	O	1	H	H	DVDD_SD		
		GP0[0]			0x80	I/O	PIN					
W31	SD1_DAT[0]	SD1_DAT[0]	PINCNTL3 / 0x4814 0808	0x000E 0000	0x01	I/O	PIN	H	H	DVDD_SD		
Y27	SD1_DAT[3]	SD1_DAT[3]	PINCNTL6 / 0x4814 0814	0x000E 0000	0x01	I/O	PIN	H	H	DVDD_SD		
AA30	SD1_DAT[1]_SDIRQ	SD1_DAT[1]_SDIRQ	PINCNTL4 / 0x4814 080C	0x000E 0000	0x01	I/O	PIN	H	H	DVDD_SD		
U29	SD1_DAT[2]_SDRW	SD1_DAT[2]_SDRW	PINCNTL5 / 0x4814 0810	0x000E 0000	0x01	I/O	PIN	H	H	DVDD_SD		
AC4	SD2_DAT[0]	SD2_DAT[0]	PINCNTL120 / 0x4814 09DC	0x0006 0000	0x01	O	PIN	H	H	DVDD_RGMII		
		GPMC_A[4]			0x02	O	PIN					
		GP1[14]			0x80	I/O	PIN					
AD1	SD2_DAT[3]	SD2_DAT[3]	PINCNTL117 / 0x4814 09D0	0x0006 0000	0x01	I/O	PIN	H	H	DVDD_RGMII		
		GPMC_A[1]			0x02	O	PIN					
		GP2[5]			0x80	I/O	PIN					

Table 3-11. Ball Characteristics (AAR Package) (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	PINCNTL REGISTER NAME AND ADDRESS[4]	PINCNTL DEFAULT VALUE[5]	MODE [6]	TYPE [7]	DSIS [8]	BALL RESET STATE [9]	BALL RESET REL. STATE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]
AD2	SD2_DAT[4]	SD2_DAT[4]	PINCNTL116 / 0x4814 09CC	0x0006 0000	0x01	I/O	PIN	H	H	DVDD_RGMII		
		GPMC_A[27]			0x02	O	PIN					
		GPMC_A[23]			0x04	O	PIN					
		GPMC_CS[7]			0x08	O	PIN					
		EDMA_EVT0			0x20	I	PIN					
		TIM7_IO			0x40	I/O	PIN					
		GP1[22]			0x80	I/O	PIN					
AE1	SD2_DAT[5]	SD2_DAT[5]	PINCNTL115 / 0x4814 09C8	0x0006 0000	0x01	I/O	PIN	H	H	DVDD_RGMII		
		GPMC_A[26]			0x02	O	PIN					
		GPMC_A[22]			0x04	O	PIN					
		TIM6_IO			0x40	I/O	PIN					
		GP1[21]			0x80	I/O	PIN					
AE2	SD2_DAT[6]	SD2_DAT[6]	PINCNTL114 / 0x4814 09C4	0x0006 0000	0x01	I/O	PIN	H	H	DVDD_RGMII		
		GPMC_A[25]			0x02	O	PIN					
		GPMC_A[21]			0x04	O	PIN					
		UART2_TXD			0x20	O	PIN					
		GP1[20]			0x80	I/O	PIN					
AE3	SD2_DAT[7]	SD2_DAT[7]	PINCNTL113 / 0x4814 09C0	0x0006 0000	0x01	I/O	PIN	H	H	DVDD_RGMII		
		GPMC_A[24]			0x02	O	PIN					
		GPMC_A[20]			0x04	O	PIN					
		UART2_RXD			0x20	I	1					
		GP1[19]			0x80	I/O	PIN					
AC5	SD2_DAT[1]_SDIRQ	SD2_DAT[1]_SDIRQ	PINCNTL119 / 0x4814 09D8	0x0006 0000	0x01	I/O	PIN	H	H	DVDD_RGMII		
		GPMC_A[3]			0x02	O	PIN					
		GP1[13]			0x80	I/O	PIN					
AC8	SD2_DAT[2]_SDRW	SD2_DAT[2]_SDRW	PINCNTL118 / 0x4814 09D4	0x0006 0000	0x01	I/O	PIN	H	H	DVDD_RGMII		
		GPMC_A[2]			0x02	O	PIN					
		GP2[6]			0x80	I/O	PIN					
AC6	SD2_SCLK	SD2_SCLK	PINCNTL121 / 0x4814 09E0	0x0006 0000	0x01	I/O	1	H	H	DVDD_RGMII		
		GP1[15]			0x80	I/O	PIN					
H31	SERDES_CLKN	SERDES_CLKN	NA / NA	NA	0x01	I	NA	NA	NA	VDDA_SATA0_1P8		
H30	SERDES_CLKP	SERDES_CLKP	NA / NA	NA	0x01	I	NA	NA	NA	VDDA_SATA0_1P8		
J28	SPI[0]_D[0]	SPI[0]_D[0]	PINCNTL84 / 0x4814 094C	0x0006 0000	0x01	I/O	PIN	H	H	DVDD		
J27	SPI[0]_D[1]	SPI[0]_D[1]	PINCNTL83 / 0x4814 0948	0x0006 0000	0x01	I/O	PIN	H	H	DVDD		
N24	SPI[0]_SCLK	SPI[0]_SCLK	PINCNTL82 / 0x4814 0944	0x0006 0000	0x01	I/O	PIN	H	H	DVDD		

Table 3-11. Ball Characteristics (AAR Package) (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	PINCNTL REGISTER NAME AND ADDRESS[4]	PINCNTL DEFAULT VALUE[5]	MODE [6]	TYPE [7]	DSIS [8]	BALL RESET STATE [9]	BALL RESET REL. STATE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]
G29	SPI[0]_SCS[0]	SPI[0]_SCS[0]	PINCNTL81 / 0x4814 0940	0x0006 0000	0x01	I/O	PIN	H	H	DVDD		
G28	SPI[0]_SCS[1]	SPI[0]_SCS[1]	PINCNTL80 / 0x4814 093C	0x0006 0000	0x01	I/O	1	H	H	DVDD		
		SD1_SDCD			0x02	I	1					
		SATA0_ACT0_LED			0x04	O	PIN					
		EDMA_EVT1			0x20	I	PIN					
		TIM4_IO			0x40	I/O	PIN					
		GP1[6]			0x80	I/O	PIN					
N23	SPI[1]_D[0]	SPI[1]_D[0]	PINCNTL88 / 0x4814 095C	0x0006 0000	0x01	I/O	PIN	H	H	DVDD		
		GP1[26]			0x80	I/O	PIN					
M27	SPI[1]_D[1]	SPI[1]_D[1]	PINCNTL87 / 0x4814 0958	0x0006 0000	0x01	I/O	PIN	H	H	DVDD		
		GP1[18]			0x80	I/O	PIN					
M29	SPI[1]_SCLK	SPI[1]_SCLK	PINCNTL86 / 0x4814 0954	0x0006 0000	0x01	I/O	PIN	H	H	DVDD		
		GP1[17]			0x80	I/O	PIN					
J29	SPI[1]_SCS[0]	SPI[1]_SCS[0]	PINCNTL85 / 0x4814 0950	0x0006 0000	0x01	I/O	PIN	H	H	DVDD		
		GP1[16]			0x80	I/O	PIN					
T29	TCLK	TCLK	NA / NA	NA	0x01	I	NA	H	H	DVDD		
N28	TDI	TDI	NA / NA	NA	0x01	I	NA	H	H	DVDD		
U26	TDO	TDO	NA / NA	NA	0x01	O	NA	H	H	DVDD		
AG1	TIM2_IO	TIM2_IO	PINCNTL232 / 0x4814 0B9C	0x0004 0000	0x40	I/O	PIN	L	L	DVDD_RGMII		
		GP1[10]			0x80	I/O	PIN					
T31	TMS	TMS	NA / NA	NA	0x01	I	NA	H	H	DVDD		
U24	TRST	TRST	NA / NA	NA	0x01	I	NA	L	L	DVDD		
B9	TV_OUT0	TV_OUT0	NA / NA	NA	0x01	O	NA	NA	NA	VDDA_VDAC_1P8		
B11	TV_RSET	TV_RSET	NA / NA	NA	0x01	A	NA	NA	NA	VDDA_VDAC_1P8		
B10	TV_VFB0	TV_VFB0	NA / NA	NA	0x01	O	NA	NA	NA	VDDA_VDAC_1P8		
D30	UART0_CTS	UART0_CTS	PINCNTL72 / 0x4814 091C	0x000E 0000	0x01	I/O	1	H	H	DVDD		
		DCAN1_TX			0x08	I/O	1					
		SPI[1]_SCS[3]			0x10	I/O	1					
		SD0_SDCD			0x40	I	1					

Table 3-11. Ball Characteristics (AAR Package) (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	PINCNTL REGISTER NAME AND ADDRESS[4]	PINCNTL DEFAULT VALUE[5]	MODE [6]	TYPE [7]	DSIS [8]	BALL RESET STATE [9]	BALL RESET REL. STATE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]
E31	UART0_DCD	UART0_DCD	PINCNTL74 / 0x4814 0924	0x000E 0000	0x01	I	1	H	H	DVDD		
		SPI[0]_SCS[3]			0x10	I/O	1					
		I2C[2]_SCL			0x20	I/O	1					
		SD1_POW			0x40	O	PIN					
		GP1[2]			0x80	I/O	PIN					
E29	UART0_DSR	UART0_DSR	PINCNTL75 / 0x4814 0928	0x000E 0000	0x01	I	1	H	H	DVDD		
		SPI[0]_SCS[2]			0x10	I/O	1					
		I2C[2]_SDA			0x20	I/O	1					
		SD1_SDWP			0x40	I	0					
		GP1[3]			0x80	I/O	PIN					
E30	UART0_DTR	UART0_DTR	PINCNTL76 / 0x4814 092C	0x000E 0000	0x01	O	PIN	H	H	DVDD		
		UART1_TXD			0x04	O	PIN					
		GP1[4]			0x80	I/O	PIN					
N26	UART0_RIN	UART0_RIN	PINCNTL77 / 0x4814 0930	0x000E 0000	0x01	I	1	H	H	DVDD		
		UART1_RXD			0x04	I	1					
		GP1[5]			0x80	I/O	PIN					
D31	UART0_RTS	UART0_RTS	PINCNTL73 / 0x4814 0920	0x000E 0000	0x01	O	PIN	H	H	DVDD		
		DCAN1_RX			0x08	I/O	1					
		SPI[1]_SCS[2]			0x10	I/O	1					
		SD2_SDCD			0x40	I	1					
J26	UART0_RXD	UART0_RXD	PINCNTL70 / 0x4814 0914	0x000E 0000	0x01	I	PIN	H	H	DVDD		
E28	UART0_TXD	UART0_TXD	PINCNTL71 / 0x4814 0918	0x000E 0000	0x01	O	PIN	H	H	DVDD		
L22	UART2_RXD	DCAN0_RX	PINCNTL69 / 0x4814 0910	0x000E 0000	0x01	I/O	1	H	H	DVDD		
		UART2_RXD			0x02	I	1					
		I2C[3]_SCL			0x20	I/O	1					
		GP1[1]			0x80	I/O	PIN					
M21	UART2_TXD	DCAN0_TX	PINCNTL68 / 0x4814 090C	0x000E 0000	0x01	I/O	1	H	H	DVDD		
		UART2_TXD			0x02	O	PIN					
		I2C[3]_SDA			0x20	I/O	1					
		GP1[0]			0x80	I/O	PIN					
B20	USB0_CE	USB0_CE	NA / NA	NA	0x01	O	NA	NA	NA	VDDA_USB_3P3		
B21	USB0_DM	USB0_DM	NA / NA	NA	0x01	I/O	NA	NA	NA	VDDA_USB_3P3		
A21	USB0_DP	USB0_DP	NA / NA	NA	0x01	I/O	NA	NA	NA	VDDA_USB_3P3		
K23	USB0_DRVVBUS	USB0_DRVVBUS	PINCNTL270 / 0x4814 0C34	0x000C 0000	0x01	O	PIN	L	L	DVDD		
		GP0[7]			0x02	I/O	PIN					

Table 3-11. Ball Characteristics (AAR Package) (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	PINCNTL REGISTER NAME AND ADDRESS[4]	PINCNTL DEFAULT VALUE[5]	MODE [6]	TYPE [7]	DSIS [8]	BALL RESET STATE [9]	BALL RESET REL. STATE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]
A20	USB0_ID	USB0_ID	NA / NA	NA	0x01	I	NA	NA	NA	VDDA_USB_3P3		
B22	USB0_VBUSIN	USB0_VBUSIN	NA / NA	NA	0x01	I	NA	NA	NA	VDDA_USB_3P3		
C21	USB1_CE	USB1_CE	NA / NA	NA	0x01	O	NA	NA	NA	VDDA_USB_3P3		
B23	USB1_DM	USB1_DM	NA / NA	NA	0x01	I/O	NA	NA	NA	VDDA_USB_3P3		
A23	USB1_DP	USB1_DP	NA / NA	NA	0x01	I/O	NA	NA	NA	VDDA_USB_3P3		
A24	USB1_ID	USB1_ID	NA / NA	NA	0x01	I	NA	NA	NA	VDDA_USB_3P3		
B24	USB1_VBUSIN	USB1_VBUSIN	NA / NA	NA	0x01	I	NA	NA	NA	VDDA_USB_3P3		
M25, N22, N25, P23, R9, T10, T9	VDDA_1P8	VDDA_1P8	NA / NA	NA	NA	PWR	NA	NA	NA	NA		
L19	VDDA_ARMPLL_1P8	VDDA_ARMPLL_1P8	NA / NA	NA	NA	PWR	NA	NA	NA	NA		
V9	VDDA_AUDIOPLL_1P8	VDDA_AUDIOPLL_1P8	NA / NA	NA	NA	PWR	NA	NA	NA	NA		
W10	VDDA_CSI2_1P8	VDDA_CSI2_1P8	NA / NA	NA	NA	PWR	NA	NA	NA	NA		
AA19	VDDA_DDRPLL_1P8	VDDA_DDRPLL_1P8	NA / NA	NA	NA	PWR	NA	NA	NA	NA		
L15	VDDA_HDDACREF_1P8	VDDA_HDDACREF_1P8	NA / NA	NA	NA	PWR	NA	NA	NA	NA		
K16	VDDA_HDDAC_1P1	VDDA_HDDAC_1P1	NA / NA	NA	NA	PWR	NA	NA	NA	NA		
L14	VDDA_HDDAC_1P8	VDDA_HDDAC_1P8	NA / NA	NA	NA	PWR	NA	NA	NA	NA		
K14	VDDA_HDMI_1P8	VDDA_HDMI_1P8	NA / NA	NA	NA	PWR	NA	NA	NA	NA		
T23	VDDA_HDVICPPLL_1P8	VDDA_HDVICPPLL_1P8	NA / NA	NA	NA	PWR	NA	NA	NA	NA		
W11	VDDA_L3L4_1P8	VDDA_L3L4PLL_1P8	NA / NA	NA	NA	PWR	NA	NA	NA	NA		
N27	VDDA_SATA0_1P8	VDDA_SATA0_1P8	NA / NA	NA	NA	PWR	NA	NA	NA	NA		
K19	VDDA_USB0_1P8	VDDA_USB0_1P8	NA / NA	NA	NA	PWR	NA	NA	NA	NA		
J17	VDDA_USB1_1P8	VDDA_USB1_1P8	NA / NA	NA	NA	PWR	NA	NA	NA	NA		
M19, M20	VDDA_USB_3P3	VDDA_USB_3P3	NA / NA	NA	NA	PWR	NA	NA	NA	NA		
J14	VDDA_VDAC_1P8	VDDA_VDAC_1P8	NA / NA	NA	NA	PWR	NA	NA	NA	NA		

Table 3-11. Ball Characteristics (AAR Package) (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	PINCNTL REGISTER NAME AND ADDRESS[4]	PINCNTL DEFAULT VALUE[5]	MODE [6]	TYPE [7]	DSIS [8]	BALL RESET STATE [9]	BALL RESET REL. STATE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]
L13	VDDA_VIDPLL_1P8	VDDA_VIDPLL_1P8	NA / NA	NA	NA	PWR	NA	NA	NA	NA		
P21	VDDS_OSC0_1P8	VDDS_OSC0_1P8	NA / NA	NA	NA	PWR	NA	NA	NA	NA		
P20	VDDS_OSC1_1P8	VDDS_OSC1_1P8	NA / NA	NA	NA	PWR	NA	NA	NA	NA		
C9	VIN[0]A_CLK	VIN[0]A_CLK	PINCNTL137 / 0x4814 0A20	0x000C 0000	0x01	I	0	L	L	DVDD		
		GP2[2]			0x80	I/O	PIN					
B18	VIN[0]A_D[0]	VIN[0]A_D[0]	PINCNTL140 / 0x4814 0A2C	0x000C 0000	0x01	I	PIN	L	L	DVDD		
		GP1[11]			0x80	I/O	PIN					
A17	VIN[0]A_D[1]	VIN[0]A_D[1]	PINCNTL141 / 0x4814 0A30	0x000C 0000	0x01	I	PIN	L	L	DVDD		
		GP1[12]			0x80	I/O	PIN					
B17	VIN[0]A_D[2]	VIN[0]A_D[2]	PINCNTL142 / 0x4814 0A34	0x000C 0000	0x01	I	PIN	L	L	DVDD		
		GP2[7]			0x80	I/O	PIN					
C17	VIN[0]A_D[3]	VIN[0]A_D[3]	PINCNTL143 / 0x4814 0A38	0x000C 0000	0x01	I	PIN	L	L	DVDD		
		GP2[8]			0x80	I/O	PIN					
D17	VIN[0]A_D[4]	VIN[0]A_D[4]	PINCNTL144 / 0x4814 0A3C	0x000C 0000	0x01	I	PIN	L	L	DVDD		
		GP2[9]			0x80	I/O	PIN					
F17	VIN[0]A_D[5]	VIN[0]A_D[5]	PINCNTL145 / 0x4814 0A40	0x000C 0000	0x01	I	PIN	L	L	DVDD		
		GP2[10]			0x80	I/O	PIN					
L20	VIN[0]A_D[6]	VIN[0]A_D[6]	PINCNTL146 / 0x4814 0A44	0x000C 0000	0x01	I	PIN	L	L	DVDD		
		GP2[11]			0x80	I/O	PIN					
H20	VIN[0]A_D[7]	VIN[0]A_D[7]	PINCNTL147 / 0x4814 0A48	0x000C 0000	0x01	I	PIN	L	L	DVDD		
		GP2[12]			0x80	I/O	PIN					
K11	VIN[0]A_D[16]	VIN[0]A_D[16]	PINCNTL156 / 0x4814 0A6C	0x000E 0000	0x01	I	PIN	H	H	DVDD_C		
		CAM_D[8]			0x02	I	PIN					
		I2C[2]_SCL			0x20	I/O	1					
		GP0[10]			0x80	I/O	PIN					
E12	VIN[0]A_D[17]	VIN[0]A_D[17]	PINCNTL157 / 0x4814 0A70	0x000C 0000	0x01	I	PIN	L	L	DVDD_C		
		CAM_D[9]			0x02	I	PIN					
		GP0[11]			0x80	I/O	PIN					
K10	VIN[0]A_D[18]	VIN[0]A_D[18]	PINCNTL158 / 0x4814 0A74	0x000E 0000	0x01	I	PIN	H	H	DVDD_C		
		CAM_D[10]			0x02	I	PIN					
		I2C[3]_SCL			0x20	I/O	1					
		GP0[12]			0x80	I/O	PIN					
D7	VIN[0]A_D[19]	VIN[0]A_D[19]	PINCNTL159 / 0x4814 0A78	0x000E 0000	0x01	I	PIN	H	H	DVDD_C		
		CAM_D[11]			0x02	I	PIN					
		I2C[3]_SDA			0x20	I/O	1					
		GP0[13]			0x80	I/O	PIN					

Table 3-11. Ball Characteristics (AAR Package) (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	PINCNTL REGISTER NAME AND ADDRESS[4]	PINCNTL DEFAULT VALUE[5]	MODE [6]	TYPE [7]	DSIS [8]	BALL RESET STATE [9]	BALL RESET REL. STATE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]
F9	VIN[0]A_D[20]	VIN[0]A_D[20]	PINCNTL160 / 0x4814 0A7C	0x000C 0000	0x01	I	PIN	L	L	DVDD_C		
		CAM_D[12]			0x02	I	PIN					
		$\overline{\text{SPI[3]\_SCS[0]}}$			0x20	I/O	1					
		GP0[14]			0x80	I/O	PIN					
C7	VIN[0]A_D[21]	VIN[0]A_D[21]	PINCNTL161 / 0x4814 0A80	0x0004 0000	0x01	I	PIN	L	L	DVDD_C		
		CAM_D[13]			0x02	I	PIN					
		SPI[3]_SCLK			0x20	I/O	1					
		GP0[15]			0x80	I/O	PIN					
A6	VIN[0]A_D[22]	VIN[0]A_D[22]	PINCNTL162 / 0x4814 0A84	0x0004 0000	0x01	I	PIN	L	L	DVDD_C		
		CAM_D[14]			0x02	I	PIN					
		SPI[3]_D[1]			0x20	I/O	PIN					
		GP0[16]			0x80	I/O	PIN					
A5	VIN[0]A_D[23]	VIN[0]A_D[23]	PINCNTL163 / 0x4814 0A88	0x0004 0000	0x01	I	PIN	L	L	DVDD_C		
		CAM_D[15]			0x02	I	PIN					
		SPI[3]_D[0]			0x20	I/O	PIN					
		GP0[17]			0x80	I/O	PIN					
C12	VIN[0]A_DE	VIN[0]A_DE	PINCNTL135 / 0x4814 0A18	0x000E 0000	0x01	I	0	H	H	DVDD		
		VIN[0]B_HSYNC			0x10	I	0					
		I2C[2]_SDA			0x40	I/O	1					
		GP2[0]			0x80	I/O	PIN					
B5	VIN[0]A_DE	VIN[0]A_DE	PINCNTL164 / 0x4814 0A8C	0x0006 0000	0x01	I	0	H	H	DVDD_C		
		CAM_D[7]			0x02	I	PIN					
		GP0[18]			0x80	I/O	PIN					
E16	VIN[0]A_D[10]_BD[2]	VIN[0]A_D[10]_BD[2]	PINCNTL150 / 0x4814 0A54	0x000C 0000	0x01	I	PIN	L	L	DVDD		
		GP2[15]			0x80	I/O	PIN					
H17	VIN[0]A_D[11]_BD[3]	VIN[0]A_D[11]_BD[3]	PINCNTL151 / 0x4814 0A58	0x000C 0000	0x01	I	PIN	L	L	DVDD		
		$\overline{\text{CAM\_WE}}$			0x20	I	0					
		GP2[16]			0x80	I/O	PIN					
J16	VIN[0]A_D[12]_BD[4]	VIN[0]A_D[12]_BD[4]	PINCNTL152 / 0x4814 0A5C	0x0004 0000	0x01	I	PIN	L	L	DVDD		
		CLKOUT1			0x20	I/O	PIN					
		GP2[17]			0x80	I/O	PIN					
H16	VIN[0]A_D[13]_BD[5]	VIN[0]A_D[13]_BD[5]	PINCNTL153 / 0x4814 0A60	0x000C 0000	0x01	I	PIN	L	L	DVDD		
		CAM_RESET			0x20	I/O	0					
		GP2[18]			0x80	I/O	PIN					
F13	VIN[0]A_D[14]_BD[6]	VIN[0]A_D[14]_BD[6]	PINCNTL154 / 0x4814 0A64	0x000C 0000	0x01	I	PIN	L	L	DVDD		
		CAM_STROBE			0x20	O	PIN					
		GP2[19]			0x80	I/O	PIN					

Table 3-11. Ball Characteristics (AAR Package) (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	PINCNTL REGISTER NAME AND ADDRESS[4]	PINCNTL DEFAULT VALUE[5]	MODE [6]	TYPE [7]	DSIS [8]	BALL RESET STATE [9]	BALL RESET REL. STATE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]
H13	VIN[0]A_D[15]_BD[7]	VIN[0]A_D[15]_BD[7]	PINCNTL155 / 0x4814 0A68	0x000C 0000	0x01	I	PIN	L	L	DVDD		
		CAM_SHUTTER			0x20	O	PIN					
		GP2[20]			0x80	I/O	PIN					
B16	VIN[0]A_D[8]_BD[0]	VIN[0]A_D[8]_BD[0]	PINCNTL148 / 0x4814 0A4C	0x000C 0000	0x01	I	PIN	L	L	DVDD		
		GP2[13]			0x80	I/O	PIN					
C16	VIN[0]A_D[9]_BD[1]	VIN[0]A_D[9]_BD[1]	PINCNTL149 / 0x4814 0A50	0x000C 0000	0x01	I	PIN	L	L	DVDD		
		GP2[14]			0x80	I/O	PIN					
J13	VIN[0]A_FLD	VIN[0]A_FLD	PINCNTL136 / 0x4814 0A1C	0x000E 0000	0x01	I	0	H	H	DVDD		
		VIN[0]B_VSYNC			0x10	I	0					
		I2C[2]_SCL			0x40	I/O	1					
		GP2[1]			0x80	I/O	PIN					
B4	VIN[0]A_FLD	VIN[0]A_FLD	PINCNTL166 / 0x4814 0A94	0x0006 0000	0x01	I	0	H	H	DVDD_C		
		CAM_D[5]			0x02	I	PIN					
		GP0[20]			0x80	I/O	PIN					
D13	VIN[0]A_HSYNC	VIN[0]A_HSYNC	PINCNTL138 / 0x4814 0A24	0x000E 0000	0x01	I	0	H	H	DVDD		
		GP2[3]			0x80	I/O	PIN					
C13	VIN[0]A_VSYNC	VIN[0]A_VSYNC	PINCNTL139 / 0x4814 0A28	0x000E 0000	0x01	I	0	H	H	DVDD		
		GP2[4]			0x80	I/O	PIN					
H12	VIN[0]B_CLK	VIN[0]B_CLK	PINCNTL134 / 0x4814 0A14	0x0004 0000	0x01	I	0	L	L	DVDD		
		CLKOUT0			0x20	O	PIN					
		GP1[9]			0x80	I/O	PIN					
C5	VIN[0]B_DE	VIN[0]B_DE	PINCNTL165 / 0x4814 0A90	0x0006 0000	0x01	I	0	H	H	DVDD_C		
		CAM_D[6]			0x02	I	PIN					
		GP0[19]			0x80	I/O	PIN					
A3	VIN[0]B_FLD	VIN[0]B_FLD	PINCNTL167 / 0x4814 0A98	0x0006 0000	0x01	I	0	H	H	DVDD_C		
		CAM_D[4]			0x02	I	PIN					
		GP0[21]			0x80	I/O	PIN					
AG4	VIN[1]B_D[0]	VIN[1]B_D[0]	PINCNTL235 / 0x4814 0BA8	0x000C 0000	0x02	I	PIN	L	L	DVDD_RGMII		
		SPI[3]_SCS[3]			0x20	I/O	1					
		I2C[2]_SDA			0x40	I/O	1					
		GP3[23]			0x80	I/O	PIN					
AH1	VIN[1]B_D[1]	VIN[1]B_D[1]	PINCNTL236 / 0x4814 0BAC	0x000C 0000	0x02	I	PIN	L	L	DVDD_RGMII		
		GP3[24]			0x80	I/O	PIN					
AH2	VIN[1]B_D[2]	VIN[1]B_D[2]	PINCNTL237 / 0x4814 0BB0	0x000C 0000	0x02	I	PIN	L	L	DVDD_RGMII		
		GP3[25]			0x80	I/O	PIN					
AJ2	VIN[1]B_D[3]	VIN[1]B_D[3]	PINCNTL238 / 0x4814 0BB4	0x000C 0000	0x02	I	PIN	L	L	DVDD_RGMII		
		GP3[26]			0x80	I/O	PIN					

Table 3-11. Ball Characteristics (AAR Package) (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	PINCNTL REGISTER NAME AND ADDRESS[4]	PINCNTL DEFAULT VALUE[5]	MODE [6]	TYPE [7]	DSIS [8]	BALL RESET STATE [9]	BALL RESET REL. STATE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]
AK1	VIN[1]B_D[4]	VIN[1]B_D[4]	PINCNTL239 / 0x4814 0BB8	0x000C 0000	0x02	I	PIN	L	L	DVDD_RGMII		
		SPI[3]_SCS[2]			0x20	I/O	1					
		GP3[27]			0x80	I/O	PIN					
AK2	VIN[1]B_D[5]	VIN[1]B_D[5]	PINCNTL240 / 0x4814 0BBC	0x0004 0000	0x02	I	PIN	L	L	DVDD_RGMII		
		GP3[28]			0x80	I/O	PIN					
AL2	VIN[1]B_D[6]	VIN[1]B_D[6]	PINCNTL241 / 0x4814 0BC0	0x0004 0000	0x02	I	PIN	L	L	DVDD_RGMII		
		GP3[29]			0x80	I/O	PIN					
AL3	VIN[1]B_D[7]	VIN[1]B_D[7]	PINCNTL242 / 0x4814 0BC4	0x0004 0000	0x02	I	PIN	L	L	DVDD_RGMII		
		GP3[30]			0x80	I/O	PIN					
C20	VOUT[0]_AVID	VOUT[0]_AVID	PINCNTL179 / 0x4814 0AC8	0x000C 0000	0x01	O	PIN	L	L	DVDD		
		VOUT[0]_FLD			0x02	O	PIN					
		SPI[3]_SCLK			0x10	I/O	1					
		TIM7_IO			0x40	I/O	PIN					
		GP2[21]			0x80	I/O	PIN					
F24	VOUT[0]_B_CB_C[2]	VOUT[0]_B_CB_C[2]	PINCNTL180 / 0x4814 0ACC	0x000C 0000	0x01	O	PIN	L	L	DVDD		
		EMU2			0x02	I/O	1					
		GP2[22]			0x80	I/O	PIN					
D21	VOUT[0]_B_CB_C[3]	VOUT[0]_B_CB_C[3]	PINCNTL181 / 0x4814 0AD0	0x000C 0000	0x01	O	PIN	L	L	DVDD		
		GP2[23]			0x80	I/O	PIN					
J23	VOUT[0]_B_CB_C[4]	VOUT[0]_B_CB_C[4]	PINCNTL182 / 0x4814 0AD4	0x000C 0000	0x01	O	PIN	L	L	DVDD		
H23	VOUT[0]_B_CB_C[5]	VOUT[0]_B_CB_C[5]	PINCNTL183 / 0x4814 0AD8	0x000C 0000	0x01	O	PIN	L	L	DVDD		
J24	VOUT[0]_B_CB_C[6]	VOUT[0]_B_CB_C[6]	PINCNTL184 / 0x4814 0ADC	0x000C 0000	0x01	O	PIN	L	L	DVDD		
E24	VOUT[0]_B_CB_C[7]	VOUT[0]_B_CB_C[7]	PINCNTL185 / 0x4814 0AE0	0x000C 0000	0x01	O	PIN	L	L	DVDD		
D24	VOUT[0]_B_CB_C[8]	VOUT[0]_B_CB_C[8]	PINCNTL186 / 0x4814 0AE4	0x000C 0000	0x01	O	PIN	L	L	DVDD		
C24	VOUT[0]_B_CB_C[9]	VOUT[0]_B_CB_C[9]	PINCNTL187 / 0x4814 0AE8	0x000C 0000	0x01	O	PIN	L	L	DVDD		
K22	VOUT[0]_CLK	VOUT[0]_CLK	PINCNTL176 / 0x4814 0ABC	0x000C 0000	0x01	O	PIN	L	L	DVDD		
B3	VOUT[0]_FLD	VOUT[0]_FLD	PINCNTL175 / 0x4814 0AB8	0x0004 0000	0x01	O	PIN	L	L	DVDD_C		
		CAM_PCLK			0x02	I	0					
		GPMC_A[12]			0x10	O	PIN					
		UART2_RTS			0x20	O	PIN					
		GP2[02]			0x80	I/O	PIN					

Table 3-11. Ball Characteristics (AAR Package) (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	PINCNTL REGISTER NAME AND ADDRESS[4]	PINCNTL DEFAULT VALUE[5]	MODE [6]	TYPE [7]	DSIS [8]	BALL RESET STATE [9]	BALL RESET REL. STATE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]
C25	VOUT[0]_G_Y_YC[2]	VOUT[0]_G_Y_YC[2]	PINCNTL188 / 0x4814 0AEC	0x000C 0000	0x01	O	PIN	L	L	DVDD		
		EMU3			0x02	I/O	1					
		GP2[24]			0x80	I/O	PIN					
C26	VOUT[0]_G_Y_YC[3]	VOUT[0]_G_Y_YC[3]	PINCNTL189 / 0x4814 0AF0	0x000C 0000	0x01	O	PIN	L	L	DVDD		
		GP2[25]			0x80	I/O	PIN					
E26	VOUT[0]_G_Y_YC[4]	VOUT[0]_G_Y_YC[4]	PINCNTL190 / 0x4814 0AF4	0x000C 0000	0x01	O	PIN	L	L	DVDD		
B26	VOUT[0]_G_Y_YC[5]	VOUT[0]_G_Y_YC[5]	PINCNTL191 / 0x4814 0AF8	0x000C 0000	0x01	O	PIN	L	L	DVDD		
A26	VOUT[0]_G_Y_YC[6]	VOUT[0]_G_Y_YC[6]	PINCNTL192 / 0x4814 0AFC	0x000C 0000	0x01	O	PIN	L	L	DVDD		
B25	VOUT[0]_G_Y_YC[7]	VOUT[0]_G_Y_YC[7]	PINCNTL193 / 0x4814 0B00	0x000C 0000	0x01	O	PIN	L	L	DVDD		
B27	VOUT[0]_G_Y_YC[8]	VOUT[0]_G_Y_YC[8]	PINCNTL194 / 0x4814 0B04	0x000C 0000	0x01	O	PIN	L	L	DVDD		
A27	VOUT[0]_G_Y_YC[9]	VOUT[0]_G_Y_YC[9]	PINCNTL195 / 0x4814 0B08	0x000C 0000	0x01	O	PIN	L	L	DVDD		
F21	VOUT[0]_HSYNC	VOUT[0]_HSYNC	PINCNTL177 / 0x4814 0AC0	0x000C 0000	0x01	O	PIN	L	L	DVDD		
C28	VOUT[0]_R_CR[2]	VOUT[0]_R_CR[2]	PINCNTL196 / 0x4814 0B0C	0x000C 0000	0x01	O	PIN	L	L	DVDD		
		EMU4			0x02	I/O	1					
		GP2[26]			0x80	I/O	PIN					
B28	VOUT[0]_R_CR[3]	VOUT[0]_R_CR[3]	PINCNTL197 / 0x4814 0B10	0x000C 0000	0x01	O	PIN	L	L	DVDD		
		GP2[27]			0x80	I/O	PIN					
B29	VOUT[0]_R_CR[4]	VOUT[0]_R_CR[4]	PINCNTL198 / 0x4814 0B14	0x000C 0000	0x01	O	PIN	L	L	DVDD		
A29	VOUT[0]_R_CR[5]	VOUT[0]_R_CR[5]	PINCNTL199 / 0x4814 0B18	0x000C 0000	0x01	O	PIN	L	L	DVDD		
C30	VOUT[0]_R_CR[6]	VOUT[0]_R_CR[6]	PINCNTL200 / 0x4814 0B1C	0x000C 0000	0x01	O	PIN	L	L	DVDD		
B30	VOUT[0]_R_CR[7]	VOUT[0]_R_CR[7]	PINCNTL201 / 0x4814 0B20	0x000C 0000	0x01	O	PIN	L	L	DVDD		
A30	VOUT[0]_R_CR[8]	VOUT[0]_R_CR[8]	PINCNTL202 / 0x4814 0B24	0x000C 0000	0x01	O	PIN	L	L	DVDD		
B31	VOUT[0]_R_CR[9]	VOUT[0]_R_CR[9]	PINCNTL203 / 0x4814 0B28	0x000C 0000	0x01	O	PIN	L	L	DVDD		
E20	VOUT[0]_VSYNC	VOUT[0]_VSYNC	PINCNTL178 / 0x4814 0AC4	0x000C 0000	0x01	O	PIN	L	L	DVDD		
F1	VOUT[1]_AVID	VOUT[1]_AVID	PINCNTL207 / 0x4814 0B38	0x0004 0000	0x01	O	PIN	L	L	DVDD		
		VIN[1]A_CLK			0x04	I	0					
		TIM6_IO			0x40	I/O	PIN					
		GP2[31]			0x80	I/O	PIN					

Table 3-11. Ball Characteristics (AAR Package) (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	PINCNTL REGISTER NAME AND ADDRESS[4]	PINCNTL DEFAULT VALUE[5]	MODE [6]	TYPE [7]	DSIS [8]	BALL RESET STATE [9]	BALL RESET REL. STATE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]
H9	VOUT[1]_B_CB_C[0]	VOUT[1]_B_CB_C[0]	PINCNTL173 / 0x4814 0AB0	0x0006 0000	0x01	O	PIN	H	H	DVDD_C		
		CAM_VS			0x02	I/O	0					
		GPMC_A[10]			0x10	O	PIN					
		UART2_TXD			0x20	O	PIN					
		GP0[27]			0x80	I/O	PIN					
D5	VOUT[1]_B_CB_C[1]	VOUT[1]_B_CB_C[1]	PINCNTL172 / 0x4814 0AAC	0x0004 0000	0x01	O	PIN	L	L	DVDD_C		
		CAM_HS			0x02	I/O	0					
		GPMC_A[9]			0x10	O	PIN					
		UART2_RXD			0x20	I	1					
		GP0[26]			0x80	I/O	PIN					
M8	VOUT[1]_B_CB_C[2]	VOUT[1]_B_CB_C[2]	PINCNTL231 / 0x4814 0B98	0x0006 0000	0x01	O	PIN	H	H	DVDD		
		GPMC_A[0]			0x02	O	PIN					
		VIN[1]A_D[7]			0x04	I	PIN					
		HDMI_CEC			0x10	I/O	1					
		SPI[2]_D[0]			0x20	I/O	PIN					
		GP3[30]			0x80	I/O	PIN					
F2	VOUT[1]_B_CB_C[3]	VOUT[1]_B_CB_C[3]	PINCNTL208 / 0x4814 0B3C	0x0004 0000	0x01	O	PIN	L	L	DVDD		
		VIN[1]A_D[0]			0x04	I	PIN					
		GP3[0]			0x80	I/O	PIN					
F3	VOUT[1]_B_CB_C[4]	VOUT[1]_B_CB_C[4]	PINCNTL209 / 0x4814 0B40	0x0004 0000	0x01	O	PIN	L	L	DVDD		
		VIN[1]A_D[1]			0x04	I	PIN					
		GP3[1]			0x80	I/O	PIN					
G1	VOUT[1]_B_CB_C[5]	VOUT[1]_B_CB_C[5]	PINCNTL210 / 0x4814 0B44	0x0004 0000	0x01	O	PIN	L	L	DVDD		
		VIN[1]A_D[2]			0x04	I	PIN					
		GP3[2]			0x80	I/O	PIN					
G2	VOUT[1]_B_CB_C[6]	VOUT[1]_B_CB_C[6]	PINCNTL211 / 0x4814 0B48	0x0004 0000	0x01	O	PIN	L	L	DVDD		
		VIN[1]A_D[3]			0x04	I	PIN					
		GP3[3]			0x80	I/O	PIN					
H3	VOUT[1]_B_CB_C[7]	VOUT[1]_B_CB_C[7]	PINCNTL212 / 0x4814 0B4C	0x0004 0000	0x01	O	PIN	L	L	DVDD		
		VIN[1]A_D[4]			0x04	I	PIN					
		GP3[4]			0x80	I/O	PIN					
G3	VOUT[1]_B_CB_C[8]	VOUT[1]_B_CB_C[8]	PINCNTL213 / 0x4814 0B50	0x0004 0000	0x01	O	PIN	L	L	DVDD		
		VIN[1]A_D[5]			0x04	I	PIN					
		I2C[3]_SCL			0x20	I/O	1					
		GP3[5]			0x80	I/O	PIN					

Table 3-11. Ball Characteristics (AAR Package) (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	PINCNTL REGISTER NAME AND ADDRESS[4]	PINCNTL DEFAULT VALUE[5]	MODE [6]	TYPE [7]	DSIS [8]	BALL RESET STATE [9]	BALL RESET REL. STATE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]
H5	VOUT[1]_B_CB_C[9]	VOUT[1]_B_CB_C[9]	PINCNTL214 / 0x4814 0B54	0x0004 0000	0x01	O	PIN	L	L	DVDD		
		VIN[1]A_D[6]			0x04	I	PIN					
		I2C[3]_SDA			0x20	I/O	1					
		GP3[6]			0x80	I/O	PIN					
D3	VOUT[1]_CLK	VOUT[1]_CLK	PINCNTL204 / 0x4814 0B2C	0x0004 0000	0x01	O	PIN	L	L	DVDD		
		VIN[1]A_HSYNC			0x04	I	0					
		GP2[28]			0x80	I/O	PIN					
J10	VOUT[1]_FLD	VOUT[1]_FLD	PINCNTL174 / 0x4814 0AB4	0x0004 0000	0x01	O	PIN	L	L	DVDD_C		
		CAM_FLD			0x02	I/O	0					
		$\overline{\text{CAM\_WE}}$			0x04	I	0					
		GPMC_A[11]			0x10	O	PIN					
		$\overline{\text{UART2\_CTS}}$			0x20	I/O	1					
		GP0[28]			0x80	I/O	PIN					
B2	VOUT[1]_G_Y_YC[0]	VOUT[1]_G_Y_YC[0]	PINCNTL169 / 0x4814 0AA0	0x0004 0000	0x01	O	PIN	L	L	DVDD_C		
		CAM_D[2]			0x02	I	PIN					
		GPMC_A[6]			0x10	O	PIN					
		GP0[23]			0x80	I/O	PIN					
A2	VOUT[1]_G_Y_YC[1]	VOUT[1]_G_Y_YC[1]	PINCNTL168 / 0x4814 0A9C	0x0006 0000	0x01	O	PIN	H	H	DVDD_C		
		CAM_D[3]			0x02	I	PIN					
		GPMC_A[5]			0x10	O	PIN					
		GP0[22]			0x80	I/O	PIN					
L2	VOUT[1]_G_Y_YC[2]	VOUT[1]_G_Y_YC[2]	PINCNTL228 / 0x4814 0B8C	0x0006 0000	0x01	O	PIN	H	H	DVDD		
		GPMC_A[13]			0x02	O	PIN					
		VIN[1]A_D[21]			0x04	I	PIN					
		HDMI_SCL			0x10	I/O	1					
		$\overline{\text{SPI[2]\_SCS[2]}}$			0x20	I/O	1					
		I2C[2]_SCL			0x40	I/O	1					
		GP3[20]			0x80	I/O	PIN					
H6	VOUT[1]_G_Y_YC[3]	VOUT[1]_G_Y_YC[3]	PINCNTL215 / 0x4814 0B58	0x0004 0000	0x01	O	PIN	L	L	DVDD		
		VIN[1]A_D[8]			0x04	I	PIN					
		GP3[7]			0x80	I/O	PIN					
J8	VOUT[1]_G_Y_YC[4]	VOUT[1]_G_Y_YC[4]	PINCNTL216 / 0x4814 0B5C	0x0004 0000	0x01	O	PIN	L	L	DVDD		
		VIN[1]A_D[9]			0x04	I	PIN					
		GP3[8]			0x80	I/O	PIN					
J1	VOUT[1]_G_Y_YC[5]	VOUT[1]_G_Y_YC[5]	PINCNTL217 / 0x4814 0B60	0x0004 0000	0x01	O	PIN	L	L	DVDD		
		VIN[1]A_D[10]			0x04	I	PIN					
		GP3[9]			0x80	I/O	PIN					

Table 3-11. Ball Characteristics (AAR Package) (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	PINCNTL REGISTER NAME AND ADDRESS[4]	PINCNTL DEFAULT VALUE[5]	MODE [6]	TYPE [7]	DSIS [8]	BALL RESET STATE [9]	BALL RESET REL. STATE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]
H4	VOUT[1]_G_Y_YC[6]	VOUT[1]_G_Y_YC[6]	PINCNTL218 / 0x4814 0B64	0x0004 0000	0x01	O	PIN	L	L	DVDD		
		VIN[1]A_D[11]			0x04	I	PIN					
		GP3[10]			0x80	I/O	PIN					
J9	VOUT[1]_G_Y_YC[7]	VOUT[1]_G_Y_YC[7]	PINCNTL219 / 0x4814 0B68	0x0004 0000	0x01	O	PIN	L	L	DVDD		
		VIN[1]A_D[12]			0x04	I	PIN					
		GP3[11]			0x80	I/O	PIN					
L3	VOUT[1]_G_Y_YC[8]	VOUT[1]_G_Y_YC[8]	PINCNTL220 / 0x4814 0B6C	0x0004 0000	0x01	O	PIN	L	L	DVDD		
		VIN[1]A_D[13]			0x04	I	PIN					
		GP3[12]			0x80	I/O	PIN					
K1	VOUT[1]_G_Y_YC[9]	VOUT[1]_G_Y_YC[9]	PINCNTL221 / 0x4814 0B70	0x0004 0000	0x01	O	PIN	L	L	DVDD		
		VIN[1]A_D[14]			0x04	I	PIN					
		GP3[13]			0x80	I/O	PIN					
E2	VOUT[1]_HSYNC	VOUT[1]_HSYNC	PINCNTL205 / 0x4814 0B30	0x0004 0000	0x01	O	PIN	L	L	DVDD		
		VIN[1]A_VSYNC			0x04	I	0					
		SPI[3]_D[1]			0x10	I/O	PIN					
		GP2[29]			0x80	I/O	PIN					
C2	VOUT[1]_R_CR[0]	VOUT[1]_R_CR[0]	PINCNTL171 / 0x4814 0AA8	0x0004 0000	0x01	O	PIN	L	L	DVDD_C		
		CAM_D[0]			0x02	I	PIN					
		GPMC_A[8]			0x10	O	PIN					
		GP0[25]			0x80	I/O	PIN					
C1	VOUT[1]_R_CR[1]	VOUT[1]_R_CR[1]	PINCNTL170 / 0x4814 0AA4	0x0004 0000	0x01	O	PIN	L	L	DVDD_C		
		CAM_D[1]			0x02	I	PIN					
		GPMC_A[7]			0x10	O	PIN					
		GP0[24]			0x80	I/O	PIN					
L6	VOUT[1]_R_CR[2]	VOUT[1]_R_CR[2]	PINCNTL230 / 0x4814 0B94	0x0004 0000	0x01	O	PIN	L	L	DVDD		
		GPMC_A[15]			0x02	O	PIN					
		VIN[1]A_D[23]			0x04	I	PIN					
		HDMI_HPDET			0x10	I	0					
		SPI[2]_D[1]			0x20	I/O	PIN					
		GP3[22]			0x80	I/O	PIN					
L4	VOUT[1]_R_CR[3]	VOUT[1]_R_CR[3]	PINCNTL229 / 0x4814 0B90	0x0006 0000	0x01	O	PIN	H	H	DVDD		
		GPMC_A[14]			0x02	O	PIN					
		VIN[1]A_D[22]			0x04	I	PIN					
		HDMI_SDA			0x10	I/O	1					
		SPI[2]_SCLK			0x20	I/O	1					
		I2C[2]_SDA			0x40	I/O	1					
		GP3[21]			0x80	I/O	PIN					

Table 3-11. Ball Characteristics (AAR Package) (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	PINCNTL REGISTER NAME AND ADDRESS[4]	PINCNTL DEFAULT VALUE[5]	MODE [6]	TYPE [7]	DSIS [8]	BALL RESET STATE [9]	BALL RESET REL. STATE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]
H2	VOUT[1]_R_CR[4]	VOUT[1]_R_CR[4]	PINCNTL222 / 0x4814 0B74	0x0004 0000	0x01	O	PIN	L	L	DVDD		
		VIN[1]A_D[15]			0x04	I	PIN					
		SPI[3]_SCS[1]			0x20	I/O	1					
		GP3[14]			0x80	I/O	PIN					
M11	VOUT[1]_R_CR[5]	VOUT[1]_R_CR[5]	PINCNTL223 / 0x4814 0B78	0x0004 0000	0x01	O	PIN	L	L	DVDD		
		VIN[1]A_D[16]			0x04	I	PIN					
		SPI[3]_SCLK			0x20	I/O	1					
		GP3[15]			0x80	I/O	PIN					
L12	VOUT[1]_R_CR[6]	VOUT[1]_R_CR[6]	PINCNTL224 / 0x4814 0B7C	0x0004 0000	0x01	O	PIN	L	L	DVDD		
		VIN[1]A_D[17]			0x04	I	PIN					
		SPI[3]_D[1]			0x20	I/O	PIN					
		GP3[16]			0x80	I/O	PIN					
M10	VOUT[1]_R_CR[7]	VOUT[1]_R_CR[7]	PINCNTL225 / 0x4814 0B80	0x0004 0000	0x01	O	PIN	L	L	DVDD		
		VIN[1]A_D[18]			0x04	I	PIN					
		SPI[3]_D[0]			0x20	I/O	PIN					
		GP3[17]			0x80	I/O	PIN					
J2	VOUT[1]_R_CR[8]	VOUT[1]_R_CR[8]	PINCNTL226 / 0x4814 0B84	0x0004 0000	0x01	O	PIN	L	L	DVDD		
		VIN[1]A_D[19]			0x04	I	PIN					
		GP3[18]			0x80	I/O	PIN					
K2	VOUT[1]_R_CR[9]	VOUT[1]_R_CR[9]	PINCNTL227 / 0x4814 0B88	0x0004 0000	0x01	O	PIN	L	L	DVDD		
		VIN[1]A_D[20]			0x04	I	PIN					
		GP3[19]			0x80	I/O	PIN					
F5	VOUT[1]_VSYNC	VOUT[1]_VSYNC	PINCNTL206 / 0x4814 0B34	0x0004 0000	0x01	O	PIN	L	L	DVDD		
		VIN[1]A_FLD			0x04	I	0					
		VIN[1]A_DE			0x08	I	0					
		SPI[3]_D[0]			0x10	I/O	PIN					
		GP2[30]			0x80	I/O	PIN					
AL18	VREFSSTL_DDR[0]	VREFSSTL_DDR[0]	NA / NA	NA	NA	PWR	NA	NA	NA	DVDD_DDR[0]		

Table 3-11. Ball Characteristics (AAR Package) (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	PINCNTL REGISTER NAME AND ADDRESS[4]	PINCNTL DEFAULT VALUE[5]	MODE [6]	TYPE [7]	DSIS [8]	BALL RESET STATE [9]	BALL RESET REL. STATE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]
A1, A31, AA13, AA14, AA15, AA16, AA17, AA18, AA27, AC25, AD24, AD25, AD3, AD4, AD5, AD6, AD7, AE12, AE19, AE20, AE23, AE24, AE25, AE26, AE27, AE28, AE5, AE6, AE7, AE8, AE9, AF12, AF20, AF24, AF25, AF7, AG11, AG19, AG24, AG25, AG7, AH12, AH20, AH7, AL1, AL31, D25, D8, E21, E25, E7, E8, F20, F25, F7, F8, G20, G23, G24, G25, G26, G27, G4, G5, G6, G7, G8, H26, H7, J7, L16, M16, N13, N14, N16, N17, P11, P12, P14, P18, R11, R12, R14, R18, R20, R21, T11, T12, T14, T15, T16, T19, T20, T21, U14, U18, U23, V18, W16, W17, Y16, Y17, Y25, Y26, Y28	VSS	VSS	NA / NA	NA	NA	GND	NA	NA	NA	NA		
U30	VSSA_AUXOSC	VSSA_AUXOSC	NA / NA	NA	NA	GND	NA	NA	NA	NA		
AC7, V14	VSSA_CSI2	VSSA_CSI2	NA / NA	NA	NA	GND	NA	NA	NA	NA		
G30	VSSA_DEVOSC	VSSA_DEVOSC	NA / NA	NA	NA	GND	NA	NA	NA	NA		
G9, H8	VSSA_HDMI	VSSA_HDMI	NA / NA	NA	NA	GND	NA	NA	NA	NA		
D20, N19, N20	VSSA_USB	VSSA_USB	NA / NA	NA	NA	GND	NA	NA	NA	NA		
C8	VSSA_VDAC	VSSA_VDAC	NA / NA	NA	NA	GND	NA	NA	NA	NA		

3.3 Terminal Functions

The terminal functions tables identify the external signal names, the associated pin (ball) numbers along with the mechanical package designator, the pin type, whether the pin has any internal pullup or pulldown resistors, and a functional pin description. For more detailed information on device configurations, peripheral selection, and multiplexed/shared pin see *Device Configurations* section.

(1) **SIGNAL NAME:** The signal name

(2) **DESCRIPTION:** Description of the signal

(3) **TYPE:** Ball type for this specific function:

- I = Input
- O = Output
- I/O = Input/Output
- D = Open drain
- DS = Differential
- A = Analog

(4) **BALL:** Package ball location

3.3.1 Boot Configuration

Table 3-12. Boot Configuration Terminal Functions

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	AAR BALL [4]
BTMODE[0]	Boot Mode Selection 0. ARM Cortex-A8 Boot Mode Configuration Bits. This pin is multiplexed between ARM Cortex-A8 boot mode and the General-Purpose Memory Controller (GPMC) peripheral functions. At reset, the boot mode inputs BTMODE[4:0] are sampled to determine the ARM boot configuration. For more details on the types of boot modes supported, see Section 4.2, Boot Modes, of this document, along with the ROM Code Memory and Peripheral Booting chapter of the device Technical Reference Manual. After reset, this pin functions as GPMC multiplexed data/address pin 0 (GPMC_D[0]).	I	W6
BTMODE[1]	Boot Mode Selection 1. ARM Cortex-A8 Boot Mode Configuration Bits. This pin is multiplexed between ARM Cortex-A8 boot mode and the General-Purpose Memory Controller (GPMC) peripheral functions. At reset, the boot mode inputs BTMODE[4:0] are sampled to determine the ARM boot configuration. For more details on the types of boot modes supported, see Section 4.2, Boot Modes, of this document, along with the ROM Code Memory and Peripheral Booting chapter of the device Technical Reference Manual. After reset, this pin functions as GPMC multiplexed data/address pin 1 (GPMC_D[1]).	I	W4

Table 3-12. Boot Configuration Terminal Functions (continued)

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	AAR BALL [4]
BTMODE[2]	Boot Mode Selection 2. ARM Cortex-A8 Boot Mode Configuration Bits. This pin is multiplexed between ARM Cortex-A8 boot mode and the General-Purpose Memory Controller (GPMC) peripheral functions. At reset, the boot mode inputs BTMODE[4:0] are sampled to determine the ARM boot configuration. For more details on the types of boot modes supported, see Section 4.2, Boot Modes, of this document, along with the ROM Code Memory and Peripheral Booting chapter of the device Technical Reference Manual. After reset, this pin functions as GPMC multiplexed data/address pin 2 (GPMC_D[2]).	I	W3
BTMODE[3]	Boot Mode Selection 3. ARM Cortex-A8 Boot Mode Configuration Bits. This pin is multiplexed between ARM Cortex-A8 boot mode and the General-Purpose Memory Controller (GPMC) peripheral functions. At reset, the boot mode inputs BTMODE[4:0] are sampled to determine the ARM boot configuration. For more details on the types of boot modes supported, see Section 4.2, Boot Modes, of this document, along with the ROM Code Memory and Peripheral Booting chapter of the device Technical Reference Manual. After reset, this pin functions as GPMC multiplexed data/address pin 3 (GPMC_D[3]).	I	U2
BTMODE[4]	Boot Mode Selection 4. ARM Cortex-A8 Boot Mode Configuration Bits. This pin is multiplexed between ARM Cortex-A8 boot mode and the General-Purpose Memory Controller (GPMC) peripheral functions. At reset, the boot mode inputs BTMODE[4:0] are sampled to determine the ARM boot configuration. For more details on the types of boot modes supported, see Section 4.2, Boot Modes, of this document, along with the ROM Code Memory and Peripheral Booting chapter of the device Technical Reference Manual. After reset, this pin functions as GPMC multiplexed data/address pin 4 (GPMC_D[4]).	I	W9
BTMODE[5]	Boot Mode Selection 5. Reserved Boot Pin. This pin is multiplexed between ARM Cortex-A8 boot mode and General-Purpose Memory Controller (GPMC) peripheral functions. For proper device operation at reset, this pin should be externally pulled low. After reset, this pin functions as GPMC multiplexed data/address pin 5 (GPMC_D[5]).	I	T5
BTMODE[6]	Boot Mode Selection 6. Reserved Boot Pin. This pin is multiplexed between ARM Cortex-A8 boot mode and General-Purpose Memory Controller (GPMC) peripheral functions. For proper device operation at reset, this pin should be externally pulled low. After reset, this pin functions as GPMC multiplexed data/address pin 6 (GPMC_D[6]).	I	T3
BTMODE[7]	Boot Mode Selection 7. Reserved Boot Pin. This pin is multiplexed between ARM Cortex-A8 boot mode and General-Purpose Memory Controller (GPMC) peripheral functions. For proper device operation at reset, this pin should be externally pulled low. After reset, this pin functions as GPMC multiplexed data/address pin 7 (GPMC_D[7]).	I	T2

Table 3-12. Boot Configuration Terminal Functions (continued)

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	AAR BALL [4]
BTMODE[8]	Boot Mode Selection 8. Reserved Boot Pin. This pin is multiplexed between ARM Cortex-A8 boot mode and General-Purpose Memory Controller (GPMC) peripheral functions. For proper device operation at reset, this pin should be externally pulled low. After reset, this pin functions as GPMC multiplexed data/address pin 8 (GPMC_D[8]).	I	T1
BTMODE[9]	Boot Mode Selection 9. Reserved Boot Pin. This pin is multiplexed between ARM Cortex-A8 boot mode and General-Purpose Memory Controller (GPMC) peripheral functions. For proper device operation at reset, this pin should be externally pulled low. After reset, this pin functions as GPMC multiplexed data/address pin 9 (GPMC_D[9]).	I	T8
BTMODE[10]	Boot Mode Selection 10. XIP (NOR) on GPMC Configuration. This pin is multiplexed between ARM Cortex-A8 boot mode and General-Purpose Memory Controller (GPMC) peripheral functions. At reset, when the XIP (MUX0), XIP (MUX1), XIP w/ WAiT (MUX0) or XIP w/ WAiT (MUX1) bootmode is selected (see Table 4-1), BTMODE[10] is sampled to select between GPMC pin muxing options A or B shown in Table 4-2, XIP (on GPMC) Boot Options [Muxed or Non-Muxed]. • 0 = GPMC Option A • 1 = GPMC Option B After reset, this pin functions as GPMC multiplexed data/address pin 10 (GPMC_D[10]).	I	R6
BTMODE[11]	Boot Mode Selection 11. $\overline{\text{RSTOUT\_WD\_OUT}}$ Configuration. This pin is multiplexed between ARM Cortex-A8 boot mode and General-Purpose Memory Controller (GPMC) peripheral functions. At reset, BTMODE[11] is sampled to determine the function of the $\overline{\text{RSTOUT\_WD\_OUT}}$ pin: • 0 = $\overline{\text{RSTOUT}}$ is asserted when a Watchdog Timer reset, $\overline{\text{POR}}$, $\overline{\text{RESET}}$, or Emulation/Software-Global Cold/Warm reset occurs • 1 = $\overline{\text{RSTOUT\_WD\_OUT}}$ is asserted only when a Watchdog Timer reset occurs After reset, this pin functions as GPMC multiplexed data/address pin 11 (GPMC_D[11]).	I	R4
BTMODE[12]	Boot Mode Selection 12. GPMC CS0 default Data Bus Width input. This pin is multiplexed between ARM Cortex-A8 boot mode and General-Purpose Memory Controller (GPMC) peripheral functions. At reset, BTMODE[12] is sampled to determine the GPMC CS0 bus width: • 0 = 8-bit data bus • 1 = 16-bit data bus After reset, this pin functions as GPMC multiplexed data/address pin 12 (GPMC_D[12]).	I	R3

Table 3-12. Boot Configuration Terminal Functions (continued)

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	AAR BALL [4]
BTMODE[13]	Boot Mode Selection 13. GPMC CS0 default Address/Data multiplexing mode input. This pin is multiplexed between ARM Cortex-A8 boot mode and General-Purpose Memory Controller (GPMC) peripheral functions. At reset, BTMODE[14:13] are sampled to determine the GPMC CS0 Address/Data multiplexing: • 00 = Not muxed • 01 = A/A/D muxed • 10 = A/D muxed • 11 = Reserved After reset, this pin functions as GPMC multiplexed data/address pin 13 (GPMC_D[13]).	I	R2
BTMODE[14]	Boot Mode Selection 14. GPMC CS0 default Address/Data multiplexing mode input. This pin is multiplexed between ARM Cortex-A8 boot mode and General-Purpose Memory Controller (GPMC) peripheral functions. At reset, BTMODE[14:13] are sampled to determine the GPMC CS0 Address/Data multiplexing: • 00 = Not muxed • 01 = A/A/D muxed • 10 = A/D muxed • 11 = Reserved After reset, this pin functions as GPMC multiplexed data/address pin 14 (GPMC_D[14]).	I	R1
BTMODE[15]	Boot Mode Selection 15. GPMC CS0 default GPMC_Wait enable input. This pin is multiplexed between ARM Cortex-A8 boot mode and General-Purpose Memory Controller (GPMC) peripheral functions. At reset, BTMODE[15] is sampled to determine the GPMC CS0 Wait enable: • 0 = Wait disabled • 1 = Wait enabled After reset, this pin functions as GPMC multiplexed data/address pin 15 (GPMC_D[15]).	I	P2

3.3.2 CSI2 Interface (I/F) Signals

Table 3-13. CSI2 I/F Terminal Functions

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	AAR BALL [4]
CSI2_DX[0]	CSI2 Camera lane 0 differential pair input. When CSI2 is not used these pins can be left unconnected.	I	AB2
CSI2_DX[1]	CSI2 Camera lane 1 differential pair input. When CSI2 is not used these pins can be left unconnected.	I	AA1
CSI2_DX[2]	CSI2 Camera lane 2 differential pair input. When CSI2 is not used these pins can be left unconnected.	I	AA2
CSI2_DX[3]	CSI2 Camera lane 3 differential pair input. When CSI2 is not used these pins can be left unconnected.	I	W2
CSI2_DX[4]	CSI2 Camera lane 4 differential pair input. When CSI2 is not used these pins can be left unconnected.	I	V1
CSI2_DY[0]	CSI2 Camera lane 0 differential pair input. When CSI2 is not used these pins can be left unconnected.	I	AC2
CSI2_DY[1]	CSI2 Camera lane 1 differential pair input. When CSI2 is not used these pins can be left unconnected.	I	AB1
CSI2_DY[2]	CSI2 Camera lane 2 differential pair input. When CSI2 is not used these pins can be left unconnected.	I	Y2
CSI2_DY[3]	CSI2 Camera lane 3 differential pair input. When CSI2 is not used these pins can be left unconnected.	I	W1
CSI2_DY[4]	CSI2 Camera lane 4 differential pair input. When CSI2 is not used these pins can be left unconnected.	I	V2

3.3.3 Camera Interface (I/F)

Table 3-14. Camera I/F Terminal Functions

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	AAR BALL [4]
CAM_D[0]	Camera data input	I	C2
CAM_D[1]	Camera data input	I	C1
CAM_D[2]	Camera data input	I	B2
CAM_D[3]	Camera data input	I	A2
CAM_D[4]	Camera data input	I	A3
CAM_D[5]	Camera data input	I	B4
CAM_D[6]	Camera data input	I	C5
CAM_D[7]	Camera data input	I	B5
CAM_D[8]	Camera data input	I	K11
CAM_D[9]	Camera data input	I	E12
CAM_D[10]	Camera data input	I	K10
CAM_D[11]	Camera data input	I	D7
CAM_D[12]	Camera data input	I	F9
CAM_D[13]	Camera data input	I	C7
CAM_D[14]	Camera data input	I	A6
CAM_D[15]	Camera data input	I	A5
CAM_FLD	Camera Field Identification input	I/O	J10
CAM_HS	Camera Horizontal Synchronization	I/O	D5
CAM_PCLK	Camera Pixel Clock	I	B3
CAM_RESET	Camera Reset. Used for Strobe Synchronization	I/O	H16
CAM_SHUTTER	Camera Mechanical Shutter Control Signal	O	H13
CAM_STROBE	Camera Flash Strobe Control Signal	O	F13
CAM_VS	Camera Vertical Synchronization	I/O	H9
$\overline{\text{CAM\_WE}}$	Camera Write Enable	I	H17, J10

3.3.4 Controller Area Network (DCAN) Modules (DCAN0, DCAN1)

Table 3-15. DCAN Terminal Functions

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	AAR BALL [4]
DCAN0_RX	DCAN0 receive data pin	I/O	L22
DCAN0_TX	DCAN0 transmit data pin	I/O	M21
DCAN1_RX	DCAN1 receive data pin	I/O	D31
DCAN1_TX	DCAN1 transmit data pin	I/O	D30

3.3.5 DDR2/DDR3/DDR3L Memory Controller

Table 3-16. DDR2/DDR3/DDR3L Memory Controller 0 Terminal Functions

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	AAR BALL [4]
DDR[0]_A[0]	DDR[0] Address Bus	O	AL24
DDR[0]_A[1]	DDR[0] Address Bus	O	AC22
DDR[0]_A[2]	DDR[0] Address Bus	O	AJ23
DDR[0]_A[3]	DDR[0] Address Bus	O	AJ27
DDR[0]_A[4]	DDR[0] Address Bus	O	AK28
DDR[0]_A[5]	DDR[0] Address Bus	O	AH27
DDR[0]_A[6]	DDR[0] Address Bus	O	AK30
DDR[0]_A[7]	DDR[0] Address Bus	O	AG23
DDR[0]_A[8]	DDR[0] Address Bus	O	AL29
DDR[0]_A[9]	DDR[0] Address Bus	O	AK29
DDR[0]_A[10]	DDR[0] Address Bus	O	AD23
DDR[0]_A[11]	DDR[0] Address Bus	O	AK24
DDR[0]_A[12]	DDR[0] Address Bus	O	AH23
DDR[0]_A[13]	DDR[0] Address Bus	O	AK23
DDR[0]_A[14]	DDR[0] Address Bus	O	AL23
DDR[0]_A[15]	DDR[0] Address Bus	O	AK22
DDR[0]_BA[0]	DDR[0] Bank Address outputs	O	AK26
DDR[0]_BA[1]	DDR[0] Bank Address outputs	O	AF23
DDR[0]_BA[2]	DDR[0] Bank Address outputs	O	AH25
$\overline{\text{DDR[0]\_CAS}}$	DDR[0] Column Address Strobe output	O	AK25
DDR[0]_CKE	DDR[0] Clock Enable	O	AD20
$\overline{\text{DDR[0]\_CLK}}$	DDR[0] Negative Clock	O	AK27
DDR[0]_CLK	DDR[0] Clock	O	AL27
$\overline{\text{DDR[0]\_CS[0]}}$	DDR[0] Chip Select	O	AB21
DDR[0]_D[0]	DDR[0] Data Bus	I/O	AL9
DDR[0]_D[1]	DDR[0] Data Bus	I/O	AK9
DDR[0]_D[2]	DDR[0] Data Bus	I/O	AK10
DDR[0]_D[3]	DDR[0] Data Bus	I/O	AJ11
DDR[0]_D[4]	DDR[0] Data Bus	I/O	AH11
DDR[0]_D[5]	DDR[0] Data Bus	I/O	AD9
DDR[0]_D[6]	DDR[0] Data Bus	I/O	AF11
DDR[0]_D[7]	DDR[0] Data Bus	I/O	AL12
DDR[0]_D[8]	DDR[0] Data Bus	I/O	AJ12
DDR[0]_D[9]	DDR[0] Data Bus	I/O	AG12
DDR[0]_D[10]	DDR[0] Data Bus	I/O	AD12
DDR[0]_D[11]	DDR[0] Data Bus	I/O	AB12
DDR[0]_D[12]	DDR[0] Data Bus	I/O	AK13
DDR[0]_D[13]	DDR[0] Data Bus	I/O	AC13
DDR[0]_D[14]	DDR[0] Data Bus	I/O	AL14
DDR[0]_D[15]	DDR[0] Data Bus	I/O	AK14
DDR[0]_D[16]	DDR[0] Data Bus	I/O	AH15
DDR[0]_D[17]	DDR[0] Data Bus	I/O	AF15
DDR[0]_D[18]	DDR[0] Data Bus	I/O	AD15
DDR[0]_D[19]	DDR[0] Data Bus	I/O	AK16
DDR[0]_D[20]	DDR[0] Data Bus	I/O	AJ16

Table 3-16. DDR2/DDR3/DDR3L Memory Controller 0 Terminal Functions (continued)

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	AAR BALL [4]
DDR[0]_D[21]	DDR[0] Data Bus	I/O	AG16
DDR[0]_D[22]	DDR[0] Data Bus	I/O	AD16
DDR[0]_D[23]	DDR[0] Data Bus	I/O	AC16
DDR[0]_D[24]	DDR[0] Data Bus	I/O	AK19
DDR[0]_D[25]	DDR[0] Data Bus	I/O	AJ19
DDR[0]_D[26]	DDR[0] Data Bus	I/O	AH19
DDR[0]_D[27]	DDR[0] Data Bus	I/O	AF19
DDR[0]_D[28]	DDR[0] Data Bus	I/O	AD19
DDR[0]_D[29]	DDR[0] Data Bus	I/O	AC19
DDR[0]_D[30]	DDR[0] Data Bus	I/O	AJ20
DDR[0]_D[31]	DDR[0] Data Bus	I/O	AG20
DDR[0]_DQM[0]	Data Mask for lower byte data bus DDR[0]_D[7:0]	O	AL8
DDR[0]_DQM[1]	Data Mask for DDR[0]_D[15:8]	O	AK12
DDR[0]_DQM[2]	Data Mask for DDR[0]_D[23:16]	O	AJ15
DDR[0]_DQM[3]	Data Mask for upper byte data bus DDR[0]_D[31:24]	O	AK18
DDR[0]_DQS[0]	Data Strobe for lower byte data bus DDR[0]_D[7:0]	I/O	AL11
$\overline{\text{DDR[0]\_DQS[0]}}$	Complimentary data strobe for lower byte data bus DDR[0]_D[7:0]	I/O	AK11
$\overline{\text{DDR[0]\_DQS[1]}}$	Complimentary data strobe for DDR[0]_D[15:8]	I/O	AK15
DDR[0]_DQS[1]	Data Strobe for DDR[0]_D[15:8]	I/O	AL15
DDR[0]_DQS[2]	Data Strobe for DDR[0]_D[23:16]	I/O	AL17
$\overline{\text{DDR[0]\_DQS[2]}}$	Complimentary data strobe for DDR[0]_D[23:16]	I/O	AK17
$\overline{\text{DDR[0]\_DQS[3]}}$	Complimentary data strobe for upper byte data bus DDR[0]_D[31:24]	I/O	AK20
DDR[0]_DQS[3]	Data Strobe for upper byte data bus DDR[0]_D[31:24]	I/O	AL20
DDR[0]_ODT[0]	DDR[0] On-Die Termination for Chip Select 0	O	AL21
$\overline{\text{DDR[0]\_RAS}}$	DDR[0] Row Address Strobe output	O	AJ25
DDR[0]_RST	DDR[0] Reset output	O	AA20
DDR[0]_VTP	DDR VTP Compensation Resistor Connection	I	AL30
$\overline{\text{DDR[0]\_WE}}$	DDR[0] Write Enable	O	AL26

3.3.6 EDMA

Table 3-17. EDMA Terminal Functions

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	AAR BALL [4]
EDMA_EVT0	External EDMA Event 0	I	AD2, W8
EDMA_EVT1	External EDMA Event 1	I	G28, Y11
EDMA_EVT2	External EDMA Event 2	I	AG30, Y3
EDMA_EVT3	External EDMA Event 3	I	AB9, AF27

3.3.7 GPMC

Table 3-18. GPMC Terminal Functions

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	AAR BALL [4]
GPMC_A[0]	GPMC Address 0	O	AK3, M8
GPMC_A[1]	GPMC Address 1	O	AD1, AK4
GPMC_A[2]	GPMC Address 2	O	AC8, AJ4
GPMC_A[3]	GPMC Address 3	O	AC5, AL5
GPMC_A[4]	GPMC Address 4	O	AC4, AK5
GPMC_A[5]	GPMC Address 5	O	A2, AJ6
GPMC_A[6]	GPMC Address 6	O	AL6, B2
GPMC_A[7]	GPMC Address 7	O	AK6, C1
GPMC_A[8]	GPMC Address 8	O	AJ7, C2
GPMC_A[9]	GPMC Address 9	O	AK7, D5
GPMC_A[10]	GPMC Address 10	O	AE4, H9
GPMC_A[11]	GPMC Address 11	O	AK8, J10
GPMC_A[12]	GPMC Address 12	O	AJ8, B3
GPMC_A[13]	GPMC Address 13	O	AH8, L2
GPMC_A[14]	GPMC Address 14	O	AG8, L4
GPMC_A[15]	GPMC Address 15	O	AF8, L6
GPMC_A[16]	GPMC Address 16	O	M1
GPMC_A[17]	GPMC Address 17	O	M2
GPMC_A[18]	GPMC Address 18	O	M3
GPMC_A[19]	GPMC Address 19	O	M5
GPMC_A[20]	GPMC Address 20	O	AE3, N9
GPMC_A[21]	GPMC Address 21	O	AE2, N1
GPMC_A[22]	GPMC Address 22	O	AE1, N2
GPMC_A[23]	GPMC Address 23	O	AD2, R8
GPMC_A[24]	GPMC Address 24	O	AC3, AE3, Y11
GPMC_A[25]	GPMC Address 25	O	AA12, AE2, Y3
GPMC_A[26]	GPMC Address 26	O	AE1, AK3, W8
GPMC_A[27]	GPMC Address 27	O	AD2, AK3
GPMC_$\overline{\text{ADV}}$_ALE	GPMC Address Valid output or Address Latch Enable output	O	AA10
$\overline{\text{GPMC\_BE[1]}}$	GPMC Upper Byte Enable output	O	Y11
GPMC_$\overline{\text{BE[0]}}$_CLE	GPMC Lower Byte Enable output or Command Latch Enable output	O	Y3
GPMC_CLK	GPMC Clock output	O	AB9
$\overline{\text{GPMC\_CS[0]}}$	GPMC Chip Select 0	O	AC9
$\overline{\text{GPMC\_CS[1]}}$	GPMC Chip Select 1	O	AA12
$\overline{\text{GPMC\_CS[2]}}$	GPMC Chip Select 2	O	AC3
$\overline{\text{GPMC\_CS[3]}}$	GPMC Chip Select 3	O	AF2
$\overline{\text{GPMC\_CS[4]}}$	GPMC Chip Select 4	O	AG6
$\overline{\text{GPMC\_CS[5]}}$	GPMC Chip Select 5	O	AB9
$\overline{\text{GPMC\_CS[6]}}$	GPMC Chip Select 6	O	AA10
$\overline{\text{GPMC\_CS[7]}}$	GPMC Chip Select 7	O	AD2
GPMC_D[0]	GPMC Multiplexed Data/Address I/O	I/O	W6
GPMC_D[1]	GPMC Multiplexed Data/Address I/O	I/O	W4
GPMC_D[2]	GPMC Multiplexed Data/Address I/O	I/O	W3
GPMC_D[3]	GPMC Multiplexed Data/Address I/O	I/O	U2

Table 3-18. GPMC Terminal Functions (continued)

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	AAR BALL [4]
GPMC_D[4]	GPMC Multiplexed Data/Address I/O	I/O	W9
GPMC_D[5]	GPMC Multiplexed Data/Address I/O	I/O	T5
GPMC_D[6]	GPMC Multiplexed Data/Address I/O	I/O	T3
GPMC_D[7]	GPMC Multiplexed Data/Address I/O	I/O	T2
GPMC_D[8]	GPMC Multiplexed Data/Address I/O	I/O	T1
GPMC_D[9]	GPMC Multiplexed Data/Address I/O	I/O	T8
GPMC_D[10]	GPMC Multiplexed Data/Address I/O	I/O	R6
GPMC_D[11]	GPMC Multiplexed Data/Address I/O	I/O	R4
GPMC_D[12]	GPMC Multiplexed Data/Address I/O	I/O	R3
GPMC_D[13]	GPMC Multiplexed Data/Address I/O	I/O	R2
GPMC_D[14]	GPMC Multiplexed Data/Address I/O	I/O	R1
GPMC_D[15]	GPMC Multiplexed Data/Address I/O	I/O	P2
$\overline{\text{GPMC\_OE\_RE}}$	GPMC Output Enable output	O	Y8
GPMC_WAIT[0]	GPMC Wait input 0	I	W8
GPMC_WAIT[1]	GPMC Wait input 1	I	AB9
$\overline{\text{GPMC\_WE}}$	GPMC Write Enable output	O	Y5

3.3.8 General-Purpose Input/Outputs (GPIOs)

3.3.8.1 GP0

Table 3-19. GP0 Terminal Functions

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	AAR BALL [4]
GP0[0]	Interrupt-Capable General-Purpose Input/Output (I/O)	I/O	Y29
GP0[1]	Interrupt-Capable General-Purpose Input/Output (I/O)	I/O	AB30
GP0[2]	Interrupt-Capable General-Purpose Input/Output (I/O)	I/O	AA29
GP0[3]	Interrupt-Capable General-Purpose Input/Output (I/O)	I/O	AA28
GP0[4]	Interrupt-Capable General-Purpose Input/Output (I/O)	I/O	AA26
GP0[5]	Interrupt-Capable General-Purpose Input/Output (I/O)	I/O	Y31
GP0[6]	Interrupt-Capable General-Purpose Input/Output (I/O)	I/O	Y30
GP0[7]	Interrupt-Capable General-Purpose Input/Output (I/O)	I/O	K23
GP0[8]	Interrupt-Capable General-Purpose Input/Output (I/O)	I/O	AF27
GP0[9]	Interrupt-Capable General-Purpose Input/Output (I/O)	I/O	AG30
GP0[10]	Interrupt-Capable General-Purpose Input/Output (I/O)	I/O	K11
GP0[11]	Interrupt-Capable General-Purpose Input/Output (I/O)	I/O	E12
GP0[12]	Interrupt-Capable General-Purpose Input/Output (I/O)	I/O	AB31, K10
GP0[13]	Interrupt-Capable General-Purpose Input/Output (I/O)	I/O	AC30, D7
GP0[14]	Interrupt-Capable General-Purpose Input/Output (I/O)	I/O	F9
GP0[15]	Interrupt-Capable General-Purpose Input/Output (I/O)	I/O	C7
GP0[16]	Interrupt-Capable General-Purpose Input/Output (I/O)	I/O	A6
GP0[17]	Interrupt-Capable General-Purpose Input/Output (I/O)	I/O	A5
GP0[18]	Interrupt-Capable General-Purpose Input/Output (I/O)	I/O	B5
GP0[19]	Interrupt-Capable General-Purpose Input/Output (I/O)	I/O	C5
GP0[20]	Interrupt-Capable General-Purpose Input/Output (I/O)	I/O	B4
GP0[21]	Interrupt-Capable General-Purpose Input/Output (I/O)	I/O	A3
GP0[22]	Interrupt-Capable General-Purpose Input/Output (I/O)	I/O	A2
GP0[23]	Interrupt-Capable General-Purpose Input/Output (I/O)	I/O	B2
GP0[24]	Interrupt-Capable General-Purpose Input/Output (I/O)	I/O	C1
GP0[25]	Interrupt-Capable General-Purpose Input/Output (I/O)	I/O	C2
GP0[26]	Interrupt-Capable General-Purpose Input/Output (I/O)	I/O	D5
GP0[27]	Interrupt-Capable General-Purpose Input/Output (I/O)	I/O	H9
GP0[28]	Interrupt-Capable General-Purpose Input/Output (I/O)	I/O	J10

3.3.8.2 GP1

Table 3-20. GP1 Terminal Functions

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	AAR BALL [4]
GP1[0]	Interrupt-Capable General-Purpose Input/Output (I/O)	I/O	M21
GP1[1]	Interrupt-Capable General-Purpose Input/Output (I/O)	I/O	L22
GP1[2]	Interrupt-Capable General-Purpose Input/Output (I/O)	I/O	E31
GP1[3]	Interrupt-Capable General-Purpose Input/Output (I/O)	I/O	E29
GP1[4]	Interrupt-Capable General-Purpose Input/Output (I/O)	I/O	E30
GP1[5]	Interrupt-Capable General-Purpose Input/Output (I/O)	I/O	N26
GP1[6]	Interrupt-Capable General-Purpose Input/Output (I/O)	I/O	G28
GP1[7]	Interrupt-Capable General-Purpose Input/Output (I/O)	I/O	U28
GP1[8]	Interrupt-Capable General-Purpose Input/Output (I/O)	I/O	AG6
GP1[9]	Interrupt-Capable General-Purpose Input/Output (I/O)	I/O	H12

Table 3-20. GP1 Terminal Functions (continued)

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	AAR BALL [4]
GP1[10]	Interrupt-Capable General-Purpose Input/Output (I/O)	I/O	AG1
GP1[11]	Interrupt-Capable General-Purpose Input/Output (I/O)	I/O	AG2, B18
GP1[12]	Interrupt-Capable General-Purpose Input/Output (I/O)	I/O	A17, AG3
GP1[13]	Interrupt-Capable General-Purpose Input/Output (I/O)	I/O	AC5, M3
GP1[14]	Interrupt-Capable General-Purpose Input/Output (I/O)	I/O	AC4, M5
GP1[15]	Interrupt-Capable General-Purpose Input/Output (I/O)	I/O	AC6, N9
GP1[16]	Interrupt-Capable General-Purpose Input/Output (I/O)	I/O	J29, N1
GP1[17]	Interrupt-Capable General-Purpose Input/Output (I/O)	I/O	M29, N2
GP1[18]	Interrupt-Capable General-Purpose Input/Output (I/O)	I/O	M27, R8
GP1[19]	Interrupt-Capable General-Purpose Input/Output (I/O)	I/O	AE3
GP1[20]	Interrupt-Capable General-Purpose Input/Output (I/O)	I/O	AE2
GP1[21]	Interrupt-Capable General-Purpose Input/Output (I/O)	I/O	AE1
GP1[22]	Interrupt-Capable General-Purpose Input/Output (I/O)	I/O	AD2
GP1[23]	Interrupt-Capable General-Purpose Input/Output (I/O)	I/O	AC9
GP1[24]	Interrupt-Capable General-Purpose Input/Output (I/O)	I/O	AA12
GP1[25]	Interrupt-Capable General-Purpose Input/Output (I/O)	I/O	AC3
GP1[26]	Interrupt-Capable General-Purpose Input/Output (I/O)	I/O	AF2, N23
GP1[27]	Interrupt-Capable General-Purpose Input/Output (I/O)	I/O	AB9
GP1[28]	Interrupt-Capable General-Purpose Input/Output (I/O)	I/O	AA10
GP1[29]	Interrupt-Capable General-Purpose Input/Output (I/O)	I/O	Y3
GP1[30]	Interrupt-Capable General-Purpose Input/Output (I/O)	I/O	Y11
GP1[31]	Interrupt-Capable General-Purpose Input/Output (I/O)	I/O	W8

3.3.8.3 GP2

Table 3-21. GP2 Terminal Functions

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	AAR BALL [4]
GP2[0]	Interrupt-Capable General-Purpose Input/Output (I/O)	I/O	C12
GP2[1]	Interrupt-Capable General-Purpose Input/Output (I/O)	I/O	J13
GP2[2]	Interrupt-Capable General-Purpose Input/Output (I/O)	I/O	C9
GP2[02]	Interrupt-Capable General-Purpose Input/Output (I/O)	I/O	B3
GP2[3]	Interrupt-Capable General-Purpose Input/Output (I/O)	I/O	D13
GP2[4]	Interrupt-Capable General-Purpose Input/Output (I/O)	I/O	C13
GP2[5]	Interrupt-Capable General-Purpose Input/Output (I/O)	I/O	AD1, M1
GP2[6]	Interrupt-Capable General-Purpose Input/Output (I/O)	I/O	AC8, M2
GP2[7]	Interrupt-Capable General-Purpose Input/Output (I/O)	I/O	B17
GP2[8]	Interrupt-Capable General-Purpose Input/Output (I/O)	I/O	C17
GP2[9]	Interrupt-Capable General-Purpose Input/Output (I/O)	I/O	D17
GP2[10]	Interrupt-Capable General-Purpose Input/Output (I/O)	I/O	F17
GP2[11]	Interrupt-Capable General-Purpose Input/Output (I/O)	I/O	L20
GP2[12]	Interrupt-Capable General-Purpose Input/Output (I/O)	I/O	H20
GP2[13]	Interrupt-Capable General-Purpose Input/Output (I/O)	I/O	B16
GP2[14]	Interrupt-Capable General-Purpose Input/Output (I/O)	I/O	C16
GP2[15]	Interrupt-Capable General-Purpose Input/Output (I/O)	I/O	E16
GP2[16]	Interrupt-Capable General-Purpose Input/Output (I/O)	I/O	H17
GP2[17]	Interrupt-Capable General-Purpose Input/Output (I/O)	I/O	J16
GP2[18]	Interrupt-Capable General-Purpose Input/Output (I/O)	I/O	H16

Table 3-21. GP2 Terminal Functions (continued)

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	AAR BALL [4]
GP2[19]	Interrupt-Capable General-Purpose Input/Output (I/O)	I/O	F13
GP2[20]	Interrupt-Capable General-Purpose Input/Output (I/O)	I/O	H13
GP2[21]	Interrupt-Capable General-Purpose Input/Output (I/O)	I/O	C20
GP2[22]	Interrupt-Capable General-Purpose Input/Output (I/O)	I/O	F24
GP2[23]	Interrupt-Capable General-Purpose Input/Output (I/O)	I/O	D21
GP2[24]	Interrupt-Capable General-Purpose Input/Output (I/O)	I/O	C25
GP2[25]	Interrupt-Capable General-Purpose Input/Output (I/O)	I/O	C26
GP2[26]	Interrupt-Capable General-Purpose Input/Output (I/O)	I/O	C28
GP2[27]	Interrupt-Capable General-Purpose Input/Output (I/O)	I/O	B28
GP2[28]	Interrupt-Capable General-Purpose Input/Output (I/O)	I/O	D3
GP2[29]	Interrupt-Capable General-Purpose Input/Output (I/O)	I/O	E2
GP2[30]	Interrupt-Capable General-Purpose Input/Output (I/O)	I/O	F5
GP2[31]	Interrupt-Capable General-Purpose Input/Output (I/O)	I/O	F1

3.3.8.4 GP3

Table 3-22. GP3 Terminal Functions

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	AAR BALL [4]
GP3[0]	Interrupt-Capable General-Purpose Input/Output (I/O)	I/O	F2
GP3[1]	Interrupt-Capable General-Purpose Input/Output (I/O)	I/O	F3
GP3[2]	Interrupt-Capable General-Purpose Input/Output (I/O)	I/O	G1
GP3[3]	Interrupt-Capable General-Purpose Input/Output (I/O)	I/O	G2
GP3[4]	Interrupt-Capable General-Purpose Input/Output (I/O)	I/O	H3
GP3[5]	Interrupt-Capable General-Purpose Input/Output (I/O)	I/O	G3
GP3[6]	Interrupt-Capable General-Purpose Input/Output (I/O)	I/O	H5
GP3[7]	Interrupt-Capable General-Purpose Input/Output (I/O)	I/O	H6
GP3[8]	Interrupt-Capable General-Purpose Input/Output (I/O)	I/O	J8
GP3[9]	Interrupt-Capable General-Purpose Input/Output (I/O)	I/O	J1
GP3[10]	Interrupt-Capable General-Purpose Input/Output (I/O)	I/O	H4
GP3[11]	Interrupt-Capable General-Purpose Input/Output (I/O)	I/O	J9
GP3[12]	Interrupt-Capable General-Purpose Input/Output (I/O)	I/O	L3
GP3[13]	Interrupt-Capable General-Purpose Input/Output (I/O)	I/O	K1
GP3[14]	Interrupt-Capable General-Purpose Input/Output (I/O)	I/O	H2
GP3[15]	Interrupt-Capable General-Purpose Input/Output (I/O)	I/O	M11
GP3[16]	Interrupt-Capable General-Purpose Input/Output (I/O)	I/O	L12
GP3[17]	Interrupt-Capable General-Purpose Input/Output (I/O)	I/O	M10
GP3[18]	Interrupt-Capable General-Purpose Input/Output (I/O)	I/O	J2
GP3[19]	Interrupt-Capable General-Purpose Input/Output (I/O)	I/O	K2
GP3[20]	Interrupt-Capable General-Purpose Input/Output (I/O)	I/O	L2
GP3[21]	Interrupt-Capable General-Purpose Input/Output (I/O)	I/O	L4
GP3[22]	Interrupt-Capable General-Purpose Input/Output (I/O)	I/O	L6
GP3[23]	Interrupt-Capable General-Purpose Input/Output (I/O)	I/O	AG4
GP3[24]	Interrupt-Capable General-Purpose Input/Output (I/O)	I/O	AH1
GP3[25]	Interrupt-Capable General-Purpose Input/Output (I/O)	I/O	AH2
GP3[26]	Interrupt-Capable General-Purpose Input/Output (I/O)	I/O	AJ2
GP3[27]	Interrupt-Capable General-Purpose Input/Output (I/O)	I/O	AK1
GP3[28]	Interrupt-Capable General-Purpose Input/Output (I/O)	I/O	AK2

Table 3-22. GP3 Terminal Functions (continued)

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	AAR BALL [4]
GP3[29]	Interrupt-Capable General-Purpose Input/Output (I/O)	I/O	AL2
GP3[30]	Interrupt-Capable General-Purpose Input/Output (I/O)	I/O	AL3, M8
GP3[31]	Interrupt-Capable General-Purpose Input/Output (I/O)	I/O	AJ31

3.3.9 Ground Pins (VSS)

Table 3-23. Ground Terminal Functions

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	AAR BALL [4]
VSS	Ground (GND)	GND	A1, A31, AA13, AA14, AA15, AA16, AA17, AA18, AA27, AC25, AD24, AD25, AD3, AD4, AD5, AD6, AD7, AE12, AE19, AE20, AE23, AE24, AE25, AE26, AE27, AE28, AE5, AE6, AE7, AE8, AE9, AF12, AF20, AF24, AF25, AF7, AG11, AG19, AG24, AG25, AG7, AH12, AH20, AH7, AL1, AL31, D25, D8, E21, E25, E7, E8, F20, F25, F7, F8, G20, G23, G24, G25, G26, G27, G4, G5, G6, G7, G8, H26, H7, J7, L16, M16, N13, N14, N16, N17, P11, P12, P14, P18, R11, R12, R14, R18, R20, R21, T11, T12, T14, T15, T16, T19, T20, T21, U14, U18, U23, V18, W16, W17, Y16, Y17, Y25, Y26, Y28
VSSA_AUXOSC	Supply Ground for Auxiliary Oscillator. If internal oscillator is bypassed, this pin should be connected to ground.	GND	U30
VSSA_CSI2	Analog GND for CSI2. Connect to ground even if the CSI2 is not being used.	GND	AC7, V14
VSSA_DEVOSC	Supply Ground for DEV Oscillator. If the internal oscillator is bypassed, this pin should be connected to ground.	GND	G30
VSSA_HDMI	Analog GND for HDMI. For proper device operation, this pin must always be connected to ground, even if HDMI is not being used.	GND	G9, H8
VSSA_USB	Analog GND for USB0 and USB1. For proper device operation, this pin must always be connected to ground, even if USB is not being used.	GND	D20, N19, N20
VSSA_VDAC	Analog GND for VDAC. For proper device operation, this pin must always be connected to ground, even if VDAC is not being used.	GND	C8

3.3.10 HDMI

Table 3-24. HDMI Terminal Functions

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	AAR BALL [4]
HDMI_CEC	HDMI Consumer Electronics Control I/O	I/O	M8, N2
HDMI_CLKN	HDMI Clock Output. When the HDMI PHY is powered down, this pin should be left unconnected.	O	B15
HDMI_CLKP	HDMI Clock Output. When the HDMI PHY is powered down, this pin should be left unconnected.	O	A15
HDMI_DN0	HDMI Data 0 output. When the HDMI PHY is powered down, this pin should be left unconnected.	O	A14
HDMI_DN1	HDMI Data 1 output. When the HDMI PHY is powered down, this pin should be left unconnected.	O	B13
HDMI_DN2	HDMI Data 2 output. When the HDMI PHY is powered down, this pin should be left unconnected.	O	A12
HDMI_DP0	HDMI Data 0 output. When the HDMI PHY is powered down, this pin should be left unconnected.	O	B14
HDMI_DP1	HDMI Data 1 output. When the HDMI PHY is powered down, this pin should be left unconnected.	O	B12
HDMI_DP2	HDMI Data 2 output. When the HDMI PHY is powered down, this pin should be left unconnected.	O	A11
HDMI_HPDET	HDMI Hot Plug Detect Input	I	L6, R8
HDMI_SCL	HDMI I2C Serial Clock Output	I/O	D2, L2
HDMI_SDA	HDMI I2C Serial Data I/O	I/O	D1, L4

3.3.11 I2C

Table 3-25. I2C Terminal Functions

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	AAR BALL [4]
I2C[0]_SCL	I2C[0] Clock I/O. For proper device operation, this pin must be pulled up via external resistor.	I/O	T27
I2C[0]_SDA	I2C[0] Data I/O. For proper device operation, this pin must be pulled up via external resistor.	I/O	T24
I2C[1]_SCL	I2C[1] Clock I/O. For proper device operation in I2C mode, this pin must be pulled up via external resistor.	I/O	D2
I2C[1]_SDA	I2C[1] Data I/O. For proper device operation in I2C mode, this pin must be pulled up via external resistor.	I/O	D1
I2C[2]_SCL	I2C[2] Clock I/O. For proper device operation in I2C mode, this pin must be pulled up via external resistor.	I/O	E31, J13, K11, L2
I2C[2]_SDA	I2C[2] Data I/O. For proper device operation in I2C mode, this pin must be pulled up via external resistor.	I/O	AG4, C12, E29, L4
I2C[3]_SCL	I2C[3] Clock I/O. For proper device operation in I2C mode, this pin must be pulled up via external resistor.	I/O	AE31, G3, K10, L22
I2C[3]_SDA	I2C[3] Data I/O. For proper device operation in I2C mode, this pin must be pulled up via external resistor.	I/O	AE30, D7, H5, M21

3.3.12 McASP

3.3.12.1 McASP0

Table 3-26. McASP0 Terminal Functions

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	AAR BALL [4]
MCA[0]_ACLKR	McASP0 Receive Bit Clock I/O	I/O	AD30
MCA[0]_ACLKX	McASP0 Transmit Bit Clock I/O	I/O	AD28
MCA[0]_AFSR	McASP0 Receive Frame Sync I/O	I/O	AF30
MCA[0]_AFSX	McASP0 Transmit Frame Sync I/O	I/O	AE29
MCA[0]_AHCLKX	McASP0 Transmit High-Frequency Master Clock I/O	I/O	AF31
MCA[0]_AXR[0]	McASP0 Transmit/Receive Data I/O	I/O	AF29
MCA[0]_AXR[1]	McASP0 Transmit/Receive Data I/O	I/O	AE31
MCA[0]_AXR[2]	McASP0 Transmit/Receive Data I/O	I/O	AE30
MCA[0]_AXR[3]	McASP0 Transmit/Receive Data I/O	I/O	AC31
MCA[0]_AXR[4]	McASP0 Transmit/Receive Data I/O	I/O	AD26
MCA[0]_AXR[5]	McASP0 Transmit/Receive Data I/O	I/O	AD27

3.3.12.2 McASP1

Table 3-27. McASP1 Terminal Functions

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	AAR BALL [4]
MCA[1]_ACLKR	McASP1 Receive Bit Clock I/O	I/O	AD29
MCA[1]_ACLKX	McASP1 Transmit Bit Clock I/O	I/O	AC23
MCA[1]_AFSR	McASP1 Receive Frame Sync I/O	I/O	AC24
MCA[1]_AFSX	McASP1 Transmit Frame Sync I/O	I/O	AB22
MCA[1]_AHCLKX	McASP1 Transmit High-Frequency Master Clock I/O	I/O	AF27
MCA[1]_AXR[0]	McASP1 Transmit/Receive Data I/O	I/O	Y22
MCA[1]_AXR[1]	McASP1 Transmit/Receive Data I/O	I/O	Y21

3.3.13 Oscillator/PLL, Audio Reference Clocks, and Clock Generator

3.3.13.1 Audio Reference Clocks

Table 3-28. Audio Reference Clocks Terminal Functions

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	AAR BALL [4]
AUD_CLKIN0	Audio Reference Clock 0 for Audio Peripherals	I	AF31
AUD_CLKIN1	Audio Reference Clock 1 for Audio Peripherals	I	AF27
AUD_CLKIN2	Audio Reference Clock 2 for Audio Peripherals	I	AG30

3.3.13.2 CLOCK GENERATOR

Table 3-29. Clock Generator Terminal Functions

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	AAR BALL [4]
CLKOUT0	Device Clock output 0. Can be used as a system clock for other devices.	O	AJ31, H12
CLKOUT1	Device Clock output 1. Can be used as a system clock for other devices.	O	AB9, J16

3.3.13.3 OSCILLATOR/PLL

Table 3-30. Oscillator/PLL Terminal Functions

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	AAR BALL [4]
AUXOSC_MXI	Auxiliary Crystal input [Optional Audio/Video Reference Crystal Input]. Crystal connection to internal oscillator for auxiliary clock. Functions as AUX_CLKIN clock input when an external oscillator is used. If neither a crystal or external clock is used, this pin should be connected to ground.	I	V30
AUXOSC_MXO	Auxiliary Crystal output [Optional Audio/Video Reference Crystal Output]. When auxiliary oscillator is BYPASSED, leave this pin unconnected.	O	U31
CLKIN32	RTC Clock input. Optional 32.768 KHz clock for RTC reference.	I	AJ31
DEVOSC_MXI	Device Crystal input. Crystal connection to internal oscillator for system clock. Functions as DEV_CLKIN clock input when an external oscillator is used.	I	F30
DEVOSC_MXO	Device Crystal output. Crystal connection to internal oscillator for system clock. When device oscillator is BYPASSED, leave this pin unconnected.	O	G31
DEVOSC_WAKE	Oscillator Wake-up input	I	U28
DEV_CLKIN	Clock input when an external oscillator is used	I	F30

3.3.14 Reserved Pins

Table 3-31. Reserved Terminal Functions

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	AAR BALL [4]
RSV0	Reserved. Leave unconnected, do not connect to power or ground.		J25
RSV1	Reserved. Leave unconnected, do not connect to power or ground.		H27
RSV2	Reserved. Leave unconnected, do not connect to power or ground.		H24
RSV24	Reserved. Leave unconnected, do not connect to power or ground.		J30
RSV25	Reserved. Leave unconnected, do not connect to power or ground.		K30
RSV26	Reserved. Leave unconnected, do not connect to power or ground.		K31
RSV3	Reserved. Leave unconnected, do not connect to power or ground.		H28
RSV31	Reserved. Leave unconnected, do not connect to power or ground.		P31
RSV32	Reserved. Leave unconnected, do not connect to power or ground.		R30
RSV33	Reserved. Leave unconnected, do not connect to power or ground.		T30
RSV34	Reserved. Leave unconnected, do not connect to power or ground.		AH24
RSV35	Reserved. Leave unconnected, do not connect to power or ground.		AJ24
RSV36	Reserved. Leave unconnected, do not connect to power or ground.		L31
RSV39	Reserved. Leave unconnected, do not connect to power or ground.		H25
RSV4	Reserved. Leave unconnected, do not connect to power or ground.	PWR	G17
RSV40	Reserved. Leave unconnected, do not connect to power or ground.		H29
RSV41	Reserved. Leave unconnected, do not connect to power or ground.		AD8
RSV42	Reserved. Leave unconnected, do not connect to power or ground.	O	AK21
RSV43	Reserved. Leave unconnected, do not connect to power or ground.		P30
RSV5	Reserved. Leave unconnected, do not connect to power or ground.	PWR	G16
RSV53	For proper device operation, this pin must always be connected to a 1.8-V Power Supply.	PWR	M26
RSV54	For proper device operation, this pin must always be connected to a 1.8-V Power Supply.	PWR	M28

3.3.15 Reset, Interrupts, and JTAG Interface

3.3.15.1 Interupts

Table 3-32. Interrupts Terminal Functions

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	AAR BALL [4]
$\overline{\text{NMI}}$	Non-Maskable Interrupt input	I	AH31

3.3.15.2 JTAG

Table 3-33. JTAG Terminal Functions

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	AAR BALL [4]
EMU0	Emulator pin 0	I/O	A18
EMU1	Emulator pin 1	I/O	B19
EMU2	Emulator pin 2	I/O	F24
EMU3	Emulator pin 3	I/O	C25
EMU4	Emulator pin 4	I/O	C28
RTCK	JTAG return clock output. The internal pullup (IPU) is enabled for this pin when the device is in reset and the IPU is disabled (DIS) when reset is released.	O	N29
TCLK	JTAG test clock input	I	T29
TDI	JTAG test data input	I	N28
TDO	JTAG test port data output	O	U26
TMS	JTAG test port mode select input. For proper operation, do not oppose the IPU on this pin.	I	T31
$\overline{\text{TRST}}$	JTAG test port reset input	I	U24

3.3.15.3 Reset

Table 3-34. Reset Terminal Functions

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	AAR BALL [4]
$\overline{\text{POR}}$	Power-On Reset input	I	AH30
$\overline{\text{RESET}}$	Device Reset input	I	AH29
$\overline{\text{RSTOUT\_WD\_OUT}}$	Reset output (RSTOUT) or watchdog out (WD_OUT). If this pin is unused, it can be left unconnected.	O	AJ30

3.3.16 SD Signals (MMC/SD/SDIO)

3.3.16.1 SD0

Table 3-35. SD0 Terminal Functions

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	AAR BALL [4]
SD0_CLK	SD0 Clock output	O	AB30
SD0_CMD	SD0 Command output	O	AA29
SD0_DAT[0]	SD0 Data0 I/O. Functions as data bit 0 for 4-/8-bit SD mode and single data bit for 1-bit SD mode.	I/O	AA28
SD0_DAT[3]	SD0 Data3 I/O. Functions as data bit 3 for 4-/8-bit SD mode.	I/O	Y30
SD0_DAT[4]	SD0 Data4 I/O. Functions as data bit 4 for 8-bit SD mode.	I/O	Y22
SD0_DAT[5]	SD0 Data5 I/O. Functions as data bit 5 for 8-bit SD mode.	I/O	Y21
SD0_DAT[6]	SD0 Data6 I/O. Functions as data bit 6 for 8-bit SD mode.	I/O	AB31
SD0_DAT[7]	SD0 Data7 I/O. Functions as data bit 7 for 8-bit SD mode.	I/O	AC30
$\overline{\text{SD0\_DAT[1]\_SDIRQ}}$	SD0 Data1 I/O. Functions as data bit 1 for 4-/8-bit SD mode and as an IRQ input for 1-bit SD mode.	I/O	AA26
$\overline{\text{SD0\_DAT[2]\_SDRW}}$	SD0 Data2 I/O. Functions as data bit 2 for 4-/8-bit SD mode and as a Read Wait input for 1-bit SD mode.	I/O	Y31
SD0_SDCD	SD0 Card Detect input	I	D30

3.3.16.2 SD1

Table 3-36. SD1Terminal Functions

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	AAR BALL [4]
SD1_CLK	SD1 Clock output	O	W30
SD1_CMD	SD1 Command output	O	AA29, Y29
SD1_DAT[0]	SD1 Data0 I/O. Functions as data bit 0 for 4-/8-bit SD mode and single data bit for 1-bit SD mode.	I/O	W31
SD1_DAT[3]	SD1 Data3 I/O. Functions as data bit 3 for 4-/8-bit SD mode.	I/O	Y27
SD1_DAT[4]	SD1 Data4 I/O. Functions as data bit 4 for 8-bit SD mode.	I/O	AA28
SD1_DAT[5]	SD1 Data5 I/O. Functions as data bit 5 for 8-bit SD mode.	I/O	AA26
SD1_DAT[6]	SD1 Data6 I/O. Functions as data bit 6 for 8-bit SD mode.	I/O	Y31
SD1_DAT[7]	SD1 Data7 I/O. Functions as data bit 7 for 8-bit SD mode.	I/O	Y30
$\overline{\text{SD1\_DAT[1]\_SDIRQ}}$	SD1 Data1 I/O. Functions as data bit 1 for 4-/8-bit SD mode and as an IRQ input for 1-bit SD mode.	I/O	AA30
$\overline{\text{SD1\_DAT[2]\_SDRW}}$	SD1 Data2 I/O. Functions as data bit 2 for 4-/8-bit SD mode and as a Read Wait input for 1-bit SD mode.	I/O	U29
SD1_POW	SD1 Card Power Enable output	O	E31
SD1_SDCD	SD1 Card Detect input	I	G28
SD1_SDWP	SD1 Card Write Protect input	I	E29

3.3.16.3 SD2

Table 3-37. SD2Terminal Functions

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	AAR BALL [4]
SD2_CMD	SD2 Command output	O	AG6
SD2_DAT[0]	SD2 Data0 I/O. Functions as data bit 0 for 4-/8-bit SD mode and single data bit for 1-bit SD mode.	O	AC4
SD2_DAT[3]	SD2 Data3 I/O. Functions as data bit 3 for 4-/8-bit SD mode.	I/O	AD1
SD2_DAT[4]	SD2 Data4 I/O. Functions as data bit 4 for 8-bit SD mode.	I/O	AD2
SD2_DAT[5]	SD2 Data5 I/O. Functions as data bit 5 for 8-bit SD mode.	I/O	AE1
SD2_DAT[6]	SD2 Data6 I/O. Functions as data bit 6 for 8-bit SD mode.	I/O	AE2
SD2_DAT[7]	SD2 Data7 I/O. Functions as data bit 7 for 8-bit SD mode.	I/O	AE3
$\overline{\text{SD2\_DAT[1]\_SDIRQ}}$	SD2 Data1 I/O. Functions as data bit 1 for 4-/8-bit SD mode and as an IRQ input for 1-bit SD mode.	I/O	AC5
$\overline{\text{SD2\_DAT[2]\_SDRW}}$	SD2 Data2 I/O. Functions as data bit 2 for 4-/8-bit SD mode and as a Read Wait input for 1-bit SD mode.	I/O	AC8
SD2_SCLK	SD2 Clock output	I/O	AC6
SD2_SDCD	SD2 Card Detect input	I	D31

3.3.17 SPI

3.3.17.1 SPI 0

Table 3-38. SPI 0 Terminal Functions

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	AAR BALL [4]
SPI[0]_D[0]	SPI Data I/O. Can be configured as either MISO or MOSI.	I/O	J28
SPI[0]_D[1]	SPI Data I/O. Can be configured as either MISO or MOSI.	I/O	J27
SPI[0]_SCLK	SPI Clock I/O	I/O	N24
$\overline{\text{SPI[0]\_SCS[0]}}$	SPI Chip Select I/O	I/O	G29
$\overline{\text{SPI[0]\_SCS[1]}}$	SPI Chip Select I/O	I/O	G28
$\overline{\text{SPI[0]\_SCS[2]}}$	SPI Chip Select I/O	I/O	E29
$\overline{\text{SPI[0]\_SCS[3]}}$	SPI Chip Select I/O	I/O	E31

3.3.17.2 SPI 1

Table 3-39. SPI 1 Terminal Functions

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	AAR BALL [4]
SPI[1]_D[0]	SPI Data I/O. Can be configured as either MISO or MOSI.	I/O	N23
SPI[1]_D[1]	SPI Data I/O. Can be configured as either MISO or MOSI.	I/O	M27
SPI[1]_SCLK	SPI Clock I/O	I/O	M29
$\overline{\text{SPI[1]\_SCS[0]}}$	SPI Chip Select I/O	I/O	J29
$\overline{\text{SPI[1]\_SCS[1]}}$	SPI Chip Select I/O	I/O	U28
$\overline{\text{SPI[1]\_SCS[2]}}$	SPI Chip Select I/O	I/O	D31
$\overline{\text{SPI[1]\_SCS[3]}}$	SPI Chip Select I/O	I/O	D30

3.3.17.3 SPI 2

Table 3-40. SPI 2 Terminal Functions

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	AAR BALL [4]
SPI[2]_D[0]	SPI Data I/O. Can be configured as either MISO or MOSI.	I/O	AK6, M8, N1
SPI[2]_D[1]	SPI Data I/O. Can be configured as either MISO or MOSI.	I/O	AL6, L6, N2
SPI[2]_SCLK	SPI Clock I/O	I/O	AJ6, L4, R8
$\overline{\text{SPI[2]\_SCS[0]}}$	SPI Chip Select I/O	I/O	AF2
$\overline{\text{SPI[2]\_SCS[1]}}$	SPI Chip Select I/O	I/O	N9
$\overline{\text{SPI[2]\_SCS[2]}}$	SPI Chip Select I/O	I/O	L2
$\overline{\text{SPI[2]\_SCS[3]}}$	SPI Chip Select I/O	I/O	AK5

3.3.17.4 SPI 3

Table 3-41. SPI 3 Terminal Functions

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	AAR BALL [4]
SPI[3]_D[0]	SPI Data I/O. Can be configured as either MISO or MOSI.	I/O	A5, F5, M10
SPI[3]_D[1]	SPI Data I/O. Can be configured as either MISO or MOSI.	I/O	A6, E2, L12

Table 3-41. SPI 3 Terminal Functions (continued)

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	AAR BALL [4]
SPI[3]_SCLK	SPI Clock I/O	I/O	C20, C7, M11
$\overline{\text{SPI[3]\_SCS[0]}}$	SPI Chip Select I/O	I/O	F9
$\overline{\text{SPI[3]\_SCS[1]}}$	SPI Chip Select I/O	I/O	H2
$\overline{\text{SPI[3]\_SCS[2]}}$	SPI Chip Select I/O	I/O	AK1
$\overline{\text{SPI[3]\_SCS[3]}}$	SPI Chip Select I/O	I/O	AG4

3.3.18 Serial ATA (SATA) Signals

3.3.18.1 SATA0

Table 3-42. Serial ATA 0 (SATA0) Terminal Functions

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	AAR BALL [4]
SATA0_ACT0_LED	Serial ATA Disk 0 Activity LED Output	O	G28
SATA0_RXN0	Serial ATA Data0 Receive. When the SATA SERDES are powered down, these pins should be left unconnected.	I	L30
SATA0_RXP0	Serial ATA Data0 Receive. When the SATA SERDES are powered down, these pins should be left unconnected.	I	M30
SATA0_TXN0	Serial ATA Data0 Transmit. When the SATA SERDES are powered down, these pins should be left unconnected.	O	N30
SATA0_TXP0	Serial ATA Data0 Transmit. When the SATA SERDES are powered down, these pins should be left unconnected.	O	N31
SERDES_CLKN	Optional SATA Reference Clock Inputs. When these pins are not used as optional SATA Reference Clock Inputs, these pins can be left unconnected.	I	H31
SERDES_CLKP	Optional SATA Reference Clock Inputs. When these pins are not used as optional SATA Reference Clock Inputs, these pins can be left unconnected.	I	H30

3.3.19 Supply Voltages

Table 3-43. Supply Voltages Terminal Functions

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	AAR BALL [4]
CVDD	Variable Voltage Supply for the CORE_L Core Logic Voltage Domain	PWR	P15, P17, R15, R17, T13, T17, T18, U11, U12, U15, U17, V11, V12, V15, V17, W13, W14, W19, W20, Y13, Y14, Y19, Y20
CVDD_ARM	Variable Voltage Supply for the ARM_L Core Logic Voltage Domain. For actual voltage supply ranges, see Recommended Operating Conditions.	PWR	K17, L17, L18, M13, M14, M17
CVDD_HDVICP	Variable Voltage Supply for the HDVICP_L Core Logic Voltage Domain. For actual voltage supply ranges, see Recommended Operating Conditions.	PWR	U20, U21, V20, V21, W22
DVDD	3.3 V/1.8 V Power Supply for General I/Os	PWR	D16, E17, F16, L5, M4, M6, M7, N10, N11, T26, T28, U27
DVDD_C	3.3 V/1.8 V Power Supply for Camera I/F I/Os. For proper device operation, this pin must always be connected to a DVDD Power Supply, even if the Camera I/F is not being used.	PWR	D12, E13, F12, G12, G13
DVDD_DDR[0]	1.35 V/1.5 V/1.8 V Power Supply for DDR[0] I/Os	PWR	AB14, AB15, AB17, AB18, AC15, AC17, AC18, AE15, AE16, AF16, AG15, AH16
DVDD_GPMC	3.3 V/1.8 V Power Supply for GPMC I/Os. For proper device operation, this pin must always be connected to a DVDD Power Supply, even if the GPMC is not being used.	PWR	R5, R7, T4, T6, T7
DVDD_RGMII	3.3 V/1.8 V Power Supply for General I/Os. For proper device operation, this pin must always be connected to a DVDD Power Supply.	PWR	W5, W7, Y4, Y6, Y7
DVDD_SD	3.3 V/1.8 V Power Supply for MMC/SD/SDIO I/Os. For proper device operation, this pin must always be connected to a DVDD Power Supply, even if the interface is not being used.	PWR	T25, U25
LDOCAP_ARM	ARM Cortex-A8 VBB LDO output. This pin must always be connected via a 1-uF capacitor to VSS.	A	J19
LDOCAP_ARMRAM	ARM Cortex-A8 RAM LDO output. This pin must always be connected via a 1-uF capacitor to VSS.	A	K20
LDOCAP_HDVICP	HDVICP2 VBB LDO output.This pin must always be connected via a 1-uF capacitor to VSS.	A	W23
LDOCAP_HDVICPRAM	HDVICP2 RAM LDO output. This pin must always be connected via a 1-uF capacitor to VSS.	A	Y24
LDOCAP_RAM0	CORE RAM0 LDO output. This pin must always be connected via a 1-uF capacitor to VSS.	A	U9
LDOCAP_RAM1	CORE RAM1 LDO output. This pin must always be connected via a 1-uF capacitor to VSS.	A	T22
LDOCAP_RAM2	CORE RAM2 LDO output. This pin must always be connected via a 1-uF capacitor to VSS.	A	AB10
LDOCAP_SERDESCLK	SERDES_CLKP/N Pins LDO output. This pin must always be connected via a 1-uF capacitor to VSS.	A	M24
VDDA_1P8	1.8 V Power Supply for on-chip LDOs and I/O biasing	PWR	M25, N22, N25, P23, R9, T10, T9
VDDA_ARMPLL_1P8	1.8 V Analog Power Supply for PLL_ARM	PWR	L19
VDDA_AUDIOPLL_1P8	1.8 V Analog Power Supply for PLL_AUDIO and PLL_HDVPSS. For proper device operation, this pin must always be connected to a 1.8-V Power Supply.	PWR	V9

Table 3-43. Supply Voltages Terminal Functions (continued)

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	AAR BALL [4]
VDDA_CSI2_1P8	1.8 V Analog Power Supply for CSI2. For proper device operation, this pin must always be connected to a 1.8-V Power Supply, even if the CSI2 is not being used.	PWR	W10
VDDA_DDRPLL_1P8	1.8 V Analog Power Supply for PLL_DDR	PWR	AA19
VDDA_HDDACREF_1P8	1.8 V Reference Power Supply for HDDAC. For proper device operation, this pin must always be connected to a 1.8-V Power Supply, even if the HDDAC is not being used.	PWR	L15
VDDA_HDDAC_1P1	1.1 V Power Supply for HD-DAC Digital Logic. For proper device operation, this pin must always be connected to a 1.1-V Power Supply, or if the HD-DAC is not being used it can be connected to a power supply in the range of 0.9–1.35 V (same level as other core voltages).	PWR	K16
VDDA_HDDAC_1P8	1.8 V Power Supply for HDDAC Analog Circuit. For proper device operation, this pin must always be connected to a 1.8-V Power Supply, even if the HDDAC is not being used.	PWR	L14
VDDA_HDMI_1P8	1.8 V Analog Power Supply for HDMI. For proper device operation, this pin must always be connected to a 1.8-V Power Supply, even if the HDMI is not being used.	PWR	K14
VDDA_HDVICPPLL_1P8	1.8 V Analog Power Supply for PLL_HDVICP. For proper device operation, this pin must always be connected to a 1.8-V Power Supply, even if the HDVICP2 is not being used.	PWR	T23
VDDA_L3L4PLL_1P8	1.8 V Analog Power Supply for PLL_L3L4	PWR	W11
VDDA_SATA0_1P8	1.8 V Analog Power Supply for SATA0. For proper device operation, this pin must always be connected to a 1.8-V Power Supply, even if the SATA0 is not being used.	PWR	N27
VDDA_USB0_1P8	1.8 V Analog Power Supply for USB0. For proper device operation, this pin must always be connected to a 1.8-V Power Supply, even if the USB0 is not being used.	PWR	K19
VDDA_USB1_1P8	1.8 V Analog Power Supply for USB1 .For proper device operation, this pin must always be connected to a 1.8-V Power Supply, even if the USB1 is not being used.	PWR	J17
VDDA_USB_3P3	3.3 V Analog Power Supply for USB0 and USB1. For proper device operation, this pin must always be connected to a 3.3-V Power Supply, even if USB0 and USB1 are not being used.	PWR	M19, M20
VDDA_VDAC_1P8	1.8 V Reference Power Supply for VDAC. For proper device operation, this pin must always be connected to a 1.8-V Power Supply, even if the VDAC is not being used.	PWR	J14
VDDA_VIDPLL_1P8	1.8 V Analog Power Supply for PLL_VIDEO0 and PLL_VIDEO1. For proper device operation, this pin must always be connected to a 1.8-V Power Supply.	PWR	L13
VDDS_OSC0_1P8	Oscillator0 IO secondary supply and LJCB LDO supply	PWR	P21
VDDS_OSC1_1P8	Oscillator1 IO secondary power supply	PWR	P20
VREFSSTL_DDR[0]	Reference Power Supply DDR[0]	PWR	AL18

3.3.20 Timer

Table 3-44. Timer Terminal Functions

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	AAR BALL [4]
TIM2_IO	Timer 2 capture event input or PWM output	I/O	AF27, AG1, M3
TIM3_IO	Timer 3 capture event input or PWM output	I/O	AG30, AJ31, M5
TIM4_IO	Timer 4 capture event input or PWM output	I/O	AB9, G28, N2
TIM5_IO	Timer 5 capture event input or PWM output	I/O	AA10, R8, U28
TIM6_IO	Timer 6 capture event input or PWM output	I/O	AE1, F1, Y3
TIM7_IO	Timer 7 capture event input or PWM output	I/O	AD2, C20, Y11

3.3.21 UART

3.3.21.1 UART0

Table 3-45. UART0 Terminal Functions

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	AAR BALL [4]
UART0_CTS	UART0 Clear to Send Input. Functions as SD transceiver control output in IrDA and CIR modes.	I/O	D30
UART0_DCD	UART0 Data Carrier Detect Input	I	E31
UART0_DSR	UART0 Data Set Ready Input	I	E29
UART0_DTR	UART0 Data Terminal Ready Output	O	E30
UART0_RIN	UART0 Ring Indicator Input	I	N26
UART0_RTS	UART0 Request to Send Output. Indicates module is ready to receive data. Functions as transmit data output in IrDA modes.	O	D31
UART0_RXD	UART0 Receive Data Input. Functions as IrDA receive input in IrDA modes and CIR receive input in CIR mode.	I	J26
UART0_TXD	UART0 Transmit Data Output. Functions as CIR transmit output in CIR mode.	O	E28

3.3.21.2 UART1

Table 3-46. UART1 Terminal Functions

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	AAR BALL [4]
UART1_CTS	UART1 Clear to Send Input. Functions as SD transceiver control output in IrDA and CIR modes.	I/O	AG8
UART1_RTS	UART1 Request to Send Output. Indicates module is ready to receive data. Functions as transmit data output in IrDA modes.	O	AF8
UART1_RXD	UART1 Receive Data Input. Functions as IrDA receive input in IrDA modes and CIR receive input in CIR mode. (N26:MUX0, AJ8:MUX1)	I	AJ8, N26
UART1_TXD	UART1 Transmit Data Output. Functions as CIR transmit output in CIR mode. (E30:MUX0, AH8:MUX1)	O	AH8, E30

3.3.21.3 UART2

Table 3-47. UART2 Terminal Functions

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	AAR BALL [4]
UART2_CTS	UART2 Clear to Send Input. Functions as SD transceiver control output in IrDA and CIR modes.	I/O	J10
UART2_RTS	UART2 Request to Send Output. Indicates module is ready to receive data. Functions as transmit data output in IrDA modes.	O	B3
UART2_RXD	UART2 Receive Data Input. Functions as IrDA receive input in IrDA modes and CIR receive input in CIR mode. (D5:MUX0, L22:MUX1, AE3:MUX3)	I	AE3, D5, L22
UART2_TXD	UART2 Transmit Data Output. Functions as CIR transmit output in CIR mode. (H9:MUX0, M21:MUX1, AE2:MUX3)	O	AE2, H9, M21

3.3.22 USB

3.3.22.1 USB0

Table 3-48. USB0 Terminal Functions

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	AAR BALL [4]
USB0_CE	USB0 charger enable. When the USB0 PHY is powered down, this pin should be left unconnected.	O	B20
USB0_DM	USB0 bidirectional data differential signal pair [plus/minus]. When the USB0 PHY is powered down, this pin should be left unconnected.	I/O	B21
USB0_DP	USB0 bidirectional data differential signal pair [plus/minus]. When the USB0 PHY is powered down, this pin should be left unconnected.	I/O	A21
USB0_DRVVBUS	USB0 Contoller VBUS Control ouput. When this pin is used as USB0_DRVVBUS and the USB0 Controller is operating as a Host, this signal is used by the USB0 Controller to enable the external VBUS charge pump. When the USB0 PHY is powered down, this pin should be left unconnected.	O	K23
USB0_ID	USB0 identification input. When the USB0 PHY is powered down, this pin should be left unconnected.	I	A20
USB0_VBUSIN	5-V USB0 VBUS comparator input. This analog input pin senses the level of the USB VBUS voltage and should connect directly to the USB VBUS voltage. When the USB0 PHY is powered down, this pin should be left unconnected.	I	B22

3.3.22.2 USB1

Table 3-49. USB1 Terminal Functions

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	AAR BALL [4]
USB1_CE	USB1 charger enable. When the USB1 PHY is powered down, this pin should be left unconnected.	O	C21
USB1_DM	USB1 bidirectional data differential signal pair [plus/minus]. When the USB1 PHY is powered down, this pin should be left unconnected.	I/O	B23
USB1_DP	USB1 bidirectional data differential signal pair [plus/minus]. When the USB1 PHY is powered down, this pin should be left unconnected.	I/O	A23
USB1_DRVVBUS	USB1 Contoller VBUS Control ouput. When this pin is used as USB1_DRVVBUS and the USB1 Controller is operating as a Host, this signal is used by the USB1 Controller to enable the external VBUS charge pump. When the USB1 PHY is powered down, this pin should be left unconnected.	O	AF31
USB1_ID	USB1 identification input. When the USB1 PHY is powered down, this pin should be left unconnected.	I	A24
USB1_VBUSIN	5-V USB1 VBUS comparator input. This analog input pin senses the level of the USB VBUS voltage and should connect directly to the USB VBUS voltage. When the USB1 PHY is powered down, this pin should be left unconnected.	I	B24

3.3.23 Video Input (Digital)

3.3.23.1 Video Input 0 (Digital)

Table 3-50. Video Input 0 (Digital) Terminal Functions

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	AAR BALL [4]
VIN[0]A_CLK	Video Input 0 Port A Clock input. Input clock for 8-bit, 16-bit, or 24-bit Port A video capture.	I	C9
VIN[0]A_D[0]	Video Input 0 Data inputs. For 16-bit capture, D[7:0] are Cb/Cr Port A inputs. For 8-bit capture, D[7:0] are Port A YCbCr data inputs. For RGB capture, D[7:0] are B data inputs.	I	B18
VIN[0]A_D[1]	Video Input 0 Data inputs. For 16-bit capture, D[7:0] are Cb/Cr Port A inputs. For 8-bit capture, D[7:0] are Port A YCbCr data inputs. For RGB capture, D[7:0] are B data inputs.	I	A17
VIN[0]A_D[2]	Video Input 0 Data inputs. For 16-bit capture, D[7:0] are Cb/Cr Port A inputs. For 8-bit capture, D[7:0] are Port A YCbCr data inputs. For RGB capture, D[7:0] are B data inputs.	I	B17
VIN[0]A_D[3]	Video Input 0 Data inputs. For 16-bit capture, D[7:0] are Cb/Cr Port A inputs. For 8-bit capture, D[7:0] are Port A YCbCr data inputs. For RGB capture, D[7:0] are B data inputs.	I	C17
VIN[0]A_D[4]	Video Input 0 Data inputs. For 16-bit capture, D[7:0] are Cb/Cr Port A inputs. For 8-bit capture, D[7:0] are Port A YCbCr data inputs. For RGB capture, D[7:0] are B data inputs.	I	D17
VIN[0]A_D[5]	Video Input 0 Data inputs. For 16-bit capture, D[7:0] are Cb/Cr Port A inputs. For 8-bit capture, D[7:0] are Port A YCbCr data inputs. For RGB capture, D[7:0] are B data inputs.	I	F17
VIN[0]A_D[6]	Video Input 0 Data inputs. For 16-bit capture, D[7:0] are Cb/Cr Port A inputs. For 8-bit capture, D[7:0] are Port A YCbCr data inputs. For RGB capture, D[7:0] are B data inputs.	I	L20
VIN[0]A_D[7]	Video Input 0 Data inputs. For 16-bit capture, D[7:0] are Cb/Cr Port A inputs. For 8-bit capture, D[7:0] are Port A YCbCr data inputs. For RGB capture, D[7:0] are B data inputs.	I	H20
VIN[0]A_D[16]	Video Input 0 Data inputs. For RGB capture, D[23:16] are R data inputs.	I	K11
VIN[0]A_D[17]	Video Input 0 Data inputs. For RGB capture, D[23:16] are R data inputs.	I	E12
VIN[0]A_D[18]	Video Input 0 Data inputs. For RGB capture, D[23:16] are R data inputs.	I	K10
VIN[0]A_D[19]	Video Input 0 Data inputs. For RGB capture, D[23:16] are R data inputs.	I	D7
VIN[0]A_D[20]	Video Input 0 Data inputs. For RGB capture, D[23:16] are R data inputs.	I	F9
VIN[0]A_D[21]	Video Input 0 Data inputs. For RGB capture, D[23:16] are R data inputs.	I	C7
VIN[0]A_D[22]	Video Input 0 Data inputs. For RGB capture, D[23:16] are R data inputs.	I	A6
VIN[0]A_D[23]	Video Input 0 Data inputs. For RGB capture, D[23:16] are R data inputs.	I	A5
VIN[0]A_DE	Video Input 0 Port A Data Enable input. Discrete data valid signal for Port A RGB capture mode or YCbCr capture without embedded syncs (BT.601 modes).	I	B5, C12

Table 3-50. Video Input 0 (Digital) Terminal Functions (continued)

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	AAR BALL [4]
VIN[0]A_D[10]_BD[2]	Video Input 0 Data inputs. For 16-bit capture, D[15:8] are Y Port A inputs. For 8-bit capture, D[15:8] are Port B YCbCr data inputs. For RGB capture, D[15:8] are G data inputs.	I	E16
VIN[0]A_D[11]_BD[3]	Video Input 0 Data inputs. For 16-bit capture, D[15:8] are Y Port A inputs. For 8-bit capture, D[15:8] are Port B YCbCr data inputs. For RGB capture, D[15:8] are G data inputs.	I	H17
VIN[0]A_D[12]_BD[4]	Video Input 0 Data inputs. For 16-bit capture, D[15:8] are Y Port A inputs. For 8-bit capture, D[15:8] are Port B YCbCr data inputs. For RGB capture, D[15:8] are G data inputs.	I	J16
VIN[0]A_D[13]_BD[5]	Video Input 0 Data inputs. For 16-bit capture, D[15:8] are Y Port A inputs. For 8-bit capture, D[15:8] are Port B YCbCr data inputs. For RGB capture, D[15:8] are G data inputs.	I	H16
VIN[0]A_D[14]_BD[6]	Video Input 0 Data inputs. For 16-bit capture, D[15:8] are Y Port A inputs. For 8-bit capture, D[15:8] are Port B YCbCr data inputs. For RGB capture, D[15:8] are G data inputs.	I	F13
VIN[0]A_D[15]_BD[7]	Video Input 0 Data inputs. For 16-bit capture, D[15:8] are Y Port A inputs. For 8-bit capture, D[15:8] are Port B YCbCr data inputs. For RGB capture, D[15:8] are G data inputs.	I	H13
VIN[0]A_D[8]_BD[0]	Video Input 0 Data inputs. For 16-bit capture, D[15:8] are Y Port A inputs. For 8-bit capture, D[15:8] are Port B YCbCr data inputs. For RGB capture, D[15:8] are G data inputs.	I	B16
VIN[0]A_D[9]_BD[1]	Video Input 0 Data inputs. For 16-bit capture, D[15:8] are Y Port A inputs. For 8-bit capture, D[15:8] are Port B YCbCr data inputs. For RGB capture, D[15:8] are G data inputs.	I	C16
VIN[0]A_FLD	Video Input 0 Port A Field ID input. Discrete field identification signal for Port A RGB capture mode or YCbCr capture without embedded syncs (BT.601 modes).	I	B4, J13
VIN[0]A_HSYNC	Video Input 0 Port A Horizontal Sync0 input. Discrete horizontal synchronization signal for Port A RGB capture mode or YCbCr capture without embedded syncs (BT.601 modes).	I	D13
VIN[0]A_VSYNC	Video Input 0 Port A Vertical Sync0 input. Discrete vertical synchronization signal for Port A RGB capture mode or YCbCr capture without embedded syncs (BT.601 modes).	I	C13
VIN[0]B_CLK	Video Input 0 Port B Clock input. Input clock for 8-bit Port B video capture. This signal is not used in 16-bit and 24-bit capture modes.	I	H12
VIN[0]B_DE	Video Input 0 Port B Data Enable input. Discrete data valid signal for Port B RGB capture mode or YCbCr capture without embedded syncs (BT.601 modes).	I	C5
VIN[0]B_FLD	Video Input 0 Port B Field ID input. Discrete field identification signal for Port B 8-bit YCbCr capture without embedded syncs (BT.601 modes). Not used in RGB or 16-bit YCbCr capture modes.	I	A3
VIN[0]B_HSYNC	Video Input 0 Port B Horizontal Sync input. Discrete horizontal synchronization signal for Port B 8-bit YCbCr capture without embedded syncs (BT.601 modes). Not used in RGB or 16-bit YCbCr capture modes.	I	C12
VIN[0]B_VSYNC	Video Input 0 Port B Vertical Sync1 input. Discrete vertical synchronization signal for Port B 8-bit YCbCr capture without embedded syncs (BT.601 modes). Not used in RGB or 16-bit YCbCr capture modes.	I	J13

3.3.23.2 Video Input 1 (Digital)

Table 3-51. Video Input 1 (Digital) Terminal Functions

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	AAR BALL [4]
VIN[1]A_CLK	Video Input 1 Port A Clock input. Input clock for 8-bit, 16-bit, or 24-bit Port A video capture. Input data is sampled on the CLK0 edge.	I	F1
VIN[1]A_D[0]	Video Input 1 Data inputs. For 16-bit capture, D[7:0] are Cb/Cr Port A inputs. For 8-bit capture, D[7:0] are Port A YCbCr data inputs. For RGB capture, D[7:0] are B Port A data inputs.	I	F2
VIN[1]A_D[1]	Video Input 1 Data inputs. For 16-bit capture, D[7:0] are Cb/Cr Port A inputs. For 8-bit capture, D[7:0] are Port A YCbCr data inputs. For RGB capture, D[7:0] are B Port A data inputs.	I	F3
VIN[1]A_D[2]	Video Input 1 Data inputs. For 16-bit capture, D[7:0] are Cb/Cr Port A inputs. For 8-bit capture, D[7:0] are Port A YCbCr data inputs. For RGB capture, D[7:0] are B Port A data inputs.	I	G1
VIN[1]A_D[3]	Video Input 1 Data inputs. For 16-bit capture, D[7:0] are Cb/Cr Port A inputs. For 8-bit capture, D[7:0] are Port A YCbCr data inputs. For RGB capture, D[7:0] are B Port A data inputs.	I	G2
VIN[1]A_D[4]	Video Input 1 Data inputs. For 16-bit capture, D[7:0] are Cb/Cr Port A inputs. For 8-bit capture, D[7:0] are Port A YCbCr data inputs. For RGB capture, D[7:0] are B Port A data inputs.	I	H3
VIN[1]A_D[5]	Video Input 1 Data inputs. For 16-bit capture, D[7:0] are Cb/Cr Port A inputs. For 8-bit capture, D[7:0] are Port A YCbCr data inputs. For RGB capture, D[7:0] are B Port A data inputs.	I	G3
VIN[1]A_D[6]	Video Input 1 Data inputs. For 16-bit capture, D[7:0] are Cb/Cr Port A inputs. For 8-bit capture, D[7:0] are Port A YCbCr data inputs. For RGB capture, D[7:0] are B Port A data inputs.	I	H5
VIN[1]A_D[7]	Video Input 1 Data inputs. For 16-bit capture, D[7:0] are Cb/Cr Port A inputs. For 8-bit capture, D[7:0] are Port A YCbCr data inputs. For RGB capture, D[7:0] are B Port A data inputs.	I	M8
VIN[1]A_D[8]	Video Input 1 Data inputs. For 16-bit capture, [15:8] are Y Port A inputs. For RGB capture, D[15:8] are G Port A data inputs.	I	H6
VIN[1]A_D[9]	Video Input 1 Data inputs. For 16-bit capture, [15:8] are Y Port A inputs. For RGB capture, D[15:8] are G Port A data inputs.	I	J8
VIN[1]A_D[10]	Video Input 1 Data inputs. For 16-bit capture, [15:8] are Y Port A inputs. For RGB capture, D[15:8] are G Port A data inputs.	I	J1
VIN[1]A_D[11]	Video Input 1 Data inputs. For 16-bit capture, [15:8] are Y Port A inputs. For RGB capture, D[15:8] are G Port A data inputs.	I	H4
VIN[1]A_D[12]	Video Input 1 Data inputs. For 16-bit capture, [15:8] are Y Port A inputs. For RGB capture, D[15:8] are G Port A data inputs.	I	J9
VIN[1]A_D[13]	Video Input 1 Data inputs. For 16-bit capture, [15:8] are Y Port A inputs. For RGB capture, D[15:8] are G Port A data inputs.	I	L3
VIN[1]A_D[14]	Video Input 1 Data inputs. For 16-bit capture, [15:8] are Y Port A inputs. For RGB capture, D[15:8] are G Port A data inputs.	I	K1
VIN[1]A_D[15]	Video Input 1 Data inputs. For 16-bit capture, [15:8] are Y Port A inputs. For RGB capture, D[15:8] are G Port A data inputs.	I	H2

Table 3-51. Video Input 1 (Digital) Terminal Functions (continued)

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	AAR BALL [4]
VIN[1]A_D[16]	Video Input 1 Data inputs. For RGB capture, D[23:16] are R Port A data inputs.	I	M11
VIN[1]A_D[17]	Video Input 1 Data inputs. For RGB capture, D[23:16] are R Port A data inputs.	I	L12
VIN[1]A_D[18]	Video Input 1 Data inputs. For RGB capture, D[23:16] are R Port A data inputs.	I	M10
VIN[1]A_D[19]	Video Input 1 Data inputs. For RGB capture, D[23:16] are R Port A data inputs.	I	J2
VIN[1]A_D[20]	Video Input 1 Data inputs. For RGB capture, D[23:16] are R Port A data inputs.	I	K2
VIN[1]A_D[21]	Video Input 1 Data inputs. For RGB capture, D[23:16] are R Port A data inputs.	I	L2
VIN[1]A_D[22]	Video Input 1 Data inputs. For RGB capture, D[23:16] are R Port A data inputs.	I	L4
VIN[1]A_D[23]	Video Input 1 Data inputs. For RGB capture, D[23:16] are R Port A data inputs.	I	L6
VIN[1]A_DE	Video Input 1 Port A Data Enable input. Discrete data valid signal for Port A YCbCr capture modes without embedded syncs (BT.601 modes).	I	F5
VIN[1]A_FLD	Video Input 1 Port A Field ID input. Discrete field identification signal for Port A YCbCr capture modes without embedded syncs (BT.601 modes).	I	F5
VIN[1]A_HSYNC	Video Input 1 Port A Horizontal Sync input. Discrete horizontal synchronization signal for Port A YCbCr capture modes without embedded syncs (BT.601 modes).	I	D3
VIN[1]A_VSYNC	Video Input 1 Port A Vertical Sync input. Discrete vertical synchronization signal for Port A YCbCr capture modes without embedded syncs (BT.601 modes).	I	E2
VIN[1]B_CLK	Video Input 1 Port B Clock input. Input clock for 8-bit Port B video capture. Input data is sampled on the CLK1 edge. This signal is not used in 16-bit and 24-bit capture modes.	I	AF2
VIN[1]B_D[0]	Video Input Port B Data inputs. For 8-bit capture, B_D[7:0] are Port B YCbCr data inputs.	I	AG4
VIN[1]B_D[1]	Video Input Port B Data inputs. For 8-bit capture, B_D[7:0] are Port B YCbCr data inputs.	I	AH1
VIN[1]B_D[2]	Video Input Port B Data inputs. For 8-bit capture, B_D[7:0] are Port B YCbCr data inputs.	I	AH2
VIN[1]B_D[3]	Video Input Port B Data inputs. For 8-bit capture, B_D[7:0] are Port B YCbCr data inputs.	I	AJ2
VIN[1]B_D[4]	Video Input Port B Data inputs. For 8-bit capture, B_D[7:0] are Port B YCbCr data inputs.	I	AK1
VIN[1]B_D[5]	Video Input Port B Data inputs. For 8-bit capture, B_D[7:0] are Port B YCbCr data inputs.	I	AK2
VIN[1]B_D[6]	Video Input Port B Data inputs. For 8-bit capture, B_D[7:0] are Port B YCbCr data inputs.	I	AL2
VIN[1]B_D[7]	Video Input Port B Data inputs. For 8-bit capture, B_D[7:0] are Port B YCbCr data inputs.	I	AL3

3.3.24 Video Output (Analog, TV)

Table 3-52. Video Output (Analog, TV) Terminal Functions

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	AAR BALL [4]
HDDAC_A	Analog HD Video DAC (G/Y). This pin should be connected to ground through a 165-ohm resistor.	O	A9
HDDAC_B	Analog HD Video DAC (B/Pb). This pin should be connected to ground through a 165-ohm resistor.	O	A8
HDDAC_C	Analog HD Video DAC (R/Pr). This pin should be connected to ground through a 165-ohm resistor.	O	B8
HDDAC_HSYNC	Analog HD Video DAC Discrete HSYNC Output	O	E9
HDDAC_IREF	Video DAC reference current. When the video DACs are used, this pin should be connected to ground through a 2.67K-ohm resistor. When the video DACs are powered down, this pin should be left unconnected.	I/O	B6
HDDAC_VREF	Video DAC reference voltage. When the video DACs are powered down, this pin should be left unconnected.	I	B7
HDDAC_VSYNC	Analog HD Video DAC Discrete VSYNC Output	O	D9
TV_OUT0	Composite Amplifier Output. In **Normal mode** (internal amplifier used), this pin drives the 75-Ohm TV load. An external resistor (Rout) should be connected between this pin and the TV_VFB0 pin and be placed as close to the pins as possible. The nominal value of Rout is 2700 Ohm. In **TVOUT Bypass mode** (internal amplifier not used), this pin is not used. When this pin is not used or the TV output is powered-down, this pin should be left unconnected.	O	B9
TV_RSET	TV Input Reference Current Setting. An external resistor (Rset) should be connected between this pin and VSSA_VDAC to set the reference current of the video DAC. The value of the resistor depends on the mode of operation. In **Normal mode** (internal amplifier used), the nominal value for Rset is 4700 Ohm. In **TVOUT Bypass mode** (internal amplifier not used), the nominal value for Rset is 10000 Ohm. When the TV output is not used, this pin should be connected to ground (VSS).	A	B11
TV_VFB0	Composite Feedback. In **Normal mode** (internal amplifier used), this pin acts as the buffer feedback node. An external resistor (Rout) should be connected between this pin and the TV_OUT0 pin. In **TVOUT Bypass mode** (internal amplifier not used), this pin acts as the direct Video DAC output and should be connected to ground through a load resistor (Rload) and to an external video amplifier. The nominal value of Rload is 1500 Ohm. When this pin is not used or the TV output is powered-down, this pin should be left unconnected.	O	B10

3.3.25 Video Output (Digital)

3.3.25.1 Video Output 0 (Digital)

Table 3-53. Video Output 0 (Digital) Terminal Functions

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	AAR BALL [4]
VOUT[0]_AVID	Video Output Active Video output. This is the discrete active video indicator output. This signal is not used for embedded sync modes.	O	C20
VOUT[0]_B_CB_C[2]	Video Output Data. These signals represent the 8 MSBs of B/Cb/C video data. For RGB mode they are blue data bits, for YUV444 mode they are Cb (Chroma) data bits, for Y/C mode they are multiplexed Cb/Cr (Chroma) data bits and for BT.656 mode they are unused.	O	F24
VOUT[0]_B_CB_C[3]	Video Output Data. These signals represent the 8 MSBs of B/Cb/C video data. For RGB mode they are blue data bits, for YUV444 mode they are Cb (Chroma) data bits, for Y/C mode they are multiplexed Cb/Cr (Chroma) data bits and for BT.656 mode they are unused.	O	D21
VOUT[0]_B_CB_C[4]	Video Output Data. These signals represent the 8 MSBs of B/Cb/C video data. For RGB mode they are blue data bits, for YUV444 mode they are Cb (Chroma) data bits, for Y/C mode they are multiplexed Cb/Cr (Chroma) data bits and for BT.656 mode they are unused.	O	J23
VOUT[0]_B_CB_C[5]	Video Output Data. These signals represent the 8 MSBs of B/Cb/C video data. For RGB mode they are blue data bits, for YUV444 mode they are Cb (Chroma) data bits, for Y/C mode they are multiplexed Cb/Cr (Chroma) data bits and for BT.656 mode they are unused.	O	H23
VOUT[0]_B_CB_C[6]	Video Output Data. These signals represent the 8 MSBs of B/Cb/C video data. For RGB mode they are blue data bits, for YUV444 mode they are Cb (Chroma) data bits, for Y/C mode they are multiplexed Cb/Cr (Chroma) data bits and for BT.656 mode they are unused.	O	J24
VOUT[0]_B_CB_C[7]	Video Output Data. These signals represent the 8 MSBs of B/Cb/C video data. For RGB mode they are blue data bits, for YUV444 mode they are Cb (Chroma) data bits, for Y/C mode they are multiplexed Cb/Cr (Chroma) data bits and for BT.656 mode they are unused.	O	E24
VOUT[0]_B_CB_C[8]	Video Output Data. These signals represent the 8 MSBs of B/Cb/C video data. For RGB mode they are blue data bits, for YUV444 mode they are Cb (Chroma) data bits, for Y/C mode they are multiplexed Cb/Cr (Chroma) data bits and for BT.656 mode they are unused.	O	D24
VOUT[0]_B_CB_C[9]	Video Output Data. These signals represent the 8 MSBs of B/Cb/C video data. For RGB mode they are blue data bits, for YUV444 mode they are Cb (Chroma) data bits, for Y/C mode they are multiplexed Cb/Cr (Chroma) data bits and for BT.656 mode they are unused.	O	C24
VOUT[0]_CLK	Video Output Clock output	O	K22
VOUT[0]_FLD	Video Output Field ID output. This is the discrete field identification output. This signal is not used for embedded sync modes.	O	B3, C20
VOUT[0]_G_Y_YC[2]	Video Output Data. These signals represent the 8 MSBs of G/Y/YC video data. For RGB mode they are green data bits, for YUV444 mode they are Y data bits, for Y/C mode they are Y (Luma) data bits and for BT.656 mode they are multiplexed Y/Cb/Cr (Luma and Chroma) data bits.	O	C25

Table 3-53. Video Output 0 (Digital) Terminal Functions (continued)

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	AAR BALL [4]
VOUT[0]_G_Y_YC[3]	Video Output Data. These signals represent the 8 MSBs of G/Y/YC video data. For RGB mode they are green data bits, for YUV444 mode they are Y data bits, for Y/C mode they are Y (Luma) data bits and for BT.656 mode they are multiplexed Y/Cb/Cr (Luma and Chroma) data bits.	O	C26
VOUT[0]_G_Y_YC[4]	Video Output Data. These signals represent the 8 MSBs of G/Y/YC video data. For RGB mode they are green data bits, for YUV444 mode they are Y data bits, for Y/C mode they are Y (Luma) data bits and for BT.656 mode they are multiplexed Y/Cb/Cr (Luma and Chroma) data bits.	O	E26
VOUT[0]_G_Y_YC[5]	Video Output Data. These signals represent the 8 MSBs of G/Y/YC video data. For RGB mode they are green data bits, for YUV444 mode they are Y data bits, for Y/C mode they are Y (Luma) data bits and for BT.656 mode they are multiplexed Y/Cb/Cr (Luma and Chroma) data bits.	O	B26
VOUT[0]_G_Y_YC[6]	Video Output Data. These signals represent the 8 MSBs of G/Y/YC video data. For RGB mode they are green data bits, for YUV444 mode they are Y data bits, for Y/C mode they are Y (Luma) data bits and for BT.656 mode they are multiplexed Y/Cb/Cr (Luma and Chroma) data bits.	O	A26
VOUT[0]_G_Y_YC[7]	Video Output Data. These signals represent the 8 MSBs of G/Y/YC video data. For RGB mode they are green data bits, for YUV444 mode they are Y data bits, for Y/C mode they are Y (Luma) data bits and for BT.656 mode they are multiplexed Y/Cb/Cr (Luma and Chroma) data bits.	O	B25
VOUT[0]_G_Y_YC[8]	Video Output Data. These signals represent the 8 MSBs of G/Y/YC video data. For RGB mode they are green data bits, for YUV444 mode they are Y data bits, for Y/C mode they are Y (Luma) data bits and for BT.656 mode they are multiplexed Y/Cb/Cr (Luma and Chroma) data bits.	O	B27
VOUT[0]_G_Y_YC[9]	Video Output Data. These signals represent the 8 MSBs of G/Y/YC video data. For RGB mode they are green data bits, for YUV444 mode they are Y data bits, for Y/C mode they are Y (Luma) data bits and for BT.656 mode they are multiplexed Y/Cb/Cr (Luma and Chroma) data bits.	O	A27
VOUT[0]_HSYNC	Video Output Horizontal Sync output. This is the discrete horizontal synchronization output. This signal is not used for embedded sync modes.	O	F21
VOUT[0]_R_CR[2]	Video Output Data. These signals represent the 8 MSBs of R/Cr video data. For RGB mode they are red data bits, for YUV444 mode they are Cr (Chroma) data bits, for Y/C mode and BT.656 modes they are unused.	O	C28
VOUT[0]_R_CR[3]	Video Output Data. These signals represent the 8 MSBs of R/Cr video data. For RGB mode they are red data bits, for YUV444 mode they are Cr (Chroma) data bits, for Y/C mode and BT.656 modes they are unused.	O	B28
VOUT[0]_R_CR[4]	Video Output Data. These signals represent the 8 MSBs of R/Cr video data. For RGB mode they are red data bits, for YUV444 mode they are Cr (Chroma) data bits, for Y/C mode and BT.656 modes they are unused.	O	B29
VOUT[0]_R_CR[5]	Video Output Data. These signals represent the 8 MSBs of R/Cr video data. For RGB mode they are red data bits, for YUV444 mode they are Cr (Chroma) data bits, for Y/C mode and BT.656 modes they are unused.	O	A29

Table 3-53. Video Output 0 (Digital) Terminal Functions (continued)

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	AAR BALL [4]
VOUT[0]_R_CR[6]	Video Output Data. These signals represent the 8 MSBs of R/Cr video data. For RGB mode they are red data bits, for YUV444 mode they are Cr (Chroma) data bits, for Y/C mode and BT.656 modes they are unused.	O	C30
VOUT[0]_R_CR[7]	Video Output Data. These signals represent the 8 MSBs of R/Cr video data. For RGB mode they are red data bits, for YUV444 mode they are Cr (Chroma) data bits, for Y/C mode and BT.656 modes they are unused.	O	B30
VOUT[0]_R_CR[8]	Video Output Data. These signals represent the 8 MSBs of R/Cr video data. For RGB mode they are red data bits, for YUV444 mode they are Cr (Chroma) data bits, for Y/C mode and BT.656 modes they are unused.	O	A30
VOUT[0]_R_CR[9]	Video Output Data. These signals represent the 8 MSBs of R/Cr video data. For RGB mode they are red data bits, for YUV444 mode they are Cr (Chroma) data bits, for Y/C mode and BT.656 modes they are unused.	O	B31
VOUT[0]_VSYNC	Video Output Vertical Sync output. This is the discrete vertical synchronization output. This signal is not used for embedded sync modes.	O	E20

3.3.25.2 Video Output 1 (Digital)

Table 3-54. Video Output 1 (Digital) Terminal Functions

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	AAR BALL [4]
VOUT[1]_AVID	Video Output Active Video output. This is the discrete active video indicator output. This signal is not used for embedded sync modes.	O	F1
VOUT[1]_B_CB_C[0]	Video Output Data. These signals represent the 2 LSBs of B/Cb/C video data for 10-bit, 20-bit, and 30-bit video modes (VOUT[1] only). For RGB mode they are blue data bits, for YUV444 mode they are Cb (Chroma) data bits, for Y/C mode they are multiplexed Cb/Cr (Chroma) data bits and for BT.656 mode they are unused. These signals are not used in 16/24-bit modes.	O	H9
VOUT[1]_B_CB_C[1]	Video Output Data. These signals represent the 2 LSBs of B/Cb/C video data for 10-bit, 20-bit, and 30-bit video modes (VOUT[1] only). For RGB mode they are blue data bits, for YUV444 mode they are Cb (Chroma) data bits, for Y/C mode they are multiplexed Cb/Cr (Chroma) data bits and for BT.656 mode they are unused. These signals are not used in 16/24-bit modes.	O	D5
VOUT[1]_B_CB_C[2]	Video Output Data. These signals represent the 8 MSBs of B/Cb/C video data. For RGB mode they are blue data bits, for YUV444 mode they are Cb (Chroma) data bits, for Y/C mode they are multiplexed Cb/Cr (Chroma) data bits and for BT.656 mode they are unused.	O	M8
VOUT[1]_B_CB_C[3]	Video Output Data. These signals represent the 8 MSBs of B/Cb/C video data. For RGB mode they are blue data bits, for YUV444 mode they are Cb (Chroma) data bits, for Y/C mode they are multiplexed Cb/Cr (Chroma) data bits and for BT.656 mode they are unused.	O	F2
VOUT[1]_B_CB_C[4]	Video Output Data. These signals represent the 8 MSBs of B/Cb/C video data. For RGB mode they are blue data bits, for YUV444 mode they are Cb (Chroma) data bits, for Y/C mode they are multiplexed Cb/Cr (Chroma) data bits and for BT.656 mode they are unused.	O	F3
VOUT[1]_B_CB_C[5]	Video Output Data. These signals represent the 8 MSBs of B/Cb/C video data. For RGB mode they are blue data bits, for YUV444 mode they are Cb (Chroma) data bits, for Y/C mode they are multiplexed Cb/Cr (Chroma) data bits and for BT.656 mode they are unused.	O	G1

Table 3-54. Video Output 1 (Digital) Terminal Functions (continued)

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	AAR BALL [4]
VOUT[1]_B_CB_C[6]	Video Output Data. These signals represent the 8 MSBs of B/Cb/C video data. For RGB mode they are blue data bits, for YUV444 mode they are Cb (Chroma) data bits, for Y/C mode they are multiplexed Cb/Cr (Chroma) data bits and for BT.656 mode they are unused.	O	G2
VOUT[1]_B_CB_C[7]	Video Output Data. These signals represent the 8 MSBs of B/Cb/C video data. For RGB mode they are blue data bits, for YUV444 mode they are Cb (Chroma) data bits, for Y/C mode they are multiplexed Cb/Cr (Chroma) data bits and for BT.656 mode they are unused.	O	H3
VOUT[1]_B_CB_C[8]	Video Output Data. These signals represent the 8 MSBs of B/Cb/C video data. For RGB mode they are blue data bits, for YUV444 mode they are Cb (Chroma) data bits, for Y/C mode they are multiplexed Cb/Cr (Chroma) data bits and for BT.656 mode they are unused.	O	G3
VOUT[1]_B_CB_C[9]	Video Output Data. These signals represent the 8 MSBs of B/Cb/C video data. For RGB mode they are blue data bits, for YUV444 mode they are Cb (Chroma) data bits, for Y/C mode they are multiplexed Cb/Cr (Chroma) data bits and for BT.656 mode they are unused.	O	H5
VOUT[1]_CLK	Video Output Clock output	O	D3
VOUT[1]_FLD	Video Output Field ID output. This is the discrete field identification output. This signal is not used for embedded sync modes.	O	J10
VOUT[1]_G_Y_YC[0]	Video Output Data. These signals represent the 2 LSBs of G/Y/YC video data for 10-bit, 20-bit, and 30-bit video modes (VOUT[1] only). For RGB mode they are green data bits, for YUV444 mode they are Y data bits, for Y/C mode they are Y (Luma) data bits and for BT.656 mode they are multiplexed Y/Cb/Cr (Luma and Chroma) data bits. These signals are not used in 8/16/24-bit modes.	O	B2
VOUT[1]_G_Y_YC[1]	Video Output Data. These signals represent the 2 LSBs of G/Y/YC video data for 10-bit, 20-bit, and 30-bit video modes (VOUT[1] only). For RGB mode they are green data bits, for YUV444 mode they are Y data bits, for Y/C mode they are Y (Luma) data bits and for BT.656 mode they are multiplexed Y/Cb/Cr (Luma and Chroma) data bits. These signals are not used in 8/16/24-bit modes.	O	A2
VOUT[1]_G_Y_YC[2]	Video Output Data. These signals represent the 8 MSBs of G/Y/YC video data. For RGB mode they are green data bits, for YUV444 mode they are Y data bits, for Y/C mode they are Y (Luma) data bits and for BT.656 mode they are multiplexed Y/Cb/Cr (Luma and Chroma) data bits.	O	L2
VOUT[1]_G_Y_YC[3]	Video Output Data. These signals represent the 8 MSBs of G/Y/YC video data. For RGB mode they are green data bits, for YUV444 mode they are Y data bits, for Y/C mode they are Y (Luma) data bits and for BT.656 mode they are multiplexed Y/Cb/Cr (Luma and Chroma) data bits.	O	H6
VOUT[1]_G_Y_YC[4]	Video Output Data. These signals represent the 8 MSBs of G/Y/YC video data. For RGB mode they are green data bits, for YUV444 mode they are Y data bits, for Y/C mode they are Y (Luma) data bits and for BT.656 mode they are multiplexed Y/Cb/Cr (Luma and Chroma) data bits.	O	J8
VOUT[1]_G_Y_YC[5]	Video Output Data. These signals represent the 8 MSBs of G/Y/YC video data. For RGB mode they are green data bits, for YUV444 mode they are Y data bits, for Y/C mode they are Y (Luma) data bits and for BT.656 mode they are multiplexed Y/Cb/Cr (Luma and Chroma) data bits.	O	J1

Table 3-54. Video Output 1 (Digital) Terminal Functions (continued)

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	AAR BALL [4]
VOUT[1]_G_Y_YC[6]	Video Output Data. These signals represent the 8 MSBs of G/Y/YC video data. For RGB mode they are green data bits, for YUV444 mode they are Y data bits, for Y/C mode they are Y (Luma) data bits and for BT.656 mode they are multiplexed Y/Cb/Cr (Luma and Chroma) data bits.	O	H4
VOUT[1]_G_Y_YC[7]	Video Output Data. These signals represent the 8 MSBs of G/Y/YC video data. For RGB mode they are green data bits, for YUV444 mode they are Y data bits, for Y/C mode they are Y (Luma) data bits and for BT.656 mode they are multiplexed Y/Cb/Cr (Luma and Chroma) data bits.	O	J9
VOUT[1]_G_Y_YC[8]	Video Output Data. These signals represent the 8 MSBs of G/Y/YC video data. For RGB mode they are green data bits, for YUV444 mode they are Y data bits, for Y/C mode they are Y (Luma) data bits and for BT.656 mode they are multiplexed Y/Cb/Cr (Luma and Chroma) data bits.	O	L3
VOUT[1]_G_Y_YC[9]	Video Output Data. These signals represent the 8 MSBs of G/Y/YC video data. For RGB mode they are green data bits, for YUV444 mode they are Y data bits, for Y/C mode they are Y (Luma) data bits and for BT.656 mode they are multiplexed Y/Cb/Cr (Luma and Chroma) data bits.	O	K1
VOUT[1]_HSYNC	Video Output Horizontal Sync output. This is the discrete horizontal synchronization output. This signal is not used for embedded sync modes.	O	E2
VOUT[1]_R_CR[0]	Video Output Data. These signals represent the 2 LSBs of R/Cr video data for 30-bit video modes. For RGB mode they are red data bits, for YUV444 mode they are Cr (Chroma) data bits, for Y/C mode and BT.656 modes they are unused. These signals are not used in 24-bit mode.	O	C2
VOUT[1]_R_CR[1]	Video Output Data. These signals represent the 2 LSBs of R/Cr video data for 30-bit video modes. For RGB mode they are red data bits, for YUV444 mode they are Cr (Chroma) data bits, for Y/C mode and BT.656 modes they are unused. These signals are not used in 24-bit mode.	O	C1
VOUT[1]_R_CR[2]	Video Output Data. These signals represent the 8 MSBs of R/Cr video data. For RGB mode they are red data bits, for YUV444 mode they are Cr (Chroma) data bits, for Y/C mode and BT.656 modes they are unused.	O	L6
VOUT[1]_R_CR[3]	Video Output Data. These signals represent the 8 MSBs of R/Cr video data. For RGB mode they are red data bits, for YUV444 mode they are Cr (Chroma) data bits, for Y/C mode and BT.656 modes they are unused.	O	L4
VOUT[1]_R_CR[4]	Video Output Data. These signals represent the 8 MSBs of R/Cr video data. For RGB mode they are red data bits, for YUV444 mode they are Cr (Chroma) data bits, for Y/C mode and BT.656 modes they are unused.	O	H2
VOUT[1]_R_CR[5]	Video Output Data. These signals represent the 8 MSBs of R/Cr video data. For RGB mode they are red data bits, for YUV444 mode they are Cr (Chroma) data bits, for Y/C mode and BT.656 modes they are unused.	O	M11
VOUT[1]_R_CR[6]	Video Output Data. These signals represent the 8 MSBs of R/Cr video data. For RGB mode they are red data bits, for YUV444 mode they are Cr (Chroma) data bits, for Y/C mode and BT.656 modes they are unused.	O	L12
VOUT[1]_R_CR[7]	Video Output Data. These signals represent the 8 MSBs of R/Cr video data. For RGB mode they are red data bits, for YUV444 mode they are Cr (Chroma) data bits, for Y/C mode and BT.656 modes they are unused.	O	M10

Table 3-54. Video Output 1 (Digital) Terminal Functions (continued)

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	AAR BALL [4]
VOUT[1]_R_CR[8]	Video Output Data. These signals represent the 8 MSBs of R/Cr video data. For RGB mode they are red data bits, for YUV444 mode they are Cr (Chroma) data bits, for Y/C mode and BT.656 modes they are unused.	O	J2
VOUT[1]_R_CR[9]	Video Output Data. These signals represent the 8 MSBs of R/Cr video data. For RGB mode they are red data bits, for YUV444 mode they are Cr (Chroma) data bits, for Y/C mode and BT.656 modes they are unused.	O	K2
VOUT[1]_VSYNC	Video Output Vertical Sync output. This is the discrete vertical synchronization output. This signal is not used for embedded sync modes.	O	F5

4 Device Configurations

4.1 Control Module Registers

4.2 Boot Modes

The state of the device after boot is determined by sampling the input states of the BTMODE[15:0] pins when device reset ($\overline{\text{POR}}$ or $\overline{\text{RESET}}$) is de-asserted. The sampled values are latched into the CONTROL_STATUS register, which is part of the Control Module. The BTMODE[15:11] values determine the following system boot settings:

- $\overline{\text{RSTOUT\_WD\_OUT}}$ Control
- GPMC CS0 Default Data Bus Width, Wait Enable, and Address/Data Multiplexing

For additional details on BTMODE[15:11] pin functions, see Table 3-12, *Boot Configuration Terminal Functions*.

The BTMODE[4:0] values determine the boot mode order according to Table 4-1, *Boot Mode Order*. The 1st boot mode listed for each BTMODE[4:0] configuration is executed as the primary boot mode. If the primary boot mode fails, the 2nd, 3rd, and 4th boot modes are executed in that order until a successful boot is completed.

The BTMODE[9:5] pins are RESERVED and should be pulled down as indicated in Table 3-12, *Boot Configuration Terminal Functions*.

When the XIP (MUX0), XIP (MUX1), XIP w/ WAiT (MUX0) or XIP w/ WAiT (MUX1) bootmode is selected (see Table 4-1), the sampled value from BTMODE[10] pin is used to select between GPMC pin muxing options shown in Table 4-2, *XIP (on GPMC) Boot Options [Muxed or Non-Muxed]*.

For more detailed information on booting the device, including which pins are used for each boot mode, see the *ROM Code Memory and Peripheral Booting* chapter in the device-specific Technical Reference Manual.

Table 4-1. Boot Mode Order

BTMODE[4:0]	1st	2nd	3rd	4th
00000	RESERVED	RESERVED	RESERVED	RESERVED
00001	UART	XIP w/WAIT (MUX0)(1)(2)	MMC	SPI
00010	UART	SPI	NAND	NANDI2C
00011	UART	SPI	XIP (MUX0)(1)(2)	MMC
00100	RESERVED	SPI	NAND	NANDI2C
00101	RESERVED	RESERVED	RESERVED	RESERVED
00110	RESERVED	RESERVED	RESERVED	RESERVED
00111	RESERVED	MMC	SPI	XIP (MUX1)(1)(2)
01000	RESERVED	RESERVED	RESERVED	RESERVED
01001	RESERVED	RESERVED	RESERVED	RESERVED
01010	RESERVED	RESERVED	RESERVED	RESERVED
01011	RESERVED	RESERVED	RESERVED	RESERVED
01100	RESERVED	RESERVED	RESERVED	RESERVED
01101	RESERVED	RESERVED	RESERVED	RESERVED
01110	RESERVED	RESERVED	RESERVED	RESERVED
01111	Fast XIP (MUX0)(1)	UART	RESERVED	RESERVED
10000	XIP (MUX1)(1)(2)	UART	RESERVED	MMC
10001	XIP w/WAIT (MUX1)(1)(2)	UART	RESERVED	MMC
10010	NAND	NANDI2C	SPI	UART
10011	NAND	NANDI2C	MMC	UART
10100	NAND	NANDI2C	SPI	RESERVED
10101	NANDI2C	MMC	RESERVED	UART
10110	SPI	MMC	UART	RESERVED
10111	MMC	SPI	UART	RESERVED
11000	SPI	MMC	RESERVED	RESERVED
11001	SPI	MMC	RESERVED	RESERVED
11010	XIP (MUX0)(1)(2)	UART	SPI	MMC
11011	XIP w/WAIT (MUX0)(1)(2)	UART	SPI	MMC
11100	RESERVED	RESERVED	RESERVED	RESERVED
11101	RESERVED	RESERVED	RESERVED	RESERVED
11110	RESERVED	RESERVED	RESERVED	RESERVED
11111	Fast XIP (MUX0)(1)	RESERVED	UART	RESERVED

(1) GPMC CS0 eXecute In Place (XIP) boot for NOR/OneNAND/ROM. MUX0/1 refers to the multiplexing option for the GPMC_A[12:0] pins. For more detailed information on booting the device, including which pins are used for each boot mode, see the *ROM Code Memory and Peripheral Booting* chapter in the device-specific Technical Reference Manual.

(2) When the XIP (MUX0), XIP (MUX1), XIP w/ WAiT (MUX0) or XIP w/ WAiT (MUX1) bootmode is selected, the sampled value from BTMODE[10] pin is used to select between GPMC pin configuration options shown in Table 4-2, *XIP (on GPMC) Boot Options*.

4.2.1 XIP (NOR) Boot Options

Table 4-2 shows the XIP (NOR) boot mode GPMC pin configuration options (Option A: BTMODE[10] = 0 and Option B: BTMODE[10] = 1). For Option B, the pull state on select pins is reconfigured to IPD and remains IPD after boot until the user software reconfigures it. In Table 4-2, GPMC_A[1:12] are configured only for Non-Muxed NOR flash. In the case of Muxed NOR Flash, GPMC_D[15:0] act as both address and data lines so configuration of GPMC_A[1:12] in XIP_Mux0 mode and XIP_Mux1 mode doesn't apply for a Muxed NOR flash and those pins are not configured by Boot ROM.

Table 4-2. XIP (on GPMC) Boot Options

SIGNAL NAME	PIN NO.	OTHER CONDITIONS	CONTROLLED I/O FUNCTION DURING XIP (NOR) BOOT			
			BTMODE[10] = 0 [OPTION A]		BTMODE[10] = 1 [OPTION B]	
			PIN FUNCTION	PULL STATE	PIN FUNCTION	PULL STATE
GPMC_CS[0]/*	AC9		GPMC_CS[0]	IPU	GPMC_CS[0]	IPU
GPMC_ADV_ALE/*	AA10	BTMODE[14:13] = 01b or 10b (Mux)	GPMC_ADV_ALE	IPU	GPMC_ADV_ALE	IPU
		BTMODE[14:13] = 00b (Non-Mux)			Default	
GPMC_OE_RE	Y8		GPMC_OE_RE	IPU	GPMC_OE_RE	IPU
GPMC_BE[0]_CLE/GPMC_A[25]/*	Y3		GPMC_BE[0]_CLE	IPD	Default	IPD
GPMC_BE[1]/GPMC_A[24]/*	Y11		Default	IPD	Default	IPD
GPMC_WE	Y5		GPMC_WE	IPU	GPMC_WE	IPU
GPMC_WAIT[0]/GPMC_A[26]/*	W8	BTMODE[15] = 1b (WAIT Used/Enabled)	GPMC_WAIT[0]	IPU	GPMC_WAIT[0]	IPU
		BTMODE[15] = 0b (WAIT Not Used/Disabled)			Default	IPD(1)
GPMC_CLK/*	AB9		GPMC_CLK	IPU	Default	IPU
GPMC_D[15:0]/*	P2, R1, R2, R3, R4, R6, T8, T1, T2, T3, T5, W9, U2, W3, W4, W6		GPMC_D[15:0]	Off	GPMC_D[15:0]	Off
/GPMC_A[27]/GPMC_A[26]/GPMC_A[0]/	AK3	BTMODE[12] = 0b (8-bit Mode)	GPMC_A[0]	IPD	GPMC_A[0]	IPD
		BTMODE[12] = 1b (16-bit Mode)			Default	
/GPMC_A[1:12]/	AK4, AJ4, AL5, AK5, AJ6, AL6, AK6, AJ7, AK7, AE4, AK8, AJ8	XIP_MUX0 Mode	GPMC_A[1:12]	IPD	GPMC_A[1:12]	IPD
		XIP_MUX1 Mode	Default	IPD	Default	IPD
/GPMC_A[1:12]/ (M1)	AD1, AC8, AC5, AC4, A2, B2, C1, C2, D5, H9, J10, B3	XIP_MUX0 Mode	Default	Default	Default	Default
		XIP_MUX1 Mode	GPMC_A[1:12]	Default	GPMC_A[1:12]	Default
/GPMC_A[13:15]/ (M0)	AH8, AG8, AF8		Default	IPD	Default	IPD
/GPMC_A[0]/ (M1)	M8	BTMODE[12] = 0b (8-bit Mode)	Default	IPU	Default	IPU
		BTMODE[12] = 1b (16-bit Mode)				
/GPMC_A[13]/ (M1)	L2	BTMODE[14:13] = 01b or 10b (Mux)	Default	IPU	Default	IPU
		BTMODE[14:13] = 00b (Non-Mux)				IPD(1)
/GPMC_A[14]/ (M1)	L4	BTMODE[14:13] = 01b or 10b (Mux)	Default	IPU	Default	IPU
		BTMODE[14:13] = 00b (Non-Mux)				IPD(1)
/GPMC_A[15]/ (M1)	L6		Default	IPD	Default	IPD
GPMC_A[16:19]/*	M1, M2, M3, M5		Default	IPD	Default	IPD
GPMC_A[20] (M0)	N9		Default	IPU	Default	IPD(1)
GPMC_A[21] (M0)	N1		Default	IPD	Default	IPD
GPMC_A[22] (M0)	N2		Default	IPU	Default	IPD(1)
GPMC_A[23] (M0)	R8		Default	IPD	Default	IPD

(1) After initial power-up the internal pullup (IPU) will be at its default configuration of IPU. During the boot ROM execution, the pull state is reconfigured to IPD and it remains IPD after boot until the user software reconfigures it.

Table 4-2. XIP (on GPMC) Boot Options (continued)

SIGNAL NAME	PIN NO.	OTHER CONDITIONS	CONTROLLED I/O FUNCTION DURING XIP (NOR) BOOT			
			BTMODE[10] = 0 [OPTION A]		BTMODE[10] = 1 [OPTION B]	
			PIN FUNCTION	PULL STATE	PIN FUNCTION	PULL STATE
/GPMC_A[24]/GPMC_A[20]/	AE3		Default	IPU	Default	IPD(1)
/GPMC_A[25]/GPMC_A[21]/	AE2		Default	IPU	Default	IPD(1)
/GPMC_A[26]/GPMC_A[22]/	AE1		Default	IPU	Default	IPD(1)
/GPMC_A[27]/GPMC_A[23]/	AD2		Default	IPU	Default	IPU
GPMC_A[24] (M1)	AC3		Default	IPU	Default	IPU
GPMC_A[25] (M1)	AA12		Default	IPU	Default	IPU

4.2.2 NAND Flash Boot

Table 4-3 lists the device pins that are configured by the ROM for the NAND Flash boot mode.

NOTE: Table 4-3 lists the configuration of the GPMC_CLK pin (pin mux and pull state) in NAND bootmodes.

The NAND flash memory is not XIP and requires shadowing before the code can be executed.

Table 4-3. Pins Used in NAND FLASH Bootmode

SIGNAL NAME	PIN NO.	TYPE	OTHER CONDITIONS
GPMC_CS[0]/*	AC9	O	BTMODE[12] = 0b (8-bit Mode) BTMODE[12] = 1b (16-bit Mode) BTMODE[14:13] = 00b (GPMC CS0 not muxed) BTMODE[15] = 0b (wait disabled)
GPMC_ADV_ALE/*	AA10	O	
GPMC_OE_RE	Y8	O	
GPMC_BE[0]_CLE/GPMC_A[25]/*	Y3	O	
GPMC_BE[1]/GPMC_A[24]/*	Y11	O	
GPMC_WE	Y5	O	
GPMC_WAIT[0]/GPMC_A[26]/*(1)	W8	I	
GPMC_CLK/*	AB9	I/O	
GPMC_D[15:0]/*	P2, R1, R2, R3, R4, R6, T8, T1, T2, T3, T5, W9, U2, W3, W4, W6	I/O	

(1) GPMC_CLK/* is not configured in BTMODE[10] = 1 [OPTION B]

4.2.3 NAND I2C Boot (I2C EEPROM)

Table 4-4 lists the device pins that are configured by the ROM for the NAND I2C boot mode.

Table 4-4. Pins Used in NAND I2C Bootmode

SIGNAL NAME	PIN NO.	TYPE
I2C[0]_SCL	T27	I/O
I2C[0]_SDA	T24	I/O

4.2.4 MMC/SD Cards Boot

Table 4-5 lists the device pins that are configured by the ROM for the MMC/SD boot mode.

Table 4-5. Pins Used in MMC/SD Bootmode

SIGNAL NAME	PIN NO.	TYPE
SD1_CLK	W30	I/O
SD1_CMD/GP0[0] [MUX0]	Y29	I/O
SD1_DAT[0]	W31	I/O
SD1_DAT[1]_SDIRQ	AA30	I/O
SD_DAT[2]_SDRW	U29	I/O
SD1_DAT[3]	Y27	I/O

4.2.5 SPI Boot

Table 4-6 lists the device pins that are configured by the ROM for the SPI boot mode.

Table 4-6. Pins Used in SPI Bootmode

SIGNAL NAME	PIN NO.	TYPE
$\overline{\text{SPI[0]\_SCS[0]}}$	G29	I/O
SPI[0]_D[0] (MISO)	J28	I/O
SPI[0]_D[1] (MOSI)	J27	I/O
SPI[0]_SCLK	N24	I/O

4.2.6 UART Bootmode

Table 4-7 lists the device pins that are configured by the ROM for the UART boot mode.

Table 4-7. Pins Used in UART Bootmode

SIGNAL NAME	PIN NO.	TYPE
UART0_RXD	J26	I
UART0_TXD	E28	O

4.3 Pin Multiplexing Control

Device level pin multiplexing is controlled on a pin-by-pin basis by the MUXMODE bits of the PINCNTL1 – PINCNTL270 registers in the Control Module.

Pin multiplexing selects which one of several peripheral pin functions controls the pin's I/O buffer output data values. Table 4-8 shows the peripheral pin functions associated with each MUXMODE setting for all multiplexed pins. The default pin multiplexing control for almost every pin is to select MUXMODE = 0x0, in which case the pin's I/O buffer is 3-stated.

In most cases, the input from each pin is routed to all of the peripherals that share the pin, regardless of the MUXMODE setting. However, in some cases a constant "0" or "1" value is routed to the associated peripheral when its peripheral function is not selected to control any output pin. For more details on the De-Selected Input State (DSIS), see the columns of each Terminal Functions table (Section 3.3, *Terminal Functions*).

Some peripheral pin functions can be routed to more than one device pin. These types of peripheral pin functions are called Multimuxed and may have different Switching Characteristics and Timing Requirements for each device pin option.

For more detailed information on the Pin Control 1 through Pin Control 270 (PINCNTLx) registers breakout, see Figure 4-1 and Table 4-8.

Figure 4-1. PINCNTL1 – PINCNTL270 (PINCNTLx) Registers Breakout

31	24	23	20	19	18	17	16
RESERVED		RESERVED		RSV	RSV	PLLTYPESEL	PLLUDEN
R - 0000 0000		R - 0000		R/W			

15	8	7	0
RESERVED		MUXMODE[7:0]	
R - 0000 0000		R/W - 0000 0000	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 4-8. PINCNTL1 – PINCNTL270 (PINCNTLx) Registers Bit Descriptions

Bit	Field	Description	Comments
31:20	RESERVED	Reserved. Read only, writes have no effect.	For PINCNTLx register reset value examples, see Table 4-9, *PNICNTLx Register Reset Value Examples*. For the full register reset values of all PINCNTLx registers.
19	RSV	Reserved. This bit ***must*** always be written with the reset (default) value.	
18	RSV	Reserved. This field ***must*** always be written as "1".	
17	PLLTYPSEL	Pullup/Pulldown Type Selection bit 0 = Pulldown (PD) selected 1 = Pullup (PU) selected	
16	PLLUDEN	Pullup/Pulldown Enable bit 0 = PU/PD enabled 1 = PU/PD disabled	
15:8	RESERVED	Reserved. Read only, writes have no effect.	
7:0	MUXMODE[7:0]	MUXMODE Selection bits These bits select the multiplexed mode pin function settings. Values other than those are illegal.	

Table 4-9. PINCNTLx Register Reset Value Examples

HEX ADDRESS RANGE	PINCNTLx REGISTER NAME	Bits 31:24	Bits 23:20	Bit 19	Bit 18	Bit 17	Bit 16	Bits 15:8	Bits 7:0	REGISTER RESET VALUE
		RESERVED	RESERVED	RESERVED	RXACTIVE	PLLTYPESEL	PLLUDEN	RESERVED	MUXMODE[7:0]	
0x4814 0800	PINCNTL1	00h	0h	0	1	1	0	00h	00h	0x0006 0000
0x4814 0804	PINCNTL2	00h	0h	1	1	1	0	00h	00h	0x000E 0000
0x4814 0808	PINCNTL3	00h	0h	1	1	1	0	00h	00h	0x000E 0000
…										
0x4814 0C34	PINCNTL270	00h	0h	1	1	0	0	00h	00h	0x000C 0000

4.4 Handling Unused Pins

When device signal pins are unused in the system, they can be left unconnected unless otherwise noted in the Terminal Functions tables (see Section 3.3). For unused input pins, the internal pull resistor should be enabled, or an external pull resistor should be used, to prevent floating inputs. All supply pins must always be connected to the correct voltage, even when their associated signal pins are unused.

4.5 DeBugging Considerations

4.5.1 Pullup/Pulldown Resistors

Proper board design should ensure that input pins to the device always be at a valid logic level and not floating. This may be achieved via pullup/pulldown resistors. The device features internal pullup (IPU) and internal pulldown (IPD) resistors on most pins to eliminate the need, unless otherwise noted, for external pullup/pulldown resistors.

An external pullup/pulldown resistor needs to be used in the following situations:

- *Boot Configuration Pins*: If the pin is both routed out and 3-stated (not driven), an external pullup/pulldown resistor is ***strongly recommended***, even if the IPU/IPD matches the desired value/state.
- *Other Input Pins*: If the IPU/IPD *does not* match the desired value/state, use an external pullup/pulldown resistor to pull the signal to the opposite rail.

For the boot configuration pins (listed in Section 3.3, *Boot Configuration Terminal Functions*), if they are both routed out and 3-stated (not driven), it is ***strongly recommended*** that an external pullup/pulldown resistor be implemented. Although, internal pullup/pulldown resistors exist on these pins and they may match the desired configuration value, providing external connectivity can help ensure that valid logic levels are latched on these device boot configuration pins. In addition, applying external pullup/pulldown resistors on the boot and configuration pins adds convenience to the user in debugging and flexibility in switching operating modes.

Tips for choosing an external pullup/pulldown resistor:

- Consider the total amount of current that may pass through the pullup or pulldown resistor. Make sure to include the leakage currents of all the devices connected to the net, as well as any internal pullup or pulldown resistors.
- Decide a target value for the net. For a pulldown resistor, this should be below the lowest V_{IL} level of all inputs connected to the net. For a pullup resistor, this should be above the highest V_{IH} level of all inputs on the net. A reasonable choice would be to target the V_{OL} or V_{OH} levels for the logic family of the limiting device; which, by definition, have margin to the V_{IL} and V_{IH} levels.
- Select a pullup/pulldown resistor with the largest possible value; but, which can still ensure that the net will reach the target pulled value when maximum current from all devices on the net is flowing through the resistor. The current to be considered includes leakage current plus, any other internal and external pullup/pulldown resistors on the net.
- For bidirectional nets, there is an additional consideration which sets a lower limit on the resistance value of the external resistor. Verify that the resistance is small enough that the weakest output buffer can drive the net to the opposite logic level (including margin).
- Remember to include tolerances when selecting the resistor value.
- For pullup resistors, also remember to include tolerances on the DV_{DD} rail.

For most systems, a 1-kΩ resistor can be used to oppose the IPU/IPD while meeting the above criteria. Users should confirm this resistor value is correct for their specific application.

For most systems, a 20-kΩ resistor can be used to compliment the IPU/IPD on the boot and configuration pins while meeting the above criteria. Users should confirm this resistor value is correct for their specific application.

For most systems, a 20-kΩ resistor can also be used as an external PU/PD on the pins that have IPUs/IPDs disabled and require an external PU/PD resistor while still meeting the above criteria. Users should confirm this resistor value is correct for their specific application.

For more detailed information on input current (I_I), and the low-/high-level input voltages (V_{IL} and V_{IH}) for the device, see Section 6.4, *Electrical Characteristics Over Recommended Ranges of Supply Voltage and Operating Temperature*.

For the internal pullup/pulldown resistors for all device pins, see the peripheral/system-specific terminal functions table.

5 System Interconnect

The device's various processors, subsystems, and peripherals are interconnected through a switch fabric architecture. The switch fabric is composed of an L3 and L4 interconnect, a switched central resource (SCR), and multiple bridges (for an overview, see Figure 5-1). Not all Initiators in the switch fabric are connected to all Target peripherals. The supported initiator and target connections are designated by a "X" in Table 5-1, *Target/Initiator Connectivity*.

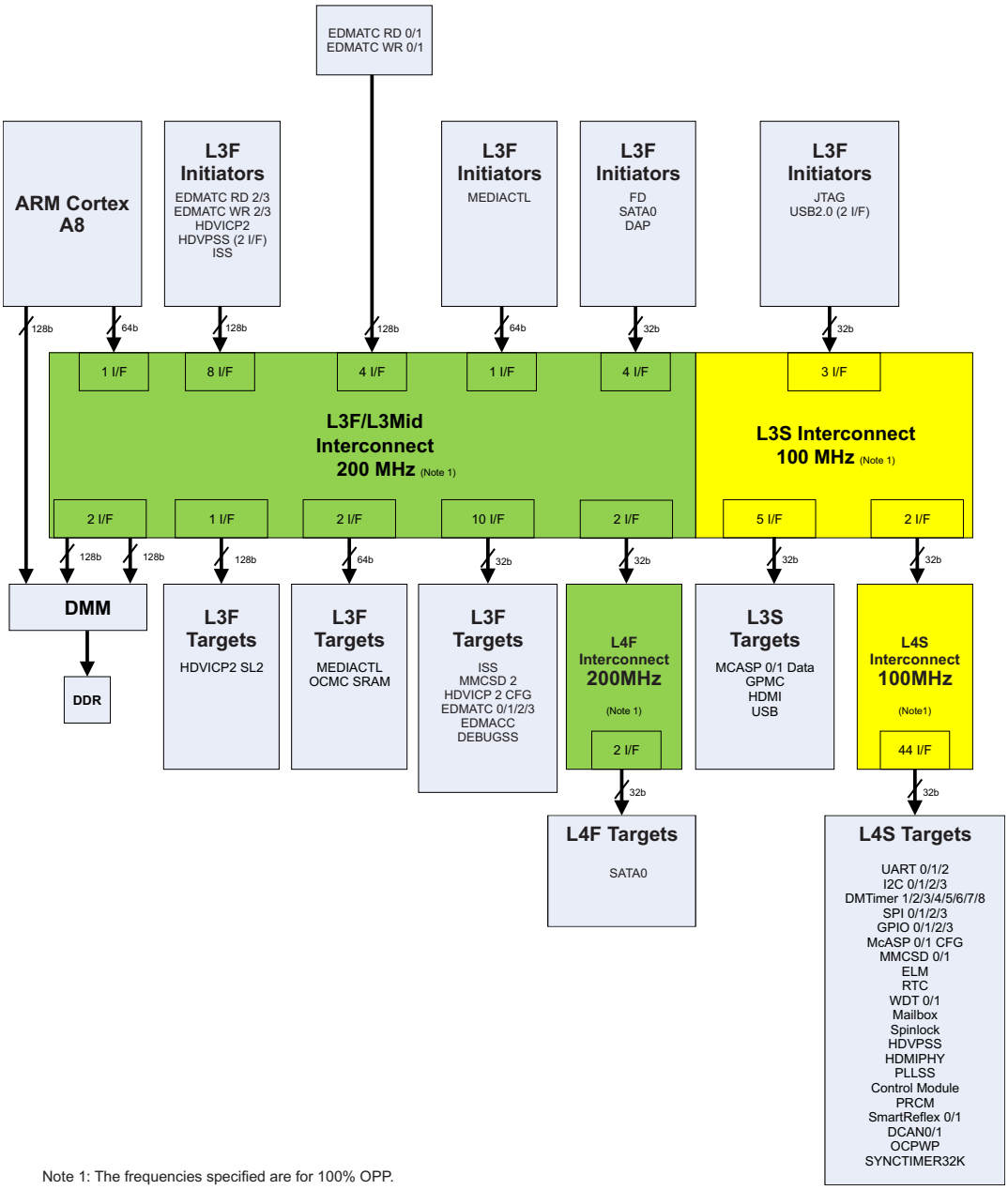


Figure 5-1. System Interconnect

Table 5-1. L3 Master/Slave Connectivity

MASTERS	SLAVES																			
	EDMA DMM Tiler/Lisa0	EDMA DMM Tiler/Lisa1	EDMA DMM ELLA	HDVICP2 SL2	HDVICP2 Hst	Media Controller	GPMC	McASP 0/1	HDMI 1.3 Tx Audio	L4 HS Periph Port 0	L4 HS Periph Port 1	L4 Std Periph Port 0	L4 Std Periph Port 1	L3 Registers	EDMA TPTC0 - 3 CFG	EDMA TPCC	OCMC RAM	USB2.0 CFG	Imaging SS	SD2
ARM M1 (128-bit)			X																	
ARM M2 (64-bit)		X		X	X	X	X	X	X	X		X		X	X	X	X	X	X	X
HDVICP2 VDMA	X																X			
HDVPSS Mstr0	X			X													X			
HDVPSS Mstr1		X		X													X			
SATA0	X			X			X										X			
USB2.0 DMA	X			X																
USB2.0 Queue Mgr	X			X			X										X			
Media Controller	X			X	X		X	X	X	X		X			X	X	X	X		X
DeBug Access Port (DAP)	X			X	X	X	X	X	X		X		X	X	X	X	X	X		
EDMA TPTC0 RD	X			X	X	X	X	X	X		X		X			X	X	X	X	X
EDMA TPTC0 WR		X		X	X	X	X	X	X		X		X			X	X	X	X	X
EDMA TPTC1 RD		X		X	X	X	X	X	X	X		X				X	X	X	X	X
EDMA TPTC1 WR	X			X	X	X	X	X	X	X		X				X	X	X	X	X
EDMA TPTC2 RD		X		X	X	X	X	X	X		X		X			X	X	X	X	X
EDMA TPTC2 WR	X			X	X	X	X	X	X		X		X			X	X	X	X	X
EDMA TPTC3 RD	X			X	X	X	X	X	X	X		X				X	X	X	X	X
EDMA TPTC3 WR		X		X	X	X	X	X	X	X		X				X	X	X	X	X
ISS		X															X			

The L4 interconnect is a non-blocking peripheral interconnect that provides low-latency access to a large number of low-bandwidth, physically-dispersed target cores. The L4 can handle incoming traffic from up to four initiators and can distribute those communication requests to and collect related responses from up to 63 targets.

The device provides two interfaces with L3 interconnect for high-speed and standard peripherals.

Table 5-2. L4 Peripheral Connectivity(1)

L4 PERIPHERALS	MASTERS				
	ARM Cortex-A8 M2 (64-bit)	EDMA TPTC0	EDMA TPTC1	EDMA TPTC2	EDMA TPTC3
L4 Fast Peripherals Port 0/1					
SATA0	Port0	Port1	Port0	Port1	Port0
L4 Slow Peripherals Port 0/1					
I2C0	Port0	Port1	Port0	Port1	Port0
I2C1	Port0	Port1	Port0	Port1	Port0
I2C2	Port0	Port1	Port0	Port1	Port0
I2C3	Port0	Port1	Port0	Port1	Port0
SPI0	Port0	Port1	Port0	Port1	Port0
SPI1	Port0	Port1	Port0	Port1	Port0
SPI2	Port0	Port1	Port0	Port1	Port0
SPI3	Port0	Port1	Port0	Port1	Port0
UART0	Port0	Port1	Port0	Port1	Port0
UART1	Port0	Port1	Port0	Port1	Port0
UART2	Port0	Port1	Port0	Port1	Port0
Timer1	Port0	Port1	Port0	Port1	Port0
Timer2	Port0	Port1	Port0	Port1	Port0
Timer3	Port0	Port1	Port0	Port1	Port0
Timer4	Port0	Port1	Port0	Port1	Port0
Timer5	Port0	Port1	Port0	Port1	Port0
Timer6	Port0	Port1	Port0	Port1	Port0
Timer7	Port0	Port1	Port0	Port1	Port0
Timer8	Port0	Port1	Port0	Port1	Port0
GPIO0	Port0	Port1	Port0	Port1	Port0
GPIO1	Port0	Port1	Port0	Port1	Port0
MMC/SD0/SDIO	Port0	Port1	Port0	Port1	Port0
MMC/SD1/SDIO	Port0	Port1	Port0	Port1	Port0
MMC/SD2/SDIO	Port0	Port1	Port0	Port1	Port0
WDT0	Port0	Port1	Port0	Port1	Port0
RTC	Port0	Port1	Port0	Port1	Port0
SmartReflex0	Port0				
SmartReflex1	Port0				
Mailbox	Port0				
Spinlock	Port0				
HDVPSS	Port0	Port1	Port0	Port1	Port0
PLLSS	Port0				
Control/Top Regs (Control Module)	Port0				
PRCM	Port0				
ELM	Port0				
HDMIPHY	Port0				

(1) X, Port0, Port1 = Connection exists.

Table 5-2. L4 Peripheral Connectivity[(1)] (continued)

L4 PERIPHERALS	MASTERS				
	ARM Cortex-A8 M2 (64-bit)	EDMA TPTC0	EDMA TPTC1	EDMA TPTC2	EDMA TPTC3
DCAN0/1	Port0	Port1	Port0	Port1	Port0
OCPWP	Port0				
McASP0 CFG	Port0	Port1	Port0	Port1	Port0
McASP1 CFG	Port0	Port1	Port0	Port1	Port0
SYNCTIMER32K	Port0	Port1	Port0	Port1	Port0

6 Device Operating Conditions

6.1 Absolute Maximum Ratings (1)(2)

Supply voltage ranges (Steady State):	Core (CVDD, CVDD_ARM, CVDD_HDVICP)	-0.3 V to 1.5 V
	HD-DAC Digital Logic, 1.1V (VDDA_HDDAC_1P1)	-0.5 V to 1.5 V
	I/O, 1.8 V (DVDD_DDR[0], VDDA_1P8, VDDA_ARMPLL_1P8, VDDA_VIDPLL_1P8, VDDA_AUDIOPLL_1P8, VDDA_DDRPLL_1P8, VDDA_L3L4PLL_1P8, VDDA_SATA0_1P8, VDDA_HDMI_1P8, VDDA_USB0_1P8, VDDA_USB1_1P8, VDDA_VDAC_1P8, VDDA_CSI2_1P8, VDDA_HDDACREF_1P8, VDDA_HDDAC_1P8, VDDA_HDVICPPLL_1P8, VDDS_OSC0_1P8, VDDS_OSC1_1P8)	-0.3 V to 2.1 V
	I/O 3.3 V (DVDD, DVDD_GPMC, DVDD_RGMII, DVDD_SD, DVDD_C)	-0.3 V to 4.0 V
	DDR Reference Voltage (VREFSSTL_DDR[0])	-0.3 V to 1.1 V
Input and Output voltage ranges:	V I/O, 1.35-V pins (Steady State)	-0.3 V to DVDD_DDR[0] + 0.3 V
	V I/O, 1.35-V pins (Transient Overshoot/Undershoot)	30% of DVDD_DDR[0] for up to 30% of the signal period
	V I/O, 1.5-V pins (Steady State)	-0.3 V to DVDD_DDR[0] + 0.3 V
	V I/O, 1.5-V pins (Transient Overshoot/Undershoot)	30% of DVDD_DDR[0] for up to 30% of the signal period
	V I/O, 1.8-V pins (Steady State)	-0.3 V to DVDD + 0.3 V -0.3 V to DVDD_x + 0.3 V
	V I/O, 1.8-V pins (Transient Overshoot/Undershoot)	25% of DVDDx for up to 30% of the signal period
	V I/O, 3.3-V pins (Steady State)	-0.3 V to DVDD + 0.3 V -0.3 V to DVDD_x + 0.3 V
	V I/O, 3.3-V pins (Transient Overshoot/Undershoot)	25% of DVDDx for up to 30% of the signal period
Operating junction temperature range, T_J:	Commercial Temperature	0°C to 95°C
Storage temperature range, T_{stg}:		-55°C to 150°C
Component-Level Electrostatic Discharge (ESD) Stress Voltage (3)	ESD-HBM (Human Body Model) (4)	±1000 V
	ESD-CDM (Charged-Device Model) (5)	±250 V
Latch-up Performance (6)	Class II (105ºC)	50 mA

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to their associated VSS or VSSA_x.
(3) Electrostatic discharge (ESD) to measure device sensitivity or immunity to damage caused by electrostatic discharges into the device.
(4) Level listed is the passing level per ANSI/ESDA/JEDEC JS-001. JEDEC document JEP155 states that 500 V HBM allows safe manufacturing with a standard ESD control process, and manufacturing with less than 500 V HBM is possible if necessary precautions are taken. Pins listed as 1000 V may actually have higher performance.
(5) Level listed is the passing level per EIA-JEDEC JESD22-C101E. JEDEC document JEP157 states that 250 V CDM allows safe manufacturing with a standard ESD control process, and manufacturing with less than 250 V CDM is possible if necessary precautions are taken. Pins listed as 250 V may actually have higher performance.
(6) Based on JEDEC JESD78D [*IC Latch-Up Test*].

6.2 Recommended Operating Conditions

PARAMETER			MIN	NOM	MAX	UNIT
CVDD	Supply voltage, Core (Scalable) DVFS only, No AVS	OPP_Nitro	1.28	1.35	1.42	V
		OPP_Turbo	1.28	1.35	1.42	
		120% OPP	1.14	1.20	1.26	
		100% OPP	1.05	1.10	1.16	
CVDD_ARM	Supply voltage, Core ARM (Scalable)	OPP_Nitro	1.28	1.35	1.42	V
		OPP_Turbo	1.28	1.35	1.42	
		120% OPP	1.14	1.20	1.26	
		100% OPP	1.05	1.10	1.16	
CVDD_HDVICP	Supply voltage, Core, HDVICP2 (Scalable)	OPP_Nitro	1.28	1.35	1.42	V
		OPP_Turbo	1.28	1.35	1.42	
		120% OPP	1.14	1.20	1.26	
		100% OPP	1.05	1.10	1.16	
DVDD	Supply voltage, I/O, standard pins(1)	3.3 V	3.14	3.3	3.47	V
		1.8 V	1.71	1.8	1.89	
DVDD_GPMC	Supply voltage, I/O, GPMC pin group	3.3 V	3.14	3.3	3.47	V
		1.8 V	1.71	1.8	1.89	
DVDD_RGMII	Supply voltage, I/O, RGMII pin group	3.3 V	3.14	3.3	3.47	V
		1.8 V	1.71	1.8	1.89	
DVDD_SD	Supply voltage, I/O, SD pin group	3.3 V	3.14	3.3	3.47	V
		1.8 V	1.71	1.8	1.89	
DVDD_C	Supply voltage, I/O, C pin group	3.3 V	3.14	3.3	3.47	V
		1.8 V	1.71	1.8	1.89	
DVDD_DDR[0]	Supply voltage, I/O, DDR[0]	DDR2	1.71	1.8	1.89	V
		DDR3	1.43	1.5	1.58	
		DDR3L	1.28	1.35	1.42	
VDDA_USB_3P3	Supply voltage, I/O, Analog, USB 3.3 V		3.14	3.3	3.47	V
VDDA_1P8 VDDA_x_1P8 VDDS_x_1P8	Supply Voltage, I/O, Analog, (VDDA_1P8, VDDA_ARMPLL_1P8, VDDA_VIDPLL_1P8, VDDA_AUDIOPLL_1P8, VDDA_DDRPLL_1P8, VDDA_L3L4PLL_1P8, VDDA_SATA0_1P8, VDDA_HDMI_1P8, VDDA_USB0_1P8, VDDA_USB1_1P8, VDDA_VDAC_1P8, VDDA_CSI2_1P8, VDDA_HDDACREF_1P8, VDDA_HDDAC_1P8, VDDA_HDVICPPLL_1P8, VDDS_OSC0_1P8, VDDS_OSC1_1P8) **Note:** HDMI, USB0/1, and VDAC relative to their respective VSSA.		1.71	1.8	1.89	V
VDDA_HDDAC_1P1	Supply voltage, I/O, Analog, HD-DAC 1.1 V		1.05	1.1	1.15	V
VSS	Supply Ground (VSS, VSSA_HDMI, VSSA_USB, VSSA_VDAC, VSSA_DEVOSC(2), VSSA_AUXOSC(2))			0		V
$V_{REFSSTL\_DDR[0]}$	IO Reference Voltage, (VREFSSTL_DDR[0])		0.49 * DVDD_DDR[0]	0.50 * DVDD_DDR[0]	0.51 * DVDD_DDR[0]	V
USBx_VBUSIN	USBx VBUS Comparator Input		4.75	5	5.25	V

(1) LVCMOS pins are all I/O pins powered by DVDD, DVDD_GPMC, DVDD_RGMII, DVDD_SD, DVDD_C supplies except for I2C[0] and I2C[1] pins.
(2) When using the internal Oscillators, the oscillator grounds (VSSA_DEVOSC, VSSA_AUXOSC) must be kept separate from other grounds and connected directly to the crystal load capacitor ground.

Recommended Operating Conditions *(continued)*

PARAMETER			MIN	NOM	MAX	UNIT
V_{IH}	High-level input voltage, LVCMOS (JTAG[TCK] pins), 3.3 V[1]		2			V
	High-level input voltage, JTAG[TCK], 3.3 V		2.15			V
	High-level input voltage, JTAG[TCK], 1.8 V		1.45			V
	High-level input voltage, I2C (I2C[0] and I2C[1])		0.7DVDD			V
	High-level input voltage, LVCMOS[1], 1.8 V		0.65DVDDx			V
	High-level input voltage, DDR[0] signals in DDR2 mode		$V_{REFSSTL\_DDR[x]}$ + 0.125			V
	High-level input voltage, DDR[0] signals in DDR3 mode		$V_{REFSSTL\_DDR[x]}$ + 0.1			V
	High-level input voltage, DDR[0] signals in DDR3L mode		$V_{REFSSTL\_DDR[x]}$ + 0.09			V
V_{IL}	Low-level input voltage, LVCMOS[1], 3.3 V				0.8	V
	Low-level input voltage, JTAG[TCK]				0.45	V
	Low-level input voltage, I2C (I2C[0] and I2C[1])				0.3DVDDx	V
	Low-level input voltage, LVCMOS[1], 1.8 V				0.35DVDDx	V
	Low-level input voltage, DDR[0] signals in DDR2 mode				$V_{REFSSTL\_DDR[x]}$ - 0.125	V
	Low-level input voltage, DDR[0] signals in DDR3 mode				$V_{REFSSTL\_DDR[x]}$ - 0.1	V
	Low-level input voltage, DDR[0] signals in DDR3L mode				$V_{REFSSTL\_DDR[x]}$ - 0.09	V
I_{OH}	High-level output current	6 mA I/O buffers			-6	mA
		DDR[0] buffer @ 50-Ω impedance setting			-8	mA
I_{OL}	Low-level output current	6 mA I/O buffers			6	mA
		DDR[0] buffer @ 50-Ω impedance setting			8	mA
V_{ID}	Differential input voltage (SERDES_CLKN/P), [AC coupled]		0.250		2.0	V
t_t	Transition time, 10% - 90%, All inputs (unless otherwise specified in the *Electrical Data/Timing* sections of each peripheral)				0.25P or 10[3]	ns
T_J	Operating junction temperature range[4]	Commercial Temperature (default)	0		95	°C

(3) Whichever is smaller. P = the period of the applied signal. Maintaining transition times as fast as possible is recommended to improve noise immunity on input signals.
(4) For more detailed information on estimating junction temps within systems, see the *IC Package Thermal Metrics* Application Report (Literature Number: SPRA953).

6.3 Reliability Data[1]

The information in this table is provided solely for convenience and does not extend or modify the warranty provided under TI's standard terms and conditions for TI semiconductor products.

Operating Condition	CVDD[2]	CVDD_ARM[2]	CVDD_HDVICP[2]	Commercial Junction Temp. (T_J)	Lifetime (POH)[3]
Nitro	1.35 V ± 5%	1.35 V ± 5%	1.35 V ± 5%	95ºC	55K
Turbo	1.35 V ± 5%	1.35 V ± 5%	1.35 V ± 5%	95ºC	59K
OPP120	1.20 V ± 5%	1.20 V ± 5%	1.20 V ± 5%	95ºC	100K
OPP100	1.10 V ± 5%	1.10 V ± 5%	1.10 V ± 5%	95ºC	100K

(1) Logic functions and parameter values are not ensured out of the range specified in the recommended operating conditions. The above notations cannot be deemed a warranty or deemed to extend or modify the warranty under TI's standard terms and conditions for TI semiconductor products.
(2) Voltage specification at the device package pin.
(3) Power-on-hours (POH) represent device operation under the specified nominal conditions continuously for the duration of the calculated lifetime. If actual application results in a system that operates at conditions less than the limits, the resulting POH may increase.

6.4 Electrical Characteristics Over Recommended Ranges of Supply Voltage and Operating Temperature (Unless Otherwise Noted)

PARAMETER		TEST CONDITIONS(1)	MIN	TYP	MAX	UNIT
V_{OH}	Low/Full speed: USBx_DM and USBx_DP		2.8		VDDA_USB_3P3	V
	High speed: USBx_DM and USBx_DP		360		440	mV
	High-level output voltage, LVCMOS(2) (3.3-V I/O)	3.3 V, DVDDx = MIN, I_{OH} = MAX	2.4			V
	High-level output voltage, LVCMOS(2) (1.8-V I/O)	1.8 V, DVDDx = MIN, I_{OH} = MAX	1.26			V
	High-level output voltage, DDR[0] signals in DDR2 mode	1.8 V, I_{OL} = 6mA, 50 ohm load	DVDD_DDR[0] - 0.4			V
	HIgh-level output voltage, DDR[0] signals in DDR3 mode	1.5 V, I_{OL} = 6mA, 50 ohm load	DVDD_DDR[0] - 0.4			V
	HIgh-level output voltage, DDR[0] signals in DDR3L mode	1.35 V, I_{OL} = 6mA, 50 ohm load	DVDD_DDR[0] - 0.4			V
V_{OL}	Low/Full speed: USBx_DM and USBx_DP		0.0		0.3	V
	High speed: USBx_DM and USBx_DP		-10		10	mV
	Low-level output voltage, LVCMOS(2) (3.3-V I/O)	3.3 V, DVDDx = MAX, I_{OL} = MAX			0.4	V
	Low-level output voltage, LVCMOS(2) (1.8-V I/O)	1.8 V, DVDDx = MAX, I_{OL} = MAX			0.4	V
	Low-level output voltage, I2C (I2C[0], I2C[1])	1.8/3.3 V, I_{OL} = 4mA			0.4	V
	Low-level output voltage, DDR[0] signals in DDR2 mode	1.8 V, I_{OL} = 6mA, 50 ohm load			0.4	V
	Low-level output voltage, DDR[0] signals in DDR3 mode	1.5 V, I_{OL} = 6mA, 50 ohm load			0.4	V
	Low-level output voltage, DDR[0] signals in DDR3L mode	1.35 V, I_{OL} = 6mA, 50 ohm load			0.4	V
	LDOs (applies to all LDOCAP_x pins)				1.5	V

(1) For test conditions shown as MIN, MAX, or TYP, use the appropriate value specified in the recommended operating conditions table.
(2) LVCMOS pins are all I/O pins powered by DVDD, DVDD_GPMC, DVDD_RGMII, DVDD_SD, DVDD_C supplies except for I2C[0] and I2C[1] pins.

Electrical Characteristics Over Recommended Ranges of Supply Voltage and Operating Temperature (Unless Otherwise Noted) *(continued)*

PARAMETER		TEST CONDITIONS(1)	MIN	TYP	MAX	UNIT
I_I(3)	Input current, LVCMOS(2), 3.3 V mode	$0 < V_I <$ DVDDx, 3.3 V pull disabled	-20		20	µA
		$0 < V_I <$ DVDDx, 3.3 V pulldown enabled(4)	20	100	300	µA
		$0 < V_I <$ DVDDx, 3.3 V pullup enabled(4)	-20	-100	-300	µA
	Input current, LVCMOS(2), 1.8 V mode	$0 < V_I <$ DVDDx, 1.8 V pull disabled	-5		5	µA
		$0 < V_I <$ DVDDx, 1.8 V pulldown enabled(4)	50	100	200	µA
		$0 < V_I <$ DVDDx, 1.8 V pullup enabled(4)	-50	-100	-200	µA
	Input current, I2C (I2C[0], I2C[1])	3.3 V mode	-20		20	µA
		1.8 V mode	-5		5	µA
I_{OZ}(5)	I/O Off-state output current	3.3 V mode, pull enabled	-300		300	µA
		3.3 V mode, pull disabled	-20		20	µA
		1.8 V mode, pull enabled	-200		200	µA
		1.8 V mode, pull disabled	-5		5	µA
C_I	Input capacitance LVCMOS(2)				12	pF
C_o	Output capacitance LVCMOS(2)				12	pF

(3) I_I applies to input-only pins and bi-directional pins. For input-only pins, I_I indicates the input leakage current. For bi-directional pins, I_I indicates the input leakage current and off-state (Hi-Z) output leakage current.
(4) Applies only to pins with an internal pullup (IPU) or pulldown (IPD) resistor.
(5) I_{OZ} applies to output-only pins, indicating off-state (Hi-Z) output leakage current.

7 Power, Reset, Clocking, and Interrupts

7.1 Power, Reset and Clock Management (PRCM) Module

The PRCM module is the centralized management module for the power, reset, and clock control signals of the device. It interfaces with all the components on the device for power, clock, and reset management through power-control signals. It integrates enhanced features to allow the device to adapt energy consumption dynamically, according to changing application and performance requirements. The innovative hardware architecture allows a substantial reduction in leakage current.

The PRCM module is composed of two main entities:

- Power reset manager (PRM): Handles the power, reset, wake-up management, and system clock source control (oscillator)
- Clock manager (CM): Handles the clock generation, distribution, and management.

For more details on the PRCM, see the *Power, Reset, and Clock Management (PRCM) Module* chapter in the device-specific Technical Reference Manual.

7.2 Power

7.2.1 Voltage and Power Domains

Every Module within the device belongs to a Core Logic Voltage Domain, Memory Voltage Domain, and a Power Domain (see Table 7-1).

Table 7-1. Voltage and Power Domains

CORE LOGIC VOLTAGE DOMAIN	MEMORY VOLTAGE DOMAIN	POWER DOMAIN	MODULE(S)
ARM_L	ARM_M	ALWAYS ON	ARM Cortex-A8 Subsystem, SmartReflex Sensor 0
CORE_L	CORE_M		HDMI, DCAN0/1, DMM, EDMA, ELM, DDR, GPIO Banks 0/1/2/3, GPMC, I2C0/1/2/3, IPC, MCASP0/1, OCMC SRAM, PRCM, RTC, SATA0, SD/MMC0/1/2, SPI01/2/3, Timer1/2/3/4/5/6/7/8, UART0/1/2, USB0/1, WDT0, System Interconnect, JTAG, Media Controller, ISS, SmartReflex Control Module 0/1, SmartReflex Sensor 1
		HDVPSS	HDVPSS, SD-DAC, HD-DAC
HDVICP_L	HDVICP_M	HDVICP	HDVICP2, SmartReflex Sensor 2

7.2.1.1 Core Logic Voltage Domains

The device contains three Core Logic Voltage Domains. These domains define groups of Modules that share the same supply voltage for their core logic. Each Core Logic Voltage Domain is powered by a dedicated supply voltage rail that can be independently scaled using SmartReflex technology to trade off power versus performance. Table 7-2 shows the mapping between the Core Logic Voltage Domains and their associated supply pins.

Table 7-2. Core Logic Voltage Domains and Supply Pin Associations

CORE LOGIC VOLTAGE DOMAIN	SUPPLY PIN NAME
ARM_L	CVDD_ARM
CORE_L	CVDD
HDVICP_L	CVDD_HDVICP

Note: A regulated supply voltage ***must*** be supplied to each Core Logic Voltage Domain at all times, regardless of the Core Logic Power Domain states.

7.2.1.2 Power Domains

The device contains four Power Domains which supply power to both the Core Logic and SRAM within their associated modules. Each Power Domain, except for the ALWAYS ON domain, has an internal power switch that can completely remove power from that domain. All power switches are turned "OFF" by default after reset, and software can individually turn them "ON/OFF" via Control Module registers.

Note: All Modules within a Power Domain are unavailable when the domain is powered "OFF". For instructions on powering "ON/OFF" the Power domains, see the *Power, Reset, and Clock Management (PRCM) Module* chapter of the device-specific *Technical Reference Manual.*

7.2.2 SmartReflex™ [Currently Not Supported]

The device contains SmartReflex modules that help to minimize power consumption on the Core Logic Voltage Domains by using external variable-voltage power supplies. Based on the device process, temperature, and desired performance, the SmartReflex modules advise the host processor to raise or lower the supply voltage to each domain for minimal power consumption.

The communication link between the host processor and the external regulators is a system-level decision and can be accomplished using GPIOs, I2C, SPI, or other methods. The following sections briefly describe the two major techniques employed by SmartReflex: Dynamic Voltage Frequency Scaling (DVFS) and Adaptive Voltage Scaling (AVS).

7.2.2.1 Dynamic Voltage Frequency Scaling (DVFS) [Currently Supports Only Discrete OPPs]

Each device Core Logic Voltage Domain can be run independently at one of several Operating Performance Points (OPPs). An OPP for a specific Core Logic Voltage Domain is defined by: (1) maximum frequencies of operation for Modules within the Domain and (2) an associated supply voltage range. Trading off power versus performance, OPPs with lower maximum frequencies also have lower voltage ranges for power savings.

The OPP for a domain can be changed in real-time without requiring a reset. This feature is called Dynamic Voltage Frequency Scaling (DVFS) Table 7-3 contains a list of voltage ranges and maximum module frequencies for the OPPs of each Core Logic Voltage Domain.

NOTE

Not all devices support all OPP frequencies.

Table 7-3. Device Operating Points (OPPs)

OPP	CORE LOGIC VOLTAGE DOMAINS						
	ARM	HDVICP2	CORE				
	Cortex A8 (MHz)	HDVICP2	HDVPSS (MHz)	ISS (MHz)	Media Ctlr. (MHz)	L3/L4, Core (MHz)	DDR (MHz)(1)
100%(1.1 V) (AAR0x)	600	220	200	400	200	200	400
120% (1.2 V) (AAR0x)	720	290	200	400	200	200	400
Turbo (1.35 V) (AAR1x)	970	410	240	480	240	240	533
Nitro (1.35 V) (AAR2x)	1000	450	260	560	280	240	533

(1) All DDR access ***must*** be suspended prior to changing the DDR frequency of operation.

Although the OPP for each Core Logic Voltage Domain is independently selectable, not all combinations of OPPs are supported. Table 7-4 marks the supported ARM OPPs for a given CORE OPP.

Table 7-4. Supported OPP Combinations(1)

CORE	ARM				HDVICP2			
	Nitro	Turbo	OPP120	OPP100	Nitro	Turbo	OPP120	OPP100
Nitro	X				X			
Turbo		X				X		
OPP120			X	X			X	X
OPP100				X				X

(1) "X" denotes supported combinations.

7.2.2.2 Adaptive Voltage Scaling [Currently Not Supported]

As mentioned in Section 7.2.2.1, *Dynamic Voltage Frequency Scaling (DVFS)* above, every OPP has an associated voltage range. Based on the silicon process, temperature, and chosen OPP, the SmartReflex modules guide software in adjusting the Core Logic Voltage Domain supply voltage (CVDD) within these ranges. This technique is called Adaptive Voltage Scaling (AVS). AVS occurs continuously and in real-time, helping to minimize power consumption in response to changing operating conditions.

7.2.3 Memory Power Management

In order to reduce SRAM leakage, many SRAM blocks can be switched from ACTIVE mode to SHUTDOWN mode. When SRAM is put in SHUTDOWN mode, the voltage supplied to it is automatically removed and all data in that SRAM is lost.

All SRAM located in a switchable power domain (all domains except ALWAYS_ON) automatically enters SHUTDOWN mode whenever its associated power domain goes into the "OFF" state. The SRAM returns to the ACTIVE state when the corresponding Power Domain returns to the "ON" state.

In addition, the following SRAM within the ALWAYS_ON Power Domain can also be independently put into SHUTDOWN by programming the x_MEM_PWRDN registers in the Control Module:

- Media Controller SRAM
- OCMC SRAM

7.2.4 SERDES_CLKP/N LDO

The SERDES_CLKP/N input buffers are powered by an internal LDO which is programmed through the REFCLK_LJCBLDO_CTRL register in the Control Module.

7.2.5 Dual Voltage I/Os

The device supports dual voltages on some of its I/Os. These I/Os are partitioned into the following groups, and each group has its own dedicated supply pins: DVDD, DVDD_GPMC, DVDD_C, and DVDD_SD. The supply voltage for each group can be independently powered with either 1.8 V or 3.3 V.

For the mapping between pins and power groups, see Section 3.3, *Terminal Functions* of the datasheet.

In addition, the I/O voltage on the DDR interface is independently selectable between 1.35 V, 1.5 V or 1.8 V to support various DDR device types.

7.2.6 I/O Power-Down Modes

On the device, there are power-down modes available for the following PHYs:

- Video DACs
- DDR
- USB
- HDMI
- CSI2
- SATA

When a PHY controller is in a power domain that is to be turned "OFF", software must configure the corresponding PHY into power-down mode, prior to putting the power domain in the "OFF" state.

7.2.7 Standby and Deep Sleep Modes

The device supports Low-Power Standby and Deep-Sleep Modes as described below.

Standby Mode is defined as a state in which:

- All switchable power domains are in "OFF" state
- The ARM Cortex-A8 is executing an IDLE loop at its lowest frequency of operation
- All functional blocks not needed for a given application are clock gated

Deep Sleep Mode is defined to be the same as Standby Mode, with the addition of gating the crystal oscillator to further eliminate all active power. The device core voltages can be reduced for optimal power savings.

For detailed instructions on entering and exiting from Standby and Deep Sleep Modes, see the *Power, Reset, and Clock Management (PRCM) Module* chapter in the device-specific Technical Reference Manual.

7.2.8 Supply Sequencing

The device power supplies are organized into five Supply Sequencing Groups:

1. CVDD Core Logic supply (CVDD)
2. All CVDD_x supplies (CVDD_ARM and CVDD_HDVICP)
3. All 1.35-/1.5-/1.8-V DVDD_DDR[0] Supplies (1.35 V for DDR3L, 1.5 V for DDR3, 1.8 V for DDR2)
4. All 1.8-V Supplies (DVDD_x, VDDA_x_1P8, VDDA_1P8)
5. All 3.3-V Supplies (DVDD, DVDD_x, DVDD_C, VDDA_x_3P3)

To ensure proper device operation, a specific power-up and power-down sequence must be followed. Some TI power-supply devices include features that facilitate these power sequencing requirements — for example, TI's TPS659113 integrated PMIC. For more information on TI power supplies and their features, visit www.ti.com/processorpower.

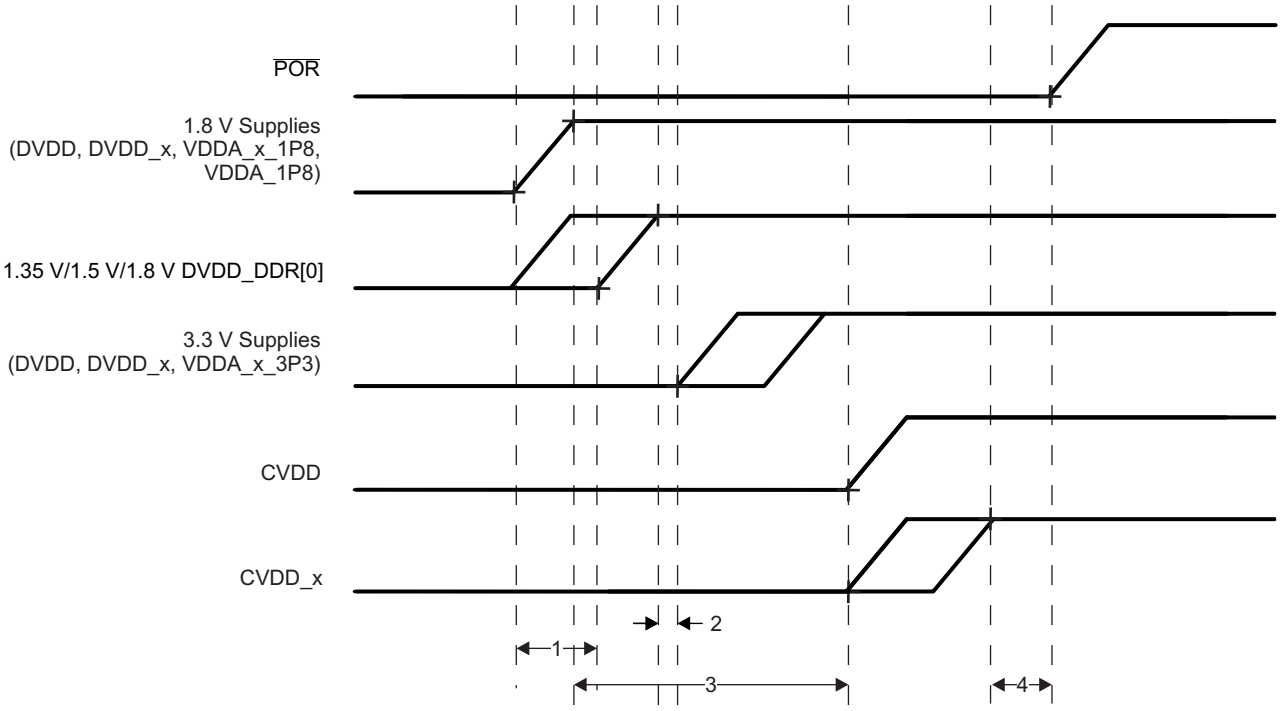
7.2.8.1 Power-Up Sequence

For proper device operation, the following power-up sequence in Table 7-5 and Figure 7-1 ***must*** be followed.

Table 7-5. Power-Up Sequence Ramping Values

NO.	DESCRIPTION	MIN	MAX	UNIT
1	1.8 V supplies to 1.35-/1.5-/1.8-V DVDD_DDR[x] supplies	0 (1)		ms
2	DVDD_DDR supplies stable to 3.3 V supplies ramp start	0 (2)		ms
3	1.8 V supplies stable to CVDD, CVDD_x variable supplies ramp start	0 (1)		ms
4	All supplies valid to power-on-reset ($\overline{\text{POR}}$ high)	4 096		Master Clocks

(1) The 1.8 V supplies ***must*** be ≥ 1.35-/1.5-/1.8-V DVDD_DDR[x] and CVDD, CVDD_x variable supplies.
(2) Both 1.8 V and DVDD_DDR[x] supplies must be powered up and stable prior to starting the ramp of the 3.3 V supplies.



Both 1.8 V and DVDD_DDR[x] supplies must be powered up and stable prior to starting the ramp of the 3.3 V supplies.
CVDD powered-up coincidently or prior to CVDD_ARM and CVDD_HDVICP supplies.

Figure 7-1. Power-Up Sequence

7.2.8.2 Power-Down Sequence

For proper device operation, the following power-down sequence in Table 7-6, Figure 7-2, Figure 7-3, and Figure 7-4 ***must*** be followed.

Table 7-6. Power-Down Sequence Ramping Values

NO.	DESCRIPTION	MIN	MAX	UNIT
5	CVDD, CVDD_x variable supplies to 1.8 V supplies	0		ms
6	1.35-/1.5-/1.8-V DVDD_DDR[x] supplies to 1.8 V supplies	0		ms
7	3.3 V supplies to 1.8 V supplies	(1)	(1)	ms
8	CVDD_x supplies to CVDD supply	(2)	(2)	ms

(1) The 3.3 V supplies ***must*** never be more than 2 V above the 1.8 V supplies (see Figure 7-3).
(2) The CVDD supply must be powered down coincidentally or after CVDD_ARM and CVDD_HDVICP supplies (see Figure 7-4).

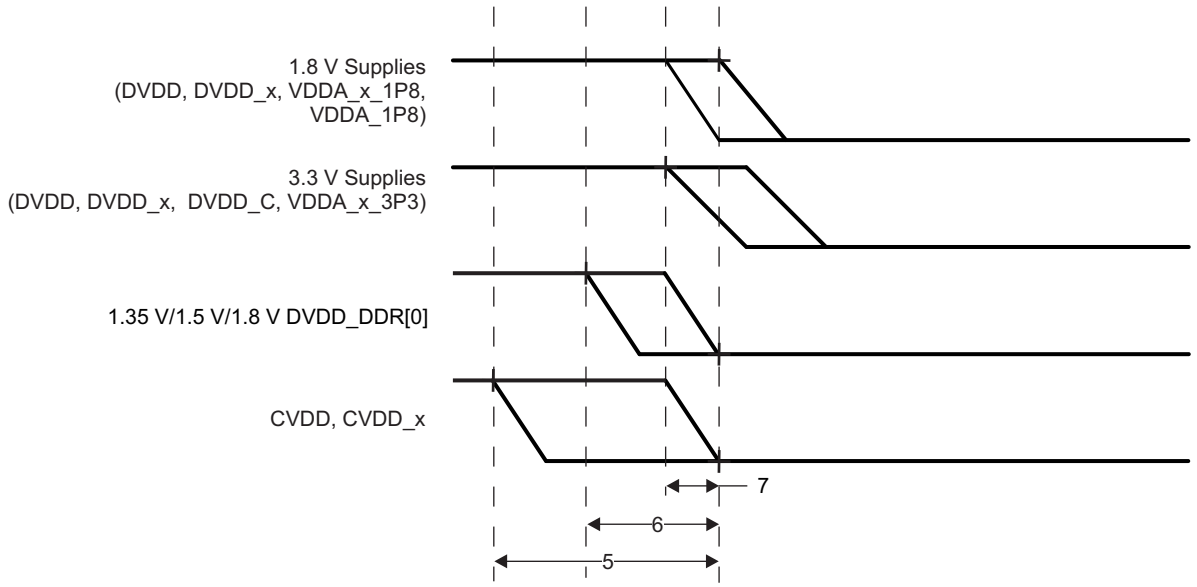
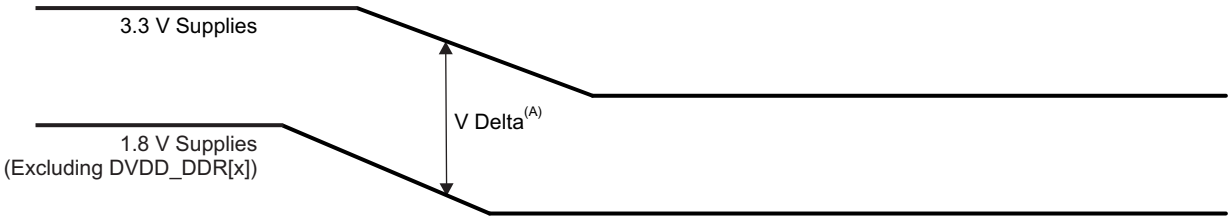


Figure 7-2. Power-Down Sequence



A. V Delta Max = 2 V.

Figure 7-3. 3.3 V Supplies Falling After 1.8 V Supplies Delta

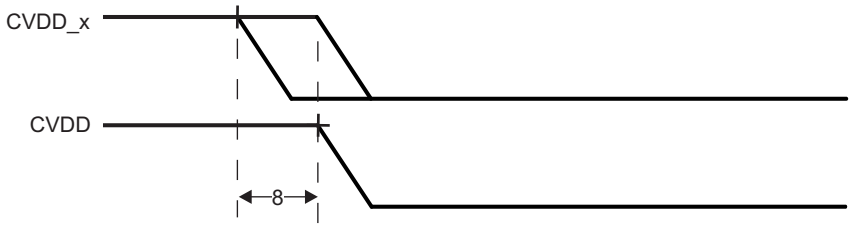


Figure 7-4. CVDD and CVDD_x Power-Down Sequence

7.2.9 Power-Supply Decoupling

7.2.9.1 Analog and PLL

PLL and Analog supplies benefit from filters or ferrite beads to keep the noise from causing problems. The minimum recommendation is a ferrite bead along with at least one capacitor on the device side of the bead. An additional recommendation is to add one capacitor just before the bead to form a Pi filter. The filter needs to be as close as possible to the device pin, with the device side capacitor being the most important component to be close to the device pin. PLL pins close together can be combined on the same supply, but analog pins should all have their own filters. PLL pins farther away from each other may need their own filtered supply.

7.2.9.2 Digital

Recommended capacitors for power supply decoupling are all 0.1uF in the smallest body size that can be used. Capacitors are more effective in the smallest physical size to limit lead inductance. For example, 0201 sized capacitors are better than 0402 sized capacitors, and so on. TI recommends using capacitors no larger than 0402. Place at least one capacitor for every two power pins. For those power pins that have only one pin, a capacitor is still required. Place one bulk (10 uF or larger) capacitor for every 10 or so power pins as closely as possible to the chip. These larger caps do not need to be under the chip footprint.

Pay special attention not to put so much capacitance on the supply that it slows the start-up voltage ramp enough to change the power sequencing order. Also be sure to verify that the main chip reset is low until after all supplies are at their correct voltage and stable.

DDR peripheral related supply capacitor numbers are provided in Section 8.12, *DDR2/DDR3/DDR3L Memory Controller*.

7.3 Reset

7.3.1 System-Level Reset Sources

The device has several types of system-level resets. Table 7-7 lists these reset types, along with the reset initiator, and the effects of each reset on the device.

Table 7-7. System-Level Reset Types

TYPE	INITIATOR	RESETS ALL MODULES, EXCLUDING EMULATION, PLL AND CLOCK CONFIG	RESETS EMULATION	PLL AND CLOCK CONFIG	LATCHES BOOT PINS	ASSERTS RSTOUT_WD_OUT PIN
Power-on Reset (POR)	POR pin	Yes	Yes	Yes	Yes	Optional(1)(2)
External Warm Reset	RESET pin	Yes	No	No	Yes	Optional(1)(2)
Emulation Warm Reset	On-Chip Emulation Logic	Yes	No	No	No	Optional(1)
Watchdog Reset	Watchdog Timer	Yes	No	No	No	Yes
Software Global Cold Reset	Software	Yes	Yes	Yes	No	Optional(1)
Software Global Warm Reset	Software	Yes	No	No	No	Optional(1)
Test Reset	TRST pin	No	Yes	No	No	No

(1) RSTOUT_WD_OUT pin asserted only if BTMODE[11] was latched as "0" when coming out of reset.
(2) While POR and/or RESET is asserted, the RSTOUT_WD_OUT pin is 3-stated and the internal pull resistor is disabled; therefore, an external pullup/pulldown can be used to set the state of this pin (high/low) while POR and/or RESET is asserted. For more detailed information on external PUs/PDs, see Section 4.5.1, *Pullup/Pulldown Resistors*.

7.3.2 Power-on Reset (POR pin)

Power-on Reset (POR) is initiated by the POR pin and is used to reset the entire chip, including the Test and Emulation logic. POR is also referred to as a cold reset since it is required to be asserted when the device goes through a power-up cycle. However, a device power-up cycle is not required to initiate a Power-on Reset.

The following sequence ***must*** be followed during a Power-on Reset:

1. Wait for the power supplies to reach normal operating conditions while keeping the POR pin asserted.
2. Wait for the input clock sources DEV_CLKIN, AUX_CLKIN, and SERDES_CLKN/P to be stable (if used by the system) while keeping the POR pin asserted (low).
3. Once the power supplies and the input clock sources are stable, the POR pin must remain asserted (low) [see Section 7.3.16, *Reset Electrical Data/Timing*]. Within the low period of the POR pin, the following happens:
   (a) All pins except Emulation pins enter a Hi-Z mode and the associated pulls, if applicable, will be enabled.
   (b) The PRCM asserts reset to all modules within the device.
   (c) The PRCM begins propagating these clocks to the chip with the PLLs in BYPASS mode.
4. The POR pin may now be de-asserted (driven high). When the POR pin is de-asserted (high):
   (a) The BTMODE[15:0] pins are latched.
   (b) Reset to the ARM Cortex-A8 and Modules without a local processor is de-asserted.
   (c) RSTOUT_WD_OUT is briefly asserted if BTMODE[11] was latched as "0".
   (d) The clock, reset, and power-down state of each peripheral is determined by the default settings of the PRCM.
   (e) The ARM Cortex-A8 begins executing from the Boot ROM.

7.3.3 External Warm Reset (RESET pin)

An external warm reset is activated by driving the RESET pin active-low. This resets everything in the device, except for the Test and Emulation logic. An emulator session stays alive during warm reset.

The following sequence ***must*** be followed during a warm reset:

1. Power supplies and input clock sources should already be stable.
2. The RESET pin must be asserted (low)[see Section 7.3.16, *Reset Electrical Data/Timing*]. Within the low period of the RESET pin, the following happens:
   (a) All pins, except Test and Emulation pins, enter a Hi-Z mode and the associated pulls, if applicable, will be enabled.
   (b) The PRCM asserts reset to all modules within the device, except for the Test and Emulation logic, PLL, and Clock configuration.
3. The RESET pin may now be de-asserted (driven high). When the RESET pin is de-asserted (high):
   (a) The BTMODE[15:0] pins are latched.
   (b) Reset to the ARM Cortex-A8 and modules without a local processor is de-asserted, with the exception of Test and Emulation logic, PLL, and Clock configuration.
   (c) RSTOUT_WD_OUT is asserted [see Section 7.3.16, *Reset Electrical Data/Timing*], if BTMODE[11] was latched as "0".
   (d) The clock, reset, and power-down state of each peripheral is determined by the default settings of the PRCM.
   (e) The ARM Cortex-A8 begins executing from the Boot ROM.

7.3.4 Emulation Warm Reset

An Emulation Warm Reset is activated by the on-chip Emulation Module. It has the same effect and requirements as an External Warm Reset (RESET), with the following exceptions:

- BTMODE[15:0] pins are not re-latched
- RSTOUT_WD_OUT is not 3-stated and is actively driven based on the value previously latched on the BTMODE[11] pin.

The emulator initiates an Emulation Warm Reset via the ICEPICK module. To invoke the Emulation Warm Reset via the ICEPICK module, the user can perform the following from the Code Composer Studio™ IDE menu: Target -> Reset -> System Reset.

7.3.5 Watchdog Reset

A Watchdog Reset is initiated when the Watchdog Timer counter reaches zero. It has the same effect and requirements as an External Warm Reset (RESET pin), with the following exceptions:

- BTMODE[15:0] pins are not re-latched
- RSTOUT_WD_OUT is not 3-stated and is actively driven based on the value previously latched on the BTMODE[11] pin.

In addition, a Watchdog Reset always results in RSTOUT_WD_OUT being asserted, regardless of whether the BTMODE[11] pin was latched as "0" or "1".

7.3.6 Software Global Cold Reset

A Software Global Cold Reset is initiated under software control. It has the same effect and requirements as a POR Reset, with the following exceptions:

- BTMODE[15:0] pins are not re-latched
- RSTOUT_WD_OUT is not 3-stated and is actively driven based on the value previously latched on the BTMODE[11] pin.

Software initiates a Software Global Cold Reset by writing a "1" to the RST_GLOBAL_COLD_SW bit in the PRM_RSTCTRL register in the PRCM.

For more detailed information on the PRM_RSTCTRL register, see the PRCM Registers section of the *Power, Reset, and Clock Management (PRCM) Module* chapter in the device-specific Technical Reference Manual.

7.3.7 Software Global Warm Reset

A Software Global Warm Reset is initiated under software control. It has the same effect and requirements as a External Warm Reset (RESET pin), with the following exceptions:

- BTMODE[15:0] pins are not re-latched
- RSTOUT_WD_OUT is not 3-stated and is actively driven based on the value previously latched on the BTMODE[11] pin.

Software initiates a Software Global Warm Reset by writing a "1" to the RST_GLOBAL_WARM_SW bit in the PRM_RSTCTRL register in the PRCM.

For more detailed information on the PRM_RSTCTRL register, see the PRCM Registers section of the *Power, Reset, and Clock Management (PRCM) Module* chapter in the device-specific Technical Reference Manual.

7.3.8 Test Reset (TRST pin)

A Test Reset is activated by the emulator asserting the TRST pin. The only effect a Test Reset has is to reset the Test and Emulation Logic.

7.3.9 Local Reset

The Local Reset for various Modules within the device is controlled by programming the PRCM and/or the Peripheral Module's internal registers. Only the associated Module is reset when a Local Reset is asserted, leaving the rest of the device unaffected.

For more details on Peripheral Local Resets, see the Reset Management section of the *Power, Reset, and Clock Management (PRCM) Module* chapter in the device-specific Technical Reference Manual.

7.3.10 Reset Priority

If any of the above reset sources occur simultaneously, the device only processes the highest-priority reset request. The reset request priorities, from high-to-low, are as follows:

1. Power-on Reset (POR)
2. Test Reset (TRST)
3. External Warm Reset (RESET pin)
4. Emulation Warm Resets
5. Watchdog Reset
6. Software Global Cold/Warm Resets

7.3.11 Reset Status Register

The Reset Status Register (PRM_RSTST) contains information about the last reset that occurred in the system. For more information on this register, see the *Power, Reset, and Clock Management (PRCM) Module* chapter in the device-specific Technical Reference Manual.

7.3.12 RSTOUT_WD_OUT Pin

The RSTOUT_WD_OUT pin reflects device reset status and is de-asserted (high) when the device is out reset. This output will always be asserted when a Watchdog Timer reset (Watchdog Reset) occurs. In addition, this output is always 3-stated and the internal pull resistor is disabled on this pin while POR and/or RESET is asserted; therefore, an external pullup/pulldown can be used to set the state of this pin (high/low) while POR and/or RESET is asserted. For more detailed information on external PUs/PDs, see Section 4.5.1, *Pullup/Pulldown Resistors*.

If the BTMODE[11] pin is latched as a "0" at the rising edge of POR or RESET, then RSTOUT_WD_OUT is also asserted when any of the below resets occur:

- Power-On Reset (asserted after the BTMODE[11] pin is latched)

- External Warm Reset (asserted after the BTMODE[11] pin is latched)
- Emulation Warm Reset
- Software Global Cold/Warm Reset

The RSTOUT_WD_OUT pin remains asserted until the PRCM releases the host ARM Cortex-A8 processor for reset.

7.3.13 Effect of Reset on Emulation & Trace

The device Emulation & Trace Logic will only be reset by the following sources:

- Power-On Reset
- Software Global Cold Reset
- Test Reset

Other than these three reset types, none of the other resets will affect the Emulation and Trace Logic. However, the multiplexing of the EMU[4:2] pins is reset by all system reset types except Test Reset.

7.3.14 Reset During Power Domain Switching

Each Power Domain has a dedicated Warm Reset and Cold Reset. Warm Reset for a Power Domain is asserted under either of the following two conditions:

1. An External Warm Reset, Emulation Warm Reset, or Software Global Warm Reset occurs
2. When that Power Domain switches from the "ON" state to the "OFF" state

Cold Reset for a Power Domain is asserted under either of the following two conditions:

1. Power-On Reset or Software Global Cold Reset occurs
2. When that Power Domain switches from the "OFF" state to the "ON" state

7.3.15 Pin Behaviors at Reset

When any reset, other than Test Reset, (all described in Section 7.3.1, *System-Level Reset Sources*) is asserted, all device I/O pins are reset into a Hi-Z state except for:

- Emulation Pins. These pins are only put into a Hi-Z state when Test Reset (TRST) is asserted.
- RSTOUT_WD_OUT Pin during any reset types except for POR and RESET. For more detailed information on RSTOUT_WD_OUT pin behavior, see Section 7.3.12, *RSTOUT_WD_OUT Pin*.
- DDR[0] Address/Control Pins (CLK, CLK, CKE, WE, CS[0], RAS, CAS, ODT[0], RST, BA[2:0], A[15:0]). These pins are 3-stated during reset. However, these pins are then driven to the same value as their internal pull resistor reset value when reset is released.

In addition, the PINCNTL registers, which control pin multiplexing, enabling the IPUs/IPDs, and enabling the receiver, are reset to their default state.

Internal pull-up/down (IPU/IPD) resistors are enabled during and immediately after reset as described in Section 3.3, *Terminal Functions* of this document.

NOTE

The reset pin state is after all the power supplies are ramped up and stable. The state is not not ensured during power-up sequencing.

Upon coming out of reset, the ARM Cortex-A8 starts executing code from the internal Boot ROM. The Boot ROM code modifies the PINCNTLx registers to configure the associated pins for the chosen primary and backup Bootmodes.

7.3.16 Reset Electrical Data/Timing

NOTE

For supported OPP frequencies, see Table 7-3, *Device Operating Points (OPPs)*.

Table 7-8. Timing Requirements for Reset (see Figure 7-5 and Figure 7-6)

NO.				OPP100		UNIT
				MIN	MAX	
1	$t_{w(RESET)}$	Pulse duration, $\overline{POR}$ low or $\overline{RESET}$ low		12P[1]		ns
2	$t_{su(BOOT)}$	Setup time, BTMODE[15:0] pins valid before $\overline{POR}$ high or $\overline{RESET}$ high	$\overline{POR}$	2P[2]		ns
			$\overline{RESET}$	2P[2]		ns
3	$t_{h(BOOT)}$	Hold time, BTMODE[15:0] pins valid after $\overline{POR}$ high or $\overline{RESET}$ high		0		ns

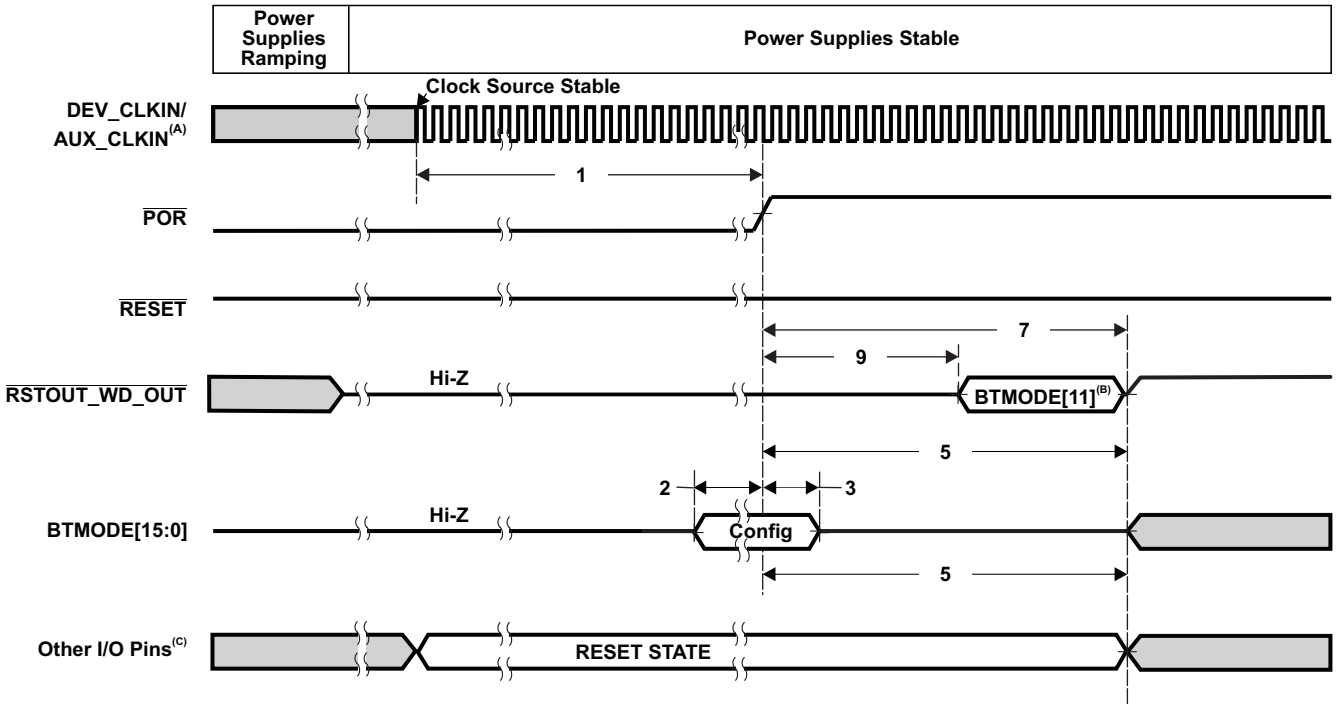
(1) The device clock source ***must*** be stable and at a valid frequency prior to meeting the $t_{w(RESET)}$ requirement.
(2) P = 1/(DEV Clock) frequency in ns.

Table 7-9. Switching Characteristics Over Recommended Operating Conditions During Reset (see Figure 7-6)

NO.	PARAMETER			OPP100		UNIT
				MIN	MAX	
4	$t_{d(RSTL-IORST)}$	Delay time, $\overline{RESET}$ low or $\overline{POR}$ low to all I/Os entering their reset state			14	ns
5	$t_{d(RSTH-IOFUNC)}$	Delay time, $\overline{RESET}$ high or $\overline{POR}$ high to all I/Os exiting their reset state			14	ns
6	$t_{d(RSTH-RSTOUTH)}$	Delay time, $\overline{RESET}$ high to $\overline{RSTOUT\_WD\_OUT}$ high[1][2]	$\overline{RESET}$ assertion $t_{w(RESET)}$ ≥ 30P	0	2P	ns
			$\overline{RESET}$ assertion $t_{w(RESET)}$ < 30P	0	32P - $t_{w(RESET)}$	ns
7	$t_{d(PORH-RSTOUTH)}$	Delay time, $\overline{POR}$ high to $\overline{RSTOUT\_WD\_OUT}$ high[1][2]		0	12500P	ns
8	$t_{d(RSTL-RSTOUTZ)}$	Delay time, $\overline{RESET}$ low to $\overline{RSTOUT\_WD\_OUT}$ Hi-Z[1][2]		0	2P	ns
9	$t_{d(PORH-RSTOUTL)}$	Delay time, $\overline{POR}$ high to $\overline{RSTOUT\_WD\_OUT}$ driven based on latched BTMODE[11] value[1][2]		0	2P	ns
10	$t_{d(RSTH-RSTOUTD)}$	Delay time, $\overline{RESET}$ high to $\overline{RSTOUT\_WD\_OUT}$ driven based on latched BTMODE[11] value[1][2]		0	2P	ns

(1) For more detailed information on $\overline{RSTOUT\_WD\_OUT}$ pin behavior, see Section 7.3.12, *$\overline{RSTOUT\_WD\_OUT}$ Pin*.
(2) P = 1/(DEV Clock) frequency in ns.

Figure 7-5 shows the Power-Up Timing. Figure 7-6 shows the Warm Reset ($\overline{\text{RESET}}$) Timing. Max Reset Timing is identical to Warm Reset Timing, except the BTMODE[15:0] pins are ***not*** re-latched.

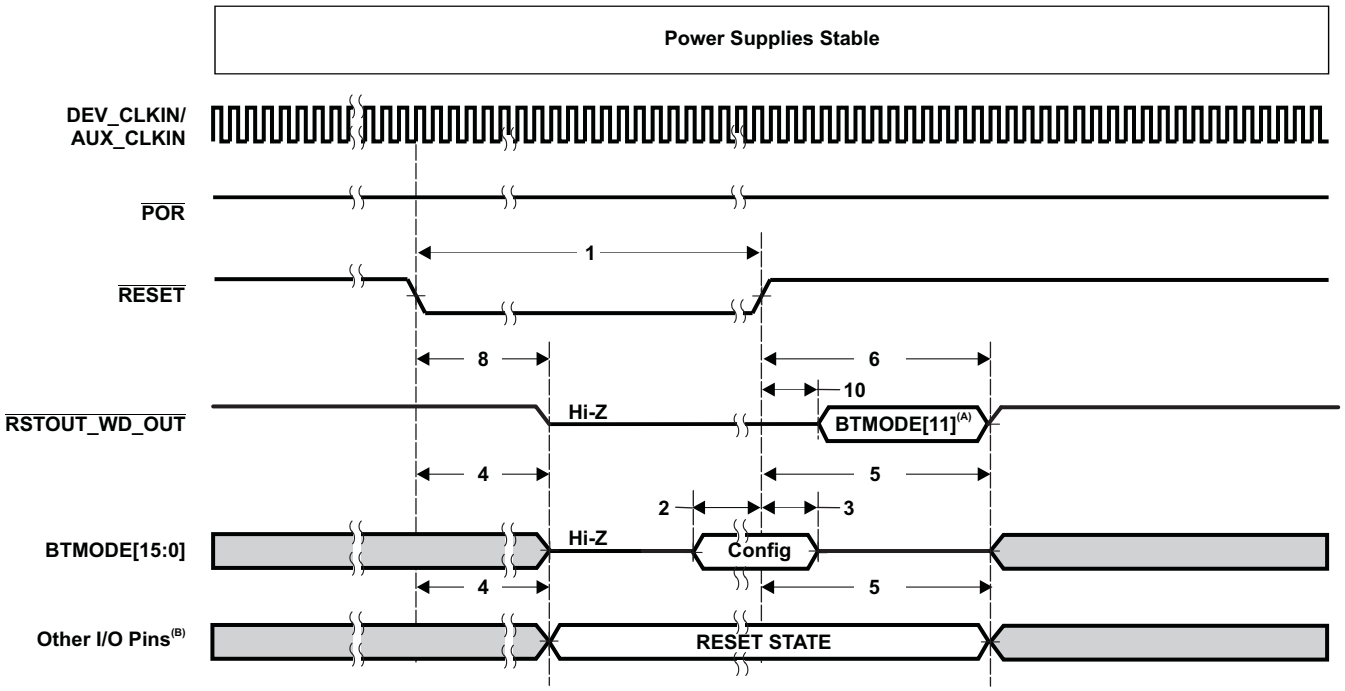


A. Power supplies and DEV_CLKIN/AUX_CLKIN must be stable before the start of $t_{w(RESET)}$.

B. $\overline{\text{RSTOUT\_WD\_OUT}}$ only asserted if BTMODE[11] was latched as a "0" when coming out of reset.

C. For more detailed information on the RESET STATE of each pin, see Section 7.3.15, *Pin Behaviors at Reset*. Also see , *Terminal Functions* for the IPU/IPD settings during reset.

Figure 7-5. Power-Up Timing



A. RSTOUT_WD_OUT only asserted if BTMODE[11] was latched as a "0" when coming out of reset.

B. For more detailed information on the RESET STATE of each pin, see Section 7.3.15, *Pin Behaviors at Reset*. Also see , *Terminal Functions* for the IPU/IPD settings during reset.

Figure 7-6. Warm Reset (RESET) Timing

7.4 Clocking

The device clocks are generated from several reference clocks that are fed to on-chip PLLs and dividers (both inside and outside of the PRCM Module). Figure 7-7 shows a high-level overview of the device system clocking structure (Note: to reduce complexity, not all clocking connections are shown). For detailed information on the device clocks, see the Clock Generation and Management section of the *Power, Reset, and Clock Management (PRCM) Module* chapter in the device-specific Technical Reference Manual.

NOTE

For supported OPP frequencies, see Table 7-3, *Device Operating Points (OPPs)*.

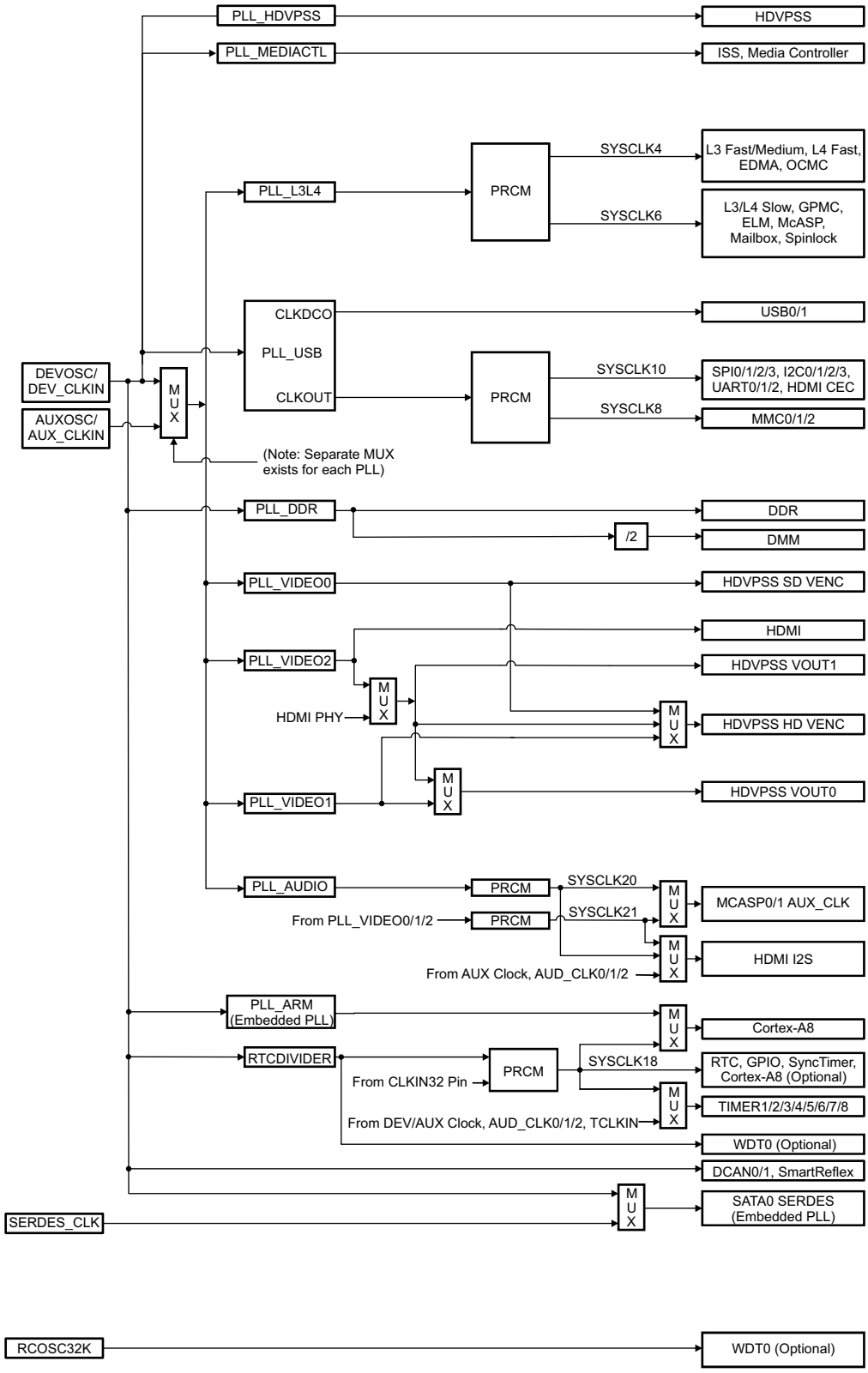


Figure 7-7. System Clocking Overview

7.4.1 Device (DEV) and Auxiliary (AUX) Clock Inputs

The device provides two clock inputs, Device (DEVOSC_MXI/DEV_CLKIN) and Auxiliary (AUXOSC_MXI/AUX_CLKIN). The Device (DEV) clock is used to generate the majority of the internal reference clocks, while the Auxiliary (AUX) clock can optionally be used as a source for the Audio and/or Video PLLs.

The DEV and AUX clocks can be sourced in two ways:

1. Using an external crystal in conjunction with the internal oscillator *or*
2. Using an external 1.8-V LVCMOS-compatible clock input

Note: The external crystals used with the internal oscillators ***must*** operate in fundamental parallel resonant mode *only*. There is no overtone support.

The DEV Clock should in most cases be 20 MHz. However, it can optionally range anywhere from 20 - 30 MHz if the following are true:

- The DEV Clock is not used to source the SATA reference clock
- A precise 32768-Hz clock is not needed for Real-Time Clock functionality
- If the boot mode is FAST XIP

The AUX Clock is optional and can range from 20-30 MHz. It can be used to source the Audio and/or Video PLLs when a very precise audio or video frequency is required.

7.4.1.1 Using the Internal Oscillators

When the internal oscillators are used to generate the DEV and AUX clocks, external crystals are required to be connected across the DEVOSC or AUXOSC oscillator MXI and MXO pins, along with two load capacitors (see Figure 7-8 and Figure 7-9). The external crystal load capacitors should also be connected to the associated oscillator ground pin (VSSA_DEVOSC or VSSA_AUXOSC). The capacitors should ***not*** be connected to board ground (VSS).

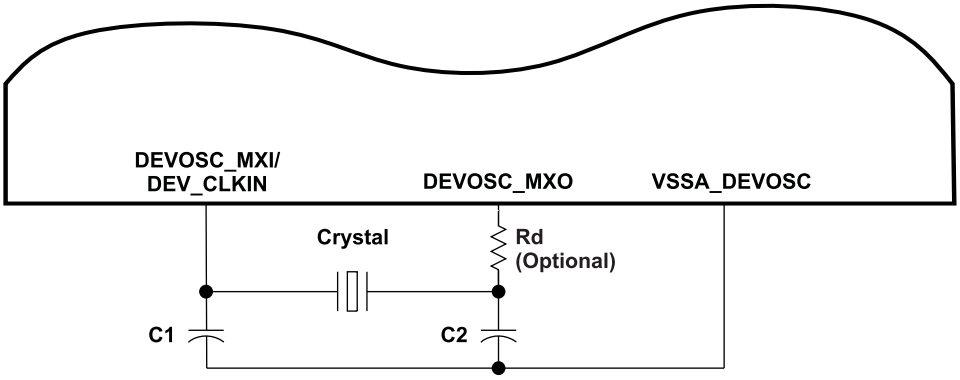


Figure 7-8. Device Oscillator

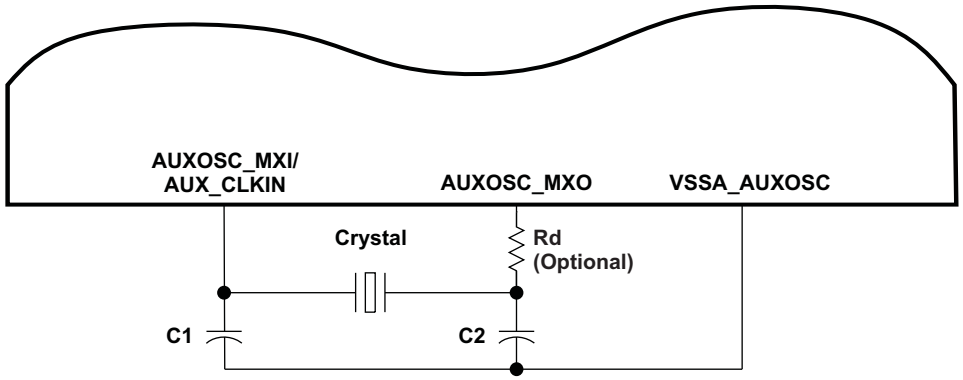


Figure 7-9. Auxiliary Oscillator

The load capacitors, C1 and C2 in the above pictures, should be chosen such that the below equation is satisfied. CL in the equation is the load specified by the crystal manufacturer. All discrete components used to implement the oscillator circuit should be placed as close as possible to the associated oscillator MXI, MXO, and VSS pins.

$$C_L = \frac{C_1 C_2}{(C_1 + C_2)} + \text{Cshunt}$$

Table 7-10. Input Requirements for Crystal Circuit on the Device Oscillator (DEVOSC)

PARAMETER		MIN	TYP	MAX	UNIT
	Start-up time (from power up until oscillating at stable frequency)			4	ms
	Crystal Oscillation frequency(1)	20	20	30	MHz
	Parallel Load Capacitance (C1 and C2)	12		24	pF
	Crystal ESR			50	Ω
	Crystal Shunt Capacitance (Cshunt)		5		pF
	Crystal Oscillation Mode		Fundamental Only		n/a
	Crystal Frequency stability			±50	ppm

(1) 20-MHz DEV clock is required for all bootmodes other than Fast XIP. For more detailed information on boot modes, see the *ROM Code Memory and Peripheral Booting* chapter in the device-specific Technical Reference Manual.

Table 7-11. Input Requirements for Crystal Circuit on the Auxiliary Oscillator (AUXOSC)

PARAMETER		MIN	TYP	MAX	UNIT
	Start-up time (from power up until oscillating at stable frequency)			4	ms
	Crystal Oscillation frequency	20		30	MHz
	Parallel Load Capacitance (C1 and C2)	12		24	pF
	Crystal ESR			50	Ω
	Crystal Shunt Capacitance (Cshunt)		5		pF
	Crystal Oscillation Mode		Fundamental Only		n/a
	Crystal Frequency stability(1)			±50	ppm

(1) Applies only when sourcing the HDMI or HDVPSS DAC clocks from the AUXOSC

7.4.1.2 Using a 1.8V LVCMOS-Compatible Clock Input

A 1.8-V LVCMOS-Compatible Clock Input can be used instead of the internal oscillators as the DEV and AUX clock inputs to the system. The external connections to support this are shown in Figure 7-10 and Figure 7-11. The DEV_CLKIN and AUX_CLKIN pins are connected to the 1.8-V LVCMOS-Compatible clock sources. The DEV_MXO and AUX_MXO pins are left unconnected. The VSSA_DEVOSC and VSSA_AUXOSC pins are connected to board ground (VSS).

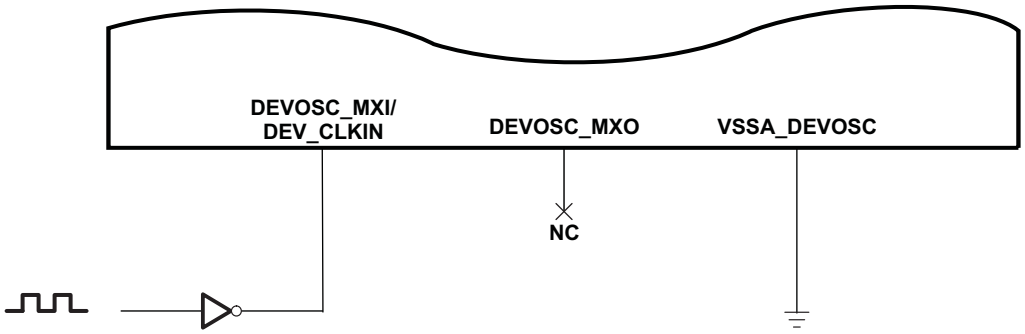


Figure 7-10. 1.8-V LVCMOS-Compatible Clock Input (DEV_OSC)

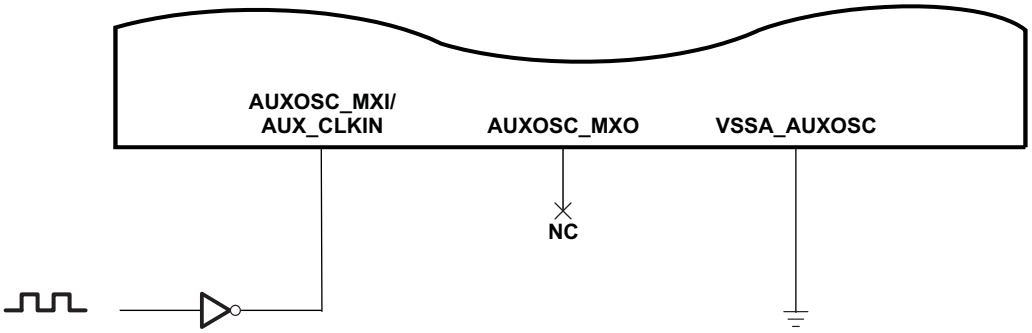


Figure 7-11. 1.8-V LVCMOS-Compatible Clock Input (AUX_OSC)

The clock source ***must*** meet the DEVOSC_MXI/DEV_CLKIN timing requirements shown in Table 7-14, *Timing Requirements for DEVOSC_MXI/DEV_CLKIN*.

The clock source must meet the AUXOSC_MXI/AUX_CLKIN timing requirements shown in Table 7-15, *Timing Requirements for AUXOSC_MXI/AUX_CLKIN*.

7.4.2 SERDES_CLKN/P Input Clock

A high-quality, low-jitter differential clock source is required for the SERDES and is an optional clock source for the SATA PHY. The clock is required to be AC coupled to the device's SERDES_CLKP and SERDES_CLKN pins according to the specifications in Table 7-12. Both the clock source and the coupling capacitors should be placed physically as close to the processor as possible. In addition, make sure to follow any PCB routing and termination recommendations that the clock source manufacturer recommends.

Table 7-12. SERDES_CLKN/P AC Coupling Capacitors Recommendations

PARAMETER		MIN	TYP	MAX	UNIT
	SERDES_CLKN/P AC coupling capacitor value	0.25	0.27	4.0	nF
	SERDES_CLKN/P AC coupling capacitor package size(1)(2)		0402	0603	EIA

(1) L x W, 10 Mil units, that is, a 0402 is a 40 x 20 Mil surface mount capacitor.
(2) The physical size of the capacitor should be as small as practical. Use the same size on both lines in each pair placed side-by-side.

The value of this capacitor depends on several factors including differential input clock swing. For a 100MHz differential clock with an approximate 1V voltage swing, the recommended typical value for the SerDes Clock AC Coupling Capacitors is 270pF.

Deviating from this recommendation can result in the reduction of clock signal amplitude or lowering the noise rejection characteristics.

In addition, LVDS clock sources that are compliant to the above specification, but with the following exceptions, are also acceptable:

Table 7-13. Acceptable Exceptions to the REFCLK AC Specifications for LVDS Clock Sources

PARAMETER		MIN	MAX	UNIT
V_{IH}	Differential High-Level Input Voltage	125	1000	mV
V_{IL}	Differential Low-Level Input Voltage	-1000	-125	mV

7.4.3 CLKIN32 Input Clock

An external 32768-Hz clock input can optionally be provided at the CLKIN32 pin to serve as a reference clock in place of the RTCDIVIDER clock for the following Modules:

- RTC
- GPIO0/1/2/3
- TIMER1/2/3/4/5/6/7
- ARM Cortex-A8
- SYNCTIMER

The CLKIN32 source must meet the timing requirements shown in Table 7-16.

7.4.4 Output Clocks Select Logic

The device includes two selectable general-purpose clock outputs (CLKOUT0 and CLKOUT1). The source for these output clocks is controlled by the CLKOUT_MUX register in the Control Module (see Figure 7-12).

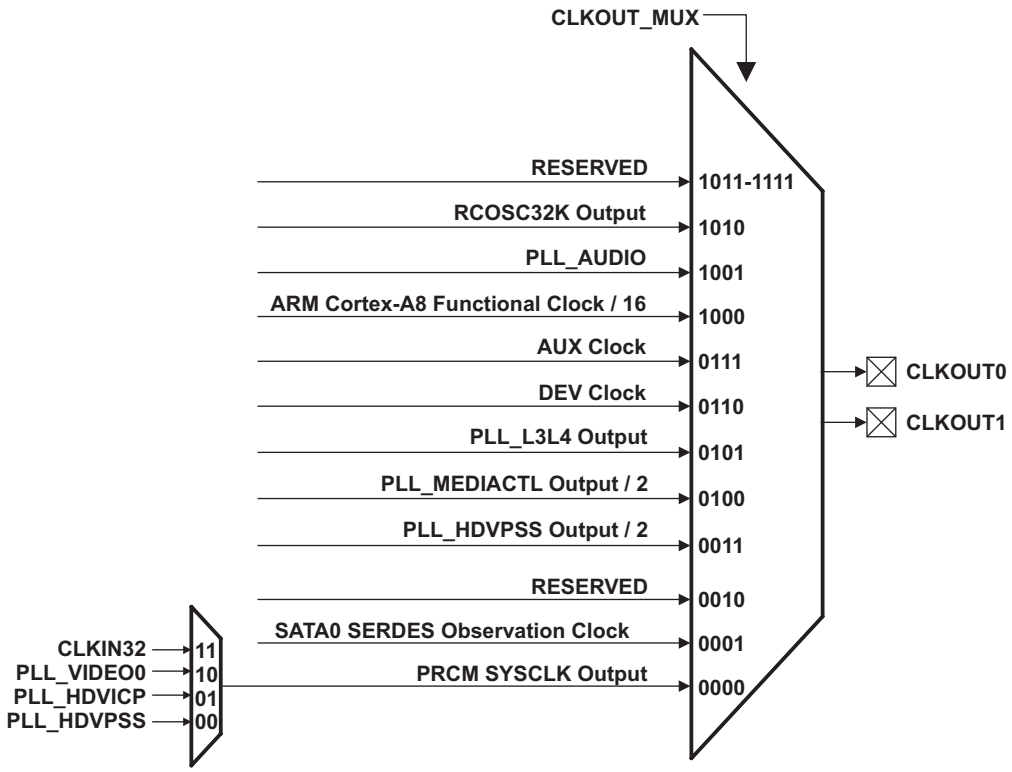


Figure 7-12. CLKOUTx Source Selection Logic

For detailed information on the CLKOUTx switching characteristics, see Table 7-17.

7.4.5 Input/Output Clocks Electrical Data/Timing

Note: If an external clock oscillator is used, a single clean power supply should be used to power both the device and the external clock oscillator circuit.

Table 7-14. Timing Requirements for DEVOSC_MXI/DEV_CLKIN(1) (2) (3)(see Figure 7-13)

NO.			OPP100			UNIT
			MIN	NOM	MAX	
1	$t_{c(DMXI)}$	Cycle time, DEVOSC_MXI/DEV_CLKIN	33.$\overline{33}$	50	50	ns
2	$t_{w(DMXIH)}$	Pulse duration, DEVOSC_MXI/DEV_CLKIN high	0.45C		0.55C	ns
3	$t_{w(DMXIL)}$	Pulse duration, DEVOSC_MXI/DEV_CLKIN low	0.45C		0.55C	ns
4	$t_{t(DMXI)}$	Transition time, DEVOSC_MXI/DEV_CLKIN			7	ns
5	$t_{J(DMXI)}$	Period jitter, DEVOSC_MXI/DEV_CLKIN			0.02C	ns
		Frequency Stability			±50	ppm

(1) The DEVOSC_MXI/DEV_CLKIN frequency and PLL settings should be chosen such that the resulting SYSCLKs and Module Clocks are within the specific ranges shown in the Section 7.4.7, *SYSCLKs* and Section 7.4.8, *Module Clocks*.
(2) The reference points for the rise and fall transitions are measured at V_{IL} MAX and V_{IH} MIN.
(3) C = DEV_CLKIN cycle time in ns. For example, when DEVOSC_MXI/DEV_CLKIN frequency is 20 MHz, use C = 50 ns.

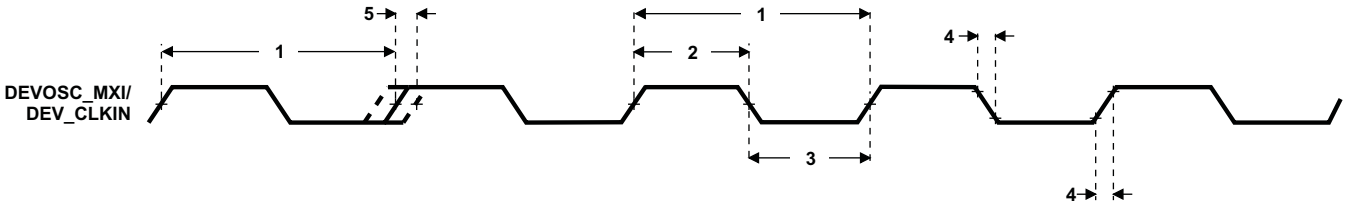


Figure 7-13. DEV_MXI/DEV_CLKIN Timing

Table 7-15. Timing Requirements for AUX_MXI/AUX_CLKIN (1) (2) (see Figure 7-14)

NO.			OPP100			UNIT
			MIN	NOM	MAX	
1	$t_{c(AMXI)}$	Cycle time, AUXOSC_MXI/AUX_CLKIN	33.$\overline{3}$	50	50	ns
2	$t_{w(AMXIH)}$	Pulse duration, AUXOSC_MXI/AUX_CLKIN high	0.45C		0.55C	ns
3	$t_{w(AMXIL)}$	Pulse duration, AUXOSC_MXI/AUX_CLKIN low	0.45C		0.55C	ns
4	$t_{t(AMXI)}$	Transition time, AUXOSC_MXI/AUX_CLKIN			7	ns
5	$t_{J(AMXI)}$	Period jitter, AUXOSC_MXI/AUX_CLKIN			0.02C	ns
6	S_f	Frequency stability, AUXOSC_MXI/AUX_CLKIN (3)			± 50	ppm

(1) The reference points for the rise and fall transitions are measured at V_{IL} MAX and V_{IH} MIN.
(2) C = AUX_CLKIN cycle time in ns. For example, when AUXOSC_MXI/AUX_CLKIN frequency is 20 MHz, use C = 50 ns.
(3) Applies only when sourcing the HDMI or HDVPSS DAC clocks from the AUXOSC.

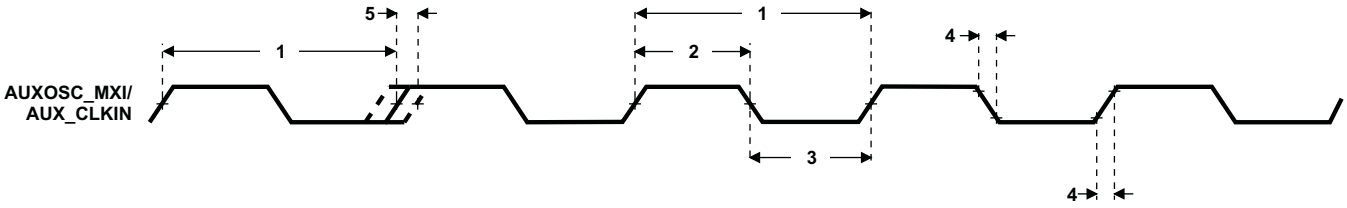


Figure 7-14. AUX_MXI/AUX_CLKIN Timing

Table 7-16. Timing Requirements for CLKIN32 (1)(2) (see Figure 7-15)

NO.			OPP100			UNIT
			MIN	NOM	MAX	
1	$t_{c(CLKIN32)}$	Cycle time, CLKIN32	1/32768			s
2	$t_{w(CLKIN32H)}$	Pulse duration, CLKIN32 high	0.45C		0.55C	ns
3	$t_{w(CKIN32L)}$	Pulse duration, CLKIN32 low	0.45C		0.55C	ns
4	$t_{t(CLKIN32)}$	Transition time, CLKIN32			7	ns
5	$t_{J(CLKIN32)}$	Period jitter, CLKIN32			0.02C	ns

(1) The reference points for the rise and fall transitions are measured at V_{IL} MAX and V_{IH} MIN.
(2) C = CLKIN32 cycle time in ns. For example, when CLKIN32 frequency is 32768 Hz, use C = 1/32768 s.

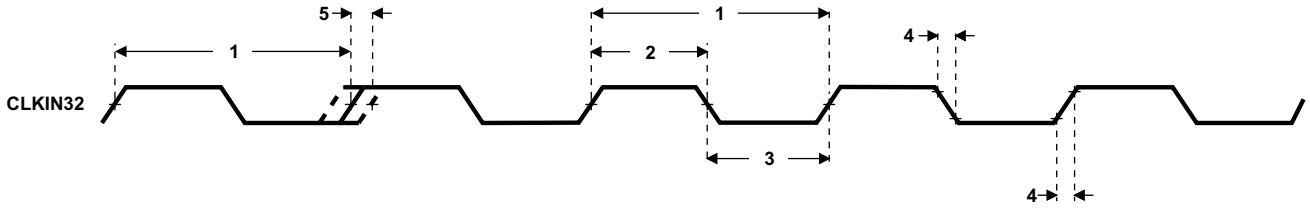


Figure 7-15. CLKIN32 Timing

Table 7-17. Switching Characteristics Over Recommended Operating Conditions for CLKOUTx (CLKOUT0 and CLKOUT1)(1) (2) (see Figure 7-16)

NO.	PARAMETER		OPP100		UNIT
			MIN	MAX	
1	$t_{c(CLKOUTx)}$	Cycle time, CLKOUTx	5		ns
2	$t_{w(CLKOUTxH)}$	Pulse duration, CLKOUTx high	0.45P	0.55P	ns
3	$t_{w(CLKOUTxL)}$	Pulse duration, CLKOUTx low	0.45P	0.55P	ns
4	$t_{t(CLKOUTx)}$	Transition time, CLKOUTx		0.05P	ns

(1) The reference points for the rise and fall transitions are measured at V_{OL} MAX and V_{OH} MIN.
(2) P = 1/CLKOUTx clock frequency in nanoseconds (ns). For example, when CLKOUTx frequency is 200 MHz, use P = 5 ns.

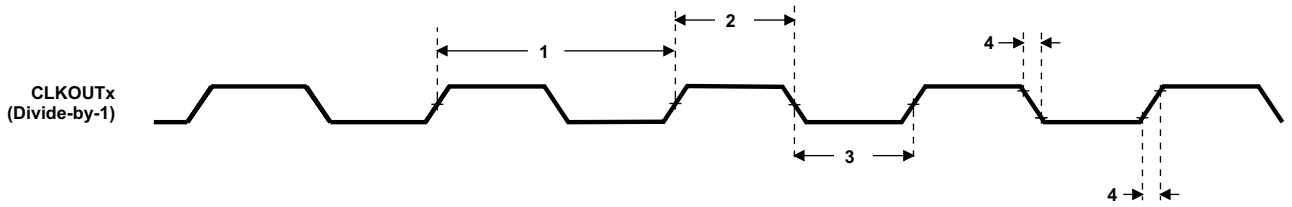


Figure 7-16. CLKOUTx Timing

7.4.6 PLLs

The device contains 10 top-level PLLs, and embedded PLLs (within the ARM Cortex-A8, SATA, and CSI) that provide clocks to different parts of the system. Figure 7-17 and Figure 7-18 show simplified block diagrams of the Top-Level PLL and PLL_ARM. In addition, see the System Clocking Overview (Figure 7-7) for a high-level view of the device clock architecture including the PLL reference clock sources and connections.

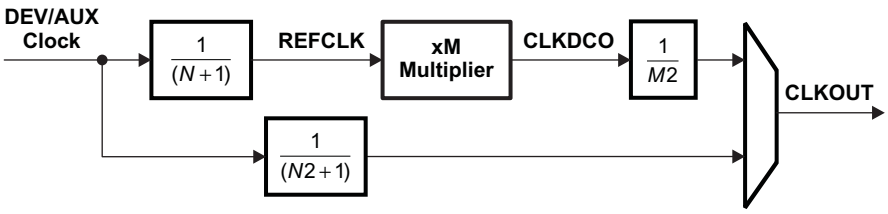


Figure 7-17. Top-Level PLL Simplified Block Diagram

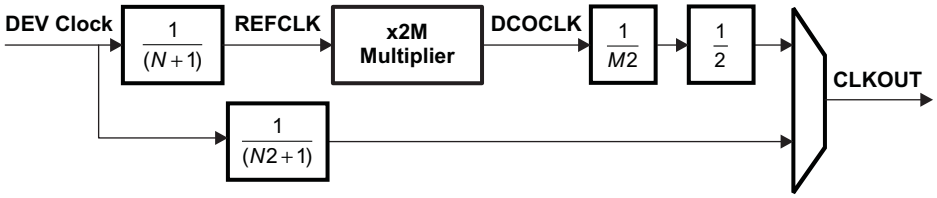


Figure 7-18. PLL_ARM Simplified Block Diagram

The reference clock for most of the PLLs comes from the DEV input clock, with select PLLs also having the option to use the AUX input clock as a reference. Also, each PLL supports a Bypass mode in which the reference clock can be directly passed to the PLL CLKOUT through a divider. All device PLL's will come-up in Bypass mode after reset.

For details on programming the device PLLs, see the *Control Module* chapter in the device-specific Technical Reference Manual.

7.4.6.1 PLL Power Supply Filtering

The device PLLs are supplied externally via the VDDA_**x**PLL_1P8 power-supply pins (where "**x**" represents ARM, VID0, VID1, AUDIO, DDR, and/or L3). External filtering must be added on the PLL supply pins to ensure that the requirements in Table 7-18 are met.

Table 7-18. PLL Power Supply Requirements

PARAMETER	MIN	MAX	UNIT
Dynamic noise at VDDA_**x**PLL_1P8 pins		50	mV p-p

7.4.6.2 PLL Multipliers and Dividers

The Top-Level and PLL_ARM PLLs support the internal multiplier and divider values shown in Table 7-19, *Top-Level PLL Multiplier and Divider Limits* and Table 7-20, *PLL_ARM Multiplier and Divider Limits*. The PLLs must be programmed to conform to the various REFCLK, CLKDCO, DCOCLK, and CLKOUT limits described in Section 7.4.6.3, *PLL Frequency Limits*.

Table 7-19. Top-Level PLL Multiplier and Divider Limits

PARAMETER	MIN	MAX
N Pre-Divider	0	255

Table 7-19. Top-Level PLL Multiplier and Divider Limits (continued)

PARAMETER	MIN	MAX
PLL Multiplier (M)	2	4095(1)
M2 Post Divider	1	127
N2 Bypass Divider	0	15

(1) The PLL Multiplier supports fractional values (up to 18-bits of fraction) except when the PLL Multiplier is > 4093.

Table 7-20. PLL_ARM Multiplier and Divider Limits

PARAMETER	MIN	MAX
N Pre-Divider	0	127
PLL Multiplier (M)(1)	2	2047(2)
M2 Post Divider	1	31
N2 Bypass Divider	0	15

(1) This parameter describes the limits on the programmable multiplier value M. The multiplication factor for the PLL_ARM is equal to 2 * M (also see Figure 7-18).
(2) The PLL Multiplier supports fractional values (up to 18-bits of fraction) except when the PLL Multiplier is < 20 OR > 2045.

7.4.6.3 PLL Frequency Limits

Each PLL supports a minimum and maximum operating frequency for its REFCLK, CKLDCO, and CLKOUT values. The PLLs must be configured not to exceed any of the constraints placed on these values shown in Table 7-21 through Table 7-23. Care must be taken to stay within these limits when selecting external clock input frequencies, internal divider values, and PLL multiply ratios. In addition, limits shown in these tables may be further restricted by the clock frequency limitations of the device modules using these clocks. For more detailed information on the SYSCLK and Module Clock frequency limits, see Section 7.4.7, *SYSCLKs* and Section 7.4.8, *Module Clocks*.

Table 7-21. Top-Level PLL Frequency Ranges (ALL OPPs)

CLOCK	MIN	MAX	UNIT
REFCLK	0.5	2.5	MHz
CLKDCO (HS1)(1)	1000	2000	MHz
CLKDCO (HS2)(2)	500	1000	MHz
CLKOUT	see Table 7-23	see Table 7-23	MHz

(1) The PLL has two modes of operation: HS1 and HS2. The mode of operation should be set, according to the desired CLKDCO frequency, by programming the SELFREQDCO field of the ADPLLLJx_CLKCTRL registers in the Control Module.
(2) CLKDCO of the PLL_USB is used undivided by the USB modules; therefore, CLKDCO for the PLL_USB PLL must be programmed to 960 MHz for proper operation.

Table 7-22. ARM Cortex-A8 Embedded PLL (PLL_ARM) Frequency Ranges (ALL OPPs)

CLOCK	MIN	MAX	UNIT
REFCLK	0.032	52	MHz
DCOCLK	20	2000	MHz
CLKOUT	see Table 7-23	see Table 7-23	MHz

Table 7-23. PLL CLKOUT Frequency Ranges

PLL	OPP100		UNIT
	MIN	MAX	
PLL_ARM	10	600	MHz
PLL_HDVICP	10	266	MHz
PLL_L3L4	10	200	MHz

Table 7-23. PLL CLKOUT Frequency Ranges (continued)

PLL	OPP100		UNIT
	MIN	MAX	
PLL_DDR	10	400	MHz
PLL_HDVPSS	10	200	MHz
PLL_AUDIO	10	200	MHz
PLL_MEDIACTL	10	400	MHz
PLL_USB	10(1)	960	MHz
PLL_VIDEO0	10	200	MHz
PLL_VIDEO1	10	200	MHz
PLL_VIDEO2	10	200	MHz

(1) When the USB is used, PLL_USB **must** be fixed at 960 MHz.

7.4.6.4 PLL Register Description(s)

The PLL Control Registers reside in the Control Module and are listed in Section 4.1, *Control Module* of this datasheet.

7.4.7 SYSCLKs

In some cases, the system clock inputs and PLL outputs are sent to the PRCM Module for division and multiplexing before being routed to the various device Modules. These clock outputs from the PRCM Module are called SYSCLKs. Table Table 7-24 lists the device SYSCLKs along with their maximum supported clock frequencies. In addition, limits shown in these tables may be further restricted by the clock frequency limitations of the device modules using these clocks. For more details on Module Clock frequency limits, see Section 7.4.8 *Module Clocks*.

NOTE

For supported OPP frequencies, see Table 7-3, *Device Operating Points (OPPs)*.

Table 7-24. Maximum SYSCLK Clock Frequencies

SYSCLK	MAX CLOCK FREQUENCY OPP100 (MHz)
SYSCLK1	RSV
SYSCLK2	RSV
SYSCLK3	266
SYSCLK4	220
SYSCLK5	RSV
SYSCLK6	110
SYSCLK7	RSV
SYSCLK8	192
SYSCLK9	RSV
SYSCLK10	48
SYSCLK11	RSV
SYSCLK12	RSV
SYSCLK13	RSV
SYSCLK14	27
SYSCLK15	RSV
SYSCLK16	27
SYSCLK17	RSV

Table 7-24. Maximum SYSCLK Clock Frequencies (continued)

SYSCLK	MAX CLOCK FREQUENCY OPP100 (MHz)
SYSCLK18	0.032768
SYSCLK19	192
SYSCLK20	192
SYSCLK21	192
SYSCLK22	RSV
SYSCLK23	RSV

7.4.8 Module Clocks

Device Modules either receive their clock directly from an external clock input, directly from a PLL, or from a PRCM SYSCLK output. Table 7-25 lists the clock source options for each Module on this device, along with the maximum frequency that Module can accept. To ensure proper Module functionality, the device PLLs and dividers **must** be programmed not to exceed the maximum frequencies listed in this table.

Table 7-25. Maximum Module Clock Frequencies

MODULE	CLOCK SOURCE(S)	MAX FREQUENCY OPP100 (MHz)
Cortex-A8	PLL_ARM SYSCLK18	600
DCAN0/1	DEV Clock	30
DDR0	PLL_DDR	400
DMM	PLL_DDR/2	200
EDMA	SYSCLK4	220
Face Detect	SYSCLK4	220
GPIO	SYSCLK6	110
GPIO Debounce	SYSCLK18	Fixed 0.032768
GPMC	SYSCLK6	110
HDMI	PLL_VIDEO2	186
HDMI CEC	SYSCLK10	Fixed 48
HDMI I2S	SYSCLK20 SYSCLK21 AUD_CLK0/1/2 AUX Clock	50
HDVICP2	SYSCLK3	266
HDVPSS	PLL_HDVPSS	200
HDVPSS VOUT1	PLL_VIDEO2 HDMI PHY	186
HDVPSS VOUT0	PLL_VIDEO1 PLL_VIDEO2	165
HDVPSS SD VENC	PLL_VIDEO0	Fixed 54
HDVPSS HD VENC	PLL_VIDEO0 PLL_VIDEO1 HDMI	Fixed 148.5
I2C0/1/2/3	SYSCLK10	48
ISS	PLL_ MEDIACTL	400
L3 Fast	SYSCLK4	220
L3 Medium	SYSCLK4	220
L3 Slow	SYSCLK6	110
L4 Fast	SYSCLK4	220
L4 Slow	SYSCLK6	110

Table 7-25. Maximum Module Clock Frequencies (continued)

MODULE	CLOCK SOURCE(S)	MAX FREQUENCY OPP100 (MHz)
Mailbox	SYSCLK6	110
McASP	SYSCLK6	110
McASP0/1 AUX_CLK	SYSCLK20 SYSCLK21	192
Media Controller	PLL_MEDIACTL	400
MMCSD0/1/2	SYSCLK8	192
OCMC RAM	SYSCLK4	220
SATA0 SERDES	DEV Clock SERDES_CLKx Pins	20 or 100
SmartReflex	DEV Clock	30
SPI0/1/2/3	SYSCLK10	48
Spinlock	SYSCLK6	110
Sync Timer	SYSCLK18	Fixed 0.032768
TIMER1/2/3/4/5/6/7/8	SYSCLK18 DEV Clock AUX Clock AUD_CLK0/1/2 TCLKIN	30
UART0/1/2	SYSCLK10	48
USB	PLL_USB CLKDCO	Fixed 960
WDT0	RTCDIVIDER RCOSC32K	Fixed 0.032768

7.5 Interrupts

The device has a large number of interrupts to service the needs of its many peripherals and subsystems. The ARM Cortex-A8 and Media Controller are capable of servicing these interrupts. The following sections list the device interrupt mapping and multiplexing schemes.

7.5.1 ARM Cortex-A8 Interrupts

The ARM Cortex-A8 Interrupt Controller (AINTC) is responsible for prioritizing all service requests from the System peripherals and generating either IRQs or FIQs to the Cortex-A8. The AINTC has the capability to handle up to 128 requests, and the priority of the interrupt inputs are programmable. Table 7-26 lists the interrupt sources for the AINTC.

For more details on ARM Cortex-A8 interrupt control, see the Interrupt Controller section of the *Chip Level Resources* chapter in the device-specific Technical Reference Manual.

Table 7-26. ARM Cortex-A8 Interrupt Controller (AINTC) Interrupt Sources

Cortex-A8 INTERRUPT NUMBER	ACRONYM	SOURCE
0	EMUINT	Cortex-A8 Emulation
1	COMMTX	Cortex-A8 Emulation
2	COMMRX	Cortex-A8 Emulation
3	BENCH	Cortex-A8 Emulation
4	ELM_IRQ	ELM
5	–	Reserved
6	–	Reserved
7	NMI	NMIn Pin
8	–	Reserved
9	L3DEBUG	L3 Interconnect
10	L3APPINT	L3 Interconnect
11	TINT8	TIMER8
12	EDMACOMPINT	EDMA CC Completion
13	EDMAMPERR	EDMA Memory Protection Error
14	EDMAERRINT	EDMA CC Error
15	WDTINT0	Watchdog Timer 0
16	SATAINT0	SATA0
17	USBSSINT	USB Subsystem
18	USBINT0	USB0
19	USBINT1	USB1
20-27	–	Reserved
28	SDINT1	MMC/SD1
29	SDINT2	MMC/SD2
30	I2CINT2	I2C2
31	I2CINT3	I2C3
32	GPIOINT2A	GPIO2 A
33	GPIOINT2B	GPIO2 B
34	USBWAKEUP	USB Subsystem Wakeup
35	–	Reserved
36	DSSINT	HDVPSS
37	–	Reserved
38	HDMIINT	HDMI
39	ISS_IRQ_5	ISS

Table 7-26. ARM Cortex-A8 Interrupt Controller (AINTC) Interrupt Sources (continued)

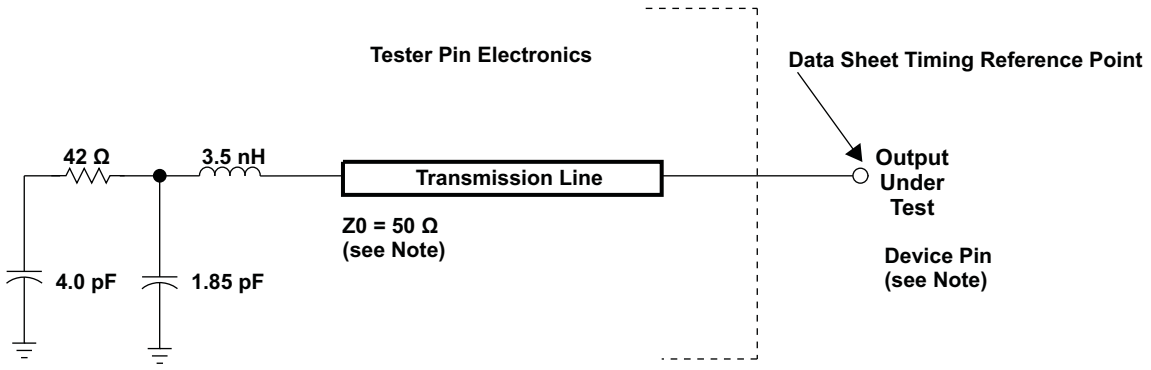
Cortex-A8 INTERRUPT NUMBER	ACRONYM	SOURCE
40-52	–	Reserved
52	DCAN0_INT0	DCAN0
53	DCAN0_INT1	DCAN0
54	DCAN0_PARITY	DCAN0 Parity
55	DCAN1_INT0	DCAN1
56	DCAN1_INT1	DCAN1
57	DCAN1_PARITY	DCAN1 Parity
58	–	Reserved
59	-	Reserved
60	–	Reserved
61	–	Reserved
62	GPIOINT3A	GPIO3
63	GPIOINT3B	GPIO3
64	SDINT0	MMC/SD0
65	SPIINT0	SPI0
66	-	Reserved
67	TINT1	TIMER1
68	TINT2	TIMER2
69	TINT3	TIMER3
70	I2CINT0	I2C0
71	I2CINT1	I2C1
72	UARTINT0	UART0
73	UARTINT1	UART1
74	UARTINT2	UART2
75	RTCINT	RTC
76	RTCALARMINT	RTC Alarm
77	MBINT	Mailbox
78	–	Reserved
79	PLLINT	PLL Recalculation Interrupt
80	MCATXINT0	McASP0 Transmit
81	MCARXINT0	McASP0 Receive
82	MCATXINT1	McASP1 Transmit
83	MCARXINT1	McASP1 Receive
84	–	Reserved
85	–	Reserved
86	–	Reserved
87	–	Reserved
88	–	Reserved
89	–	Reserved
90	SMRFLX_HDVICP	SmartReflex HDVICP Domain
91	–	Reserved
92	TINT4	TIMER4
93	TINT5	TIMER5
94	TINT6	TIMER6
95	TINT7	TIMER7
96	GPIOINT0A	GPIO0
97	GPIOINT0B	GPIO0

Table 7-26. ARM Cortex-A8 Interrupt Controller (AINTC) Interrupt Sources (continued)

Cortex-A8 INTERRUPT NUMBER	ACRONYM	SOURCE
98	GPIOINT1A	GPIO1
99	GPIOINT1B	GPIO1
100	GPMCINT	GPMC
101	DDRERR	DDR
102	–	Reserved
103	HDVICPCONT1SYNC	HDVICP2
104	HDVICPCONT2SYNC	HDVICP2
105	–	Reserved
106	–	Reserved
107	IVA0MBOXINT	HDVICP2 Mailbox
108	–	Reserved
109	–	Reserved
110	–	Reserved
111	–	Reserved
112	TCERRINT0	EDMA TC 0 Error
113	TCERRINT1	EDMA TC 1 Error
114	TCERRINT2	EDMA TC 2 Error
115	TCERRINT3	EDMA TC 3 Error
116-119	–	Reserved
120	SMRFLX_ARM	SmartReflex ARM Domain
121	SMRFLX_CORE	SmartReflex CORE Domain
122	–	Reserved
123	MCMMUINT	Media Controller
124	DMMINT	DMM
125	SPIINT1	SPI1
126	SPIINT2	SPI2
127	SPIINT3	SPI3

8 Peripheral Information and Timings

8.1 Parameter Information



NOTE: The data sheet provides timing at the device pin. For output timing analysis, the tester pin electronics and its transmission line effects must be taken into account. A transmission line with a delay of 2 ns can be used to produce the desired transmission line effect. The transmission line is intended as a load only. It is not necessary to add or subtract the transmission line delay (2 ns) from the data sheet timings.

Input requirements in this data sheet are tested with an input slew rate of < 4 Volts per nanosecond (4 V/ns) at the device pin.

Figure 8-1. Test Load Circuit for AC Timing Measurements

The load capacitance value stated is only for characterization and measurement of AC timing signals. This load capacitance value does not indicate the maximum load the device is capable of driving.

8.1.1 1.8-V and 3.3-V Signal Transition Levels

All input and output timing parameters are referenced to V_{ref} for both "0" and "1" logic levels. For 3.3-V I/O, V_{ref} = 1.5 V. For 1.8-V I/O, V_{ref} = 0.9 V.

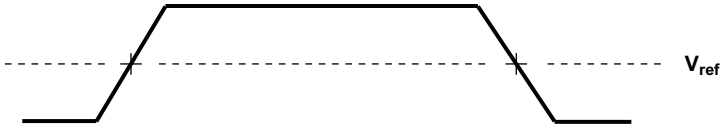


Figure 8-2. Input and Output Voltage Reference Levels for AC Timing Measurements

All rise and fall transition timing parameters are referenced to V_{IL} MAX and V_{IH} MIN for input clocks, V_{OL} MAX and V_{OH} MIN for output clocks.

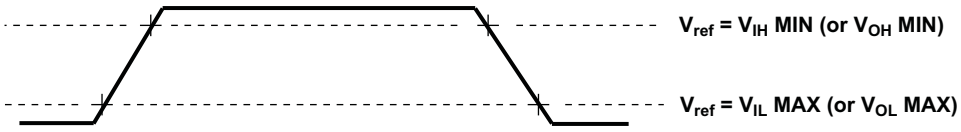


Figure 8-3. Rise and Fall Transition Time Voltage Reference Levels

8.1.2 3.3-V Signal Transition Rates

All timings are tested with an input edge rate of 4 volts per nanosecond (4 V/ns).

8.1.3 Timing Parameters and Board Routing Analysis

The timing parameter values specified in this data manual do *not* include delays by board routings. As a good board design practice, such delays must *always* be taken into account. Timing values may be adjusted by increasing/decreasing such delays. TI recommends utilizing the available I/O buffer information specification (IBIS) models to analyze the timing characteristics correctly. If needed, external logic hardware such as buffers may be used to compensate any timing differences.

8.2 Recommended Clock and Control Signal Transition Behavior

All clocks and control signals ***must*** transition between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.

NOTE

For supported OPP frequencies, see Table 7-3, *Device Operating Points (OPPs)*.

8.3 Controller Area Network Interface (DCAN)

The device provides two DCAN interfaces for supporting distributed realtime control with a high level of security. The DCAN interfaces implement the following features:

- Supports CAN protocol version 2.0 part A, B
- Bit rates up to 1 MBit/s
- 64 message objects
- Individual identifier mask for each message object
- Programmable FIFO mode for message objects
- Programmable loop-back modes for self-test operation
- Suspend mode for debug support
- Software module reset
- Automatic bus on after Bus-Off state by a programmable 32-bit timer
- Message RAM parity check mechanism
- Direct access to Message RAM during test mode
- CAN Rx/Tx pins are configurable as general-purpose IO pins
- Two interrupt lines (plus additional parity-error interrupts line)
- RAM initialization
- DMA support

For more detailed information on the DCAN peripheral, see the *DCAN Controller Area Network* chapter in the device-specific Technical Reference Manual.

8.3.1 DCAN Peripheral Register Descriptions

The DCAN peripheral registers are described in the device-specific Technical Reference Manual. Each register is documented as an offset from a base address for the peripheral. The base addresses for all of the peripherals are in the device memory map (see Section 2.10).

8.3.2 DCAN Electrical Data/Timing

Table 8-1. Timing Requirements for DCANx Receive(1) (see Figure 8-4)

NO.			OPP100/OPP120/Turbo/Nitro			UNIT
			MIN	NOM	MAX	
	f(baud)	Maximum programmable baud rate			1	Mbps
1	$t_{w(DCANRX)}$	Pulse duration, receive data bit (DCANx_RX)	H - 2		H + 2	ns

(1) H = period of baud rate, 1/programmed baud rate.

Table 8-2. Switching Characteristics Over Recommended Operating Conditions for DCANx Transmit (1)(see Figure 8-4)

NO.	PARAMETER		OPP100/OPP120/ Turbo/Nitro		UNIT
			MIN	MAX	
	f(baud)	Maximum programmable baud rate		1	Mbps
2	$t_{w(DCANTX)}$	Pulse duration, transmit data bit (DCANx_TX)	H - 2	H + 2	ns

(1) H = period of baud rate, 1/programmed baud rate.

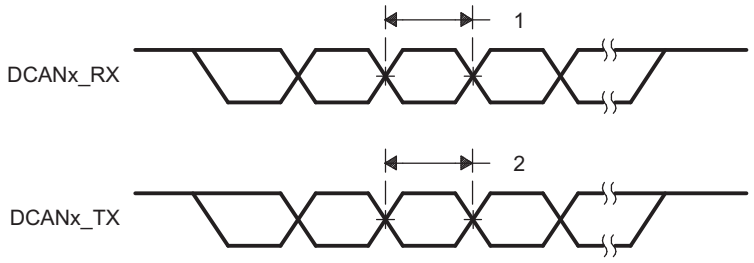


Figure 8-4. DCANx Timings

8.4 EDMA

The EDMA controller handles all data transfers between memories and the device slave peripherals on the device. These data transfers include cache servicing, non-cacheable memory accesses, user-programmed data transfers, and host accesses.

8.4.1 EDMA Channel Synchronization Events

The EDMA channel controller supports up to 64 channels which service peripherals and memory. Each EDMA channel is mapped to a default EDMA synchronization event as shown in Table 8-3. In addition, each EDMA channel can alternatively be mapped to one of the 31 multiplexed EDMA synchronization events shown in Table 8-4. The EVT_MUX_x registers in the Control Module are used to select between the default event and the multiplexed events for each channel.

For more detailed information on the EDMA module and how EDMA events are enabled, captured, processed, linked, chained, cleared, and more, see the *Enhanced Direct Memory Access Controller* chapter in the device-specific Technical Reference Manual.

Table 8-3. EDMA Default Synchronization Events

EVENT NUMBER	DEFAULT EVENT NAME	DEFAULT EVENT DESCRIPTION
0-1	–	Reserved
2	SDTXEVT1	SD1 Transmit
3	SDRXEVT1	SD1 Receive
4-7	–	Reserved
8	AXEVT0	McASP0 Transmit
9	AREVT0	McASP0 Receive
10	AXEVT1	McASP1 Transmit
11	AREVT1	McASP1 Receive
12	–	Reserved
13	–	Reserved
14	–	Reserved
15	–	Reserved
16	SPI0XEVT0	SPI0 Transmit 0
17	SPI0REVT0	SPI0 Receive 0
18	SPI0XEVT1	SPI0 Transmit 1
19	SPI0REVT1	SPI0 Receive 1
20	SPI0XEVT2	SPI0 Transmit 2
21	SPI0REVT2	SPI0 Receive 2
22	SPI0XEVT3	SPI0 Transmit 3
23	SPI0REVT3	SPI0 Receive 3
24	SDTXEVT0	SD0 Transmit
25	SDRXEVT0	SD0 Receive
26	UTXEVT0	UART0 Transmit
27	URXEVT0	UART0 Receive
28	UTXEVT1	UART1 Transmit
29	URXEVT1	UART1 Receive
30	UTXEVT2	UART2 Transmit
31	URXEVT2	UART2 Receive
42	SPI1XEVT0	SPI1 Transmit 0
43	SPI1REVT0	SPI1 Receive 0
44	SPI1XEVT1	SPI1 Transmit 1
45	SPI1REVT1	SPI1 Receive 1

Table 8-3. EDMA Default Synchronization Events (continued)

EVENT NUMBER	DEFAULT EVENT NAME	DEFAULT EVENT DESCRIPTION
46	–	Reserved
48	TINT4	TIMER4
49	TINT5	TIMER5
50	TINT6	TIMER6
51	TINT7	TIMER7
52	GPMCEVT	GPMC
58	I2CTXEVT0	I2C0 Transmit
59	I2CRXEVT0	I2C0 Receive
60	I2CTXEVT1	I2C1 Transmit
61	I2CRXEVT1	I2C1 Receive
62	–	Reserved
63	–	Reserved

Table 8-4. EDMA Multiplexed Synchronization Events

EVT_MUX_x VALUE	MULTIPLEXED EVENT NAME	MULTIPLEXED EVENT DESCRIPTION
0	-	Default Event
1	SDTXEVT2	SD2 Transmit
2	SDRXEVT2	SD2 Receive
3	I2CTXEVT2	I2C2 Transmit
4	I2CRXEVT2	I2C2 Receive
5	I2CTXEVT3	I2C3 Transmit
6	I2CRXEVT3	I2C3 Receive
7	–	Reserved
8	–	Reserved
9	–	Reserved
10	–	Reserved
11	–	Reserved
12	–	Reserved
16	SPI2XEVT0	SPI2 Transmit 0
17	SPI2REVT0	SPI2 Receive 0
18	SPI2XEVT1	SPI2 Transmit 1
19	SPI2REVT1	SPI2 Receive 1
20	SPI3XEVT0	SPI3 Transmit 0
21	SPI3REVT0	SPI3 Receive 0
22	–	Reserved
23	TINT1	TIMER1
24	TINT2	TIMER2
25	TINT3	TIMER3
26	–	Reserved
27	–	Reserved
28	EDMAEVT0	EDMA_EVT0 Pin
29	EDMAEVT1	EDMA_EVT1 Pin
30	EDMAEVT2	EDMA_EVT2 Pin
31	EDMAEVT3	EDMA_EVT3 Pin

8.4.2 EDMA Peripheral Register Description

The EDMA peripheral registers are described in the device-specific Technical Reference Manual. Each register is documented as an offset from a base address for the peripheral. The base addresses for all of the peripherals are in the device memory map (see Section 2.10).

8.5 Emulation Features and Capability

8.5.1 Advanced Event Triggering (AET)

The device supports Advanced Event Triggering (AET). This capability can be used to debug complex problems as well as understand performance characteristics of user applications. AET provides the following capabilities:

- **Hardware Program Breakpoints:** specify addresses or address ranges that can generate events such as halting the processor or triggering the trace capture.
- **Data Watchpoints:** specify data variable addresses, address ranges, or data values that can generate events such as halting the processor or triggering the trace capture.
- **Counters:** count the occurrence of an event or cycles for performance monitoring.
- **State Sequencing:** allows combinations of hardware program breakpoints and data watchpoints to precisely generate events for complex sequences.

For more information on AET, see the following documents:

- *Using Advanced Event Triggering to Find and Fix Intermittent Real-Time Bugs* application report (Literature Number: SPRA753).
- *Using Advanced Event Triggering to Debug Real-Time Problems in High Speed Embedded Microprocessor Systems* application report (Literature Number: SPRA387).

8.5.2 Trace

The device supports Trace at the Cortex™-A8 and System levels. Trace is a debug technology that provides a detailed, historical account of application code execution, timing, and data accesses. Trace collects, compresses, and exports debug information for analysis. The debug information can be exported to the Embedded Trace Buffer (ETB), or to the 5-pin Trace Interface (system trace only). Trace works in real-time and does not impact the execution of the system.

For more information on board design guidelines for Trace Advanced Emulation, see the *Emulation and Trace Headers Technical Reference Manual* (Literature Number: SPRU655).

8.5.3 IEEE 1149.1 JTAG

The JTAG (IEEE Standard 1149.1-1990 Standard-Test-Access Port and Boundary Scan Architecture) interface is used for BSDL testing and emulation of the device. The TRST pin only needs to be released when it is necessary to use a JTAG controller to debug the device or exercise the device's boundary scan functionality. For maximum reliability, the device includes an internal pulldown (IPD) on the TRST pin to ensure that TRST is always asserted upon power up and the device's internal emulation logic is always properly initialized. JTAG controllers from Texas Instruments actively drive TRST high. However, some third-party JTAG controllers may not drive TRST high but expect the use of a pullup resistor on TRST. When using this type of JTAG controller, assert TRST to initialize the device after powerup and externally drive TRST high before attempting any emulation or boundary-scan operations.

The main JTAG features include:

- 32KB embedded trace buffer (ETB)
- 5-pin system trace interface for debug
- Supports Advanced Event Triggering (AET)
- All processors can be emulated via JTAG ports
- All functions on EMU pins of the device:
  - EMU[1:0] - cross-triggering, boot mode (WIR), STM trace
  - EMU[4:2] - STM trace only (single direction)

8.5.3.1 JTAG ID (JTAGID) Register Description

Table 8-5. JTAG ID Register(1)

HEX ADDRESS	ACRONYM	REGISTER NAME
0x4814 0600	JTAGID	JTAG Identification Register(2)

(1) IEEE Standard 1149.1-1990 Standard-Test-Access Port and Boundary Scan Architecture.
(2) Read-only. Provides the device 32-bit JTAG ID.

The JTAG ID register is a read-only register that identifies to the customer the JTAG/device ID. For this device, the JTAG ID register resides at address location 0x4814 0600. For the actual register bit names and their associated bit field descriptions, see Figure 8-5 and Table 8-6.

31 28	27 12	11 1	0
VARIANT (4-bit)	PART NUMBER (16-bit)	MANUFACTURER (11-bit)	LSB
R-xxxx	R-1011 1001 0110 1011	R-0000 0010 111	R-1

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Figure 8-5. JTAG ID Register Description - Device Register Value: 0x0B8F 202F

Table 8-6. JTAG ID Register Selection Bit Descriptions

Bit	Field	Description
31:28	VARIANT	Variant (4-bit) value. Device value: xxxx. This value reflects the device silicon revision [For example, 0x0 (0000) for initial silicon (1.0)]. For more detailed information on the current device silicon revision, see the device-specific *Silicon Errata*.
27:12	PART NUMBER	Part Number (16-bit) value. Device value: 0xB96B (1011 1001 0110 1011)
11:1	MANUFACTURER	Manufacturer (11-bit) value. Device value: 0x017 (0000 0010 111)
0	LSB	LSB. This bit is read as a ""1 for this device.

8.5.3.2 JTAG Electrical Data/Timing

Table 8-7. Timing Requirements for IEEE 1149.1 JTAG

(see Figure 8-6)

NO.			OPP100/OPP120/ Turbo/Nitro		UNIT
			MIN	MAX	
1	$t_{c(TCK)}$	Cycle time, TCK	59		ns
1a	$t_{w(TCKH)}$	Pulse duration, TCK high (40% of t_c)	23.6		ns
1b	$t_{w(TCKL)}$	Pulse duration, TCK low (40% of t_c)	23.6		ns
3	$t_{su(TDI-TCK)}$	Input setup time, TDI valid to TCK high (20% of (t_c * 0.5))	5.9		ns
3	$t_{su(TMS-TCK)}$	Input setup time, TMS valid to TCK high (20% of (t_c * 0.5))	5.9		ns
4	$t_{h(TCK-TDI)}$	Input hold time, TDI valid from TCK high	29.5		ns
	$t_{h(TCK-TMS)}$	Input hold time, TMS valid from TCK high	29.5		ns

Table 8-8. Switching Characteristics Over Recommended Operating Conditions for IEEE 1149.1 JTAG

(see Figure 8-6)

NO.	PARAMETER		OPP100/OPP120/ Turbo/Nitro		UNIT
			MIN	MAX	
2	$t_{d(TCKL-TDOV)}$	Delay time, TCK low to TDO valid	0	23.575(1)	ns

(1) (0.5 * t_c) - 2

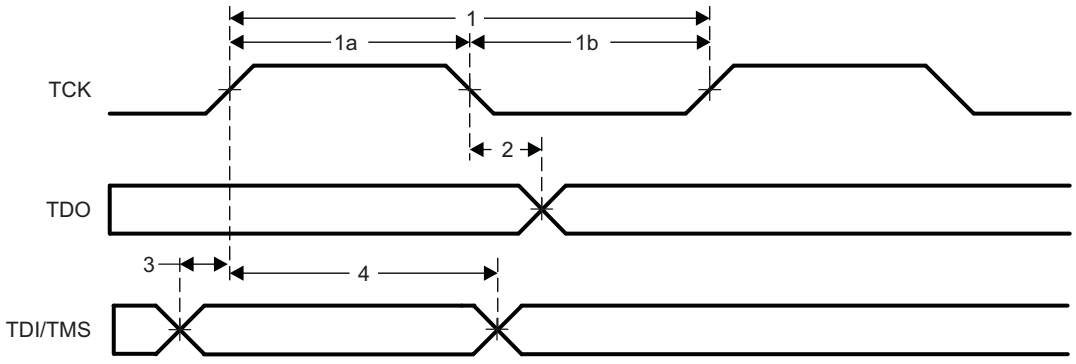


Figure 8-6. JTAG Timing

Table 8-9. Timing Requirements for IEEE 1149.1 JTAG With RTCK

(see Figure 8-6)

NO.			OPP100/OPP120/ Turbo/Nitro		UNIT
			MIN	MAX	
1	$t_{c(TCK)}$	Cycle time, TCK	59		ns
1a	$t_{w(TCKH)}$	Pulse duration, TCK high (40% of t_c)	23.6		ns
1b	$t_{w(TCKL)}$	Pulse duration, TCK low (40% of t_c)	23.6		ns
3	$t_{su(TDI-TCK)}$	Input setup time, TDI valid to TCK high (20% of (t_c * 0.5))	5.9		ns
3	$t_{su(TMS-TCK)}$	Input setup time, TMS valid to TCK high (20% of (t_c * 0.5))	5.9		ns
4	$t_{h(TCK-TDI)}$	Input hold time, TDI valid from TCK high	29.5		ns
	$t_{h(TCK-TMS)}$	Input hold time, TMS valid from TCK high	29.5		ns

Table 8-10. Switching Characteristics Over Recommended Operating Conditions for IEEE 1149.1 JTAG With RTCK

(see Figure 8-7)

NO.	PARAMETER		OPP100/OPP120/ Turbo/Nitro		UNIT
			MIN	MAX	
5	$t_{d(TCK-RTCK)}$	Delay time, TCK to RTCK with no selected subpaths (that is, ICEPick is the only tap selected - when the ARM is in the scan chain, the delay time is a function of the ARM functional clock.)	0	24	ns
6	$t_{c(RTCK)}$	Cycle time, RTCK	59		ns
7	$t_{w(RTCKH)}$	Pulse duration, RTCK high (40% of t_c)	23.6		ns
8	$t_{w(RTCKL)}$	Pulse duration, RTCK low (40% of t_c)	23.6		ns

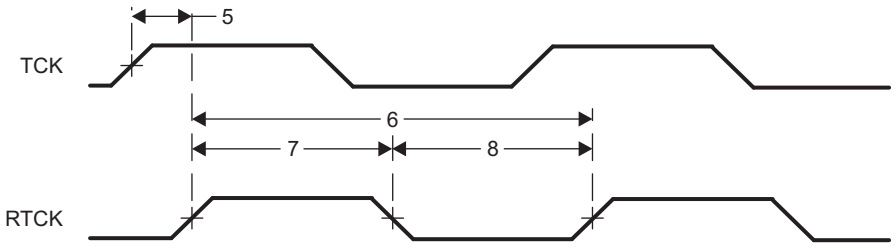


Figure 8-7. JTAG With RTCK Timing

Table 8-11. Switching Characteristics Over Recommended Operating Conditions for STM Trace

(see Figure 8-8)

NO.	PARAMETER		OPP100/OPP120/ Turbo/Nitro		UNIT
			MIN	MAX	
1	$t_{w(EMUH50)}$	Pulse duration, EMUx high detected at 50% V_{OH} with 60/40 duty cycle	4 (1)		ns
	$t_{w(EMUH90)}$	Pulse duration, EMUx high detected at 90% V_{OH}	3.5		ns
2	$t_{w(EMUL50)}$	Pulse duration, EMUx low detected at 50% V_{OH} with 60/40 duty cycle	4 (1)		ns
	$t_{w(EMUL10)}$	Pulse duration, EMUx low detected at 10% V_{OH}	3.5		ns
3	$t_{sko(EMU)}$	Output skew time, time delay difference between EMUx pins configured as trace.	-0.5	0.5	ns
	$t_{skp(EMU)}$	Pulse skew, magnitude of difference between high-to-low (t_{PHL}) and low-to-high (t_{PLH}) propagation delays		0.6 (1)	ns
	$t_{sldp\_o(EMU)}$	Output slew rate EMUx	3.3		V/ns

(1) This parameter applies to the maximum trace export frequency operating in a 40/60 duty cycle.

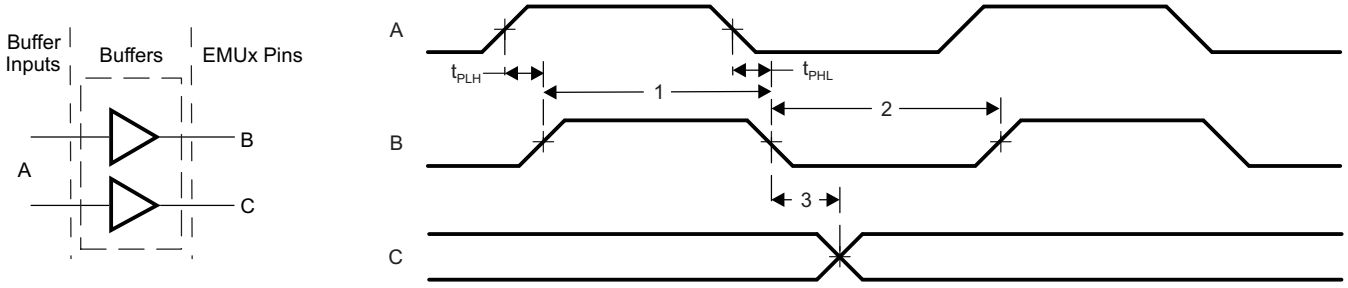


Figure 8-8. STM Trace Timing

8.6 General-Purpose Input/Output (GPIO)

The GPIO peripheral provides general-purpose pins that can be configured as either inputs or outputs. When configured as an output, a write to an internal register controls the state driven on the output pin. When configured as an input, the state of the input is detectable by reading the state of an internal register. In addition, the GPIO peripheral can produce CPU interrupts in different interrupt generation modes. The GPIO peripheral provides generic connections to external devices.

The device contains four GPIO modules and each GPIO module consists of up to 32 identical channels.

The device GPIO peripheral supports the following:

- Up to 125 1.8-V/3.3-V GPIO pins, GP0[0:28], GP1[0:31], GP2[0:31], and GP3[0:31] (the exact number available varies as a function of the device configuration). Each channel can be configured to be used in the following applications:
  - Data input/output
  - Keyboard interface with a de-bouncing cell
  - Synchronous interrupt generation (in active mode) upon the detection of external events (signal transitions and/or signal levels).
- Synchronous interrupt requests from each channel are processed by four identical interrupt generation sub-modules to be used independently by the ARM or Media Controller. Interrupts can be triggered by rising and/or falling edge, specified for each interrupt-capable GPIO signal.
- Shared registers can be accessed through "Set & Clear" protocol. Software writes 1 to corresponding bit positions to set or to clear GPIO signals. This allows multiple software processes to toggle GPIO output signals without critical section protection (disable interrupts, program GPIO, re-enable interrupts, to prevent context switching to another process during GPIO programming).
- Separate input/output registers.
- Output register in addition to set/clear so that, if preferred by software, some GPIO output signals can be toggled by direct write to the output registers.
- Output register, when read, reflects output drive status. This, in addition to the input register reflecting pin status and open-drain I/O cell, allows wired logic to be implemented.

For more detailed information on GPIOs, see the *General-Purpose I/O (GPIO) Interface* chapter in the device-specific Technical Reference Manual.

8.6.1 GPIO Peripheral Register Descriptions

The GPIO peripheral registers are described in the device-specific Technical Reference Manual. Each register is documented as an offset from a base address for the peripheral. The base addresses for all of the peripherals are in the device memory map (see Section 2.10).

8.6.2 GPIO Electrical Data/Timing

Table 8-12. Timing Requirements for GPIO Inputs

(see Figure 8-9)

NO.			OPP100/OPP120/ Turbo/Nitro		UNIT
			MIN	MAX	
1	$t_{w(GPIH)}$	Pulse duration, GPx[31:0] input high	12P(1)		ns
2	$t_{w(GPIL)}$	Pulse duration, GPx[31:0] input low	12P(1)		ns

(1) P = Module clock.

Table 8-13. Switching Characteristics Over Recommended Operating Conditions for GPIO Outputs

(see Figure 8-9)

NO.	PARAMETER		OPP100/OPP120/ Turbo/Nitro		UNIT
			MIN	MAX	
3	$t_{w(GPOH)}$	Pulse duration, GPx[31:0] output high	36P-8(1)		ns
4	$t_{w(GPOL)}$	Pulse duration, GPx[31:0] output low	36P-8(1)		ns

(1) P = Module clock.

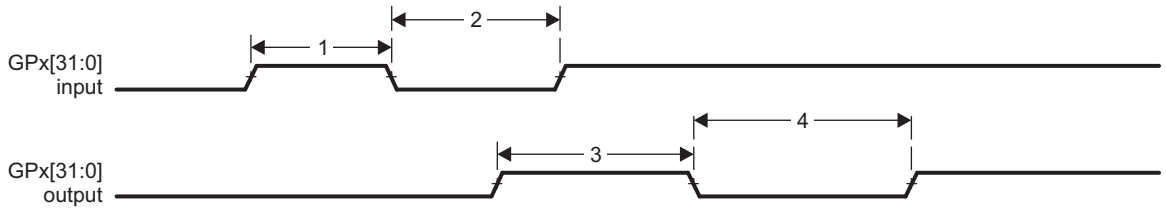


Figure 8-9. GPIO Port Timing

8.7 General-Purpose Memory Controller (GPMC) and Error Location Module (ELM)

The GPMC is a device memory controller used to provide a glueless interface to external memory devices such as NOR Flash, NAND Flash (with BCH and Hamming Error Code Detection for 8-bit or 16-bit NAND Flash), SRAM, and Pseudo-SRAM. It includes flexible asynchronous protocol control for interface to SRAM-like memories and custom logic (FPGA, CPLD, ASICs, etc.).

Other supported features include:

- 8-/16-bit wide multiplexed address/data bus
- 512 MBytes maximum addressing capability divided among up to eight chip selects
- Non-multiplexed address/data mode
- Pre-fetch and write posting engine associated with system DMA to get full performance from NAND device with minimum impact on NOR/SRAM concurrent access.

The device also contains an Error Locator Module (ELM) which is used to extract error addresses from syndrome polynomials generated using a BCH algorithm. Each of these polynomials gives a status of the read operations for a 512 bytes block from a NAND flash and its associated BCH parity bits, plus optionally spare area information. The ELM has the following features:

- 4-bit, 8-bit and 16-bit per 512byte block error location based on BCH algorithms
- Eight simultaneous processing contexts
- Page-based and continuous modes
- Interrupt generation on error location process completion
  - When the full page has been processed in page mode
  - For each syndrome polynomial in continuous mode

8.7.1 GPMC and ELM Peripherals Register Descriptions

The GPMC and ELM peripheral registers are described in the device-specific Technical Reference Manual. Each register is documented as an offset from a base address for the peripheral. The base addresses for all of the peripherals are in the device memory map (see Section 2.10).

8.7.2 GPMC Electrical Data/Timing

8.7.2.1 GPMC and NOR Flash Interface Synchronous Mode Timing (Non-Multiplexed and Multiplexed Modes)

Table 8-14. Timing Requirements for GPMC and NOR Flash Interface - Synchronous Mode

(see Figure 8-10, Figure 8-11, Figure 8-12 for Non-Multiplexed Modes)
(see Figure 8-13, Figure 8-14, Figure 8-15 for Multiplexed Modes)

NO.			OPP100/OPP120/Turbo/Nitro		UNIT
			MIN	MAX	
13	$t_{su(DV-CLKH)}$	Setup time, read GPMC_D[15:0] valid before GPMC_CLK high	3.2		ns
14	$t_{h(CLKH-DV)}$	Hold time, read GPMC_D[15:0] valid after GPMC_CLK high	2.5		ns
22	$t_{su(WAITV-CLKH)}$	Setup time, GPMC_WAIT[x] valid before GPMC_CLK high	3.2		ns
23	$t_{h(CLKH-WAITV)}$	Hold time, GPMC_WAIT[x] valid after GPMC_CLK high	2.5		ns

Table 8-15. Switching Characteristics Over Recommended Operating Conditions for GPMC and NOR Flash Interface - Synchronous Mode

(see Figure 8-10, Figure 8-11, Figure 8-12 for Non-Multiplexed Modes)
(see Figure 8-13, Figure 8-14, Figure 8-15 for Multiplexed Modes)

NO.	PARAMETER		OPP100/OPP120/Turbo/Nitro		UNIT
			MIN	MAX	
1	$t_{c(CLK)}$	Cycle time, output clock GPMC_CLK period	16 (1)		ns
2	$t_{w(CLKH)}$	Pulse duration, output clock GPMC_CLK high	0.5P (2)		ns
	$t_{w(CLKL)}$	Pulse duration, output clock GPMC_CLK low	0.5P (2)		
3	$t_{d(CLKH-nCSV)}$	Delay time, GPMC_CLK rising edge to $\overline{\text{GPMC\_CS[x]}}$ transition	F - 2.2 (3)	F + 4.5 (3)	ns
4	$t_{d(CLKH-nCSIV)}$	Delay time, GPMC_CLK rising edge to $\overline{\text{GPMC\_CS[x]}}$ invalid	E - 2.2 (4)	E + 4.5 (4)	ns
5	$t_{d(ADDV-CLK)}$	Delay time, GPMC_A[27:0] address bus valid to GPMC_CLK first edge	B - 4.5 (5)	B + 2.3 (5)	ns
6	$t_{d(CLKH-ADDIV)}$	Delay time, GPMC_CLK rising edge to GPMC_A[27:0] GPMC address bus invalid	-2.3		ns
7	$t_{d(nBEV-CLK)}$	Delay time, GPMC_$\overline{\text{BE0}}$_CLE, $\overline{\text{GPMC\_BE1}}$ valid to GPMC_CLK first edge	B - 1.9 (5)	B + 2.3 (5)	ns
8	$t_{d(CLKH-nBEIV)}$	Delay time, GPMC_CLK rising edge to GPMC_$\overline{\text{BE0}}$_CLE, $\overline{\text{GPMC\_BE1}}$ invalid	D - 2.3 (6)	D + 1.9 (6)	ns

(1) Sync mode = 62.5 MHz; Async mode = 125 MHz.
(2) P = GPMC_CLK period.
(3) For nCS falling edge (CS activated):
- For GpmcFCLKDivider = 0:
  F = 0.5 * CSExtraDelay * GPMC_FCLK
- For GpmcFCLKDivider = 1:
  F = 0.5 * CSExtraDelay * GPMC_FCLK if (ClkActivationTime and CSOnTime are odd) or (ClkActivationTime and CSOnTime are even)
  F = (1 + 0.5 * CSExtraDelay) * GPMC_FCLK otherwise
- For GpmcFCLKDivider = 2:
  F = 0.5 * CSExtraDelay * GPMC_FCLK if ((CSOnTime – ClkActivationTime) is a multiple of 3)
  F = (1 + 0.5 * CSExtraDelay) * GPMC_FCLK if ((CSOnTime – ClkActivationTime – 1) is a multiple of 3)
  F = (2 + 0.5 * CSExtraDelay) * GPMC_FCLK if ((CSOnTime – ClkActivationTime – 2) is a multiple of 3)

(4) For single read: E = (CSRdOffTime – AccessTime) * (TimeParaGranularity + 1) * GPMC_FCLK
For burst read: E = (CSRdOffTime – AccessTime) * (TimeParaGranularity + 1) * GPMC_FCLK
For burst write: E = (CSWrOffTime – AccessTime) * (TimeParaGranularity + 1) * GPMC_FCLK
(5) B = ClkActivationTime * GPMC_FCLK
(6) For single read: D = (RdCycleTime – AccessTime) * (TimeParaGranularity + 1) * GPMC_FCLK
For burst read: D = (RdCycleTime – AccessTime) * (TimeParaGranularity + 1) * GPMC_FCLK
For burst write: D = (WrCycleTime – AccessTime) * (TimeParaGranularity + 1) * GPMC_FCLK

Table 8-15. Switching Characteristics Over Recommended Operating Conditions for GPMC and NOR Flash Interface - Synchronous Mode (continued)

(see Figure 8-10, Figure 8-11, Figure 8-12 for Non-Multiplexed Modes)
(see Figure 8-13, Figure 8-14, Figure 8-15 for Multiplexed Modes)

NO.	PARAMETER		OPP100/OPP120/Turbo/Nitro		UNIT
			MIN	MAX	
9	$t_{d(CLKH-nADV)}$	Delay time, GPMC_CLK rising edge to GPMC_$\overline{ADV}$_ALE transition	G - 2.3(7)	G + 4.5(7)	ns
10	$t_{d(CLKH-nADVIV)}$	Delay time, GPMC_CLK rising edge to GPMC_$\overline{ADV}$_ALE invalid	D - 2.3(6)	D + 4.5(6)	ns
11	$t_{d(CLKH-nOE)}$	Delay time, GPMC_CLK rising edge to $\overline{GPMC\_OE\_RE}$ transition	H - 2.3(8)	H + 3.5(8)	ns
12	$t_{d(CLKH-nOEIV)}$	Delay time, GPMC_CLK rising edge to $\overline{GPMC\_OE\_RE}$ invalid	E - 2.3(4)	E + 3.5(4)	ns

(7) For ADV falling edge (ADV activated):
- Case GpmcFCLKDivider = 0:
  G = 0.5 * ADVExtraDelay * GPMC_FCLK
- Case GpmcFCLKDivider = 1:
  G = 0.5 * ADVExtraDelay * GPMC_FCLK if (ClkActivationTime and ADVOnTime are odd) or (ClkActivationTime and ADVOnTime are even)
  G = (1 + 0.5 * ADVExtraDelay) * GPMC_FCLK otherwise
- Case GpmcFCLKDivider = 2:
  G = 0.5 * ADVExtraDelay * GPMC_FCLK if ((ADVOnTime – ClkActivationTime) is a multiple of 3)
  G = (1 + 0.5 * ADVExtraDelay) * GPMC_FCLK if ((ADVOnTime – ClkActivationTime – 1) is a multiple of 3)
  G = (2 + 0.5 * ADVExtraDelay) * GPMC_FCLK if ((ADVOnTime – ClkActivationTime – 2) is a multiple of 3)

For ADV rising edge (ADV deactivated) in Reading mode:
- Case GpmcFCLKDivider = 0:
  G = 0.5 * ADVExtraDelay * GPMC_FCLK
- Case GpmcFCLKDivider = 1:
  G = 0.5 * ADVExtraDelay * GPMC_FCLK if (ClkActivationTime and ADVRdOffTime are odd) or (ClkActivationTime and ADVRdOffTime are even)
  G = (1 + 0.5 * ADVExtraDelay) * GPMC_FCLK otherwise
- Case GpmcFCLKDivider = 2:
  G = 0.5 * ADVExtraDelay * GPMC_FCLK if ((ADVRdOffTime – ClkActivationTime) is a multiple of 3)
  G = (1 + 0.5 * ADVExtraDelay) * GPMC_FCLK if ((ADVRdOffTime – ClkActivationTime – 1) is a multiple of 3)
  G = (2 + 0.5 * ADVExtraDelay) * GPMC_FCLK if ((ADVRdOffTime – ClkActivationTime – 2) is a multiple of 3)

For ADV rising edge (ADV deactivated) in Writing mode:
- Case GpmcFCLKDivider = 0:
  G = 0.5 * ADVExtraDelay * GPMC_FCLK
- Case GpmcFCLKDivider = 1:
  G = 0.5 * ADVExtraDelay * GPMC_FCLK if (ClkActivationTime and ADVWrOffTime are odd) or (ClkActivationTime and ADVWrOffTime are even)
  G = (1 + 0.5 * ADVExtraDelay) * GPMC_FCLK otherwise
- Case GpmcFCLKDivider = 2:
  G = 0.5 * ADVExtraDelay * GPMC_FCLK if ((ADVWrOffTime – ClkActivationTime) is a multiple of 3)
  G = (1 + 0.5 * ADVExtraDelay) * GPMC_FCLK if ((ADVWrOffTime – ClkActivationTime – 1) is a multiple of 3)
  G = (2 + 0.5 * ADVExtraDelay) * GPMC_FCLK if ((ADVWrOffTime – ClkActivationTime – 2) is a multiple of 3)

(8) For OE falling edge (OE activated) / IO DIR rising edge (IN direction) :
- Case GpmcFCLKDivider = 0:
  H = 0.5 * OEExtraDelay * GPMC_FCLK
- Case GpmcFCLKDivider = 1:
  H = 0.5 * OEExtraDelay * GPMC_FCLK if (ClkActivationTime and OEOnTime are odd) or (ClkActivationTime and OEOnTime are even)
  H = (1 + 0.5 * OEExtraDelay) * GPMC_FCLK otherwise
- Case GpmcFCLKDivider = 2:
  H = 0.5 * OEExtraDelay * GPMC_FCLK if ((OEOnTime – ClkActivationTime) is a multiple of 3)
  H = (1 + 0.5 * OEExtraDelay) * GPMC_FCLK if ((OEOnTime – ClkActivationTime – 1) is a multiple of 3)
  H = (2 + 0.5 * OEExtraDelay) * GPMC_FCLK if ((OEOnTime – ClkActivationTime – 2) is a multiple of 3)

For OE rising edge (OE deactivated):
- Case GpmcFCLKDivider = 0:
  H = 0.5 * OEExtraDelay * GPMC_FCLK
- Case GpmcFCLKDivider = 1:
  H = 0.5 * OEExtraDelay * GPMC_FCLK if (ClkActivationTime and OEOffTime are odd) or (ClkActivationTime and OEOffTime are even)
  H = (1 + 0.5 * OEExtraDelay) * GPMC_FCLK otherwise
- Case GpmcFCLKDivider = 2:
  H = 0.5 * OEExtraDelay * GPMC_FCLK if ((OEOffTime – ClkActivationTime) is a multiple of 3)
  H = (1 + 0.5 * OEExtraDelay) * GPMC_FCLK if ((OEOffTime – ClkActivationTime – 1) is a multiple of 3)
  H = (2 + 0.5 * OEExtraDelay) * GPMC_FCLK if ((OEOffTime – ClkActivationTime – 2) is a multiple of 3)

Table 8-15. Switching Characteristics Over Recommended Operating Conditions for GPMC and NOR Flash Interface - Synchronous Mode (continued)

(see Figure 8-10, Figure 8-11, Figure 8-12 for Non-Multiplexed Modes)
(see Figure 8-13, Figure 8-14, Figure 8-15 for Multiplexed Modes)

NO.	PARAMETER		OPP100/OPP120/Turbo/Nitro		UNIT
			MIN	MAX	
15	$t_{d(CLKH-nWE)}$	Delay time, GPMC_CLK rising edge to $\overline{\text{GPMC\_WE}}$ transition	I - 2.3 (9)	I + 4.5 (9)	ns
16	$t_{d(CLKH-Data)}$	Delay time, GPMC_CLK rising edge to GPMC_D[15:0] data bus transition	J - 2.3 (10)	J + 1.9 (10)	ns
18	$t_{d(CLKH-nBE)}$	Delay time, GPMC_CLK rising edge to GPMC_$\overline{\text{BE0}}$_CLE, $\overline{\text{GPMC\_BE1}}$ transition	J - 2.3 (10)	J + 1.9 (10)	ns
19	$t_{w(nCSV)}$	Pulse duration, $\overline{\text{GPMC\_CS[x]}}$ low	A (11)		ns
20	$t_{w(nBEV)}$	Pulse duration, GPMC_$\overline{\text{BE0}}$_CLE, $\overline{\text{GPMC\_BE1}}$ low	C (12)		ns
21	$t_{w(nADVV)}$	Pulse duration, GPMC_$\overline{\text{ADV}}$_ALE low	K (13)		ns

(9) For WE falling edge (WE activated):
- Case GpmcFCLKDivider = 0:
  I = 0.5 * WEExtraDelay * GPMC_FCLK
- Case GpmcFCLKDivider = 1:
  I = 0.5 * WEExtraDelay * GPMC_FCLK if (ClkActivationTime and WEOnTime are odd) or (ClkActivationTime and WEOnTime are even)
  I = (1 + 0.5 * WEExtraDelay) * GPMC_FCLK otherwise
- Case GpmcFCLKDivider = 2:
  I = 0.5 * WEExtraDelay * GPMC_FCLK if ((WEOnTime – ClkActivationTime) is a multiple of 3)
  I = (1 + 0.5 * WEExtraDelay) * GPMC_FCLK if ((WEOnTime – ClkActivationTime – 1) is a multiple of 3)
  I = (2 + 0.5 * WEExtraDelay) * GPMC_FCLK if ((WEOnTime – ClkActivationTime – 2) is a multiple of 3)

For WE rising edge (WE deactivated):
- Case GpmcFCLKDivider = 0:
  I = 0.5 * WEExtraDelay * GPMC_FCLK
- Case GpmcFCLKDivider = 1:
  I = 0.5 * WEExtraDelay * GPMC_FCLK if (ClkActivationTime and WEOffTime are odd) or (ClkActivationTime and WEOffTime are even)
  I = (1 + 0.5 * WEExtraDelay) * GPMC_FCLK otherwise
- Case GpmcFCLKDivider = 2:
  I = 0.5 * WEExtraDelay * GPMC_FCLK if ((WEOffTime – ClkActivationTime) is a multiple of 3)
  I = (1 + 0.5 * WEExtraDelay) * GPMC_FCLK if ((WEOffTime – ClkActivationTime – 1) is a multiple of 3)
  I = (2 + 0.5 * WEExtraDelay) * GPMC_FCLK if ((WEOffTime – ClkActivationTime – 2) is a multiple of 3)

(10) J = GPMC_FCLK period.

(11) For single read: A = (CSRdOffTime - CSOnTime) * (TimeParaGranularity + 1) * GPMC_FCLK period
For burst read: A = (CSRdOffTime - CSOnTime + (n - 1) * PageBurstAccessTime) * (TimeParaGranularity + 1) * GPMC_FCLK period [n = page burst access number]
For burst write: A = (CSWrOffTime - CSOnTime + (n - 1) * PageBurstAccessTime) * (TimeParaGranularity + 1) * GPMC_FCLK period [n = page burst access number]

(12) For single read: C = RdCycleTime * (TimeParaGranularity + 1) * GPMC_FCLK
For burst read: C = (RdCycleTime + (n – 1) * PageBurstAccessTime) * (TimeParaGranularity + 1) * GPMC_FCLK [n = page burst access number]
For Burst write: C = (WrCycleTime + (n – 1) * PageBurstAccessTime) * (TimeParaGranularity + 1) * GPMC_FCLK [n = page burst access number]

(13) For read: K = (ADVRdOffTime - ADVOnTime) * (TimeParaGranularity + 1) * GPMC_FCLK
For write: K = (ADVWrOffTime - ADVOnTime) * (TimeParaGranularity + 1) * GPMC_FCLK

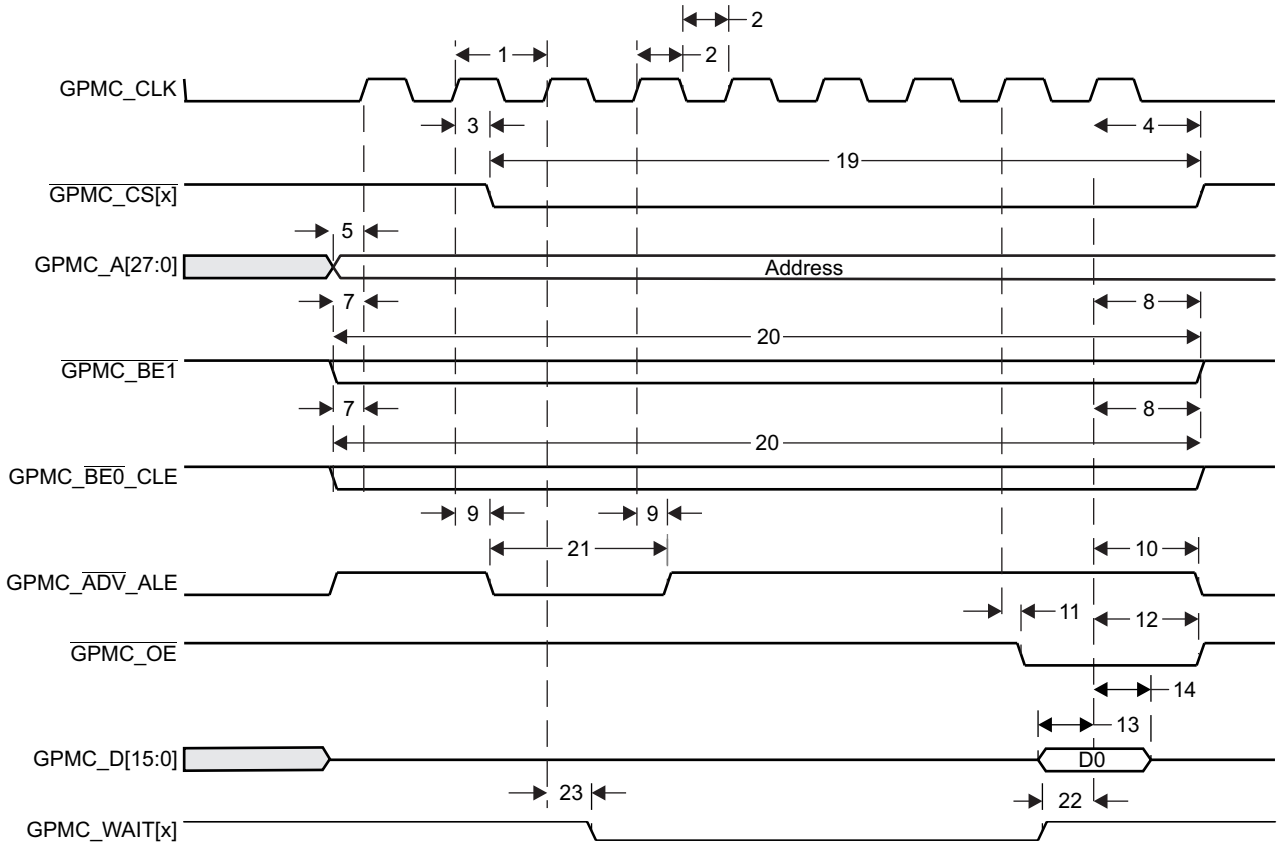


Figure 8-10. GPMC Non-Multiplexed NOR Flash - Synchronous Single Read (GPMCFCLKDIVIDER = 0)

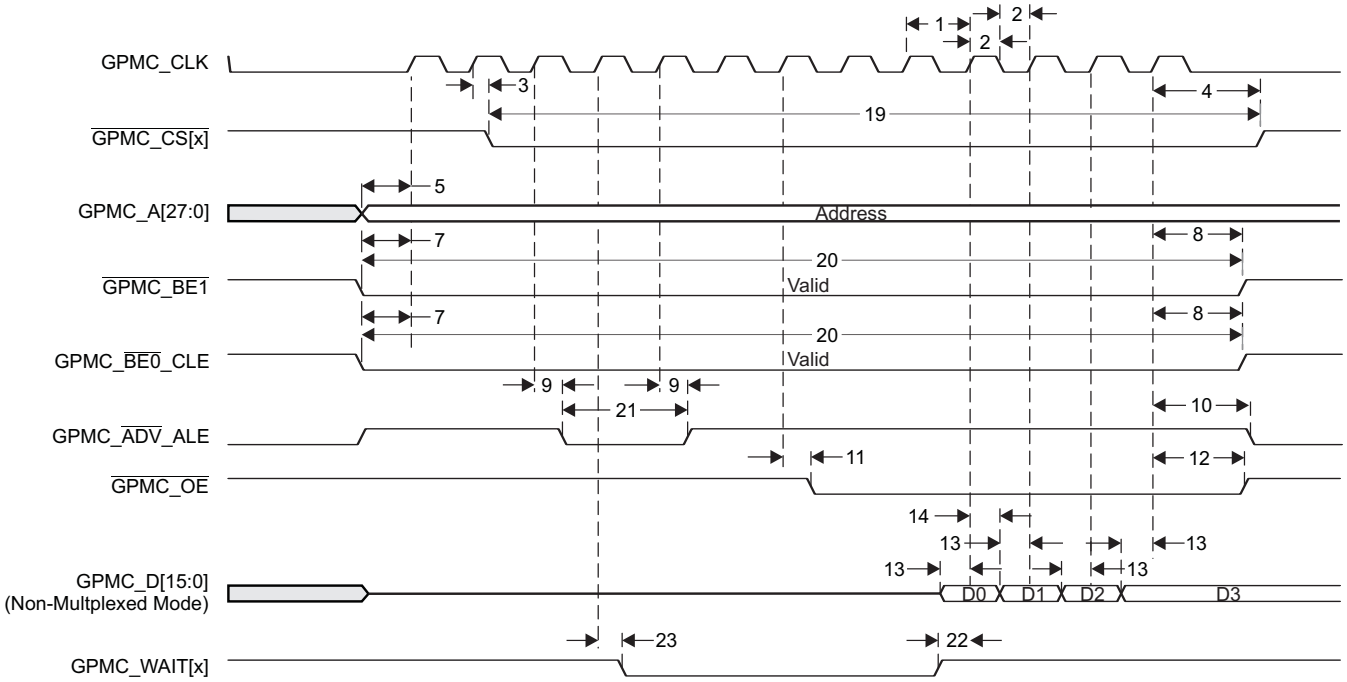


Figure 8-11. GPMC Non-Multiplexed NOR Flash - 14x16-bit Synchronous Burst Read (GPMCFCLKDIVIDER = 0)

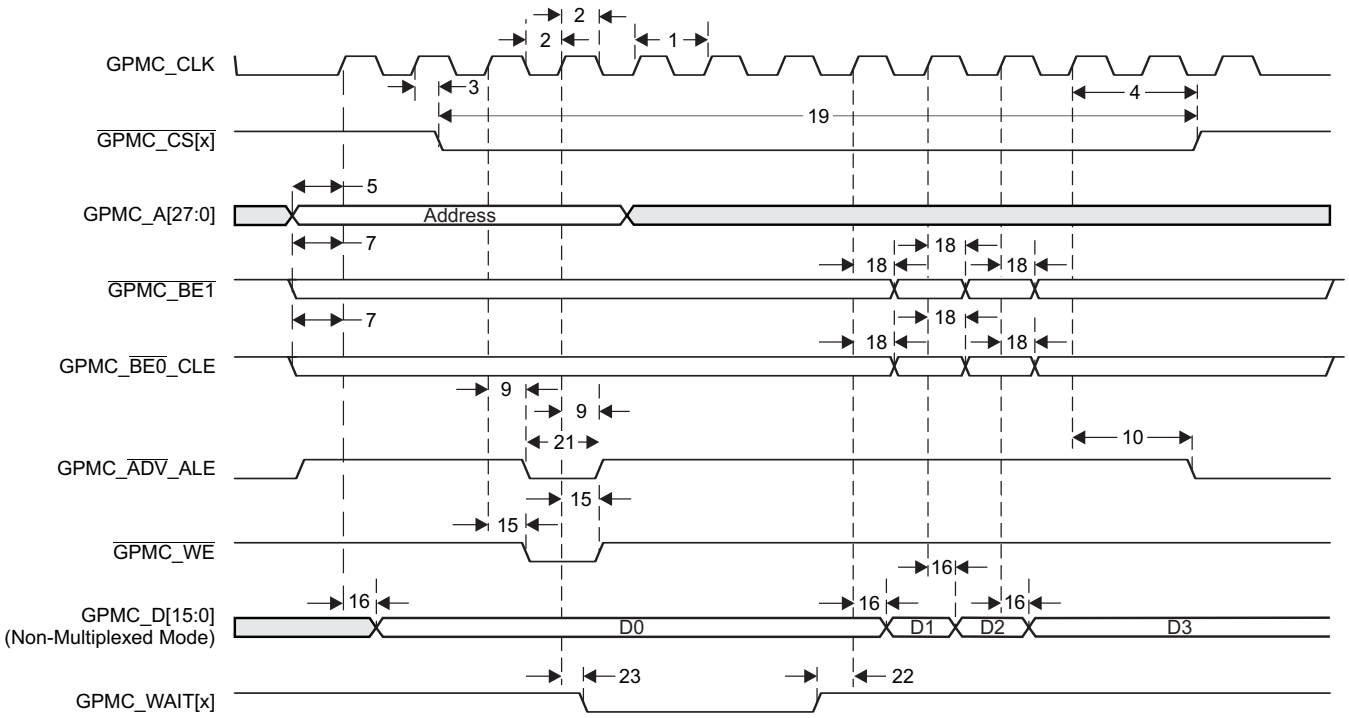


Figure 8-12. GPMC Non-Multiplexed NOR Flash - Synchronous Burst Write (GPMCFCLKDIVIDER = 0)

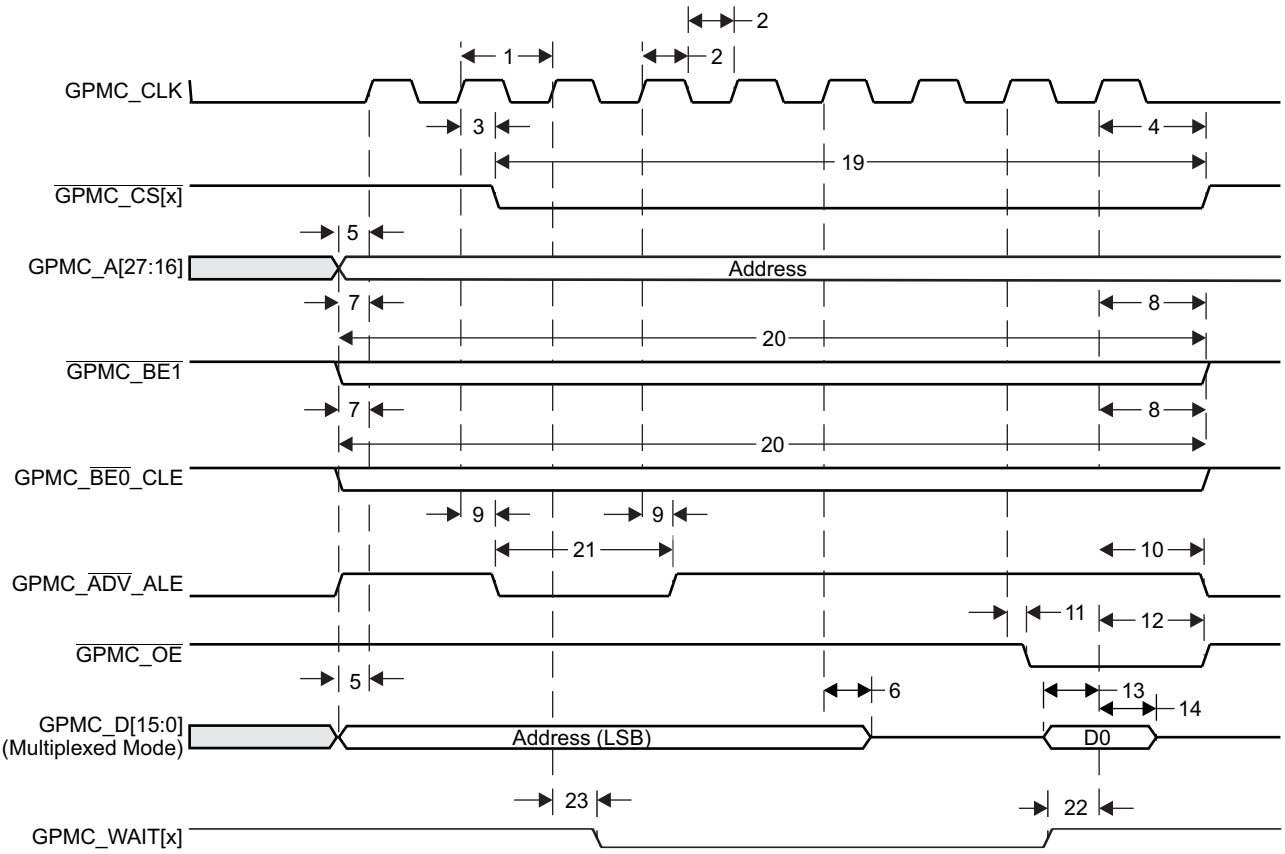


Figure 8-13. GPMC Multiplexed NOR Flash - Synchronous Single Read (GPMCFCLKDIVIDER = 0)

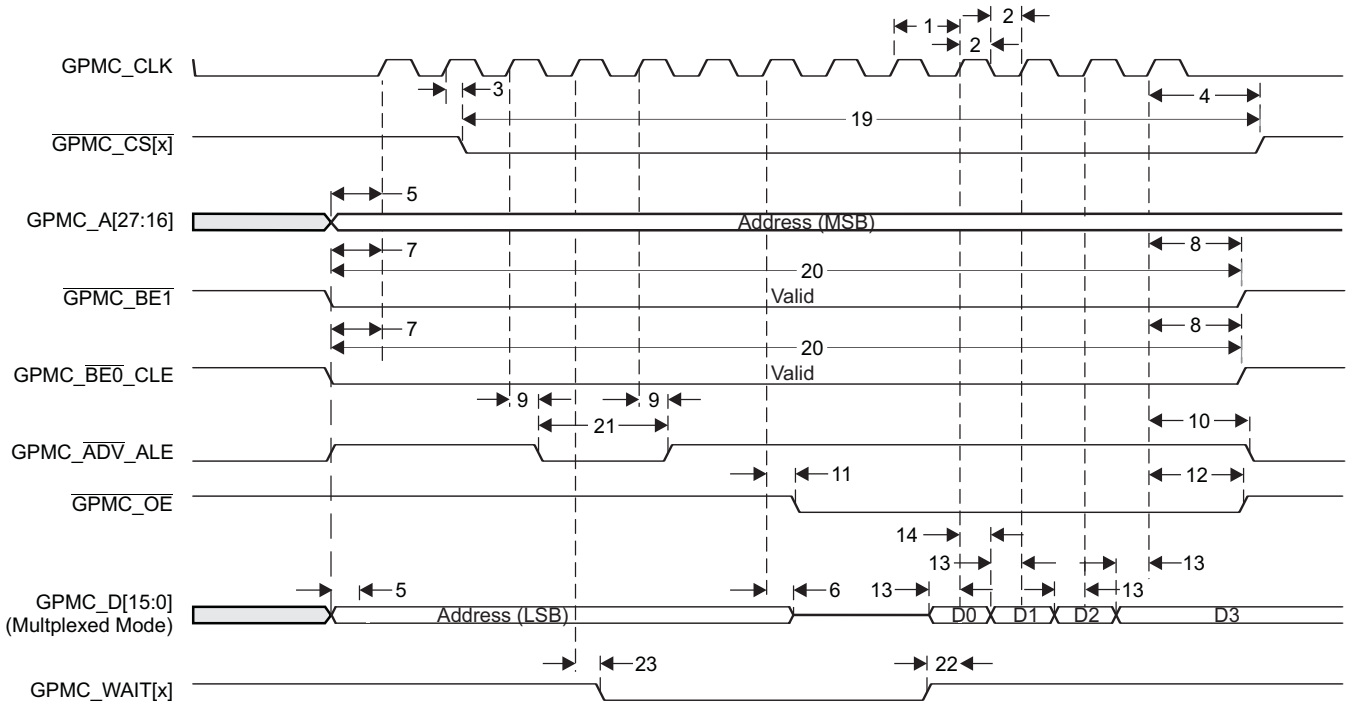


Figure 8-14. GPMC Multiplexed NOR Flash - 14x16-bit Synchronous Burst Read (GPMCFCLKDIVIDER = 0)

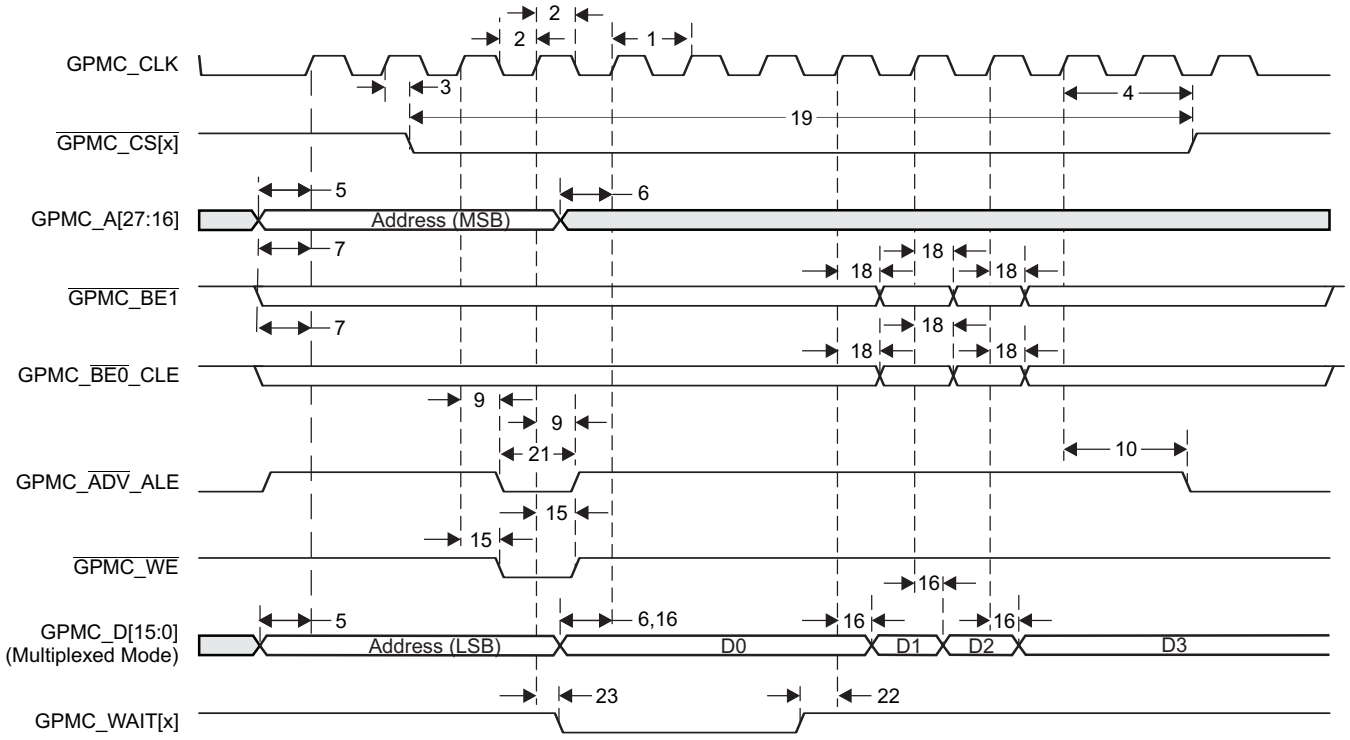


Figure 8-15. GPMC Non-Multiplexed NOR Flash - Synchronous Burst Write (GPMCFCLKDIVIDER = 0)

8.7.2.2 GPMC and NOR Flash Interface Asynchronous Mode Timing (Non-Multiplexed and Multiplexed Modes)

Table 8-16. Timing Requirements for GPMC and NOR Flash Interface - Asynchronous Mode

(see Figure 8-16, Figure 8-17 for Non-Multiplexed Mode)
(see Figure 8-18, Figure 8-20 for Multiplexed Mode)

NO.			OPP100/OPP120/Turbo/Nitro		UNIT
			MIN	MAX	
6	$t_{acc(DAT)}$	Data maximum access time (GPMC_FCLK cycles)		H (1)	cycles
21	$t_{acc1\text{-}pgmode(DAT)}$	Page mode successive data maximum access time (GPMC_FCLK cycles)		P (2)	cycles
22	$t_{acc2\text{-}pgmode(DAT)}$	Page mode first data maximum access time (GPMC_FCLK cycles)		H (1)	cycles

(1) H = AccessTime * (TimeParaGranularity + 1)
(2) P = PageBurstAccessTime * (TimeParaGranularity + 1).

Table 8-17. Switching Characteristics Over Recommended Operating Conditions for GPMC and NOR Flash Interface - Asynchronous Mode

(see Figure 8-16, Figure 8-17, Figure 8-18, Figure 8-19 for Non-Multiplexed Modes)
(see Figure 8-20, Figure 8-21 for Multiplexed Modes)

NO.	PARAMETER		OPP100/OPP120/Turbo/Nitro		UNIT
			MIN	MAX	
1	$t_{w(nBEV)}$	Pulse duration, GPMC_$\overline{BE0}$_CLE, $\overline{GPMC\_BE1}$ valid time		N (1)	ns
2	$t_{w(nCSV)}$	Pulse duration, $\overline{GPMC\_CS[x]}$ low		A (2)	ns
4	$t_{d(nCSV\text{-}nADVIV)}$	Delay time, $\overline{GPMC\_CS[x]}$ valid to GPMC_NADV_ALE invalid	B - 0.2 (3)	B + 2.0 (3)	ns
5	$t_{d(nCSV\text{-}nOEIV)}$	Delay time, $\overline{GPMC\_CS[x]}$ valid to $\overline{GPMC\_OE\_RE}$ invalid (single read)	C - 0.2 (4)	C + 2.0 (4)	ns
10	$t_{d(AV\text{-}nCSV)}$	Delay time, GPMC_A[27:0] address bus valid to $\overline{GPMC\_CS[x]}$ valid	J - 0.2 (5)	J + 2.0 (5)	ns
11	$t_{d(nBEV\text{-}nCSV)}$	Delay time, GPMC_$\overline{BE0}$_CLE, $\overline{GPMC\_BE1}$ valid to $\overline{GPMC\_CS[x]}$ valid	J - 0.2 (5)	J + 2.0 (5)	ns
13	$t_{d(nCSV\text{-}nADVV)}$	Delay time, $\overline{GPMC\_CS[x]}$ valid to GPMC_$\overline{ADV}$_ALE valid	K - 0.2 (6)	K + 2.0 (6)	ns
14	$t_{d(nCSV\text{-}nOEV)}$	Delay time, $\overline{GPMC\_CS[x]}$ valid to $\overline{GPMC\_OE\_RE}$ valid	L - 0.2 (7)	L + 2.0 (7)	ns
17	$t_{w(AIV)}$	Pulse duration, GPMC_A[27:0] address bus invalid between 2 successive R/W accesses	G (8)		ns
19	$t_{d(nCSV\text{-}nOEIV)}$	Delay time, $\overline{GPMC\_CS[x]}$ valid to $\overline{GPMC\_OE\_RE}$ invalid (burst read)	I - 0.2 (9)	I + 2.0 (9)	ns
21	$t_{w(AV)}$	Pulse duration, GPMC_A[27:0] address bus valid: second, third and fourth accesses	D (10)		ns
26	$t_{d(nCSV\text{-}nWEV)}$	Delay time, $\overline{GPMC\_CS[x]}$ valid to $\overline{GPMC\_WE}$ valid	E - 0.2 (11)	E + 2.0 (11)	ns

(1) For single read: N = RdCycleTime * (TimeParaGranularity + 1) * GPMC_FCLK
For single write: N = WrCycleTime * (TimeParaGranularity + 1) * GPMC_FCLK
For burst read: N = (RdCycleTime + (n - 1) * PageBurstAccessTime) * (TimeParaGranularity + 1) * GPMC_FCLK
For burst write: N = (WrCycleTime + (n - 1) * PageBurstAccessTime) * (TimeParaGranularity + 1) * GPMC_FCLK
(2) For single read: A = (CSRdOffTime - CSOnTime) * (TimeParaGranularity + 1) * GPMC_FCLK
For single write: A = (CSWrOffTime - CSOnTime) * (TimeParaGranularity + 1) * GPMC_FCLK
For burst read: A = (CSRdOffTime - CSOnTime + (n - 1) * PageBurstAccessTime) * (TimeParaGranularity + 1) * GPMC_FCLK
For burst write: A = (CSWrOffTime - CSOnTime + (n - 1) * PageBurstAccessTime) * (TimeParaGranularity + 1) * GPMC_FCLK
(3) = B - nCS Max Delay + nADV Min Delay
For reading: B = ((ADVRdOffTime - CSOnTime) * (TimeParaGranularity + 1) + 0.5 * (ADVExtraDelay - CSExtraDelay)) * GPMC_FCLK
For writing: B = ((ADVWrOffTime - CSOnTime) * (TimeParaGranularity + 1) + 0.5 * (ADVExtraDelay - CSExtraDelay)) * GPMC_FCLK
(4) = C - nCS Max Delay + nOE Min Delay
C = ((OEOffTime - CSOnTime) * (TimeParaGranularity + 1) + 0.5 * (OEExtraDelay - CSExtraDelay)) * GPMC_FCLK
(5) = J - Address Max Delay + nCS Min Delay
J = (CSOnTime * (TimeParaGranularity + 1) + 0.5 * CSExtraDelay) * GPMC_FCLK
(6) = K - nCS Max Delay + nADV Min Delay
K = ((ADVOnTime - CSOnTime) * (TimeParaGranularity + 1) + 0.5 * (ADVExtraDelay - CSExtraDelay)) * GPMC_FCLK
(7) = L - nCS Max Delay + nOE Min Delay
L = ((OEOnTime - CSOnTime) * (TimeParaGranularity + 1) + 0.5 * (OEExtraDelay - CSExtraDelay)) * GPMC_FCLK
(8) G = Cycle2CycleDelay * GPMC_FCLK
(9) = I - nCS Max Delay + nOE Min Delay
I = ((OEOffTime + (n - 1) * PageBurstAccessTime - CSOnTime) * (TimeParaGranularity + 1) + 0.5 * (OEExtraDelay - CSExtraDelay)) * GPMC_FCLK
(10) D = PageBurstAccessTime * (TimeParaGranularity + 1) * GPMC_FCLK
(11) = E - nCS Max Delay + nWE Min Delay
E = ((WEOnTime - CSOnTime) * (TimeParaGranularity + 1) + 0.5 * (WEExtraDelay - CSExtraDelay)) * GPMC_FCLK

Table 8-17. Switching Characteristics Over Recommended Operating Conditions for GPMC and NOR Flash Interface - Asynchronous Mode (continued)

(see Figure 8-16, Figure 8-17, Figure 8-18, Figure 8-19 for Non-Multiplexed Modes)
(see Figure 8-20, Figure 8-21 for Multiplexed Modes)

NO.	PARAMETER		OPP100/OPP120/Turbo/Nitro		UNIT
			MIN	MAX	
28	$t_{d(nCSV-nWEIV)}$	Delay time, GPMC_CS[x] valid to GPMC_WE invalid	F - 0.2(12)	F + 2.0(12)	ns
29	$t_{d(nWEV-DV)}$	Delay time, GPMC_WE valid to GPMC_D[15:0] data bus valid		2.0	ns
30	$t_{d(DV-nCSV)}$	Delay time, GPMC_D[15:0] data bus valid to GPMC_CS[x] valid	J - 0.2(5)	J + 2.0(5)	ns
37	$t_{d(ADVV-AIV)}$	Delay time, GPMC_ADV_ALE valid to GPMC_D[15:0] address invalid		2.0	ns
38	$t_{d(nOEV-AIV)}$	Delay time, GPMC_OE_RE valid to GPMC_D[15:0] address/data busses phase end		2.0	ns
39	$t_{d(AIV-ADVV)}$	Delay time, GPMC_D[15:0] address valid to GPMC_ADV_ALE invalid		2.0	ns

(12) = F - nCS Max Delay + nWE Min Delay
F = ((WEOffTime - CSOnTime) * (TimeParaGranularity + 1) + 0.5 * (WEExtraDelay - CSExtraDelay)) * GPMC_FCLK

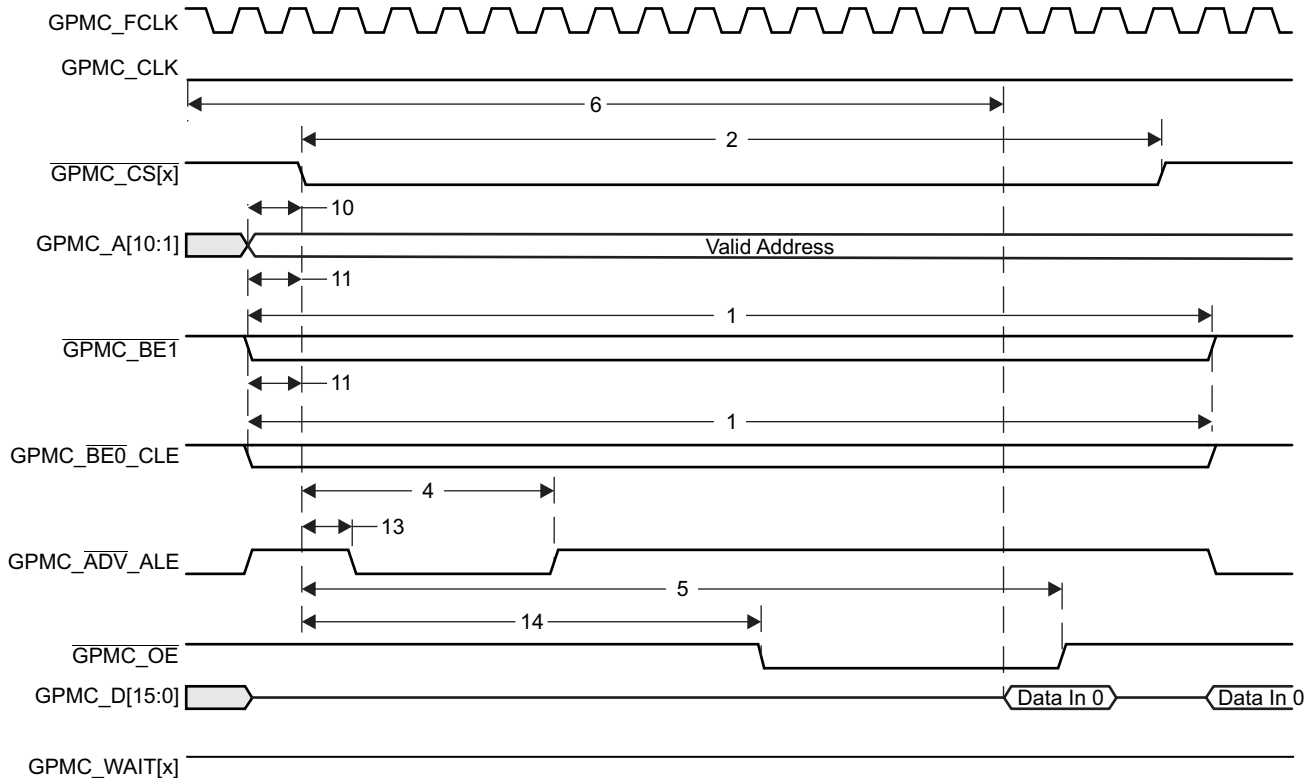


Figure 8-16. GPMC/Non-Multiplexed NOR Flash - Asynchronous Read - Single Word Timing

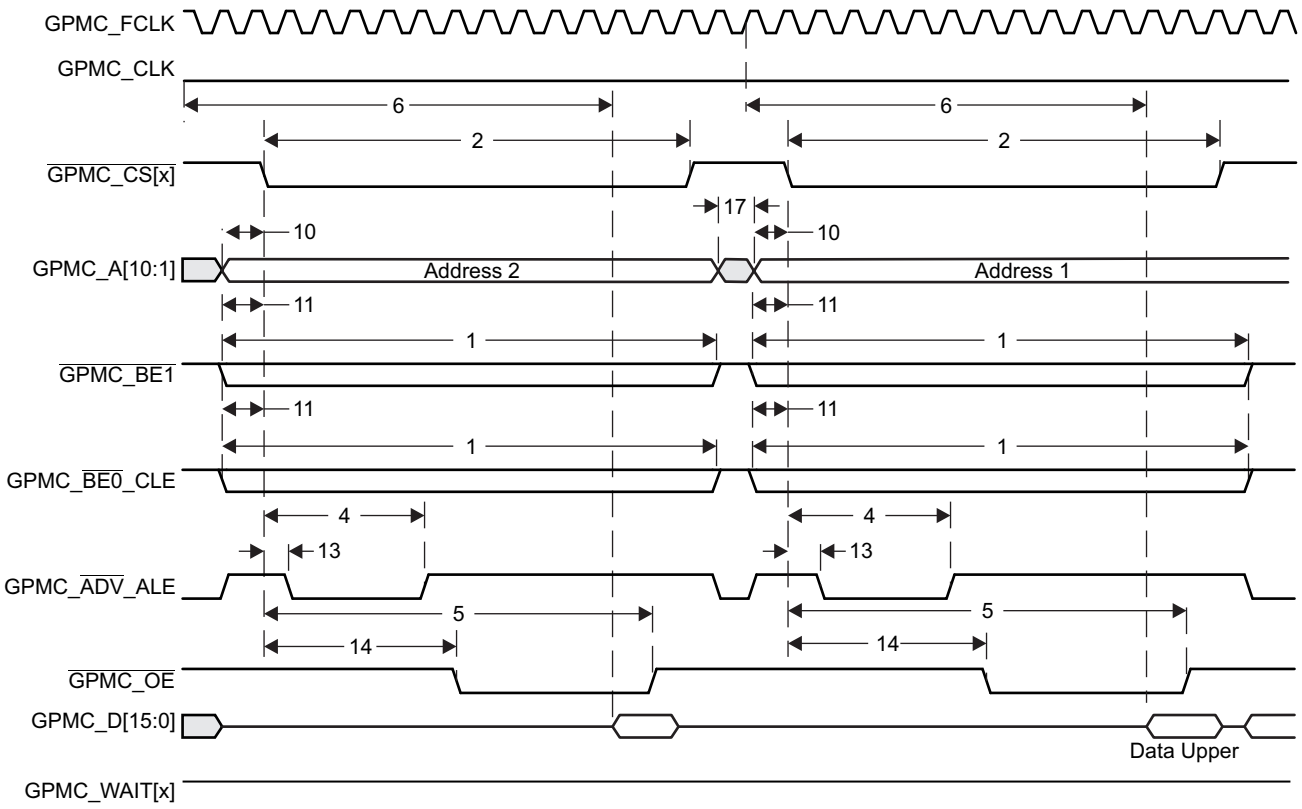


Figure 8-17. GPMC/Non-Multiplexed NOR Flash - Asynchronous Read - 32-Bit Access Timing

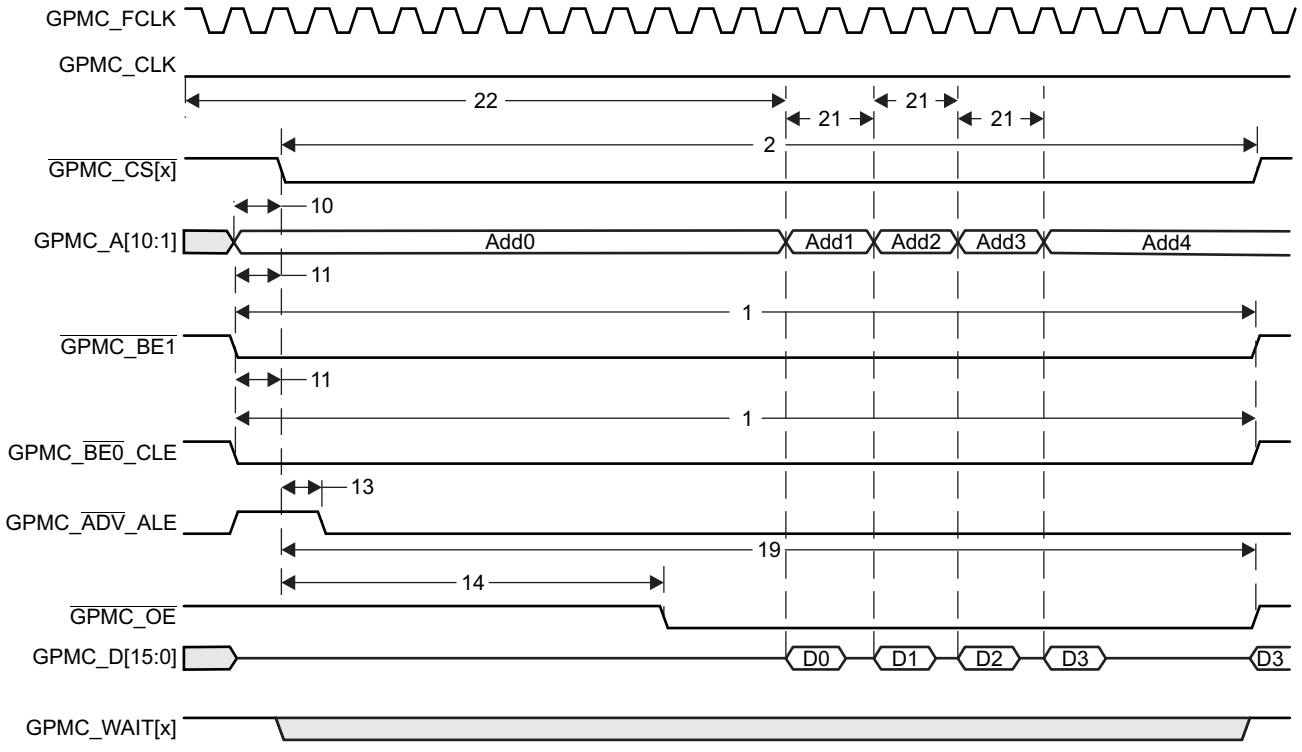


Figure 8-18. GPMC/Non-Multiplexed *Only* NOR Flash - Asynchronous Read - Page Mode 4x16-Bit Timing

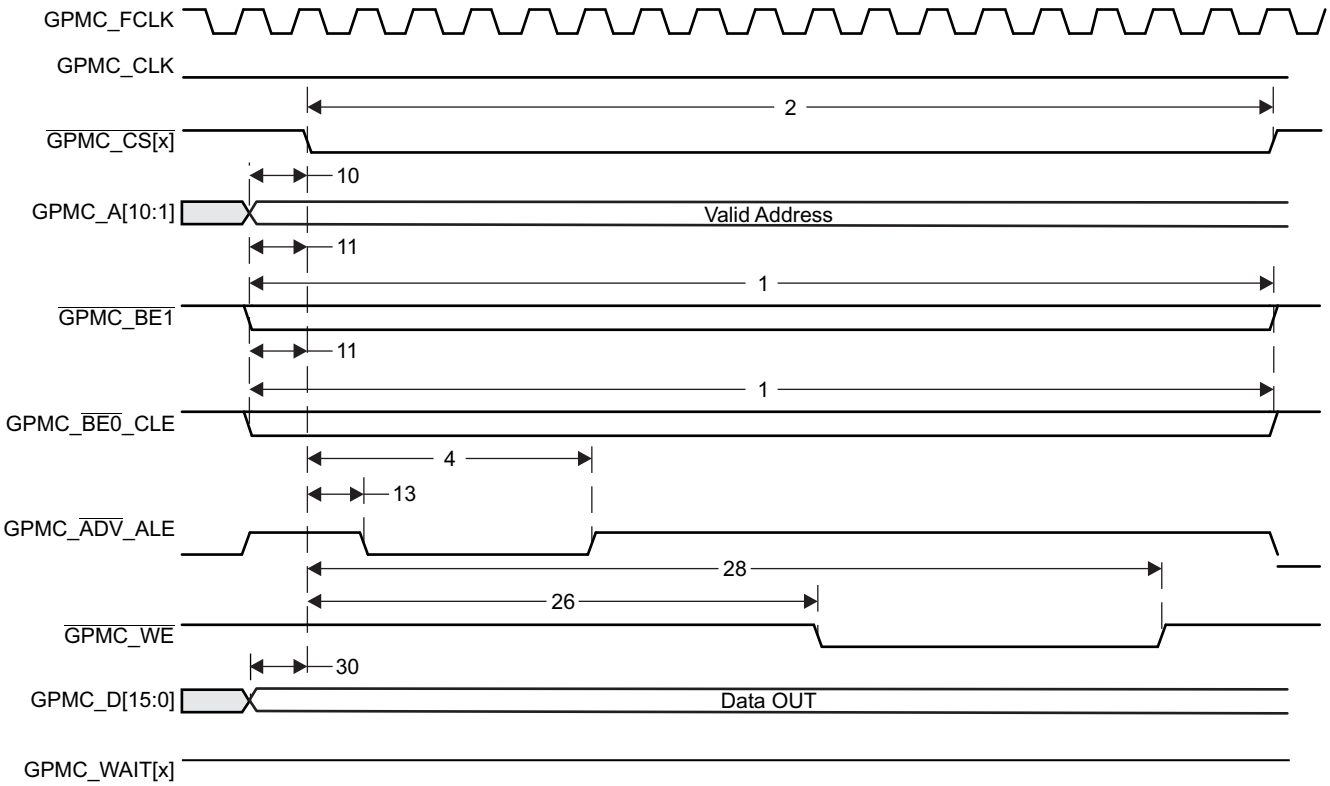


Figure 8-19. GPMC/Non-Multiplexed NOR Flash - Asynchronous Write - Single Word Timing

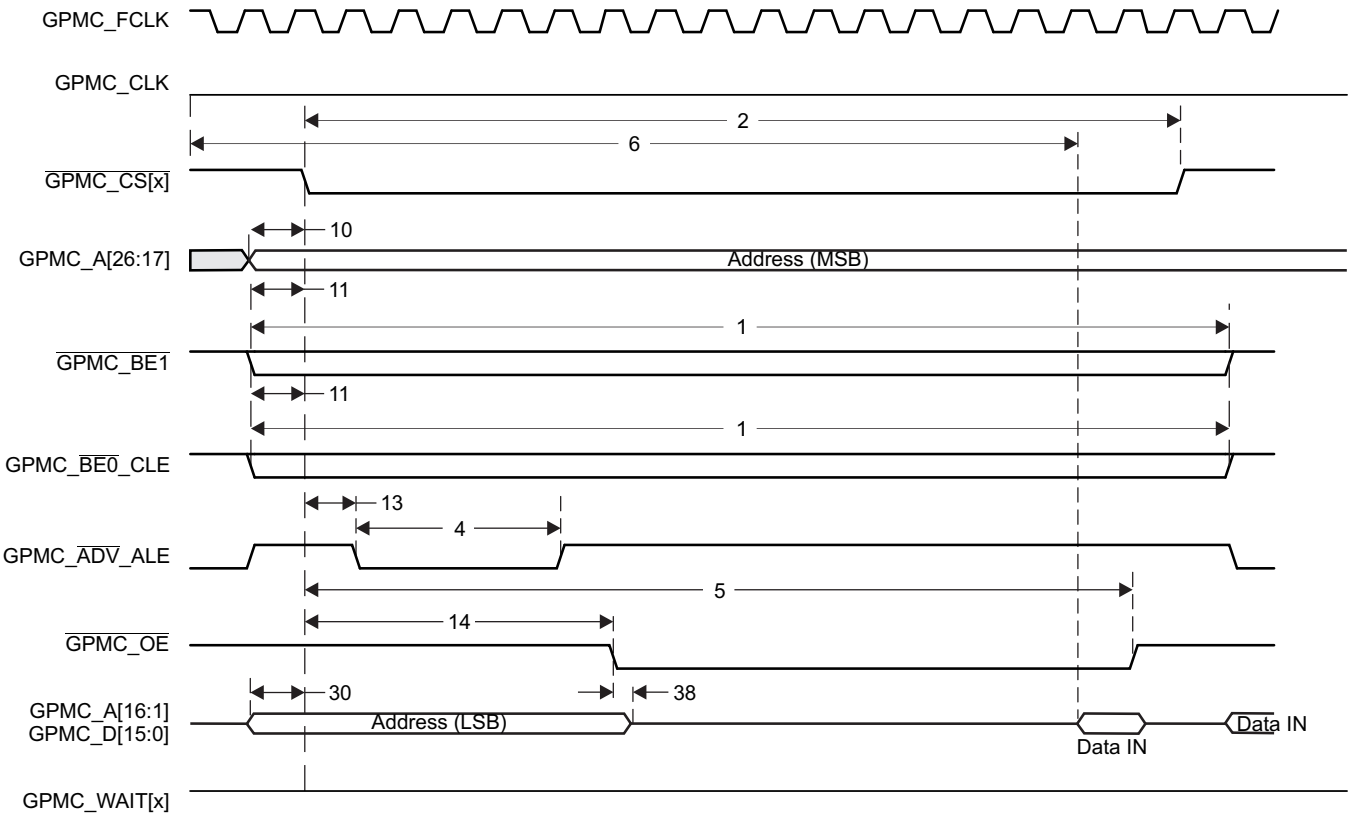


Figure 8-20. GPMC/Multiplexed NOR Flash - Asynchronous Read - Single Word Timing

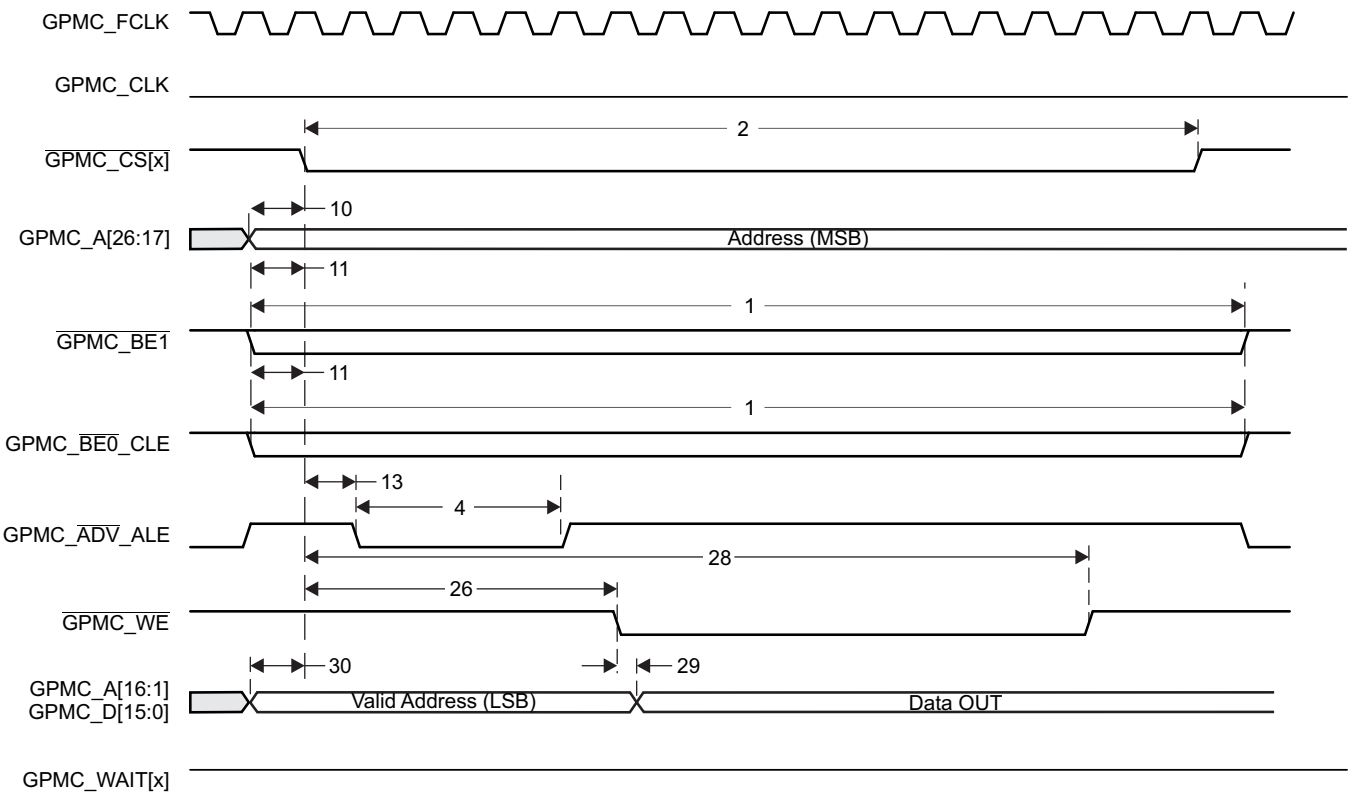


Figure 8-21. GPMC/Multiplexed NOR Flash - Asynchronous Write - Single Word Timing

8.7.2.3 GPMC/NAND Flash and ELM Interface Timing

Table 8-18. Timing Requirements for GPMC/NAND Flash Interface

(see Figure 8-24)

NO.			OPP100/OPP120/Turbo/Nitro		UNIT
			MIN	MAX	
13	$t_{acc(DAT)}$	Data maximum access time (GPMC_FCLK cycles)		J(1)	cycles

(1) J = AccessTime * (TimeParaGranularity + 1)

Table 8-19. Switching Characteristics Over Recommended Operating Conditions for GPMC/NAND Flash Interface

(see Figure 8-22, Figure 8-23, Figure 8-24, Figure 8-25)

NO.	PARAMETER		OPP100/OPP120/Turbo/Nitro		UNIT
			MIN	MAX	
1	$t_{w(nWEV)}$	Pulse duration, $\overline{GPMC\_WE}$ valid time		A(1)	ns
2	$t_{d(nCSV-nWEV)}$	Delay time, $\overline{GPMC\_CS[X]}$ valid to $\overline{GPMC\_WE}$ valid	B - 0.2(2)	B + 2.0(2)	ns
3	$t_{d(CLEH-nWEV)}$	Delay time, GPMC_$\overline{BE0}$_CLE high to $\overline{GPMC\_WE}$ valid	C - 0.2(3)	C + 2.0(3)	ns
4	$t_{d(nWEV-DV)}$	Delay time, GPMC_D[15:0] valid to $\overline{GPMC\_WE}$ valid	D - 0.2(4)	D + 2.0(4)	ns
5	$t_{d(nWEIV-DIV)}$	Delay time, $\overline{GPMC\_WE}$ invalid to GPMC_AD[15:0] invalid	E - 0.2(5)	E + 2.0(5)	ns
6	$t_{d(nWEIV-CLEIV)}$	Delay time, $\overline{GPMC\_WE}$ invalid to GPMC_$\overline{BE0}$_CLE invalid	F - 0.2(6)	F + 2.0(6)	ns
7	$t_{d(nWEIV-nCSIV)}$	Delay time, $\overline{GPMC\_WE}$ invalid to $\overline{GPMC\_CS[X]}$ invalid	G - 0.2(7)	G + 2.0(7)	ns
8	$t_{d(ALEH-nWEV)}$	Delay time, GPMC_$\overline{ADV}$_ALE High to $\overline{GPMC\_WE}$ valid	C - 0.2(3)	C + 2.0(3)	ns
9	$t_{d(nWEIV-ALEIV)}$	Delay time, $\overline{GPMC\_WE}$ invalid to GPMC_$\overline{ADV}$_ALE invalid	F - 0.2(6)	F + 2.0(6)	ns
10	$t_{c(nWE)}$	Cycle time, write cycle time		H(8)	ns
11	$t_{d(nCSV-nOEV)}$	Delay time, $\overline{GPMC\_CS[X]}$ valid to $\overline{GPMC\_OE\_RE}$ valid	I - 0.2(9)	I + 2.0(9)	ns
12	$t_{w(nOEV)}$	Pulse duration, $\overline{GPMC\_OE\_RE}$ valid time		K(10)	ns
13	$t_{c(nOE)}$	Cycle time, read cycle time		L(11)	ns
14	$t_{d(nOEIV-nCSIV)}$	Delay time, $\overline{GPMC\_OE\_RE}$ invalid to $\overline{GPMC\_CS[X]}$ invalid	M - 0.2(12)	M + 2.0(12)	ns

(1) A = (WEOffTime - WEOnTime) * (TimeParaGranularity + 1) * GPMC_FCLK
(2) = B + nWE Min Delay - nCS Max Delay
B = ((WEOnTime - CSOnTime) * (TimeParaGranularity + 1) + 0.5 * (WEExtraDelay - CSExtraDelay)) * GPMC_FCLK
(3) = C + nWE Min Delay - CLE Max Delay
C = ((WEOnTime - ADVOnTime) * (TimeParaGranularity + 1) + 0.5 * (WEExtraDelay - ADVExtraDelay)) * GPMC_FCLK
(4) = D + nWE Min Delay - Data Max Delay
D = (WEOnTime * (TimeParaGranularity + 1) + 0.5 * WEExtraDelay) * GPMC_FCLK
(5) =E + Data Min Delay - nWE Max Delay
E = ((WrCycleTime - WEOffTime) * (TimeParaGranularity + 1) - 0.5 * WEExtraDelay) * GPMC_FCLK
(6) = F + CLE Min Delay - nWE Max Delay
F = ((ADVWrOffTime - WEOffTime) * (TimeParaGranularity + 1) + 0.5 * (ADVExtraDelay - WEExtraDelay)) * GPMC_FCLK
(7) =G + nCS Min Delay - nWE Max Delay
G = ((CSWrOffTime - WEOffTime) * (TimeParaGranularity + 1) + 0.5 * (CSExtraDelay - WEExtraDelay)) * GPMC_FCLK
(8) H = WrCycleTime * (1 + TimeParaGranularity) * GPMC_FCLK
(9) = I + nOE Min Delay - nCS Max Delay
I = ((OEOnTime - CSOnTime) * (TimeParaGranularity + 1) + 0.5 * (OEExtraDelay - CSExtraDelay)) * GPMC_FCLK
(10) K = (OEOffTime - OEOnTime) * (1 + TimeParaGranularity) * GPMC_FCLK
(11) L = RdCycleTime * (1 + TimeParaGranularity) * GPMC_FCLK
(12) =M + nCS Min Delay - nOE Max Delay
M = ((CSRdOffTime - OEOffTime) * (TimeParaGranularity + 1) + 0.5 * (CSExtraDelay - OEExtraDelay))* GPMC_FCLK

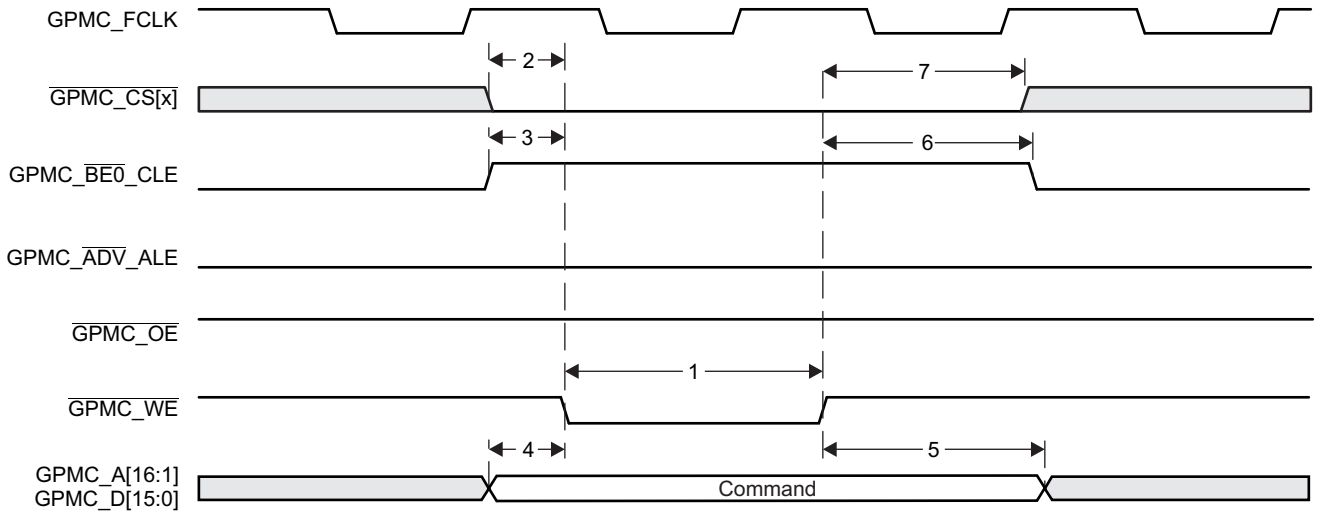


Figure 8-22. GPMC/NAND Flash - Command Latch Cycle Timing

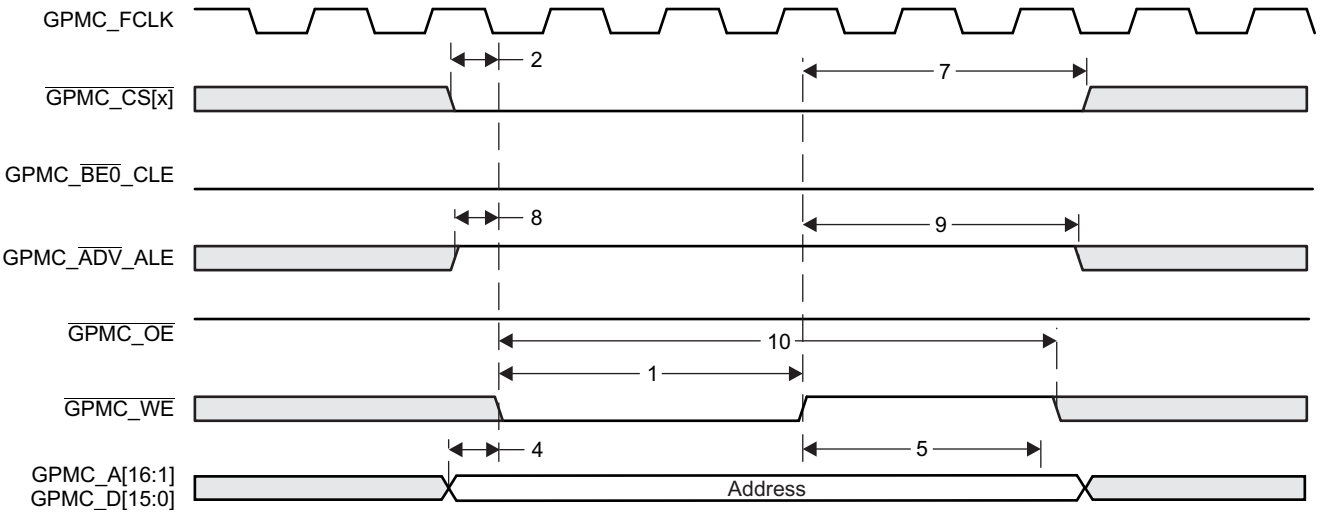


Figure 8-23. GPMC/NAND Flash - Address Latch Cycle Timing

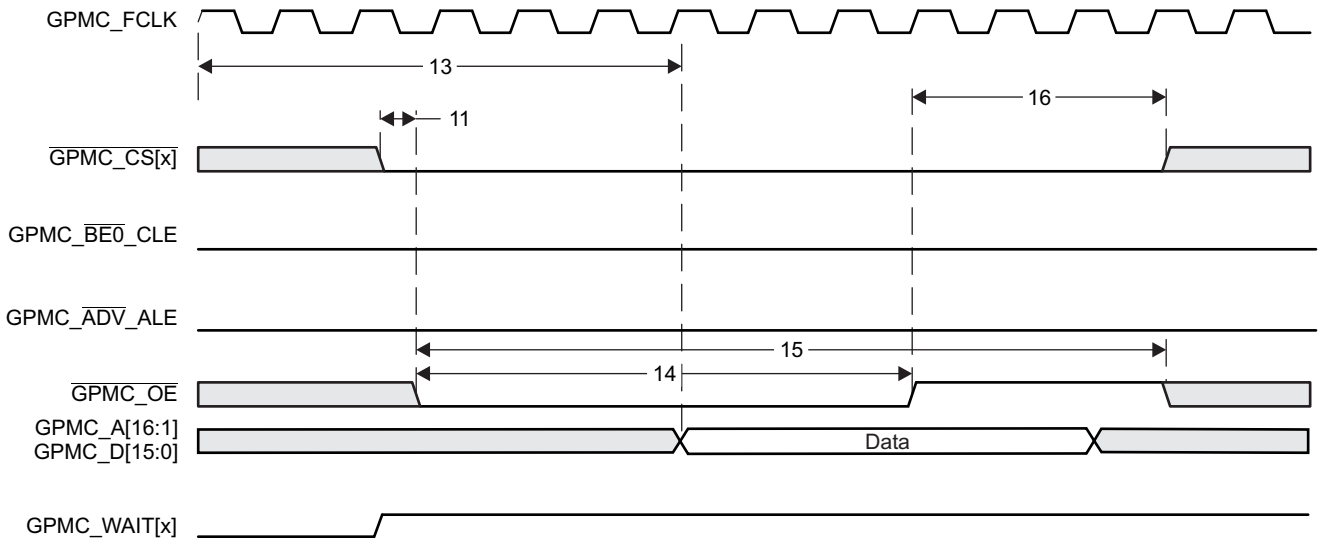


Figure 8-24. GPMC/NAND Flash - Data Read Cycle Timing

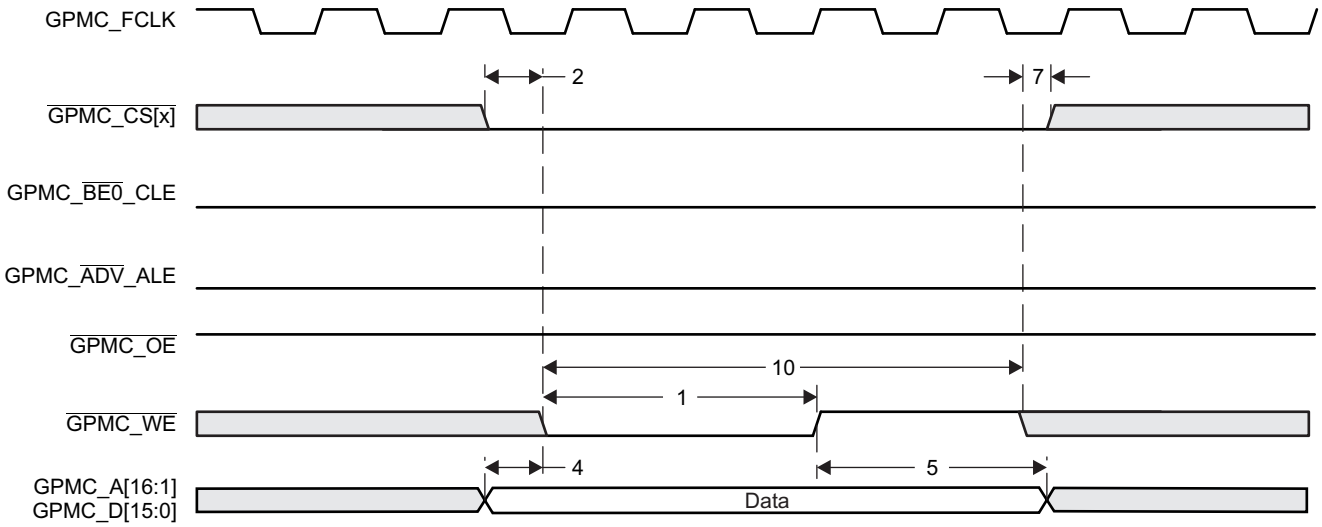


Figure 8-25. GPMC/NAND Flash - Data Write Cycle Timing

8.8 High-Definition Multimedia Interface (HDMI)

The device includes an HDMI 1.3a-compliant transmitter for digital video and audio data to display devices. The HDMI interface consists of a digital HDMI transmitter core with TMDS encoder, a core wrapper with interface logic and control registers, and a transmit PHY, with the following features:

- Hot-plug detection
- Consumer electronics control (CEC) messages
- DVI 1.0 compliant (only RGB pixel format)
- CEA 861-D and VESA DMT formats
- Supports up to 165-MHz pixel clock
  - 1920 x 1080p @75 Hz with 8-bit/component color depth
  - 1600 x 1200 @60 Hz with 8-bit/component color depth
- Support for deep-color mode:
  - 10-bit/component color depth up to 1080p @60 Hz (Max pixel clock = 148.5 MHz)
  - 12-bit/component color depth up to 720p/1080i @60 Hz (Max pixel clock = 123.75 MHz)
- TMDS clock to the HDMI-PHY is up to 185.625 MHz
- Maximum supported pixel clock:
  - 165 MHz for 8-bit color depth
  - 148.5 MHz for 10-bit color depth
  - 123.75 MHz for 12-bit color depth
- Uncompressed multichannel (up to eight channels) audio (L-PCM) support
- Master I2C interface for display data channel (DDC) connection
- Options available to support HDCP encryption engine for transmitting protected audio and video (for information, contact your local TI sales representative).

For more details on the HDMI, see the *High-Definition Multimedia Interface (HDMI)* chapter in the device-specific Technical Reference Manual.

8.8.1 HDMI Design Guidelines

This section provides PCB design and layout guidelines for the HDMI interface. The design rules constrain PCB trace length, PCB trace skew, signal integrity, cross-talk, and signal timing. Simulation and system design work has been done to ensure the HDMI interface requirements are met.

8.8.1.1 HDMI Interface Schematic

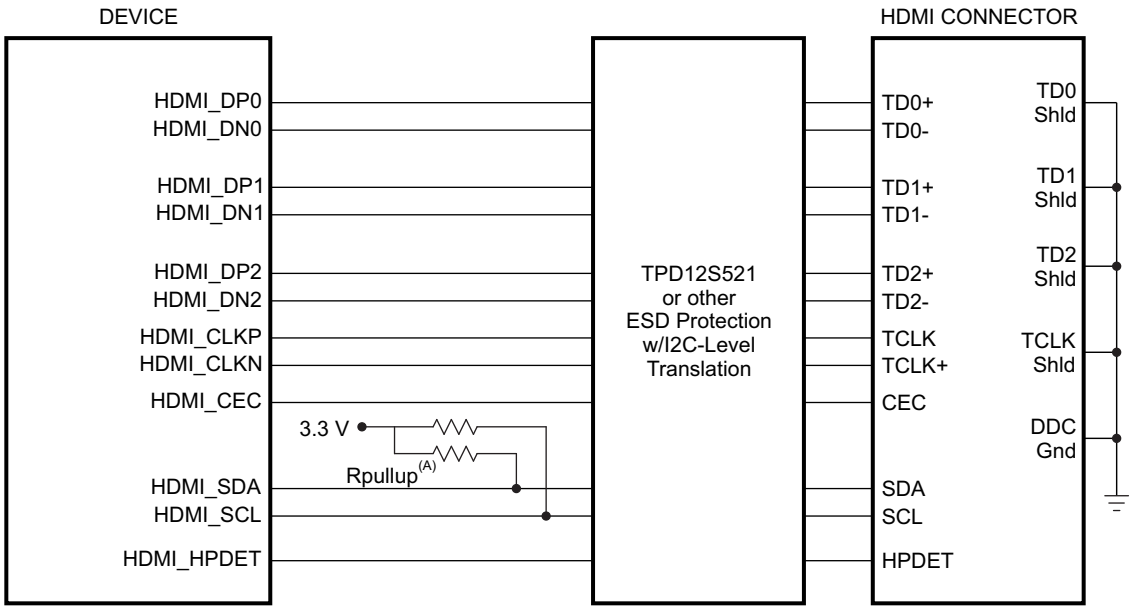
The HDMI bus is separated into three main sections:

1. Transition Minimized Differential Signaling (TMDS) high-speed digital video interface
2. Display Data Channel (I2C bus for configuration and status exchange between two devices)
3. Consumer Electronics Control (optional) for remote control of connected devices.

The DDC and CEC are low-speed interfaces, so nothing special is required for PCB layout of these signals. Their connection is shown in Figure 8-26, *HDMI Interface High-Level Schematic*.

The TMDS channels are high-speed differential pairs and, therefore, require the most care in layout. Specifications for TMDS layout are below.

Figure 8-26 shows the HDMI interface schematic. The specific pin numbers can be obtained from , *HDMI Terminal Functions*.



A. 5K-10K Ω pullup resistors are required if not integrated in the ESD protection chip.

Figure 8-26. HDMI Interface High-Level Schematic

8.8.1.2 TMDS Routing

The TMDS signals are high-speed differential pairs. Care must be taken in the PCB layout of these signals to ensure good signal integrity.

The TMDS differential signal traces must be routed to achieve 100 Ω (±10%) differential impedance and 60 Ω (±10%) single-ended impedance. Single-ended impedance control is required because differential signals are extremely difficult to closely couple on PCBs and, therefore, single-ended impedance becomes important.

These impedances are impacted by trace width, trace spacing, distance to reference planes, and dielectric material. Verify with a PCB design tool that the trace geometry for both data signal pairs results in as close to 60 Ω impedance traces as possible. For best accuracy, work with your PCB fabricator to ensure this impedance is met.

In general, closely coupled differential signal traces are not an advantage on PCBs. When differential signals are closely coupled, tight spacing and width control is necessary. Very small width and spacing variations affect impedance dramatically, so tight impedance control can be more problematic to maintain in production.

Loosely coupled PCB differential signals make impedance control much easier. Wider traces and spacing make obstacle avoidance easier, and trace width variations do not affect impedance as much; therefore, it is easier to maintain an accurate impedance over the length of the signal. The wider traces also show reduced skin effect and, therefore, often result in better signal integrity.

Table 8-20 shows the routing specifications for the TMDS signals.

Table 8-20. TMDS Routing Specifications

PARAMETER	MIN	TYP	MAX	UNIT
Processor-to-HDMI header trace length			7000	Mils
Number of stubs allowed on TMDS traces			0	Stubs
TX/RX pair differential impedance	90	100	110	Ω
TX/RX single ended impedance	54	60	66	Ω

Table 8-20. TMDS Routing Specifications (continued)

PARAMETER	MIN	TYP	MAX	UNIT
Number of vias on each TMDS trace			2	Vias(1)
TMDS differential pair to any other trace spacing	2*DS(2)			

(1) Vias must be used in pairs with their distance minimized.
(2) DS = differential spacing of the HDMI traces.

8.8.1.3 DDC Signals

As shown in Figure 8-26, *HDMI Interface High-Level Schematic*, the DDC connects just like a standard I2C bus. As such, resistor pullups must be used to pull up the open drain buffer signals unless they are integrated into the ESD protection chip used. If used, these pullup resistors should be connected to a 3.3-V supply.

8.8.1.4 HDMI ESD Protection Device (Required)

Interfaces that connect to a cable such as HDMI generally require more ESD protection than can be built into the processor's outputs. Therefore, this HDMI interface requires the use of an ESD protection chip to provide adequate ESD protection and to translate I2C voltage levels from the 3.3 V supplied by the device to the 5 volts required by the HDMI specification.

When selecting an ESD protection chip, choose the lowest capacitance ESD protection available to minimize signal degradation. In no case should the ESD protection circuit capacitance be more than 5 pF.

TI manufactures devices that provide ESD protection for HDMI signals such as the TPD12S521. For more information see the www.ti.com website.

8.8.1.5 PCB Stackup Specifications

Table 8-21 shows the stackup and feature sizes required for HDMI.

Table 8-21. HDMI PCB Stackup Specifications

PARAMETER	MIN	TYP	MAX	UNIT
PCB routing/plane layers	4	6	-	Layers
Signal routing layers	2	3	-	Layers
Number of ground plane cuts allowed within HDMI routing region	-	-	0	Cuts
Number of layers between HDMI routing region and reference ground plane	-	-	0	Layers
PCB trace width	-	4	-	Mils
PCB BGA escape via pad size	-	20	-	Mils
PCB BGA escape via hole size	-	10		Mils
Processor device BGA pad size(1)(2)		0.4		mm

(1) Non-solder mask defined pad.
(2) Per IPC-7351A BGA pad size guideline.

8.8.1.6 Grounding

Each TMDS channel has its own shield pin which should be grounded to provide a return current path for the TMDS signal.

8.9 High-Definition Video Processing Subsystem (HDVPSS)

The device High-Definition Video Processing Subsystem (HDVPSS) provides a video input interface for external imaging peripherals (for example, image sensors, video decoders, and more) and a video output interface for display devices, such as analog SDTV and HDTV displays, digital HDTV displays, digital LCD panels, and more. It includes HD and SD video encoders and an HDMI transmitter interface.

The device HDVPSS features include:

- Two display processing pipelines with de-interlacing, scaling, alpha blending, chroma keying, color space conversion, flicker filtering, and pixel format conversion.
- HD/SD compositor features for PIP support.
- Format conversions (up to 1080p 60 Hz) include scan format conversion, scan rate conversion, aspect-ratio conversion, and frame size conversion.
- Supports additional video processing capabilities by using the subsystem's memory-to-memory feature.
- Two parallel video processing pipelines support HD (up to 1080p60) and SD (NTSC/PAL) simultaneous outputs.
  - HD analog component output with OSD and embedded timing codes (BT.1120)
    - 3-channel HD-DAC with 10-bit resolution.
    - External HSYNC and VSYNC signals.
  - SD analog output with OSD with embedded timing codes (BT.656)
    - Composite output
    - 1-channel SD-DAC with 10-bit resolution
    - Options available to support MacroVision and CGMS-A (contact local TI Sales rep for information).
  - Digital HDMI 1.3a-compliant transmitter (for details, see Section 8.8, *High-Definition Multimedia Interface (HDMI)*).
  - One digital video output supporting up to 30-bits @ 165 MHz
  - One digital video output supporting up to 24-bits @ 165 MHz
  - Supports clock inversion for VOUT[0] and VOUT[1] clock signals.
- Two independently configurable external video input capture ports (up to 165 MHz).
  - 16/24-bit HD digital video input or dual clock independent 8-bit SD inputs on each capture port.
  - 8/16/24-bit digital video input
  - 8-bit digital video input
  - Embedded sync and external sync modes are supported for all input configurations (VIN1 Port B supports embedded sync only).
  - De-multiplexing of both pixel-to-pixel and line-to-line multiplexed streams, effectively supporting up to 16 simultaneous SD inputs with a glueless interface to an external multiplexer such as the TVP5158.
  - Additional features include: programmable color space conversion, scaler and chroma downsampler, ancillary VANC/VBI data capture (decoded by software).
- Graphics features:
  - Three independently-generated graphics layers.
  - Each supports full-screen resolution graphics in HD, SD or both.
  - Up/down scaler optimized for graphics.
  - Global and pixel-level alpha blending supported.

For more detailed information on specific features and registers, see the *High Definition Video Processing Subsystem* chapter in the device-specific Technical Reference Manual.

8.9.1 HDVPSS Electrical Data/Timing

Table 8-22. Timing Requirements for HDVPSS Input

(see Figure 8-27 and Figure 8-28)

NO.			OPP100/OPP120/ Turbo/Nitro		UNIT
			MIN	MAX	
VIN[X]A_CLK					
1	$t_{c(CLK)}$	Cycle time, VIN[x]A_CLK	6.06 (1)		ns
2	$t_{w(CLKH)}$	Pulse duration, VIN[x]A_CLK high (45% of t_c)	2.73		ns
3	$t_{w(CLKH)}$	Pulse duration, VIN[x]A_CLK low (45% of t_c)	2.73		ns
7	$t_{t(CLK)}$	Transition time, VIN[x]A_CLK (10%-90%)		2.64	ns
4	$t_{su(DE-CLK)}$ $t_{su(VSYNC-CLK)}$ $t_{su(FLD-CLK)}$ $t_{su(HSYNC-CLK)}$	Input setup time, control valid to VIN[x]A_CLK high/low	3.11		ns
	$t_{su(D-CLK)}$	Input setup time, data valid to VIN[x]A_CLK high/low	3.11		
5	$t_{h(CLK-DE)}$ $t_{h(CLK-VSYNC)}$ $t_{h(CLK-FLD)}$ $t_{h(CLK-HSYNC)}$	Input hold time, control valid from VIN[x]A_CLK high/low	-0.5		ns
	$t_{h(CLK-D)}$	Input hold time, data valid from VIN[x]A_CLK high/low	-0.5		
VIN[x]B_CLK					
1	$t_{c(CLK)}$	Cycle time, VIN[x]B_CLK	6.06 (1)		ns
2	$t_{w(CLKH)}$	Pulse duration, VIN[x]B_CLK high (45% of t_c)	2.73		ns
3	$t_{w(CLKH)}$	Pulse duration, VIN[x]B_CLK low (45% of t_c)	2.73		ns
7	$t_{t(CLK)}$	Transition time, VIN[x]B_CLK (10%-90%)		2.64	ns
4	$t_{su(DE-CLK)}$ $t_{su(VSYNC-CLK)}$ $t_{su(FLD-CLK)}$ $t_{su(HSYNC-CLK)}$	Input setup time, control valid to VIN[x]B_CLK high/low	3.11		ns
	$t_{su(D-CLK)}$	Input setup time, data valid to VIN[x]B_CLK high/low	3.11		
5	$t_{h(CLK-DE)}$ $t_{h(CLK-VSYNC)}$ $t_{h(CLK-FLD)}$ $t_{h(CLK-HSYNC)}$	Input hold time, control valid from VIN[x]B_CLK high/low	-0.5		ns
	$t_{h(CLK-D)}$	Input hold time, data valid from VIN[x]B_CLK high/low	-0.5		

(1) For maximum frequency of 165 MHz.

Table 8-23. Switching Characteristics Over Recommended Operating Conditions for HDVPSS Output

(see Figure 8-27 and Figure 8-29)

NO.	PARAMETER		OPP100/OPP120/Turbo/Nitro		UNIT
			MIN	MAX	
1	$t_{c(CLK)}$	Cycle time, VOUT[x]_CLK	6.06 (1)		ns
2	$t_{w(CLKH)}$	Pulse duration, VOUT[x]_CLK high (45% of t_c)	2.73		ns
3	$t_{w(CLKL)}$	Pulse duration, VOUT[x]_CLK low (45% of t_c)	2.73		ns
7	$t_{t(CLK)}$	Transition time, VOUT[x]_CLK (10%-90%)		2.64	ns
6	$t_{d(CLK-AVID)}$	Delay time, VOUT[x]_CLK low (falling) to control valid, positive clock edge	1.64	4.18	ns
	$t_{d(CLK-FLD)}$				
	$t_{d(CLK-VSYNC)}$				
	$t_{d(CLK-HSYNC)}$				
	$t_{d(CLK-RCR)}$	Delay time, VOUT[0]_CLK low (falling) to data valid, positive clock edge	1.64	4.18	ns
	$t_{d(CLK-GYYC)}$				
	$t_{d(CLK-BCBC)}$				
	$t_{d(CLK-YYC)}$	Delay time, VOUT[1]_CLK low (falling) to data valid, positive clock edge			
	$t_{d(CLK-C)}$				
	$t_{d(CLK-AVID)}$	Delay time, VOUT[x]_CLK low (falling) to control valid, negative clock edge	-1.64	4.18	ns
	$t_{d(CLK-FLD)}$				
	$t_{d(CLK-VSYNC)}$				
	$t_{d(CLK-HSYNC)}$				
	$t_{d(CLK-RCR)}$	Delay time, VOUT[0]_CLK low (falling) to data valid, negative clock edge	-1.64	4.18	ns
	$t_{d(CLK-GYYC)}$				
	$t_{d(CLK-BCBC)}$				
	$t_{d(CLK-YYC)}$	Delay time, VOUT[1]_CLK low (falling) to data valid, negative clock edge			
	$t_{d(CLK-C)}$				

(1) For maximum frequency of 165 MHz.

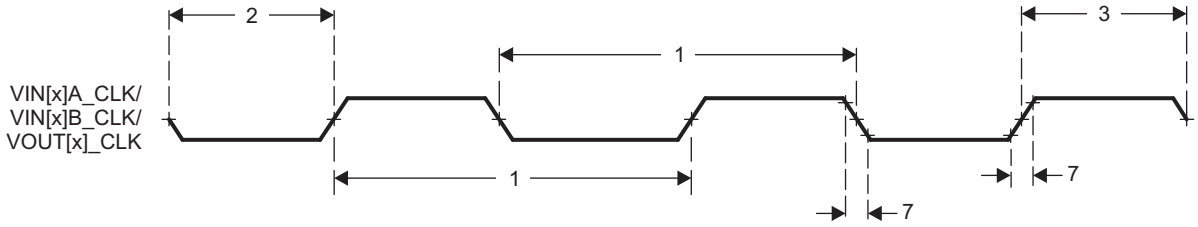


Figure 8-27. HDVPSS Clock Timing

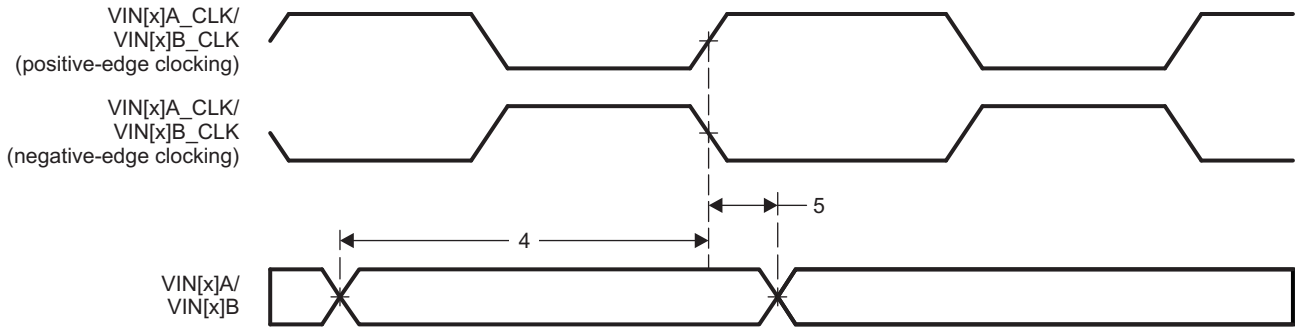


Figure 8-28. HDVPSS Input Timing

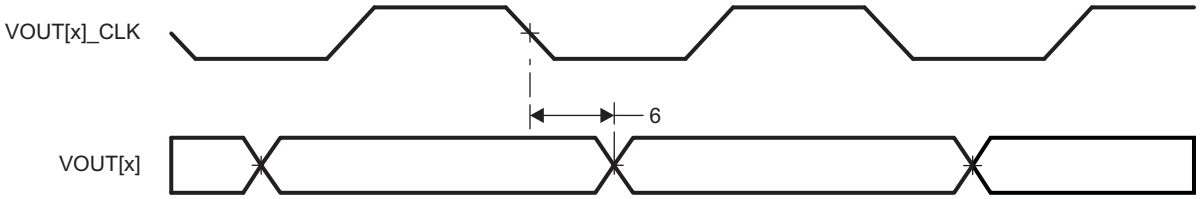
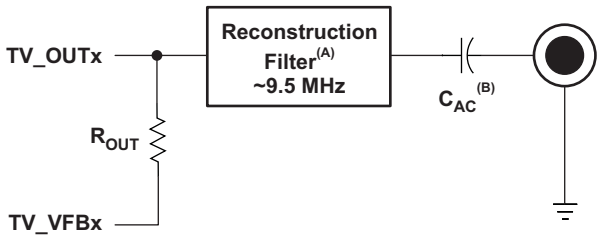


Figure 8-29. HDVPSS Output Timing

8.9.2 Video SD-DAC Guidelines and Electrical Data/Timing

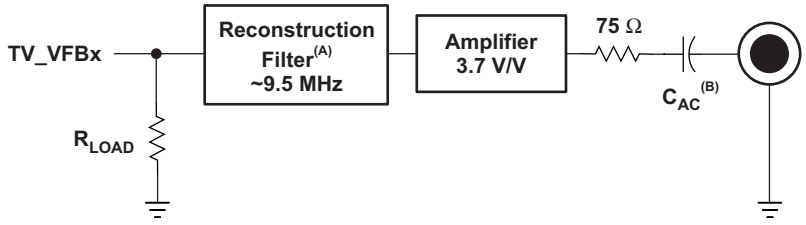
The device's analog video SD-DAC output can be operated in one of two modes: Normal mode and TVOUT Bypass mode. In Normal mode, the device's internal video amplifier is used. In TVOUT Bypass mode, the internal video amplifier is bypassed and an external amplifier is required.

Figure 8-30 shows a typical circuit that permits connecting the analog video output from the device to standard 75-Ω impedance video systems in Normal mode. Figure 8-31 shows a typical circuit that permits connecting the analog video output from the device to standard 75-Ω impedance video systems in TVOUT Bypass mode.



A. Reconstruction Filter (optional)
B. AC coupling capacitor (optional)

Figure 8-30. TV Output (Normal Mode)



A. Reconstruction Filter (optional). Note: An amplifier with an integrated reconstruction filter can alternatively be used instead of a discrete reconstruction filter.
B. AC coupling capacitor (optional)

Figure 8-31. TV Output (TVOUT Bypass Mode)

During board design, the onboard traces and parasitics must be matched for the channel. The video SD-DAC output pin (TV_OUT0/TV_VFB0) are very high-frequency analog signals and must be routed with extreme care. As a result, the paths of these signals must be as short as possible, and as isolated as possible from other interfering signals. In TVOUT Bypass mode, the load resistor and amplifier/buffer should be placed as close as possible to the TV_VFB0 pin. Other layout guidelines include:

- Take special care to bypass the VDDA_VDAC_1P8 power supply pin with a capacitor. For more information, see Section 7.2.9, *Power-Supply Decoupling*.
- In **TVOUT Bypass mode**, place the R_{LOAD} resistor as close as possible to the Reconstruction Filter and Amplifier. In addition, place the 75-Ω resistor as close as possible (< 0.5 ") to the Amplifier/buffer output pin. To maintain a high-quality video signal, the onboard traces after the 75-Ω resistor should have a characteristic impedance of 75 Ω (± 20%).
- In **Normal mode**, TV_VFB0 is the most sensitive pin in the TV out system. The R_{OUT} resistor should be placed as close as possible to the device pin. To maintain a high-quality video signal, the onboard traces leading to the TV_OUT0 pin should have a characteristic impedance of 75 Ω (± 20%) starting from the closest possible place to the device pin output.
- Minimize input trace lengths to the device to reduce parasitic capacitance.
- Include solid ground return paths.

For additional Video SD-DAC Design guidelines, see the *High Definition Video Processing Subsystem* chapter in the device-specific Technical Reference Manual.

Table 8-24. Static and Dynamic SD-DAC Specifications

VDAC STATIC SPECIFICATIONS					
PARAMETER	**TEST CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNIT**
Reference Current Setting Resistor (R_{SET})	Normal Mode	4653	4700	4747	Ω
	TVOUT Bypass Mode	9900	10000	10100	Ω
Output resistor between TV_OUT0 and TV_VFB0 pins (R_{OUT})	Normal Mode	2673	2700	2727	Ω
	TVOUT Bypass Mode	N/A			
Load Resistor (R_{LOAD})	Normal Mode	75-Ω Inside the Display			
	TVOUT Bypass Mode	1485	1500	1515	Ω
AC-Coupling Capacitor (Optional) [C_{AC}]	Normal Mode	220			uF
	TVOUT Bypass Mode	See External Amplifier Specification			
Total Capacitance from TV_OUT0 to VSSA_VDAC_1P8	Normal Mode			300	pF
	TVOUT Bypass Mode	N/A			
Resolution			10		Bits
Integral Non-Linearity (INL), Best Fit	Normal Mode	-4		4	LSB
	TVOUT Bypass Mode	-1		1	LSB
Differential Non-Linearity (DNL)	Normal Mode	-2.5		2.5	LSB
	TVOUT Bypass Mode	-1		1	LSB
Full-Scale Output Voltage	Normal Mode (R_{LOAD} = 75 Ω)		1.3		V
	TVOUT Bypass Mode (R_{LOAD} = 1.5 kΩ)		0.7		V
Full-Scale Output Current	Normal Mode	N/A			
	TVOUT Bypass Mode		470		uA
Gain Error	Normal Mode (Composite) and TVOUT Bypass Mode	-10		10	%FS
Output Impedance	Looking into TV_OUT0 nodes		75		Ω
VDAC DYNAMIC SPECIFICATIONS					
PARAMETER	**TEST CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNIT**
Output Update Rate (F_{CLK})			54	60	MHz
Signal Bandwidth	3 dB		6		MHz
Spurious-Free Dynamic Range (SFDR) within bandwidth	F_{CLK} = 54 MHz, F_{OUT} = 1 MHz		50		dBc
Signal-to-Noise Ration (SNR)	F_{CLK} = 54 MHz, F_{OUT} = 1 MHz		54		dB
Power Supply Rejection (PSR)	Normal Mode, 100 mVpp @ 6 MHz on VDDA_VDAC_1P8		6		dB
	TVOUT Bypass Mode, 100 mVpp @ 6 MHz on VDDA_VDAC_1P8		20		

8.9.3 Video HD-DAC Guidelines and Electrical Data/Timing

The device's analog video HD-DAC outputs are designed to drive a 165-Ω load. An external video buffer/amplifier is required to provide additional gain (4.5V/V) and to drive the actual video outputs. 75-Ω back termination resistors should be connected in series with the video buffer output pins. For component video applications, a reconstruction filter should precede the video buffer. One solution is to use a video buffer/amplifier with integrated reconstruction filter, such as the Texas Instruments THS7360, which provides a complete solution for the typical output circuit, shown in Figure 8-32.

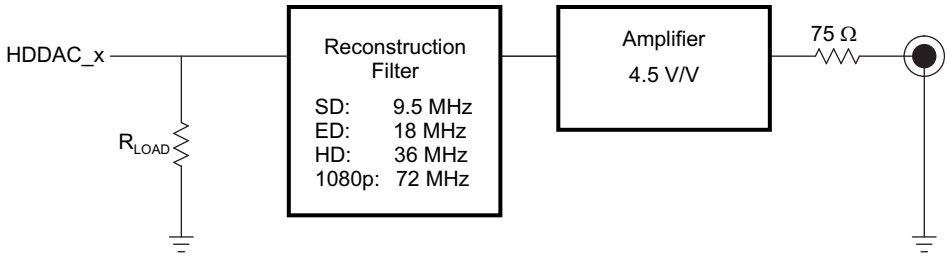


Figure 8-32. Typical Output Circuits for Analog Video from DACs

During board design, the onboard traces and parasitics must be matched for the channel. The video HD-DAC output pins (HDDAC_x) are very high-frequency analog signals and must be routed with extreme care. As a result, the path of this signal must be as short as possible, and as isolated as possible from other interfering signals. Other schematic and layout guidelines include:

- The correct external video gain (4.5V/V) must always be provided (even when not using the recommended video buffer). The recommended video buffer is the THS7360.
- The load resistor (RLOAD) should be placed as close as possible (< 0.5 in.) to the THS7360 video buffer input pins.
- The 75-Ω series resistors should be placed as close as possible (< 0.5 in.) to the THS7360 video buffer output pins.
- The trace lengths within a video format group should match as close as possible (for example, for component video outputs, the Y, Pb, and Pr trace lengths should match each other).
- The characteristic impedance of the HD-DAC output signal traces should match the HD-DAC load value (165Ω) as close as possible (±10%). The minimum trace width may limit how closely these impedances can be matched.
- The characteristic impedance of the video buffer output signal traces should match the back termination value (75 Ω) as close as possible (±10%). The minimum trace width may limit how closely these impedances can be matched.
- To provide adequate frequency response on the VGA/YPbPr output, recommend the following:
  - The length of the signal traces from the HD-DAC output pins to the THS7360 video buffer input pins should be minimized (< 1 in.) to reduce parasitic capacitance (~2 pF per inch).
  - Ensure the THS7360 reconstruction filter is properly programmed for each output format.
  - Enable 2x up-sampling for 720p/1080i component video outputs.
- To minimize noise on the VGA/YPbPr output, recommend the following:
  - The HD-DAC power supply pins (VDDA_REF_1P8V, VDDA_HD_1P8V) should be connected to a low-noise 1.8-V analog supply. Use a dedicated voltage regulator for best noise performance.
  - The THS7360 power supply pin should be connected to a low-noise 3.3-V analog supply. Use a dedicated voltage regulator for best noise performance.
  - Special care should be taken to provide adequate power supply decoupling on all analog supply pins (for example, ferrite bead and bypass capacitor).
  - Provide a ground guard adjacent to analog video signal traces to minimize noise coupling.
  - Provide a low impedance path to ground for the shield of the VGA/YPbPr output connector.
  - Include solid ground return paths.

- To provide adequate ESD protection on the VGA/YPbPr output, recommend the following:
  - Provide ESD protection on all output signals (that is, Video, Syncs and DDC I/F).
  - Minimize the distance from the ESD protection device to the VGA/YPbPr output connector.
  - Mount all ESD protection devices on the PCB level next to the ground plane to provide the lowest possible impedance path to ground.
  - Provide a low impedance path to ground for the shield of the VGA/YPbPr output connector.
- For VGA outputs, recommend the following:
  - 3.3 V to 5 V level shifters should be used for the H/V Sync signals.
  - 3.3 V to 5 V bi-directional level shifters should be used for the DDC signals. This is typically implemented using two N-channel enhancement MOSFETs.
  - Recommend using the TPD7S019 ESD protection device with integrated level shifters for the H/V Sync and DDC signals.
  - The source impedance of the H/V Sync outputs should be 50 Ω.
  - The characteristic impedance of the H/V Sync output signal traces should be 50 Ω.
  - The THS7360 reconstruction filter should be bypassed to provide maximum bandwidth.
  - The 5-V supply output should be current limited (for example, using a series resistor or resettable fuse).

For additional video HD-DAC design guidelines, see the *High Definition Video Processing Subsystem* chapter in the device-specific Technical Reference Manual.

Table 8-25. HD-DAC Recommended Operating Conditions

	MIN	NOM	MAX	UNIT
Output Load Capacitance (C_{LOAD})(1)			5	pF
Output Load Resistors (R_{LOAD})	–1%	165	+1%	Ω
Full-Scale Current Adjust Resistor (R_{HDDAC_IREF})	–1%	2.67	+1%	kΩ
Optional External Voltage Reference (HDDAC_VREF)(2)	–5%	467	+5%	mV
Required External Amplification (THS7360)	–3%	4.5	+3%	V/V

(1) The output load capacitance includes the signal trace parasitic capacitance and the video buffer input capacitance.
(2) An external voltage reference is not required since an internal bandgap reference is provided.

Table 8-26. HD-DAC Specifications

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Resolution			10		Bits
DC Accuracy					
Integral Non-Linearity (INL), best fit				2.5	LSB
Differential Non-Linearity (DNL)				1.0	LSB
Analog Output					
Full-Scale Output Current (IFS)	DAC input = 1023		3		mA
Full-Scale Output Voltage (VFS)	DAC input = 1023	–15%	494	+15%	mV
Zero Scale Offset Error (ZSET)			0.5		LSB
Channel matching				2	%
Dynamic Specifications					
Maximum Output Update Rate (FCLK)		150			MHz
Spurious - Free Dynamic Range (SFDR)	FCLK = 74.25 MHz, 30-MHz full-scale sine wave		70		dB
	FCLK = 148.5 MHz, 30-MHz full-scale sine wave		60		dB

8.10 Inter-Integrated Circuit (I2C)

The device includes four inter-integrated circuit (I2C) modules which provide an interface to other devices compliant with Philips Semiconductors Inter-IC bus (I2C-bus™) specification version 2.1. External components attached to this 2-wire serial bus can transmit/receive 8-bit data to/from the device through the I2C module. The I2C port *does not* support CBUS compatible devices.

The I2C port supports the following features:

- Compatible with Philips I2C Specification Revision 2.1 (January 2000)
- Standard and fast modes from 10 - 400 Kbps (no fail-safe I/O buffers)
- Noise filter to remove noise 50 ns or less
- Seven- and ten-bit device addressing modes
- Multimaster transmitter/slave receiver mode
- Multimaster receiver/slave transmitter mode
- Combined master transmit/receive and receive/transmit modes
- Two DMA channels, one interrupt line
- Built-in FIFO (32 byte) for buffered read or write.

For more detailed information on the I2C peripheral, see the *Inter-Integrated Circuit (I2C) Controller Module* chapter in the device-specific Technical Reference Manual.

8.10.1 I2C Peripheral Register Descriptions

The I2C peripheral registers are described in the device-specific Technical Reference Manual. Each register is documented as an offset from a base address for the peripheral. The base addresses for all of the peripherals are in the device memory map (see Section 2.10).

8.10.2 I2C Electrical Data/Timing

Table 8-27. Timing Requirements for I2C Input Timings(1)

(see Figure 8-33)

NO.			OPP100/OPP120/Turbo/Nitro				UNIT
			STANDARD MODE		FAST MODE		
			MIN	MAX	MIN	MAX	
1	$t_{c(SCL)}$	Cycle time, SCL	10		2.5		µs
2	$t_{su(SCLH-SDAL)}$	Setup time, SCL high before SDA low (for a repeated START condition)	4.7		0.6		µs
3	$t_{h(SDAL-SCLL)}$	Hold time, SCL low after SDA low (for a START and a repeated START condition)	4		0.6		µs
4	$t_{w(SCLL)}$	Pulse duration, SCL low	4.7		1.3		µs
5	$t_{w(SCLH)}$	Pulse duration, SCL high	4		0.6		µs
6	$t_{su(SDAV-SCLH)}$	Setup time, SDA valid before SCL high	250		100(2)		ns
7	$t_{h(SCLL-SDAV)}$	Hold time, SDA valid after SCL low	0(3)	3.45(4)	0(3)	0.9(4)	µs
8	$t_{w(SDAH)}$	Pulse duration, SDA high between STOP and START conditions	4.7		1.3		µs
9	$t_{r(SDA)}$	Rise time, SDA		1000	20 + 0.1C_b (5)	300	ns
10	$t_{r(SCL)}$	Rise time, SCL		1000	20 + 0.1C_b (5)	300	ns
11	$t_{f(SDA)}$	Fall time, SDA		300	20 + 0.1C_b (5)	300	ns
12	$t_{f(SCL)}$	Fall time, SCL		300	20 + 0.1C_b (5)	300	ns
13	$t_{su(SCLH-SDAH)}$	Setup time, SCL high before SDA high (for STOP condition)	4		0.6		µs
14	$t_{w(SP)}$	Pulse duration, spike (must be suppressed)			0	50	ns
15	C_b (5)	Capacitive load for each bus line		400		400	pF

(1) The I2C pins SDA and SCL do not feature fail-safe I/O buffers. These pins could potentially draw current when the device is powered down.
(2) A Fast-mode I²C-bus™ device can be used in a Standard-mode I²C-bus system, but the requirement $t_{su(SDA-SCLH)} \geq$ 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line t_r max + $t_{su(SDA-SCLH)}$ = 1000 + 250 = 1250 ns (according to the Standard-mode I²C-Bus Specification) before the SCL line is released.
(3) A device must internally provide a hold time of at least 300 ns for the SDA signal (referred to the V_{IHmin} of the SCL signal) to bridge the undefined region of the falling edge of SCL.
(4) The maximum $t_{h(SDA-SCLL)}$ has only to be met if the device does not stretch the low period [$t_{w(SCLL)}$] of the SCL signal.
(5) C_b = total capacitance of one bus line in pF. If mixed with HS-mode devices, faster fall-times are allowed.

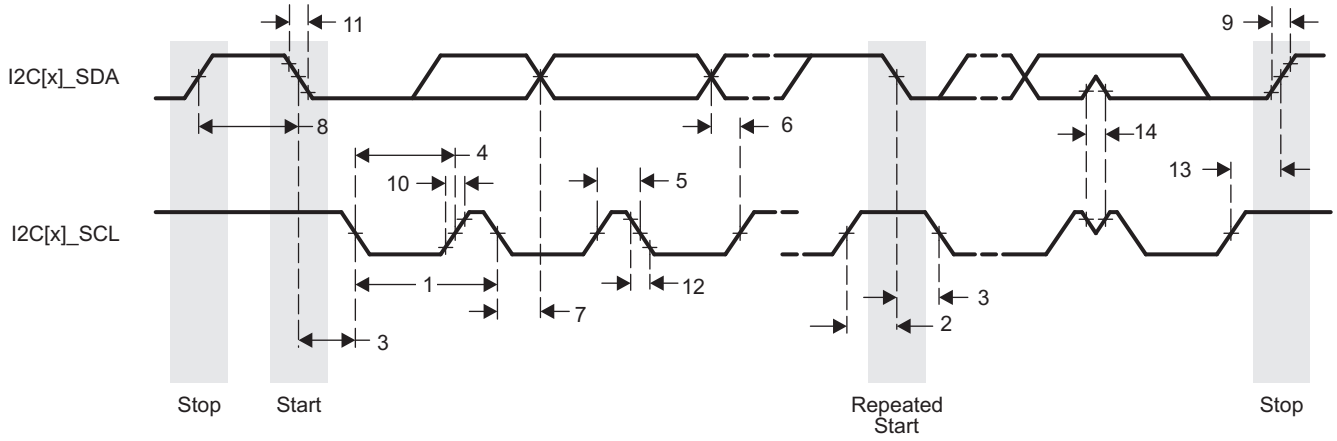


Figure 8-33. I2C Receive Timing

Table 8-28. Switching Characteristics Over Recommended Operating Conditions for I2C Output Timings

(see Figure 8-34)

NO.	PARAMETER		OPP100/OPP120/Turbo/Nitro				UNIT
			STANDARD MODE		FAST MODE		
			MIN	MAX	MIN	MAX	
16	$t_{c(SCL)}$	Cycle time, SCL	10		2.5		µs
17	$t_{su(SCLH-SDAL)}$	Setup time, SCL high before SDA low (for a repeated START condition)	4.7		0.6		µs
18	$t_{h(SDAL-SCLL)}$	Hold time, SCL low after SDA low (for a START and a repeated START condition)	4		0.6		µs
19	$t_{w(SCLL)}$	Pulse duration, SCL low	4.7		1.3		µs
20	$t_{w(SCLH)}$	Pulse duration, SCL high	4		0.6		µs
21	$t_{su(SDAV-SCLH)}$	Setup time, SDA valid before SCL high	250		100		ns
22	$t_{h(SCLL-SDAV)}$	Hold time, SDA valid after SCL low (for I2C bus devices)	0	3.45	0	0.9	µs
23	$t_{w(SDAH)}$	Pulse duration, SDA high between STOP and START conditions	4.7		1.3		µs
24	$t_{r(SDA)}$	Rise time, SDA		1000	$20 + 0.1C_b$ (1)	300	ns
25	$t_{r(SCL)}$	Rise time, SCL		1000	$20 + 0.1C_b$ (1)	300	ns
26	$t_{f(SDA)}$	Fall time, SDA		300	$20 + 0.1C_b$ (1)	300	ns
27	$t_{f(SCL)}$	Fall time, SCL		300	$20 + 0.1C_b$ (1)	300	ns
28	$t_{su(SCLH-SDAH)}$	Setup time, SCL high before SDA high (for STOP condition)	4		0.6		µs
29	C_p	Capacitance for each I2C pin		10		10	pF

(1) C_b = total capacitance of one bus line in pF. If mixed with HS-mode devices, faster fall-times are allowed.

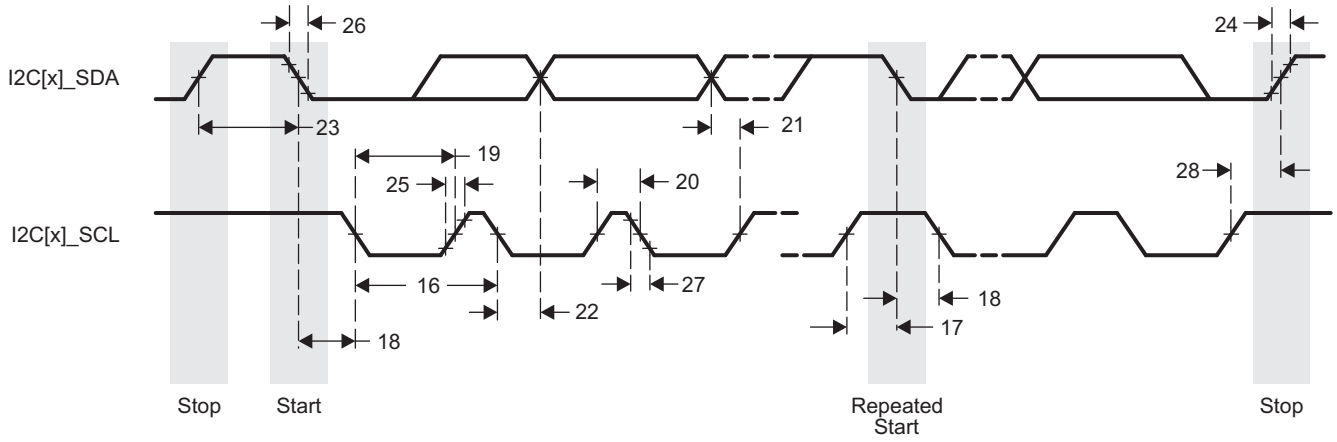


Figure 8-34. I2C Transmit Timing

8.11 Imaging Subsystem (ISS)

The device Imaging Subsystem captures and processes pixel data from external image and video inputs. The inputs can be connected to the Image Processing block through the Parallel Camera Interface (CAM). In addition, a Timing control module provides flash strobe and mechanical shutter interfaces. The features of each component of the ISS are described below.

- Parallel Camera (CAM) interface features:
  - Input format
    - Bayer pattern Raw (up to 16bit) or YCbCr 422 (8-bit or 16-bit) data.
    - ITU-R BT.656/1120 standard format
  - Generates HD/VD timing signals and field ID to an external timing generator, or can synchronize to the external timing generator.
  - Support for progressive and interlaced sensors (hardware support for up to 2 fields and firmware supports for higher number of fields, typically 3-, 4-, and 5-field sensors.
- CSI2 Serial Connection features:
  - Supports up to 1Gb/s data-rate per lane for 1, 2, and 3 Data-lane configurations, and up to 824Mbps per lane for a 4 Data-lane configuration
  - Supports up to four data configurable links in addition to the clock signaling
  - Data merger for 2-, 3-, or 4-data lane configurations
  - 1-D and 2-D addressing mode
  - Supports all primary and secondary MIPI-defined formats (RGB, RAW, YUV, and more)
  - DPCM decompression
  - Image cropping and A-Law/DPCM compression
- Image Sensor Interface (ISIF) features:
  - Support for up to 32K pixels (image size) in both the horizontal and vertical direction
  - Color space conversion for non-Bayer pattern Raw data
  - Digital black clamping with Horizontal/Vertical offset drift compensation
  - Vertical Line defect correction based on a lookup table
  - Color-dependent gain control and black level offset control
  - Ability to control output to the DDR2/DDR3/DDR3L via an external write enable signal
  - Down sampling via programmable culling patterns
  - A-law/DPCM compression
  - Generating 16-, 12- or 8-bit output to memory
- Two independent Resizers
  - Providing two different sizes of outputs simultaneously on one input
  - Maximum line width is 5376 and 2336, respectively
  - YUV422 to YUV420 conversion
  - Data output format: RGB565, ARGB888, YUV422 co sited and YUV4:2:0 planar
  - Resizer Ratio: x1/4096 ~ x20
  - Input from memory
- Timing control module features:
  - STROBE signal for flash pre-strobe and flash strobe
  - SHUTTER signal for mechanical shutter control
  - Global reset control

For more detailed information on the ISS, see the ISS Overview section, the ISS Interfaces section, and the ISS ISP section of the device-specific Technical Reference Manual.

8.11.1 ISS Peripheral Register Description

The ISS peripheral registers are described in the device-specific Technical Reference Manual. Each register is documented as an offset from a base address for the peripheral. The base addresses for all of the peripherals are in the device memory map (see Section 2.10).

8.11.2 ISSCAM Electrical Data/Timing

Table 8-29. Timing Requirements for ISSCAM(1) (see Figure 8-35)

NO.				OPP100/OPP120/Turbo/Nitro			UNIT
				MIN	NOM	MAX	
1	$t_{c(PCLK)}$	Cycle time, PCLK		6.17			ns
2	$t_{w(PCLKH)}$	Pulse duration, PCLK high		2.78			ns
3	$t_{w(PCLKL)}$	Pulse duration, PCLK low		2.78			ns
4	$t_{t(PCLK)}$	Transition time, PCLK				2.64	ns
5	$t_{su(DATA-PCLK)}$	Input setup time, Data/Control valid before PCLK high/low		3.11			ns
	$t_{su(DE-PCLK)}$			3.11			ns
	$t_{su(VS-PCLK)}$			3.11			ns
	$t_{su(HS-PCLK)}$			3.11			ns
	$t_{su(FLD-PCLK)}$			3.11			ns
6	$t_{h(PCLK-DATA)}$	Input hold time, Data valid after PCLK high/low	≤ 148.5 MHz clock rate	-0.5			ns
			> 148.5 MHz and ≤ 162 MHz clock rate	0.0			ns
	$t_{h(PCLK-DE)}$	Input hold time, Control valid after PCLK high/low		-0.5			ns
	$t_{h(PCLK-VS)}$			-0.5			ns
	$t_{h(PCLK-HS)}$			-0.5			ns
	$t_{h(PCLK-FLD)}$			-0.5			ns

(1) H = period of baud rate, 1/programmed baud rate.

Table 8-30. Switching Characteristics Over Recommended Operating Conditions for ISSCAM (see Figure 8-35)

NO.	PARAMETER		OPP100/OPP120/Turbo/Nitro		UNIT
			MIN	MAX	
15	$t_{d(PCLK-FLD)}$	Delay time, PCLK rising/falling clock edge to Control valid	1.64	14.68	ns
16	$t_{d(PCLK-VS)}$	Delay time, PCLK rising/falling clock edge to Control valid	1.64	14.68	ns
17	$t_{d(PCLK-HS)}$	Delay time, PCLK rising/falling clock edge to Control valid	1.64	14.68	ns
18	$t_{d(PCLK-STROBE)}$	Delay time, PCLK rising/falling clock edge to Control valid	1.64	14.68	ns
19	$t_{d(PCLK-SHUTTER)}$	Delay time, PCLK rising/falling clock edge to Control valid	1.64	14.68	ns

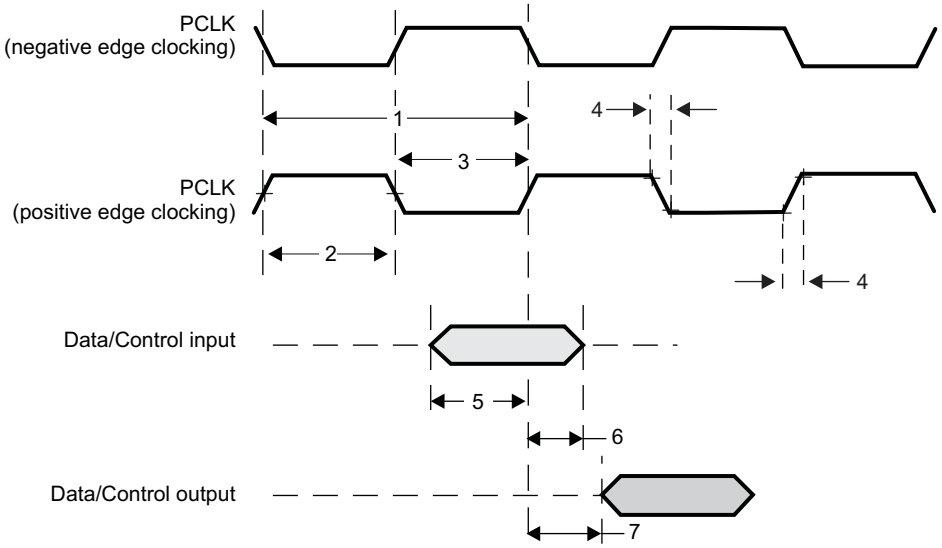


Figure 8-35. ISSCAM Timings

8.11.3 CSI2 PCB Layout Specifications

The following PCB guidelines for CSI2 working at 1 Gbps (up to 3 data lanes), 824 Mbps (up to 4 data lanes), and 800 Mbps (up to 4 data lanes) are based on a three-step design and validation methodology.

For the design of the PCB differential lines, PCB designers need to keep in mind the requirements of Step 1 and Step 2: the characteristic impedance must be 50 Ω, the total length must be smaller than 100 mm, and the length mismatch requirements must be satisfied.

After the PCB design is finished, the S-parameters of the PCB differential lines will be extracted with a 3D Maxwell Equation Solver, such as High-Frequency Structure Simulator (HFSS) or equivalent, and compared to the frequency-domain specification as outlined in Step 3 of the design methodology. If the PCB lines satisfy the frequency-domain specification, the design is done. Otherwise, the design needs to be improved.

8.11.3.1 Step 1: General Guidelines

The general guidelines for the PCB differential lines of CSI2 are given as:

- Single-ended Z0 = 50 Ω
- Total conductor length on the board < 100 mm

In this step, the general rule of thumb for the space S = 2 × W is not designated. Although the S = 2 × W rule is a good rule of thumb, it is not always the best solution. The electrical performance will be checked with the frequency-domain specification in Step 3. Even if the design does not follow the S = 2 × W rule, the differential lines are okay if the lines satisfy the frequency-domain specification in Step 3.

8.11.3.2 Step 2: Length Mismatch Guidelines

8.11.3.2.1 CSI2 at 1.0 Gbps

The guidelines of the length mismatch for CSI2 at 1.0 Gbps are presented in Table 8-31. The intralane length mismatch must be less than 0.5 mm, and the interlane length mismatch must be less than 1.5 mm.

Table 8-31. Length Mismatch Guidelines for CSI2 at 1.0 Gbps

PARAMETER	TYPICAL VALUE	UNIT
Operating speed	1000	Mbps
UI (bit time)	1000	ps
Intralane skew (UI / 300)	3	ps
Length between N and P traces	0.5	mm
Interlane skew (UI / 100)	10	ps
Length between pairs	1.5	mm

8.11.3.2.2 CSI2 at 824 Mbps

The guidelines of the length mismatch for CSI2 at 824 Mbps are presented in Table 8-32. The intralane length mismatch must be less than 0.6 mm, and the interlane length mismatch must be less than 1.8 mm.

Table 8-32. Length Mismatch Guidelines for CSI2 at 824 Mbps

PARAMETER	TYPICAL VALUE	UNIT
Operating speed	824	Mbps
UI (bit time)	1213	ps
Intralane skew (UI / 300)	4	ps
Length between N and P traces	0.6	mm
Interlane skew (UI / 100)	12	ps
Length between pairs	1.8	mm

8.11.3.2.3 CSI2 at 800 Mbps

The guidelines of the length mismatch for CSI2 at 800 Mbps are presented in Table 8-33. The intralane length mismatch must be less than 0.6 mm, and the interlane length mismatch must be less than 1.8 mm.

Table 8-33. Length Mismatch Guidelines for CSI2 at 800 Mbps

PARAMETER	TYPICAL VALUE	UNIT
Operating speed	800	Mbps
UI (bit time)	1250	ps
Intralane skew (UI / 300)	4	ps
Length between N and P traces	0.6	mm
Interlane skew (UI / 100)	12	ps
Length between pairs	1.8	mm

8.11.3.3 Step 3: Frequency-Domain Specification Guidelines

The PCB differential lines should be drawn in order to satisfy the Step 1 and Step 2 requirements. However, although the PCB designer may draw the lines carefully, the lines can have poor electrical performance due to many reasons.

Vertical connections such as vias and non-uniform line connections can degrade the electrical performance of the differential lines. The ground design around the lines can also affect the electrical performance. To ensure that the differential lines are well designed, the frequency-domain behavior must be compared to the frequency-domain specification.

1. Intralane frequency-domain specification
   - Differential-mode characteristics
     - Sdd12, Sdd11/Sdd22
   - Common-mode characteristics
     - Scc11/Scc22
   - Mode-conversion characteristics
     - Scd11, Scd12, Scd21, Scd22, Sdc11, Sdc12, Sdc21, Sdc22
2. Interlane frequency-domain specification
   - Differential-mode characteristics
     - Sdd11/Sdd22
   - Common-mode characteristics
     - Scc11/Scc22

8.12 DDR2/DDR3/DDR3L Memory Controller

The device has a dedicated interface to DDR3L, DDR3 and DDR2 SDRAM. It supports DDR2, DDR3 and DDR3L SDRAM devices with the following features:

- 16-bit or 32-bit data path to external SDRAM memory
- Memory device capacity: 64Mb, 128Mb, 256Mb, 512Mb, 1Gb, 2Gb, and 4Gb devices
- One interface with associated DDR2/DDR3/DDR3L PHY

For details on the DDR2, DDR3 and DDR3L Memory Controller, see the *DDR2/DDR3/DDR3L Memory Controller* chapter in the device-specific Technical Reference Manual.

8.12.1 DDR2/3/3L Memory Controller Register Descriptions

The DDR2/3/3L peripheral registers are described in the device-specific Technical Reference Manual. Each register is documented as an offset from a base address for the peripheral. The base addresses for all of the peripherals are in the device memory map (see Section 2.10).

8.12.2 DDR2 Routing Specifications

8.12.2.1 Board Designs

TI only supports board designs that follow the guidelines outlined in this document. The switching characteristics and the timing diagram for the DDR2 memory controller are shown in Table 8-34 and Figure 8-36.

Table 8-34. Switching Characteristics Over Recommended Operating Conditions for DDR2 Memory Controller

NO.	PARAMETER		-1G		UNIT
			MIN	MAX	
1	$t_{c(DDR\_CLK)}$	Cycle time, DDR_CLK	2.5	8	ns

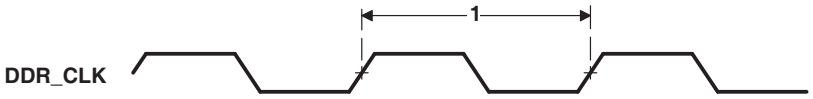


Figure 8-36. DDR2 Memory Controller Clock Timing

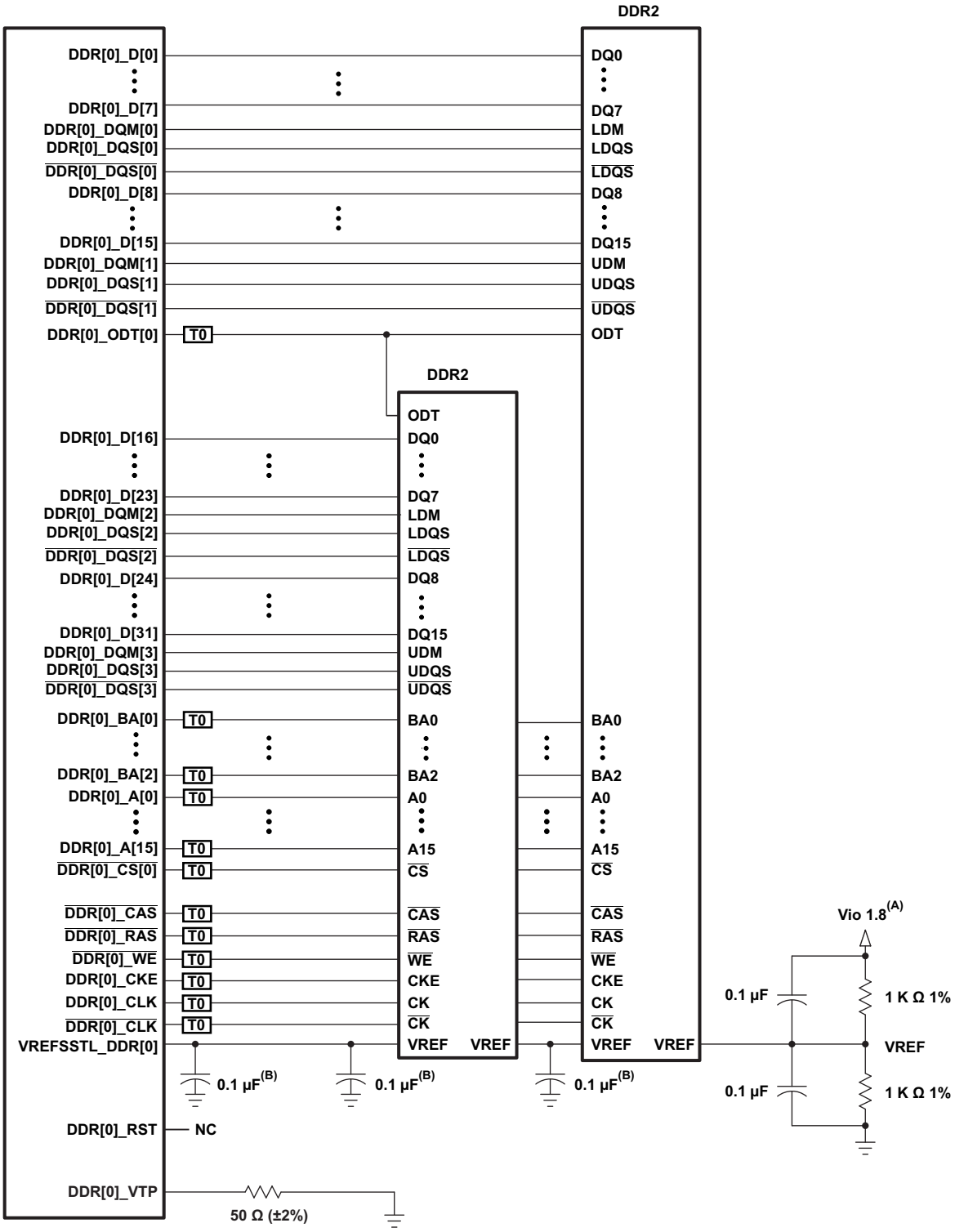
8.12.2.2 DDR2 Interface

This section provides the timing specification for the DDR2 interface as a PCB design and manufacturing specification. The design rules constrain PCB trace length, PCB trace skew, signal integrity, cross-talk, and signal timing. These rules, when followed, result in a reliable DDR2 memory system without the need for a complex timing closure process. For more information regarding the guidelines for using this DDR2 specification, see the *Understanding TI's PCB Routing Rule-Based DDR Timing Specification* Application Report (Literature Number: SPRAAV0).

8.12.2.2.1 DDR2 Interface Schematic

Figure 8-37 shows the DDR2 interface schematic for a x32 DDR2 memory system. In Figure 8-38 the x16 DDR2 system schematic is identical except that the high-word DDR2 device is deleted.

When not using a DDR2 interface, the proper method of handling the unused pins is to tie off the DQS pins by pulling the non-inverted DQS pin to the DVDD_DDR[0] supply via a 1k-Ω resistor and pulling the inverted DQS pin to ground via a 1k-Ω resistor. This needs to be done for each byte not used. Also, include the 50-Ω pulldown for DDR[0]_VTP. The DVDD_DDR[0] and VREFSSTL_DDR[0] power supply pins must be connected to their respective power supplies even if DDR[0] is not used. All other DDR interface pins can be left unconnected. Note that the supported modes for use of the DDR EMIF are 32-bits wide, 16-bits wide, or not used.

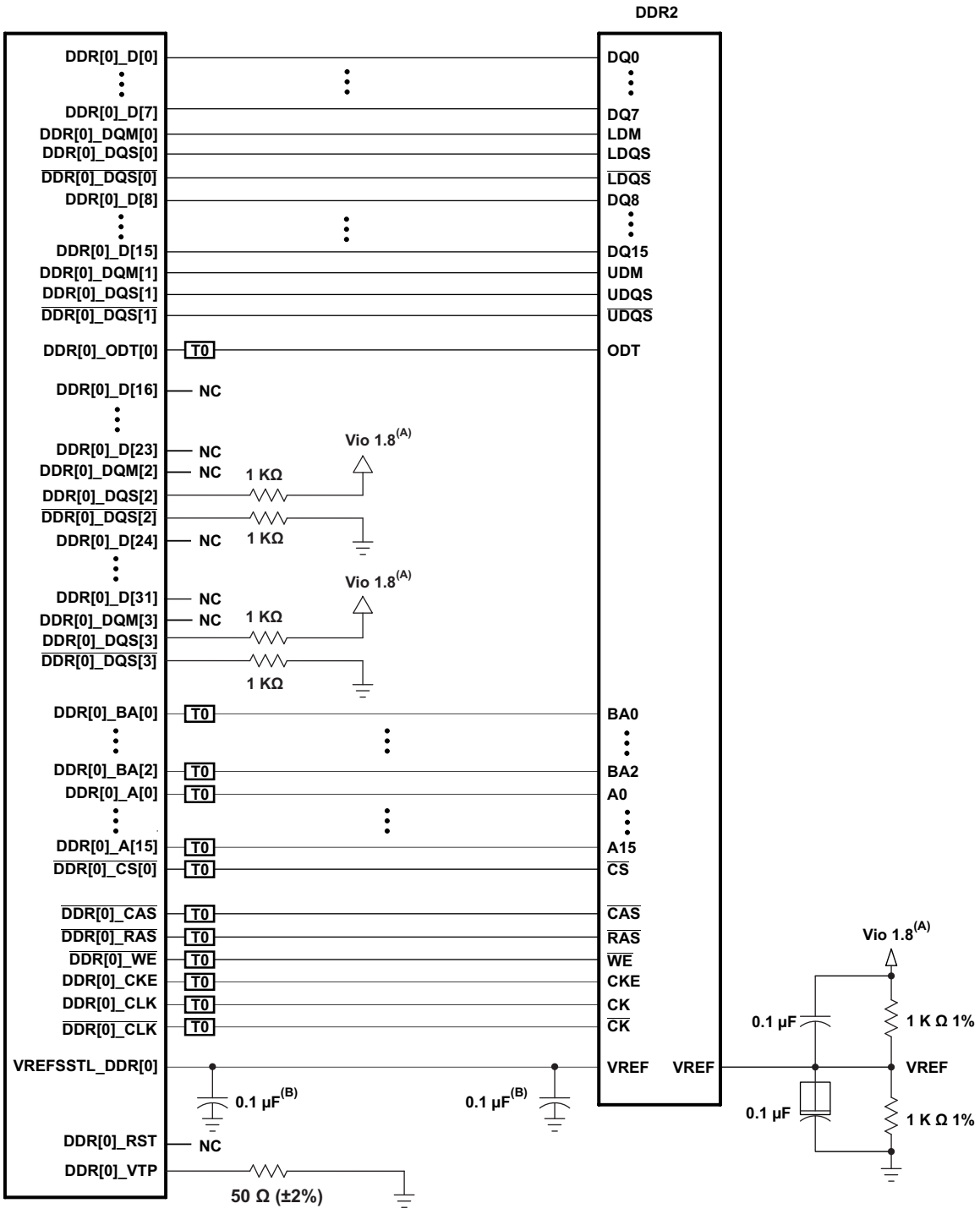


T0 Termination is required. See terminator comments.

A. Vio1.8 is the power supply for the DDR2 memories and the device DDR2 interface.

B. One of these capacitors can be eliminated if the divider and its capacitors are placed near a VREF pin.

Figure 8-37. 32-Bit DDR2 High-Level Schematic



T0 Termination is required. See terminator comments.

A. Vio1.8 is the power supply for the DDR2 memories and the device DDR2 interface.

B. One of these capacitors can be eliminated if the divider and its capacitors are placed near a VREF pin.

Figure 8-38. 16-Bit DDR2 High-Level Schematic

8.12.2.2.2 Compatible DDR2 Devices

Table 8-35 shows the parameters of the DDR2 devices that are compatible with this interface. Generally, the DDR2 interface is compatible with x16 DDR2-800 speed grade DDR2 devices.

Table 8-35. Compatible DDR2 Devices (Per Interface)

NO.	PARAMETER	MIN	MAX	UNIT
1	DDR2 device speed grade (1)	DDR2-800		
2	DDR2 device bit width	x16	x16	Bits
3	DDR2 device count (2)	1	2	Devices
4	DDR2 device ball count (3)	84	92	Balls

(1) Higher DDR2 speed grades are supported due to inherent DDR2 backwards compatibility.
(2) One DDR2 device is used for a 16-bit DDR2 memory system. Two DDR2 devices are used for a 32-bit DDR2 memory system.
(3) The 92-ball devices are retained for legacy support. New designs will migrate to 84-ball DDR2 devices. Electrically, the 92- and 84-ball DDR2 devices are the same.

8.12.2.2.3 PCB Stackup

The minimum stackup required for routing the device is a six-layer stackup as shown in Table 8-36. Additional layers may be added to the PCB stackup to accommodate other circuitry or to reduce the size of the PCB footprint.

Table 8-36. Minimum PCB Stackup

LAYER	TYPE	DESCRIPTION
1	Signal	Top routing mostly horizontal
2	Plane	Ground
3	Plane	Power
4	Signal	Internal routing
5	Plane	Ground
6	Signal	Bottom routing mostly vertical

Complete stackup specifications are provided in Table 8-37.

Table 8-37. PCB Stackup Specifications

NO.	PARAMETER	MIN	TYP	MAX	UNIT
1	PCB routing/plane layers	6			
2	Signal routing layers	3			
3	Full ground layers under DDR2 routing region	2			
4	Number of ground plane cuts allowed within DDR routing region			0	
5	Number of ground reference planes required for each DDR2 routing layer	1			
6	Number of layers between DDR2 routing layer and reference ground plane			0	
7	PCB feature spacing		4		Mils
8	PCB trace width, w		4		Mils
9	PCB BGA escape via pad size(1)		18	20	Mils
10	PCB BGA escape via hole size(1)		10		Mils
11	Processor BGA pad size		0.4		mm
13	Single-ended impedance, Zo	50		75	Ω
14	Impedance control(2)	Z-5	Z	Z+5	Ω

(1) A 20/10 via may be used if enough power routing resources are available. An 18/10 via allows for more flexible power routing to the processor.
(2) Z is the nominal singled-ended impedance selected for the PCB specified by item 13.

8.12.2.2.4 Placement

Figure 8-39 shows the required placement for the processor as well as the DDR2 devices. The dimensions for this figure are defined in Table 8-38. The placement does not restrict the side of the PCB on which the devices are mounted. The ultimate purpose of the placement is to limit the maximum trace lengths and allow for proper routing space. For a 16-bit DDR memory system, the high-word DDR2 device is omitted from the placement.

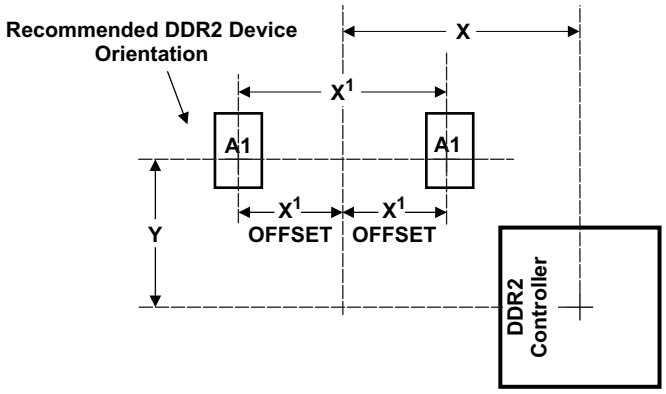


Figure 8-39. Device and DDR2 Device Placement

Table 8-38. Placement Specifications

NO.	PARAMETER	MIN	MAX	UNIT
1	X + Y (1) (2)		1660	Mils
2	X' (1) (2)		1280	Mils
3	X' Offset (1) (2) (3)		650	Mils
4	DDR2 keepout region (4)			
5	Clearance from non-DDR2 signal to DDR2 keepout region (5)	4		w

(1) For dimension definitions, see Figure 8-37.
(2) Measurements from center of processor to center of DDR2 device.
(3) For 16-bit memory systems, it is recommended that X' offset be as small as possible.
(4) DDR2 keepout region to encompass entire DDR2 routing area.
(5) Non-DDR2 signals allowed within DDR2 keepout region provided they are separated from DDR2 routing layers by a ground plane.

8.12.2.2.5 DDR2 Keepout Region

The region of the PCB used for the DDR2 circuitry must be isolated from other signals. The DDR2 keepout region is defined for this purpose and is shown in Figure 8-40. The size of this region varies with the placement and DDR routing. Additional clearances required for the keepout region are shown in Table 8-38.

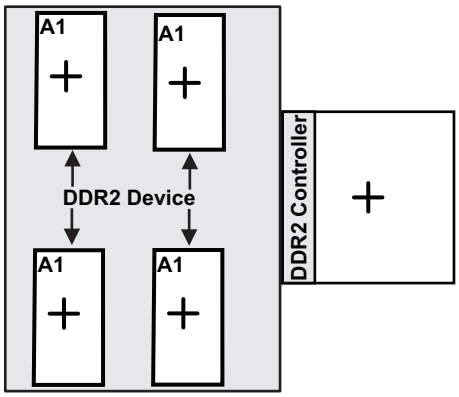


Figure 8-40. DDR2 Keepout Region

NOTE

The region shown in should encompass all the DDR2 circuitry and varies depending on placement. Non-DDR2 signals should not be routed on the DDR signal layers within the DDR2 keepout region. Non-DDR2 signals may be routed in the region, provided they are routed on layers separated from DDR2 signal layers by a ground layer. No breaks should be allowed in the reference ground layers in this region. In addition, the 1.8-V power plane should cover the entire keepout region. Routes for the DDR interface must be separated by at least 4x; the more separation, the better.

8.12.2.2.6 Bulk Bypass Capacitors

Bulk bypass capacitors are required for moderate speed bypassing of the DDR2 and other circuitry. Table 8-39 contains the minimum numbers and capacitance required for the bulk bypass capacitors. Note that this table only covers the bypass needs of the DDR2 interfaces and DDR2 device. Additional bulk bypass capacitance may be needed for other circuitry.

Table 8-39. Bulk Bypass Capacitors

No.	Parameter	Min	Max	Unit
1	DVDD18 bulk bypass capacitor count(1)	3		Devices
2	DVDD18 bulk bypass total capacitance	30		µF
3	DDR bulk bypass capacitor count(1)	1		Devices
4	DDR bulk bypass total capacitance(1)	10		µF

(1) These devices should be placed near the device they are bypassing, but preference should be given to the placement of the high-speed (HS) bypass capacitors.

8.12.2.2.7 High-Speed Bypass Capacitors

High-speed (HS) bypass capacitors are critical for proper DDR2 interface operation. It is particularly important to minimize the parasitic series inductance of the HS bypass capacitors, processor/DDR power, and processor/DDR ground connections. Table 8-40 contains the specification for the HS bypass capacitors as well as for the power connections on the PCB. Due to the number of required bypass capacitors, it is recommended that the bypass capacitors are placed before routing the board.

Table 8-40. High-Speed Bypass Capacitors

NO.	PARAMETER	MIN	MAX	UNIT
1	HS bypass capacitor package size(1)		0402	10 Mils
2	Distance from HS bypass capacitor to device being bypassed		250	Mils
3	Number of connection vias for each HS bypass capacitor(2)	2		Vias
4	Trace length from bypass capacitor contact to connection via	1	30	Mils
5	Number of connection vias for each processor power/ground ball	1		Vias
6	Trace length from processor power/ground ball to connection via		35	Mils
7	Number of connection vias for each DDR2 device power/ground ball	1		Vias
8	Trace length from DDR2 device power/ground ball to connection via		35	Mils
9	DVDD18 HS bypass capacitor count(3)	20		Devices
10	DVDD18 HS bypass capacitor total capacitance	1.2		µF
11	DDR device HS bypass capacitor count(4)(5)	8		Devices
12	DDR device HS bypass capacitor total capacitance(5)	0.4		µF

(1) LxW, 10-mil units, that is, a 0402 is a 40x20-mil surface-mount capacitor.
(2) An additional HS bypass capacitor can share the connection vias only if it is mounted on the opposite side of the board.
(3) These devices should be placed as close as possible to the device being bypassed.
(4) These devices should be placed as close as possible to the device being bypassed.
(5) Per DDR device.

8.12.2.2.8 Net Classes

Table 8-41 lists the clock net classes for the DDR2 interface. Table 8-42 lists the signal net classes, and associated clock net classes, for the signals in the DDR2 interface. These net classes are used for the termination and routing rules that follow.

Table 8-41. Clock Net Class Definitions

CLOCK NET CLASS	PROCESSOR PIN NAMES
CK	DDR[0]_CLK/$\overline{\text{DDR[0]\_CLK}}$
DQS0	DDR[0]_DQS[0]/$\overline{\text{DDR[0]\_DQS[0]}}$
DQS1	DDR[0]_DQS[1]/$\overline{\text{DDR[0]\_DQS[1]}}$
DQS2(1)	DDR[0]_DQS[2]/$\overline{\text{DDR[0]\_DQS[2]}}$
DQS3(1)	DDR[0]_DQS[3]/$\overline{\text{DDR[0]\_DQS[3]}}$

(1) Only used on 32-bit wide DDR2 memory systems.

Table 8-42. Signal Net Class Definitions

CLOCK NET CLASS	ASSOCIATED CLOCK NET CLASS	PROCESSOR PIN NAMES
ADDR_CTRL	CK	DDR[0]_BA[2:0], DDR[0]_A[15:0], DDR[0]_CS[x], DDR[0]_CAS, DDR[0]_RAS, DDR[0]_WE, DDR[0]_CKE, DDR[0]_ODT[0]
DQ0	DQS0	DDR[0]_D[7:0], DDR[0]_DQM[0]
DQ1	DQS1	DDR[0]_D[15:8], DDR[0]_DQM[1]
DQ2(1)	DQS2	DDR[0]_D[23:16], DDR[0]_DQM[2]
DQ3(1)	DQS3	DDR[0]_D[31:24], DDR[0]_DQM[3]

(1) Only used on 32-bit wide DDR2 memory systems.

8.12.2.2.9 DDR2 Signal Termination

Signal terminators are required in CK and ADDR_CTRL net classes. Serial terminators may be used on data lines to reduce EMI risk; however, serial terminations are the only type permitted. ODT's are integrated on the data byte net classes. They should be enabled to ensure signal integrity.Table 8-43 shows the specifications for the series terminators.

Table 8-43. DDR2 Signal Terminations

NO.	PARAMETER	MIN	TYP	MAX	UNIT
1	CK net class(1)(2)	0		10	Ω
2	ADDR_CTRL net class(1) (2)(3)(4)	0	22	Zo	Ω
3	Data byte net classes (DQS0-DQS3, DQ0-DQ3)(5)	0		Zo	Ω

(1) Only series termination is permitted, parallel or SST specifically disallowed on board.
(2) Only required for EMI reduction.
(3) Terminator values larger than typical only recommended to address EMI issues.
(4) Termination value should be uniform across net class.
(5) No external terminations allowed for data byte net classes. ODT is to be used.

8.12.2.2.10 VREFSSTL_DDR Routing

VREFSSTL_DDR is used as a reference by the input buffers of the DDR2 memories as well as the processor. VREF is intended to be half the DDR2 power supply voltage and should be created using a resistive divider as shown in Figure 8-38. Other methods of creating VREF are not recommended. Figure 8-41 shows the layout guidelines for VREF.

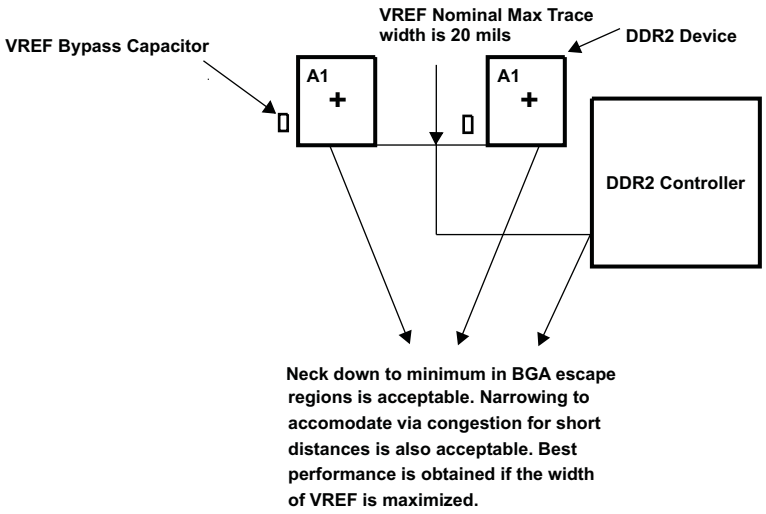


Figure 8-41. VREF Routing and Topology

8.12.2.3 DDR2 CK and ADDR_CTRL Routing

Figure 8-42 shows the topology of the routing for the CK and ADDR_CTRL net classes. The route is a balanced *T* as it is intended that the length of segments B and C be equal. In addition, the length of A (A'+A") should be maximized.

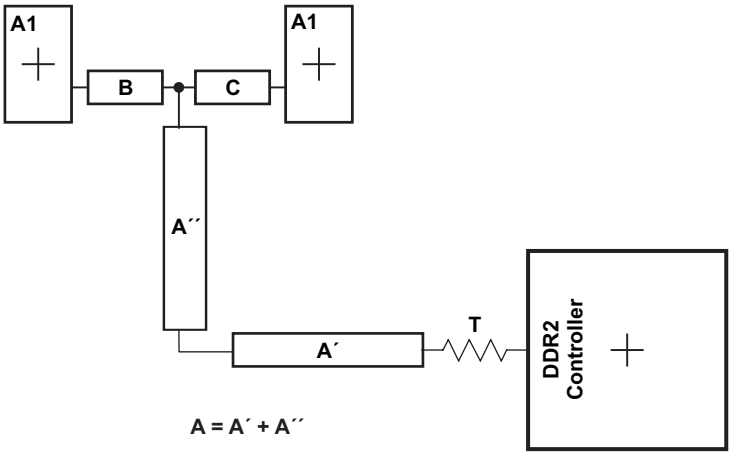


Figure 8-42. CK and ADDR_CTRL Routing and Topology

Table 8-44. CK and ADDR_CTRL Routing Specification (1)

NO.	PARAMETER	MIN	TYP	MAX	UNIT
1	Center-to-center CK-$\overline{CK}$ spacing			2w	
2	CK/$\overline{CK}$ skew(1)			25	Mils
3	CK A-to-B/A-to-C skew length mismatch(2)			25	Mils
4	CK B-to-C skew length mismatch			25	Mils
5	Center-to-center CK to other DDR2 trace spacing(3)	4w			
6	CK/ADDR_CTRL nominal trace length(4)	CACLM-50	CACLM	CACLM+50	Mils
7	ADDR_CTRL-to-CK skew length mismatch			100	Mils
8	ADDR_CTRL-to-ADDR_CTRL skew length mismatch			100	Mils
9	Center-to-center ADDR_CTRL to other DDR2 trace spacing(3)	4w			
10	Center-to-center ADDR_CTRL to other ADDR_CTRL trace spacing(3)	3w			
11	ADDR_CTRL A-to-B/A-to-C skew length mismatch(2)			100	Mils
12	ADDR_CTRL B-to-C skew length mismatch			100	Mils

(1) The length of segment A = A' + A″ as shown in Figure 8-42.
(2) Series terminator, if used, should be located closest to the device.
(3) Center-to-center spacing is allowed to fall to minimum (2w) for up to 500 mils of routed length to accommodate BGA escape and routing congestion.
(4) CACLM is the longest Manhattan distance of the CK and ADDR_CTRL net classes.

Figure 8-43 shows the topology and routing for the DQS and DQ net classes; the routes are point to point. Skew matching across bytes is not needed nor recommended.

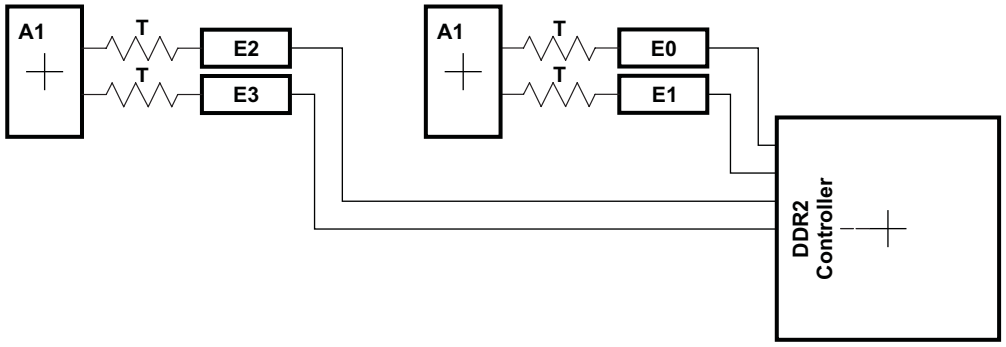


Figure 8-43. DQS and DQ Routing and Topology

Table 8-45. DQS and DQ Routing Specification

NO.	PARAMETER	MIN	TYP	MAX	UNIT
1	Center-to-center DQS-DQSn spacing in E0|E1|E2|E3			2w	
2	DQS-DQSn skew in E0|E1|E2|E3			25	Mils
3	Center-to-center DQS to other DDR2 trace spacing(1)	4w			
4	DQS/DQ nominal trace length (2)(3)(4)	DQLM-50	DQLM	DQLM+50	Mils
5	DQ-to-DQS skew length mismatch(2)(3)(4)			100	Mils
6	DQ-to-DQ skew length mismatch(2)(3)(4)			100	Mils
7	DQ-to-DQ/DQS via count mismatch(2)(3)(4)			1	Vias
8	Center-to-center DQ to other DDR2 trace spacing(1)(5)	4w			
9	Center-to-center DQ to other DQ trace spacing(1)(6)(7)	3w			
10	DQ/DQS E skew length mismatch(2)(3)(4)			100	Mils

(1) Center-to-center spacing is allowed to fall to minimum (2w) for up to 500 mils of routed length to accommodate BGA escape and routing congestion.
(2) A 16-bit DDR memory system has two sets of data net classes; one for data byte 0, and one for data byte 1, each with an associated DQS (2 DQSs) per DDR EMIF used.
(3) A 32-bit DDR memory system has four sets of data net classes; one each for data bytes 0 through 3, and each associated with a DQS (4 DQSs) per DDR EMIF used.
(4) There is no need, and it is not recommended, to skew match across data bytes; that is, from DQS0 and data byte 0 to DQS1 and data byte 1.
(5) DQs from other DQS domains are considered *other DDR2 trace*.
(6) DQs from other data bytes are considered *other DDR2 trace*.
(7) DQLM is the longest Manhattan distance of each of the DQS and DQ net classes.

8.12.3 DDR3/DDR3L Routing Specifications

8.12.3.1 Board Designs

TI only supports board designs utilizing DDR3/DDR3L memory that follow the guidelines in this document. The switching characteristics and timing diagram for the DDR3/DDR3L memory controller are shown in Table 8-46 and Figure 8-44. For the remainder of this section, DDR3 refers to both DDR3 and DDR3L.

Table 8-46. Switching Characteristics Over Recommended Operating Conditions for DDR3 Memory Controller

NO.	PARAMETER	-1G		UNIT
		MIN	MAX	
1	$t_{c(DDR\_CLK)}$ Cycle time, DDR_CLK	1.876	3.3(1)	ns

(1) This is the absolute maximum the clock period can be. Actual maximum clock period may be limited by DDR3 speed grade and operating frequency (see the *DDR2/3 Memory Controller* chapter in the device-specific Technical Reference Manual).

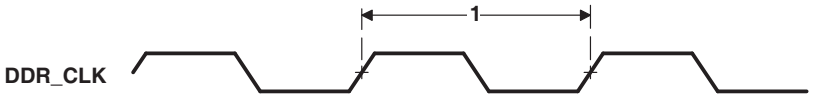


Figure 8-44. DDR3 Memory Controller Clock Timing

8.12.3.1.1 DDR3 versus DDR2

This specification only covers device PCB designs that utilize DDR3 memory. Designs using DDR2 memory should use the PCB design specifications for DDR2 memory in Section 8.12.2. While similar, the two memory systems have different requirements. It is currently not possible to design one PCB that covers both DDR2 and DDR3.

8.12.3.2 DDR3 Device Combinations

Since there are several possible combinations of device counts and single- or dual-side mounting, Table 8-47 summarizes the supported device configurations.

Table 8-47. Supported DDR3 Device Combinations

NUMBER OF DDR3 DEVICES	DDR3 DEVICE WIDTH (BITS)	MIRRORED?	DDR3 EMIF WIDTH (BITS)
1	16	N	16
2	8	Y(1)	16
2	16	N	32
2	16	Y(1)	32
4	8	N	32
4	8	Y(2)	32

(1) Two DDR3 devices are mirrored when one device is placed on the top of the board and the second device is placed on the bottom of the board.
(2) This is two mirrored pairs of DDR3 devices.

8.12.3.3 DDR3 Interface Schematic

8.12.3.3.1 32-Bit DDR3 Interface

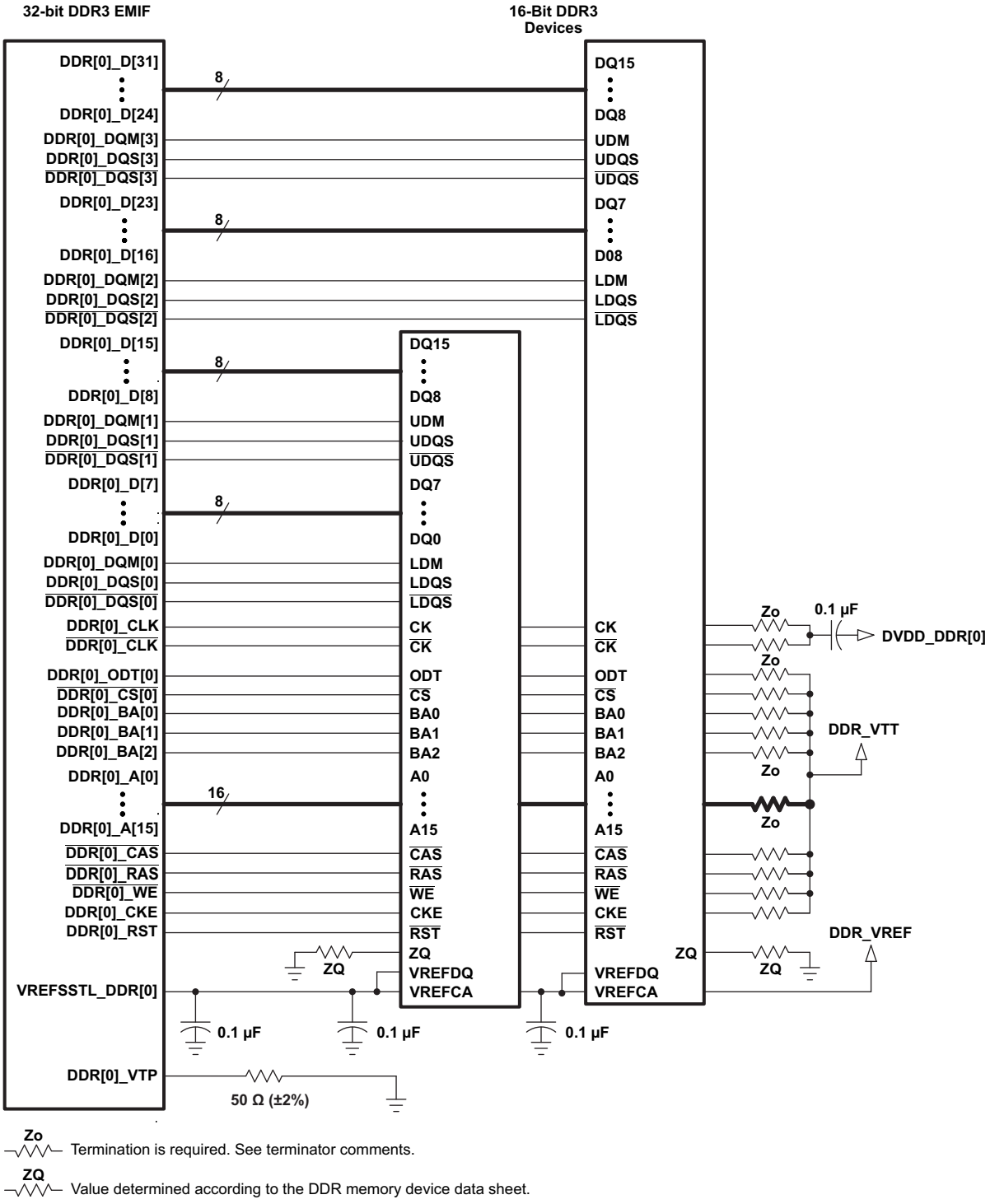
The DDR3 interface schematic varies, depending upon the width of the DDR3 devices used and the width of the bus used (16 or 32 bits). General connectivity is straightforward and very similar. 16-bit DDR devices look like two 8-bit devices. Figure 8-45 and Figure 8-46 show the schematic connections for 32-bit interfaces using x16 devices.

8.12.3.3.2 16-Bit DDR3 Interface

Note that the 16-bit wide interface schematic is practically identical to the 32-bit interface (see Figure 8-45 and Figure 8-46); only the high-word DDR memories are removed and the unused DQS inputs are tied off. The processor DDR[0]_DQS[2] and DDR[0]_DQS[3] pins should be pulled to the DDR supply via 1-kΩ resistors. Similarly, the DDR[0]_DQS[2] and DDR[0]_DQS[3] pins should be pulled to ground via 1-kΩ resistors.

When not using a DDR interface, the proper method of handling the unused pins is to tie off the DDR[0]_DQS[n] pins to the corresponding DVDD_DDR[0] supply via a 1-kΩ resistor and pulling the DDR[0]_DQS[n] pins to ground via a 1k-Ω resistor. This needs to be done for each byte not used. Although these signals have internal pullups and pulldowns, external pullups and pulldowns provide additional protection against external electrical noise causing activity on the signals.

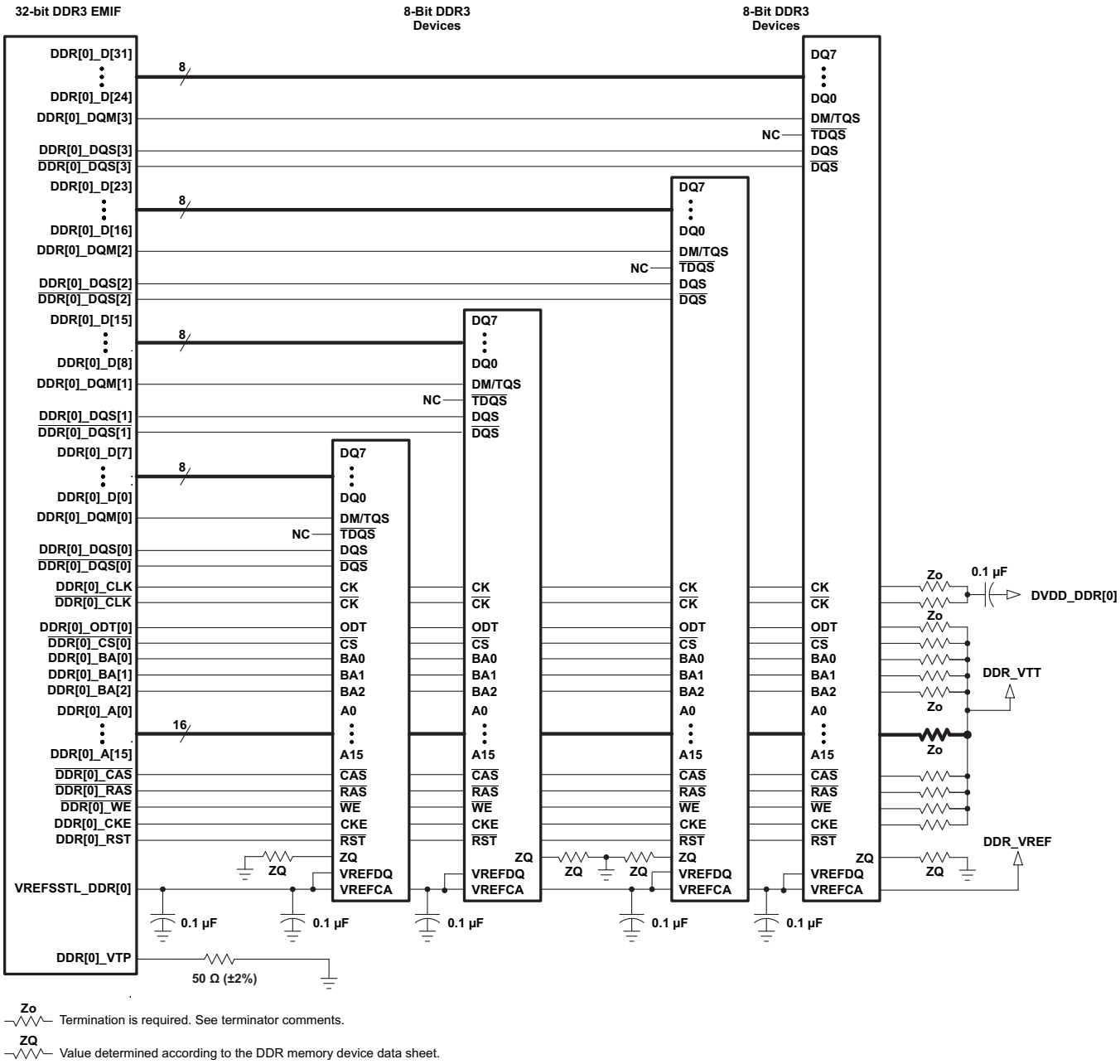
Also, include the 50-Ω pulldown for DDR[0]_VTP. The DVDD_DDR[0] and VREFSSTL_DDR[0] power supply pins must be connected to their respective power supplies even if DDR[0] is not used. All other DDR interface pins can be left unconnected. Note that the supported modes for use of the DDR EMIF are 32 bits wide, 16 bits wide, or not used.



Zo Termination is required. See terminator comments.

ZQ Value determined according to the DDR memory device data sheet.

Figure 8-45. 32-Bit, One-Bank DDR3 Interface Schematic Using Two 16-Bit DDR3 Devices



Zo — Termination is required. See terminator comments.

ZQ — Value determined according to the DDR memory device data sheet.

Figure 8-46. 32-Bit, One-Bank DDR3 Interface Schematic Using Four 8-Bit DDR3 Devices

8.12.3.4 Compatible DDR3 Devices

Table 8-48 shows the parameters of the DDR3 devices that are compatible with this interface. Generally, the interface is compatible with DDR3 devices in the x8 or x16 widths.

Table 8-48. Compatible DDR3 Devices (Per Interface)

NO.	PARAMETER	MIN	MAX	UNIT
1	DDR3 device speed grade: ≤ 400 MHz clock rate(1)	DDR3-800	(2)	
2	DDR3 device speed grade: > 400 MHz clock rate(1)	DDR3-1600	(2)	
3	DDR3 device bit width	x8	x16	Bits
4	DDR3 device count(3)	2	4	Devices

(1) DDR3 speed grade depends on desired clock rate. Data rate is 2x the clock rate. For DDR3-800, the clock rate is 400 MHz.
(2) DDR3 devices with higher speed grades are supported; however, max clock rate will still be limited to 533 MHz as stated in Table 8-46 *Switching Characteristics Over Recommended Operating Conditions for DDR3 Memory Controller*.
(3) For valid DDR3 device configurations and device counts, see Section 8.12.3.3, Figure 8-45, and Figure 8-46.

8.12.3.5 PCB Stackup

The minimum stackup for routing the DDR3 interface is a four-layer stack up as shown in Table 8-49. Additional layers may be added to the PCB stackup to accommodate other circuitry, enhance SI/EMI performance, or to reduce the size of the PCB footprint. A six-layer stackup is shown in Table 8-50. Complete stackup specifications are provided in Table 8-51.

Table 8-49. Minimum PCB Stackup

LAYER	TYPE	DESCRIPTION
1	Signal	Top routing mostly vertical
2	Plane	Split power plane
3	Plane	Full ground plane
4	Signal	Bottom routing mostly horizontal

Table 8-50. Six-Layer PCB Stackup Suggestion

LAYER	TYPE	DESCRIPTION
1	Signal	Top routing mostly vertical
2	Plane	Ground
3	Plane	Split power plane
4	Plane	Split power plane or Internal routing
5	Plane	Ground
6	Signal	Bottom routing mostly horizontal

Table 8-51. PCB Stackup Specifications

NO.	PARAMETER	MIN	TYP	MAX	UNIT
1	PCB routing/plane layers	4	6		
2	Signal routing layers	2			
3	Full ground reference layers under DDR3 routing region (1)	1			
4	Full 1.35-V/1.5-V power reference layers under the DDR3 routing region (1)	1			
5	Number of reference plane cuts allowed within DDR routing region (2)			0	
6	Number of layers between DDR3 routing layer and reference plane (3)			0	
7	PCB feature spacing		4		Mils
8	PCB trace width, w		4		Mils
9	PCB BGA escape via pad size (4)		18	20	Mils
10	PCB BGA escape via hole size		10		Mils
11	Processor BGA pad size		0.4		mm
13	Single-ended impedance, Zo	50		75	Ω
14	Impedance control (5)	Z-5	Z	Z+5	Ω

(1) Ground reference layers are preferred over power reference layers. Be sure to include bypass caps to accommodate reference layer return current as the trace routes switch routing layers.
(2) No traces should cross reference plane cuts within the DDR routing region. High-speed signal traces crossing reference plane cuts create large return current paths which can lead to excessive crosstalk and EMI radiation.
(3) Reference planes are to be directly adjacent to the signal plane to minimize the size of the return current loop.
(4) An 18-mil pad assumes Via Channel is the most economical BGA escape. A 20-mil pad may be used if additional layers are available for power routing. An 18-mil pad is required for minimum layer count escape.
(5) Z is the nominal singled-ended impedance selected for the PCB specified by item 13.

8.12.3.6 Placement

Figure 8-47 shows the required placement for the processor as well as the DDR3 devices. The dimensions for this figure are defined in Table 8-52. The placement does not restrict the side of the PCB on which the devices are mounted. The ultimate purpose of the placement is to limit the maximum trace lengths and allow for proper routing space. For a 16-bit DDR memory system, the high-word DDR3 devices are omitted from the placement.

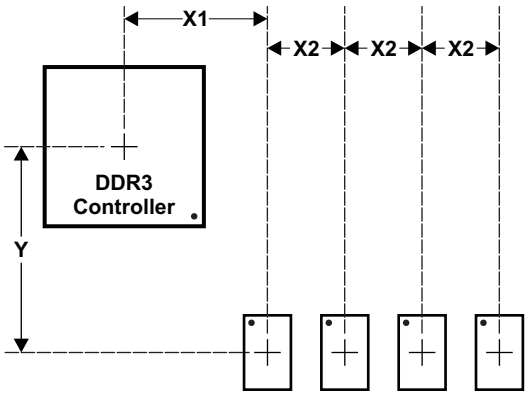


Figure 8-47. Placement Specifications

Table 8-52. Placement Specifications

NO.	PARAMETER	MIN	MAX	UNIT
1	X1[1][2][3]		1000	Mils
2	X2[1][2]		600	Mils
3	Y Offset[1][2][3]		1500	Mils
4	DDR3 keepout region			
5	Clearance from non-DDR3 signal to DDR3 keepout region[4][5]	4		w

(1) For dimension definitions, see Figure 8-47.
(2) Measurements from center of processor to center of DDR3 device.
(3) Minimizing X1 and Y improves timing margins.
(4) w is defined as the signal trace width.
(5) Non-DDR3 signals allowed within DDR3 keepout region provided they are separated from DDR3 routing layers by a ground plane.

8.12.3.7 DDR3 Keepout Region

The region of the PCB used for DDR3 circuitry must be isolated from other signals. The DDR3 keepout region is defined for this purpose and is shown in Figure 8-48. The size of this region varies with the placement and DDR routing. Additional clearances required for the keepout region are shown in Table 8-52. Non-DDR3 signals should not be routed on the DDR signal layers within the DDR3 keepout region. Non-DDR3 signals may be routed in the region, provided they are routed on layers separated from the DDR signal layers by a ground layer. No breaks should be allowed in the reference ground layers in this region. In addition, the 1.35-V/1.5-V DDR3L/DDR3 power plane should cover the entire keepout region. Also note that the DDR3 controller's signals should be separated from each other by the specification in item 5 (see Table 8-52 for item 5 specification).

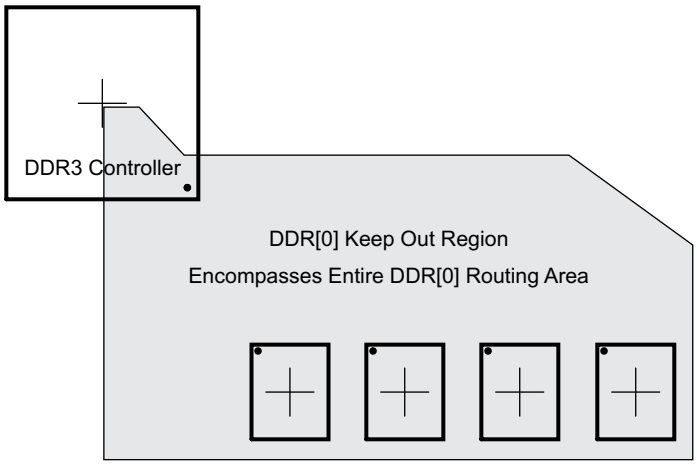


Figure 8-48. DDR3 Keepout Region

8.12.3.8 Bulk Bypass Capacitors

Bulk bypass capacitors are required for moderate speed bypassing of the DDR3 and other circuitry. Table 8-53 contains the minimum numbers and capacitance required for the bulk bypass capacitors. Note that this table only covers the bypass needs of the DDR3 controller and DDR3 devices. Additional bulk bypass capacitance may be needed for other circuitry.

Table 8-53. Bulk Bypass Capacitors

NO.	PARAMETER	MIN	MAX	UNIT
1	DVDD_DDR[0] bulk bypass capacitor count(1)	6		Devices
2	DVDD_DDR[0] bulk bypass total capacitance	140		µF

(1) These devices should be placed near the devices they are bypassing, but preference should be given to the placement of the high-speed (HS) bypass capacitors and DDR3 signal routing.

8.12.3.9 High-Speed Bypass Capacitors

High-speed (HS) bypass capacitors are critical for proper DDR3 interface operation. It is particularly important to minimize the parasitic series inductance of the HS bypass capacitors, processor/DDR power, and processor/DDR ground connections. Table 8-54 contains the specification for the HS bypass capacitors as well as for the power connections on the PCB. Generally speaking, it is good to:

1. Fit as many HS bypass capacitors as possible. Due to the number of required bypass capacitors, it is recommended that the bypass capacitors are placed before routing the board.
2. Minimize the distance from the bypass cap to the pins/balls being bypassed.
3. Use the smallest physical sized capacitors possible with the highest capacitance readily available.
4. Connect the bypass capacitor pads to their vias using the widest traces possible and using the largest hole size via possible.
5. Minimize via sharing. Note the limits on via sharing shown in Table 8-54.

Table 8-54. High-Speed Bypass Capacitors

NO.	PARAMETER	MIN	TYP	MAX	UNIT
1	HS bypass capacitor package size(1)		201	402	10 Mils
2	Distance, HS bypass capacitor to processor being bypassed(2)(3)(4)			400	Mils
3	Processor DVDD_DDR[0] HS bypass capacitor count	35			Devices
4	Processor DVDD_DDR[0] HS bypass capacitor total capacitance	2.5			µF
5	Number of connection vias for each device power/ground ball(5)				Vias
6	Trace length from device power/ground ball to connection via(2)		35	70	Mils
7	Distance, HS bypass capacitor to DDR device being bypassed(6)			150	Mils
8	DDR3 device HS bypass capacitor count(7)	12			Devices
9	DDR3 device HS bypass capacitor total capacitance(7)	0.85			µF
10	Number of connection vias for each HS capacitor(8)(9)	2			Vias
11	Trace length from bypass capacitor connect to connection via(2)(9)		35	100	Mils
12	Number of connection vias for each DDR3 device power/ground ball(10)	1			Vias
13	Trace length from DDR3 device power/ground ball to connection via(2)(8)		35	60	Mils

(1) LxW, 10-mil units, that is, a 0402 is a 40x20-mil surface-mount capacitor.
(2) Closer/shorter is better.
(3) Measured from the nearest processor power/ground ball to the center of the capacitor package.
(4) Three of these capacitors should be located underneath the processor, between the cluster of DVDD_DDR[0] balls and ground balls, between the DDR interfaces on the package.
(5) See the Via Channel™ escape for the processor package.
(6) Measured from the DDR3 device power/ground ball to the center of the capacitor package.
(7) Per DDR3 device.
(8) An additional HS bypass capacitor can share the connection vias only if it is mounted on the opposite side of the board. No sharing of vias is permitted on the same side of the board.
(9) An HS bypass capacitor may share a via with a DDR device mounted on the same side of the PCB. A wide trace should be used for the connection and the length from the capacitor pad to the DDR device pad should be less than 150 mils.
(10) Up to a total of two pairs of DDR power/ground balls may share a via.

8.12.3.9.1 Return Current Bypass Capacitors

Use additional bypass capacitors if the return current reference plane changes due to DDR3 signals hopping from one signal layer to another. The bypass capacitor here provides a path for the return current to hop planes along with the signal. As many of these return current bypass capacitors should be used as possible. Since these are returns for signal current, the signal via size may be used for these capacitors.

8.12.3.10 Net Classes

Table 8-55 lists the clock net classes for the DDR3 interface. Table 8-56 lists the signal net classes, and associated clock net classes, for signals in the DDR3 interface. These net classes are used for the termination and routing rules that follow.

Table 8-55. Clock Net Class Definitions

CLOCK NET CLASS	PROCESSOR PIN NAMES
CK	DDR[0]_CLK/$\overline{\text{DDR[0]\_CLK}}$
DQS0	DDR[0]_DQS[0]/$\overline{\text{DDR[0]\_DQS[0]}}$
DQS1	DDR[0]_DQS[1]/$\overline{\text{DDR[0]\_DQS[1]}}$
DQS2(1)	DDR[0]_DQS[2]/$\overline{\text{DDR[0]\_DQS[2]}}$
DQS3(1)	DDR[0]_DQS[3]/$\overline{\text{DDR[0]\_DQS[3]}}$

(1) Only used on 32-bit wide DDR3 memory systems.

Table 8-56. Signal Net Class Definitions

CLOCK NET CLASS	ASSOCIATED CLOCK NET CLASS	PROCESSOR PIN NAMES
ADDR_CTRL	CK	$\overline{\text{DDR[0]\_BA[2:0]}}$, DDR[0]_A[15:0], $\overline{\text{DDR[0]\_CS[x]}}$, $\overline{\text{DDR[0]\_CAS}}$, $\overline{\text{DDR[0]\_RAS}}$, $\overline{\text{DDR[0]\_WE}}$, DDR[0]_CKE, DDR[0]_ODT[0]
DQ0	DQS0	DDR[0]_D[7:0], DDR[0]_DQM[0]
DQ1	DQS1	DDR[0]_D[15:8], DDR[0]_DQM[1]
DQ2(1)	DQS2	DDR[0]_D[23:16], DDR[0]_DQM[2]
DQ3(1)	DQS3	DDR[0]_D[31:24], DDR[0]_DQM[3]

(1) Only used on 32-bit wide DDR3 memory systems.

8.12.3.11 DDR3 Signal Termination

Signal terminators are required for the CK and ADDR_CTRL net classes. The data lines are terminated by ODT and, thus, the PCB traces should be unterminated. Detailed termination specifications are covered in the routing rules in the following sections.

8.12.3.12 VREFSSTL_DDR Routing

VREFSSTL_DDR (VREF) is used as a reference by the input buffers of the DDR3 memories as well as the processor. VREF is intended to be half the DDR3 power supply voltage and is typically generated with the DDR3 1.35-V/1.5-V and VTT power supply. It should be routed as a nominal 20-mil wide trace with 0.1 µF bypass capacitors near each device connection. Narrowing of VREF is allowed to accommodate routing congestion.

8.12.3.13 VTT

Like VREF, the nominal value of the VTT supply is half the DDR3 supply voltage. Unlike VREF, VTT is expected to source and sink current, specifically the termination current for the ADDR_CTRL net class Thevinen terminators. VTT is needed at the end of the address bus and it should be routed as a power sub-plane. VTT should be bypassed near the terminator resistors.

8.12.3.14 CK and ADDR_CTRL Topologies and Routing Definition

The CK and ADDR_CTRL net classes are routed similarly and are length matched to minimize skew between them. CK is a bit more complicated because it runs at a higher transition rate and is differential. The following subsections show the topology and routing for various DDR3 configurations for CK and ADDR_CTRL. The figures in the following subsections define the terms for the routing specification detailed in Table 8-57.

8.12.3.14.1 Four DDR3 Devices

Four DDR3 devices are supported on the DDR EMIF consisting of four x8 DDR3 devices arranged as one bank (CS). These four devices may be mounted on a single side of the PCB, or may be mirrored in two pairs to save board space at a cost of increased routing complexity and parts on the backside of the PCB.

8.12.3.14.1.1 CK and ADDR_CTRL Topologies, Four DDR3 Devices

Figure 8-49 shows the topology of the CK net classes and Figure 8-50 shows the topology for the corresponding ADDR_CTRL net classes.

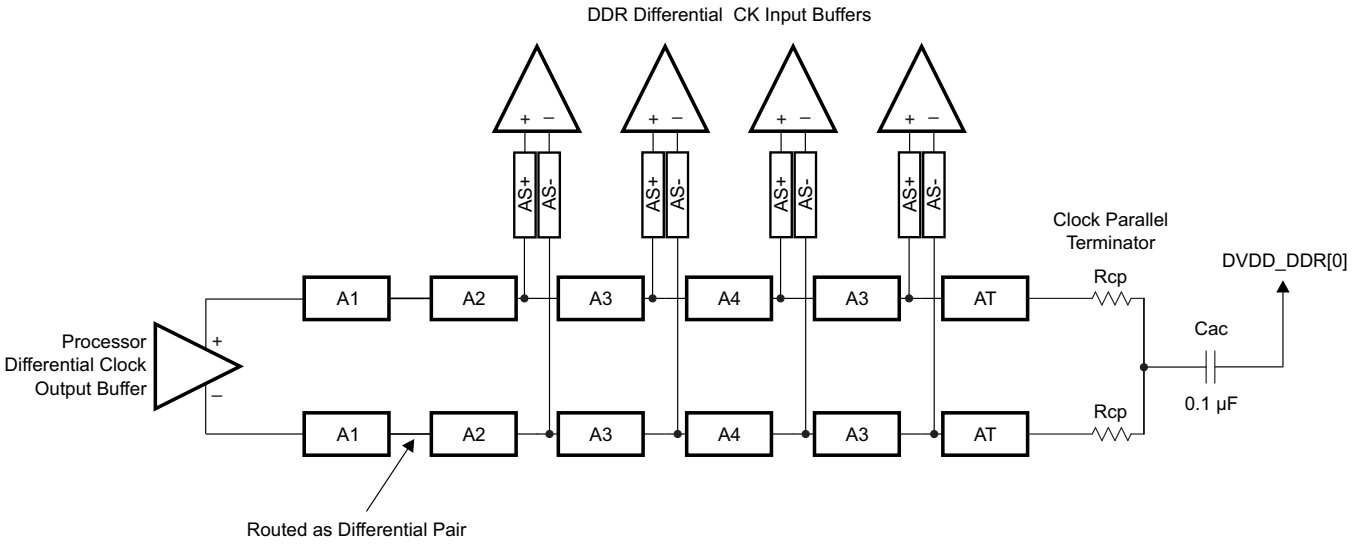


Figure 8-49. CK Topology for Four x8 DDR3 Devices

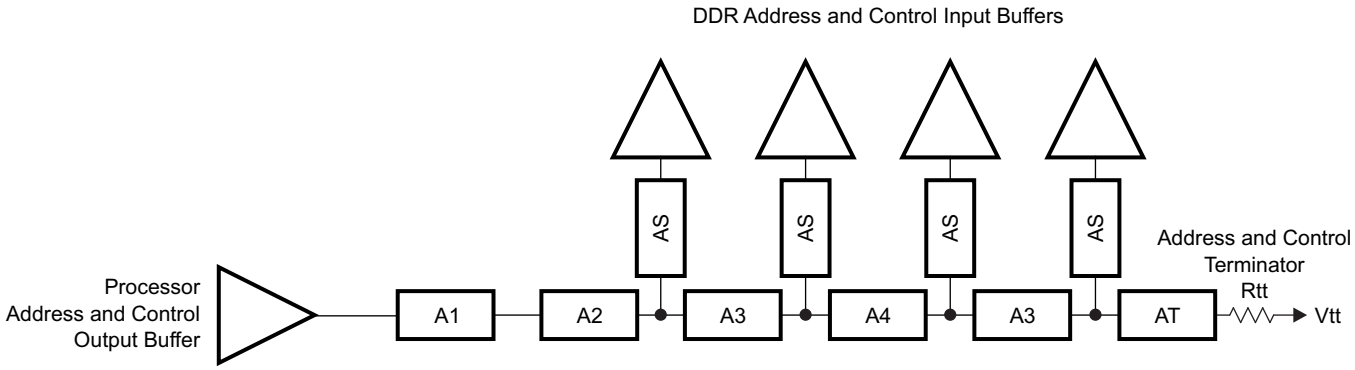


Figure 8-50. ADDR_CTRL Topology for Four x8 DDR3 Devices

8.12.3.14.1.2 CK and ADDR_CTRL Routing, Four DDR3 Devices

Figure 8-51 shows the CK routing for four DDR3 devices placed on the same side of the PCB. Figure 8-52 shows the corresponding ADDR_CTRL routing.

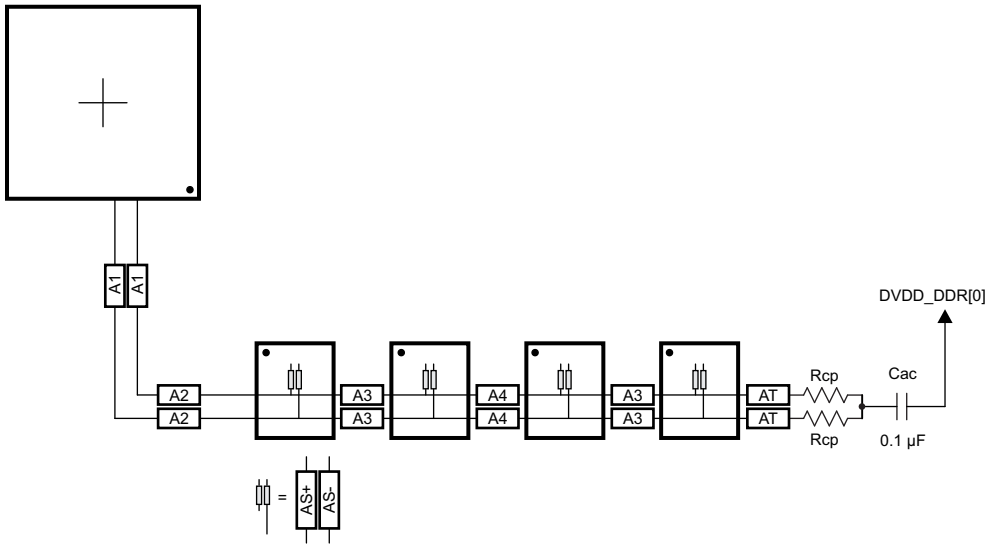


Figure 8-51. CK Routing for Four Single-Side DDR3 Devices

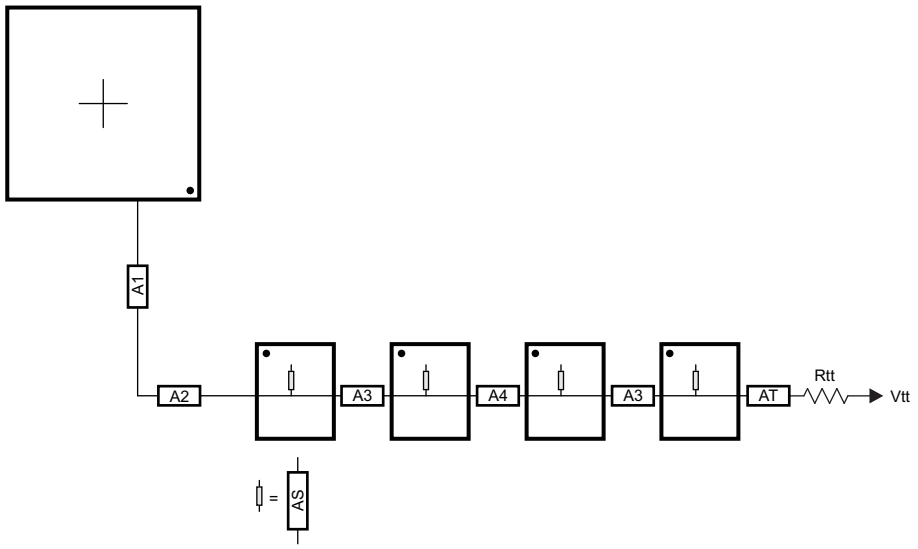


Figure 8-52. ADDR_CTRL Routing for Four Single-Side DDR3 Devices

To save PCB space, the four DDR3 memories may be mounted as two mirrored pairs at a cost of increased routing and assembly complexity. Figure 8-53 and Figure 8-54 show the routing for CK and ADDR_CTRL, respectively, for four DDR3 devices mirrored in a two-pair configuration.

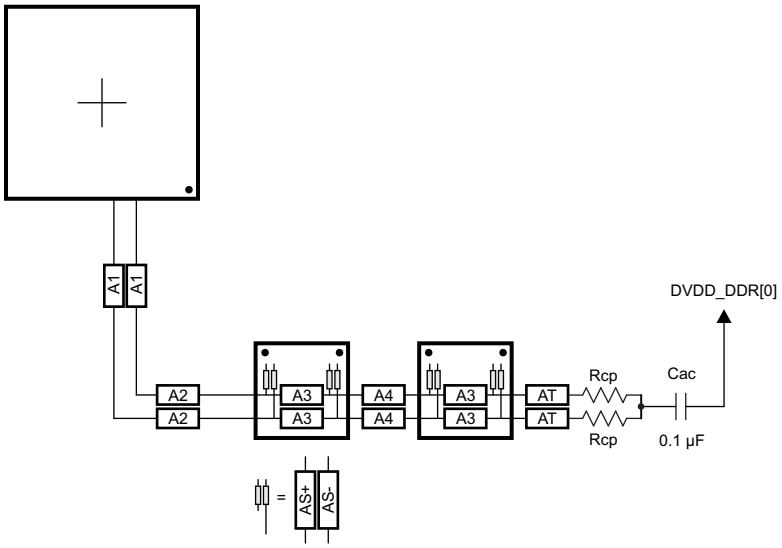


Figure 8-53. CK Routing for Four Mirrored DDR3 Devices

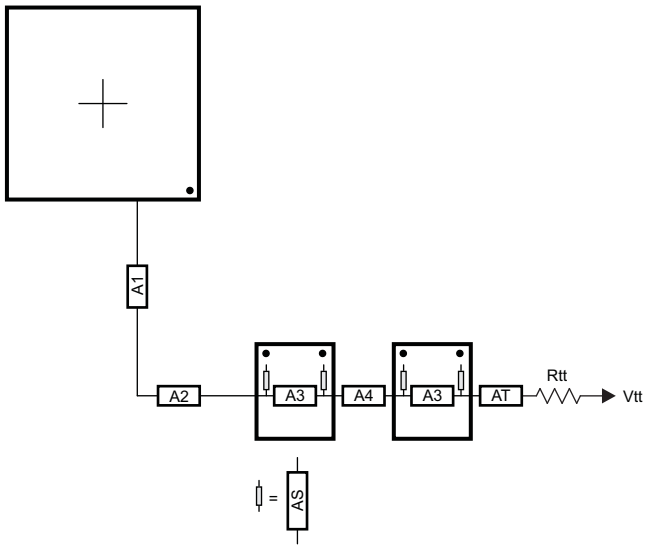


Figure 8-54. ADDR_CTRL Routing for Four Mirrored DDR3 Devices

8.12.3.14.2 Two DDR3 Devices

Two DDR3 devices are supported on the DDR EMIF consisting of two x8 DDR3 devices arranged as one bank (CS), 16 bits wide, or two x16 DDR3 devices arranged as one bank (CS), 32 bits wide. These two devices may be mounted on a single side of the PCB, or may be mirrored in a pair to save board space at a cost of increased routing complexity and parts on the backside of the PCB.

8.12.3.14.2.1 CK and ADDR_CTRL Topologies, Two DDR3 Devices

Figure 8-55 shows the topology of the CK net classes and Figure 8-56 shows the topology for the corresponding ADDR_CTRL net classes.

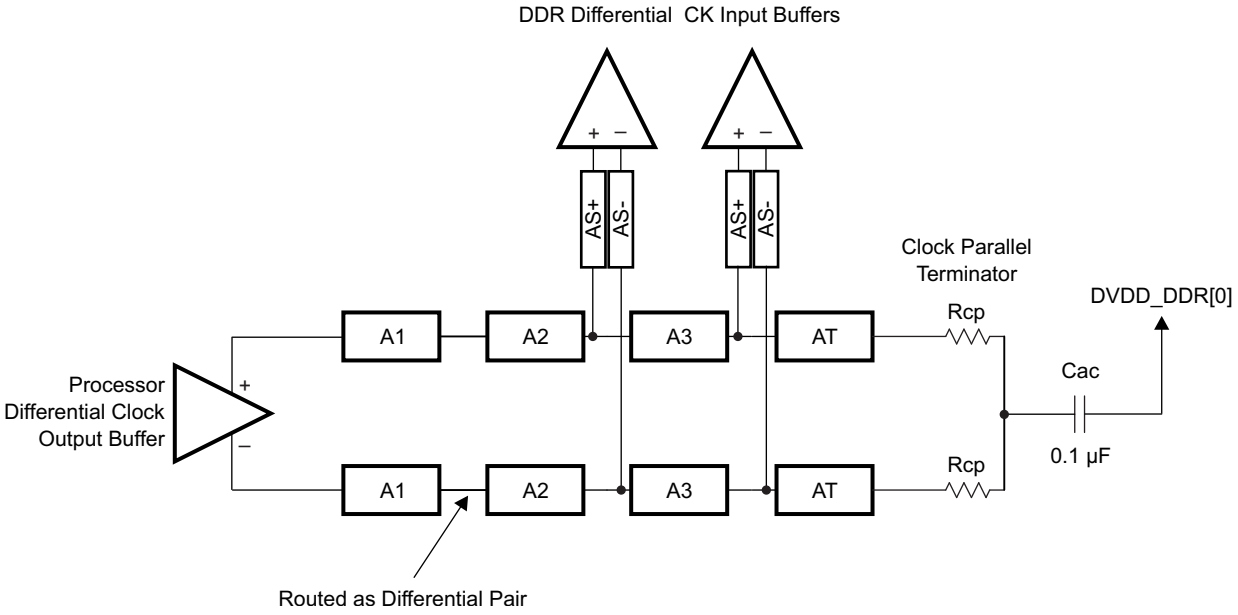


Figure 8-55. CK Topology for Two DDR3 Devices

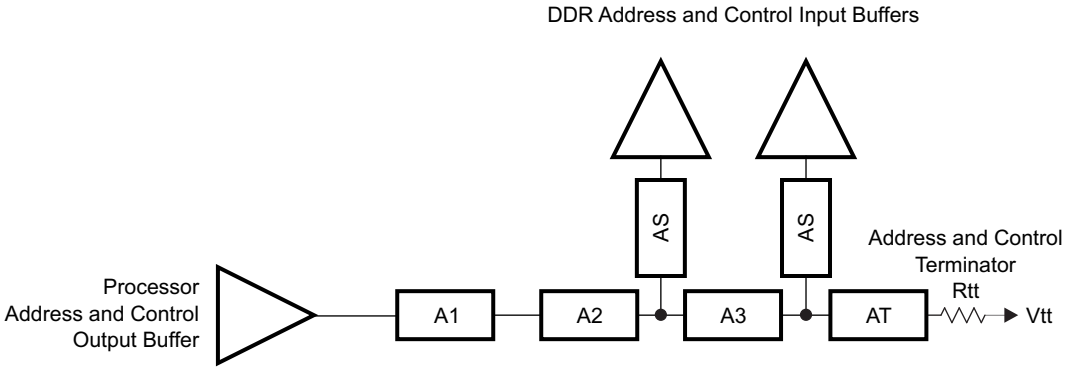


Figure 8-56. ADDR_CTRL Topology for Two DDR3 Devices

8.12.3.14.2.2 CK and ADDR_CTRL Routing, Two DDR3 Devices

Figure 8-57 shows the CK routing for two DDR3 devices placed on the same side of the PCB. Figure 8-58 shows the corresponding ADDR_CTRL routing.

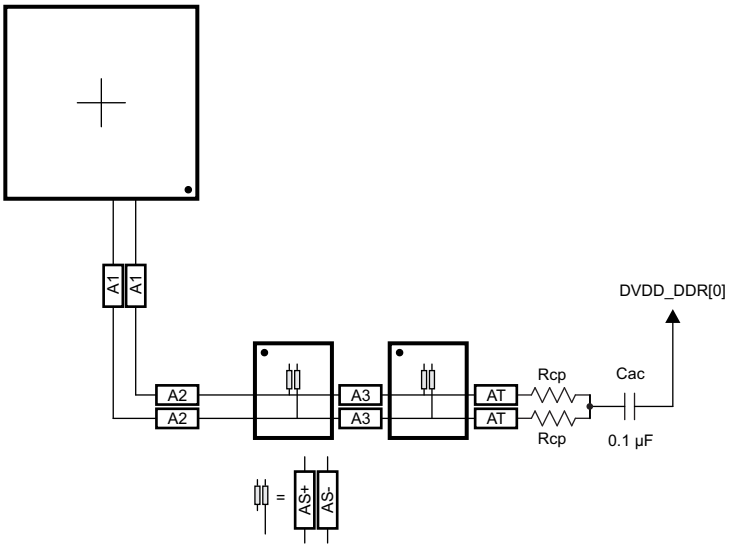


Figure 8-57. CK Routing for Two Single-Side DDR3 Devices

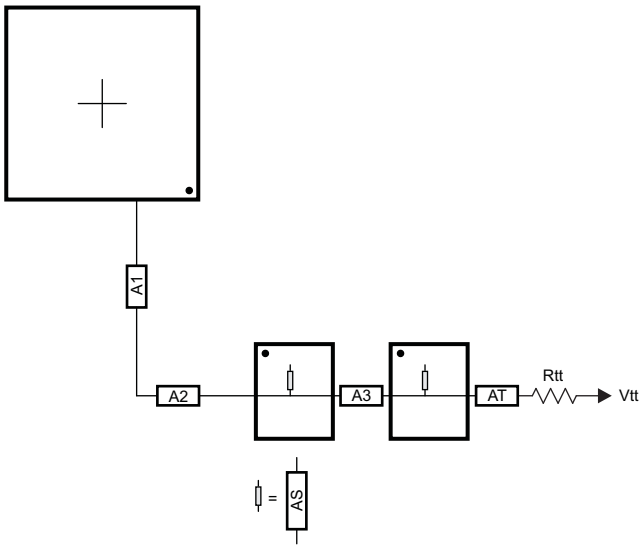


Figure 8-58. ADDR_CTRL Routing for Two Single-Side DDR3 Devices

To save PCB space, the two DDR3 memories may be mounted as a mirrored pair at a cost of increased routing and assembly complexity. Figure 8-59 and Figure 8-60 show the routing for CK and ADDR_CTRL, respectively, for two DDR3 devices mirrored in a single-pair configuration.

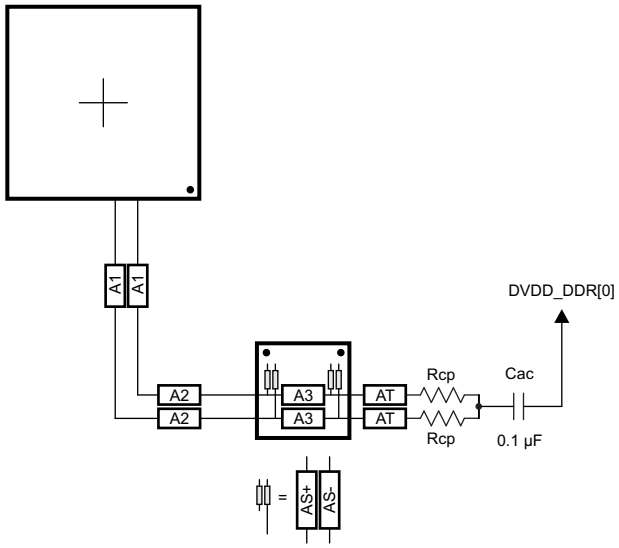


Figure 8-59. CK Routing for Two Mirrored DDR3 Devices

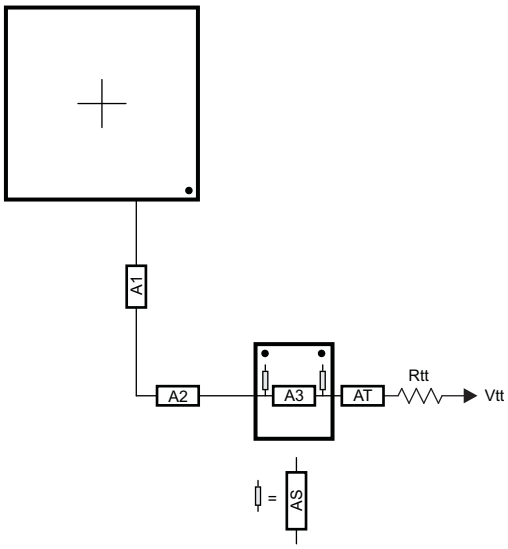


Figure 8-60. ADDR_CTRL Routing for Two Mirrored DDR3 Devices

8.12.3.14.3 One DDR3 Device

A single DDR3 device is supported on the DDR EMIF consisting of one x16 DDR3 device arranged as one bank (CS), 16 bits wide.

8.12.3.14.3.1 CK and ADDR_CTRL Topologies, One DDR3 Device

Figure 8-61 shows the topology of the CK net classes and Figure 8-62 shows the topology for the corresponding ADDR_CTRL net classes.

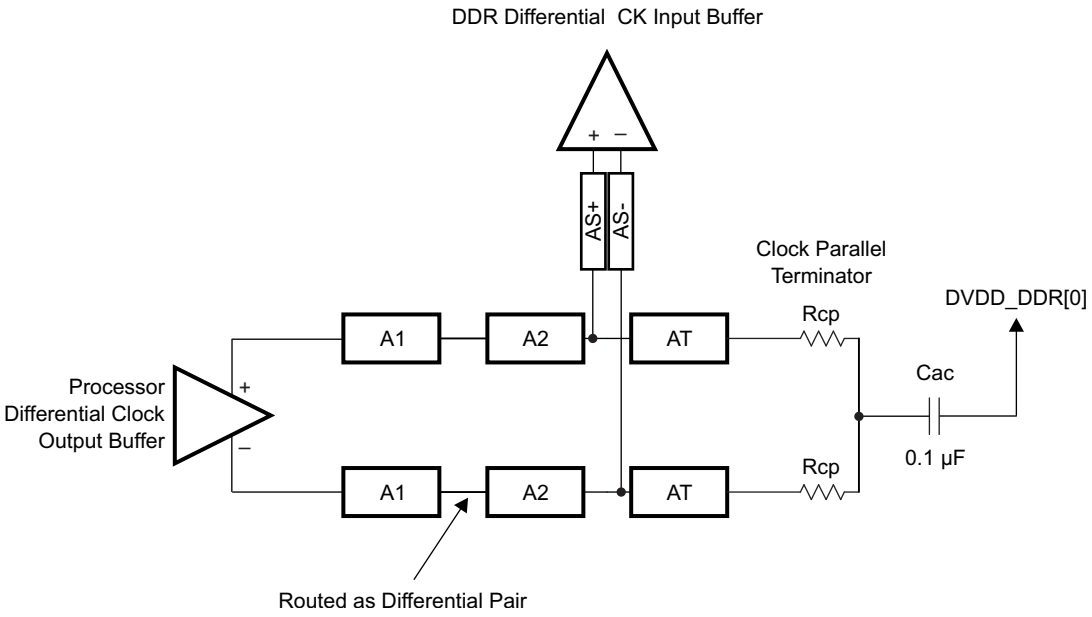


Figure 8-61. CK Topology for One DDR3 Device

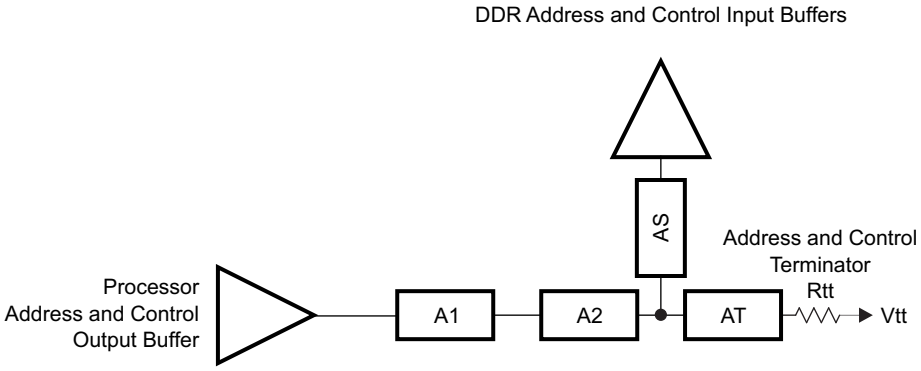


Figure 8-62. ADDR_CTRL Topology for One DDR3 Device

8.12.3.14.3.2 CK and ADDR/CTRL Routing, One DDR3 Device

Figure 8-63 shows the CK routing for one DDR3 device placed on the same side of the PCB. Figure 8-64 shows the corresponding ADDR_CTRL routing.

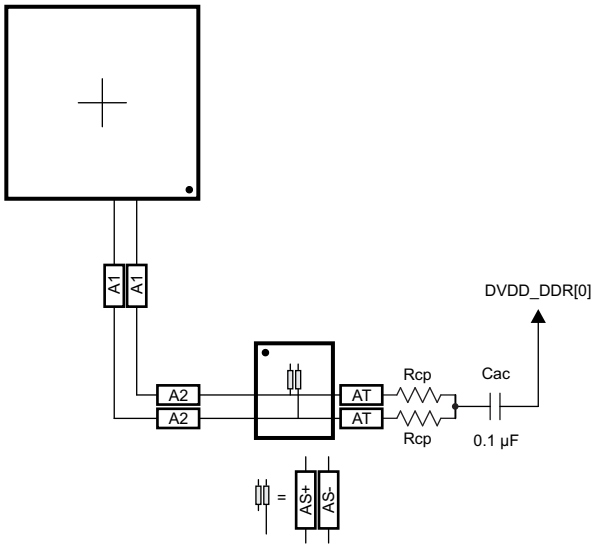


Figure 8-63. CK Routing for One DDR3 Device

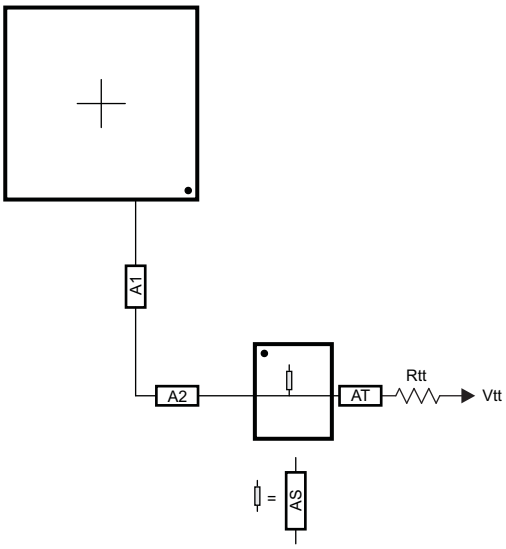


Figure 8-64. ADDR_CTRL Routing for One DDR3 Device

8.12.3.15 Data Topologies and Routing Definition

No matter the number of DDR3 devices used, the data line topology is always point to point, so its definition is simple.

8.12.3.15.1 DQS and DQ/DM Topologies, Any Number of Allowed DDR3 Devices

DQS lines are point-to-point differential, and DQ/DM lines are point-to-point singled ended. Figure 8-65 and Figure 8-66 show these topologies.

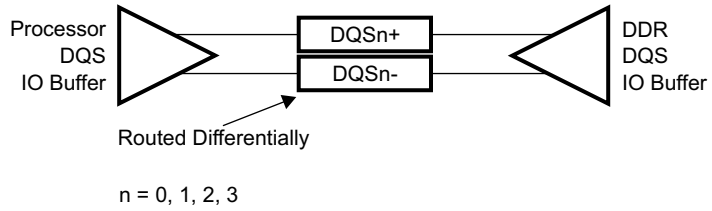


Figure 8-65. DQS Topology

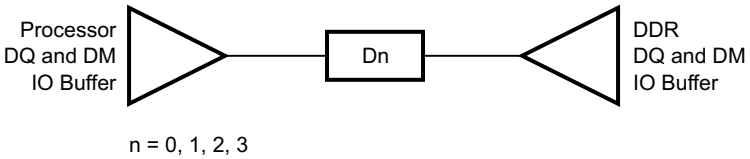


Figure 8-66. DQ/DM Topology

8.12.3.15.2 DQS and DQ/DM Routing, Any Number of Allowed DDR3 Devices

Figure 8-67 and Figure 8-68 show the DQS and DQ/DM routing.

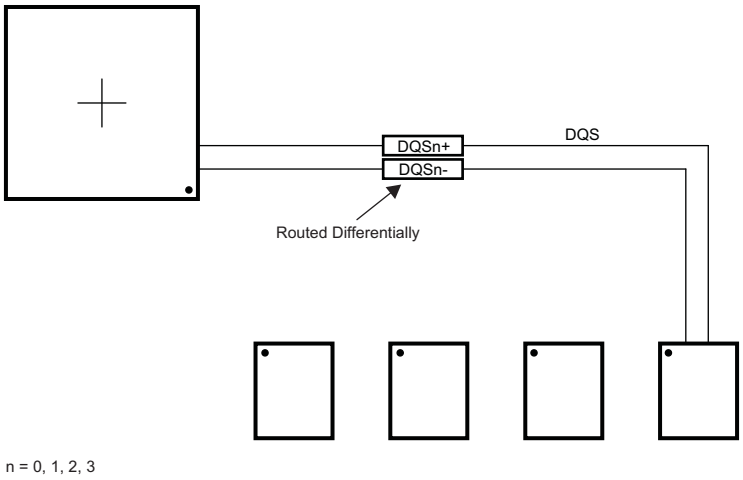


Figure 8-67. DQS Routing With Any Number of Allowed DDR3 Devices

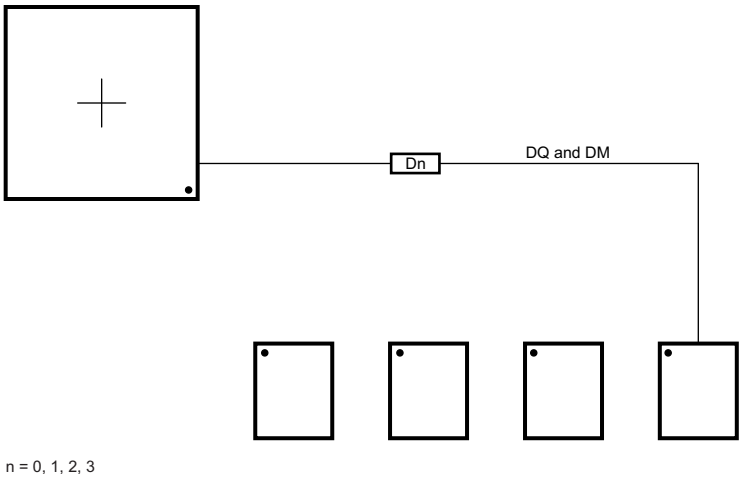


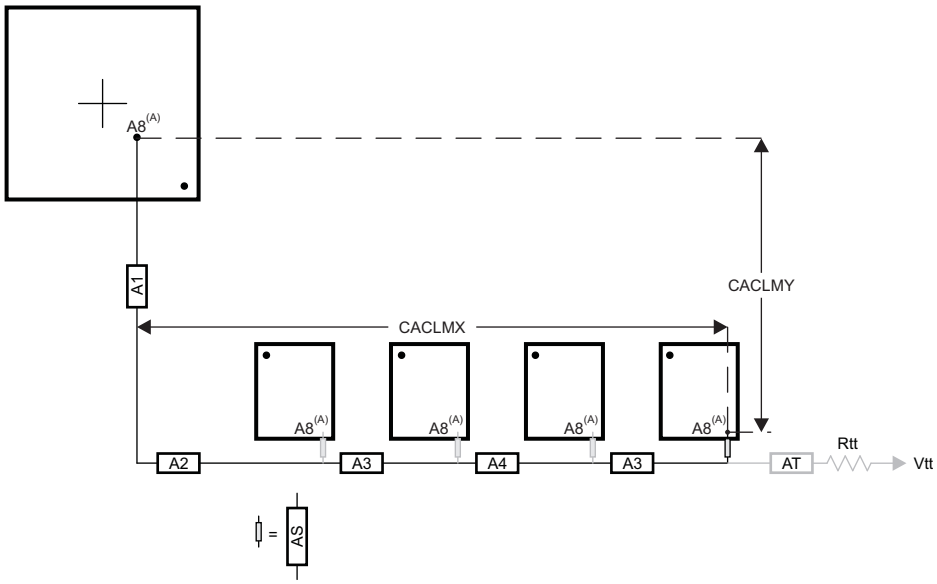
Figure 8-68. DQ/DM Routing With Any Number of Allowed DDR3 Devices

8.12.3.16 Routing Specification

8.12.3.16.1 CK and ADDR_CTRL Routing Specification

Skew within the CK and ADDR_CTRL net classes directly reduces setup and hold margin and, thus, this skew must be controlled. The only way to practically match lengths on a PCB is to lengthen the shorter traces up to the length of the longest net in the net class and its associated clock. A metric to establish this maximum length is Manhattan distance. The Manhattan distance between two points on a PCB is the length between the points when connecting them only with horizontal or vertical segments. A reasonable trace route length is to within a percentage of its Manhattan distance. CACLM is defined as Clock Address Control Longest Manhattan distance.

Given the clock and address pin locations on the processor and the DDR3 memories, the maximum possible Manhattan distance can be determined given the placement. Figure 8-69 and Figure 8-70 show this distance for four loads and two loads, respectively. It is from this distance that the specifications on the lengths of the transmission lines for the address bus are determined. CACLM is determined similarly for other address bus configurations; that is, it is based on the longest net of the CK/ADDR_CTRL net class. For CK and ADDR_CTRL routing, these specifications are contained in Table 8-57.

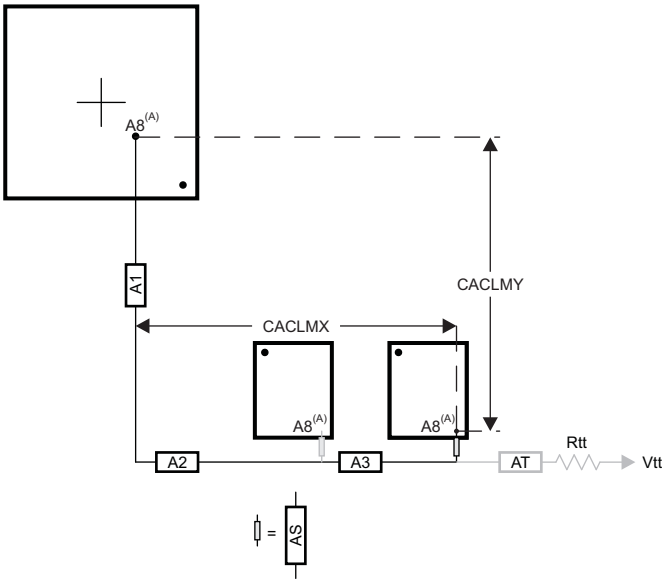


A. It is very likely that the longest CK/ADDR_CTRL Manhattan distance will be for Address Input 8 (A8) on the DDR3 memories. CACLM is based on the longest Manhattan distance due to the device placement. Verify the net class that satisfies this criteria and use as the baseline for CK/ADDR_CTRL skew matching and length control.

The length of shorter CK/ADDR_CTRL stubs as well as the length of the terminator stub are not included in this length calculation. Non-included lengths are grayed out in the figure.

Assuming A8 is the longest, CALM = CACLMY + CACLMX + 300 mils.
The extra 300 mils allows for routing down lower than the DDR3 memories and returning up to reach A8.

Figure 8-69. CACLM for Four Address Loads on One Side of PCB



A. It is very likely that the longest CK/ADDR_CTRL Manhattan distance will be for Address Input 8 (A8) on the DDR3 memories. CACLM is based on the longest Manhattan distance due to the device placement. Verify the net class that satisfies this criteria and use as the baseline for CK/ADDR_CTRL skew matching and length control.

The length of shorter CK/ADDR_CTRL stubs as well as the length of the terminator stub are not included in this length calculation. Non-included lengths are grayed out in the figure.

Assuming A8 is the longest, CALM = CACLMY + CACLMX + 300 mils.
The extra 300 mils allows for routing down lower than the DDR3 memories and returning up to reach A8.

Figure 8-70. CACLM for Two Address Loads on One Side of PCB

Table 8-57. CK and ADDR_CTRL Routing Specification(1)(2)

NO.	PARAMETER	MIN	TYP	MAX	UNIT
1	A1+A2 length			2500	mils
2	A1+A2 skew			25	mils
3	A3 length			660	mils
4	A3 skew(3)			25	mils
5	A3 skew(4)			125	mils
6	A4 length			660	mils
7	A4 skew			25	mils
8	AS length			100	mils
9	AS skew			100	mils
10	AS+/AS- length			70	mils
11	AS+/AS- skew			5	mils
12	AT length(5)		500		mils
13	AT skew(6)		100		mils
14	AT skew(7)			5	mils
15	CK/ADDR_CTRL nominal trace length(8)	CACLM-50	CACLM	CACLM+50	mils

(1) The use of vias should be minimized.
(2) Additional bypass capacitors are required when using the DVDD_DDR[0] plane as the reference plane to allow the return current to jump between the DVDD_DDR[0] plane and the ground plane when the net class switches layers at a via.
(3) Non-mirrored configuration (all DDR3 memories on same side of PCB).
(4) Mirrored configuration (one DDR3 device on top of the board and one DDR3 device on the bottom).
(5) While this length can be increased for convenience, its length should be minimized.
(6) ADDR_CTRL net class only (not CK net class). Minimizing this skew is recommended, but not required.
(7) CK net class only.
(8) CACLM is the longest Manhattan distance of the CK and ADDR_CTRL net classes + 300 mils. For definition, see Section 8.12.3.16.1, Figure 8-69, and Figure 8-70.

Table 8-57. CK and ADDR_CTRL Routing Specification[1][2] (continued)

NO.	PARAMETER	MIN	TYP	MAX	UNIT
16	Center-to-center CK to other DDR3 trace spacing[9]	4w			
17	Center-to-center ADDR_CTRL to other DDR3 trace spacing[9][10]	4w			
18	Center-to-center ADDR_CTRL to other ADDR_CTRL trace spacing[9]	3w			
19	CK center-to-center spacing[11]				
20	CK spacing to other net[9]	4w			
21	Rcp[12]	Zo-1	Zo	Zo+	Ω
22	Rtt[12][13]	Zo-5	Zo	Zo+5	Ω

(9) Center-to-center spacing is allowed to fall to minimum (2w) for up to 1250 mils of routed length.
(10) The ADDR_CTRL net class of the other DDR EMIF is considered *other DDR3 trace spacing*.
(11) CK spacing set to ensure proper differential impedance.
(12) Source termination (series resistor at driver) is specifically not allowed.
(13) Termination values should be uniform across the net class.

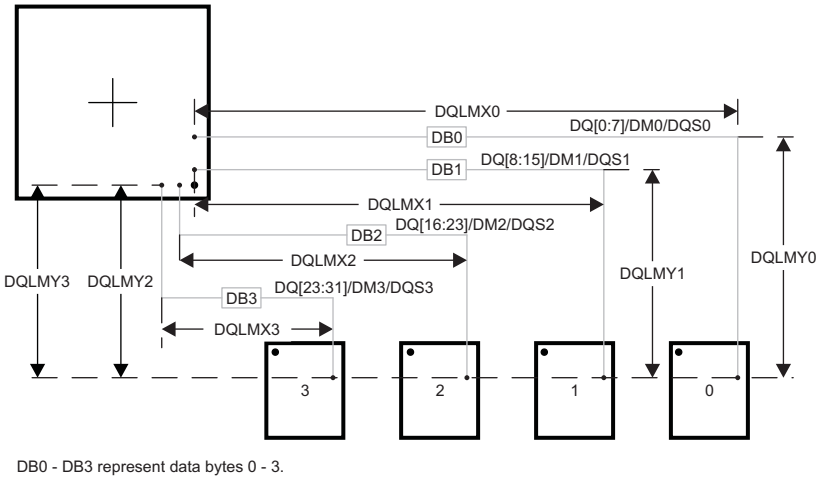
8.12.3.16.2 DQS and DQ Routing Specification

Skew within the DQS and DQ/DM net classes directly reduces setup and hold margin and thus this skew must be controlled. The only way to practically match lengths on a PCB is to lengthen the shorter traces up to the length of the longest net in the net class and its associated clock. As with CK and ADDR_CTRL, a reasonable trace route length is to within a percentage of its Manhattan distance. DQLMn is defined as DQ Longest Manhattan distance n, where n is the byte number. For a 32-bit interface, there are four DQLMs, DQLM0-DQLM3. Likewise, for a 16-bit interface, there are two DQLMs, DQLM0-DQLM1.

NOTE

It is not required, nor is it recommended, to match the lengths across all bytes. Length matching is only required within each byte.

Given the DQS and DQ/DM pin locations on the processor and the DDR3 memories, the maximum possible Manhattan distance can be determined given the placement. Figure 8-71 shows this distance for four loads. It is from this distance that the specifications on the lengths of the transmission lines for the data bus are determined. For DQS and DQ/DM routing, these specifications are contained in Table 8-58.



DB0 - DB3 represent data bytes 0 - 3.

There are four DQLMs, one for each byte (32-bit interface). Each DQLM is the longest Manhattan distance of the byte; therefore:
DQLM0 = DQLMX0 + DQLMY0
DQLM1 = DQLMX1 + DQLMY1
DQLM2 = DQLMX2 + DQLMY2
DQLM3 = DQLMX3 + DQLMY3

Figure 8-71. DQLM for Any Number of Allowed DDR3 Devices

Table 8-58. Data Routing Specification(1)

NO.	PARAMETER	MIN	TYP	MAX	UNIT
1	DB0 nominal length(2)(3)			DQLM0	mils
2	DB1 nominal length(2)(4)			DQLM1	mils
3	DB2 nominal length(2)(5)			DQLM2	mils
4	DB3 nominal length(2)(6)			DQLM3	mils
5	DBn skew(7)			25	mils
6	DQSn+ to DQSn- skew			5	mils
7	DQSn to DBn skew(7)(8)			25	mils
8	Center-to-center DBn to other DDR3 trace spacing(9)(10)	4w			
9	Center-to-center DBn to other DBn trace spacing(9)(11)	3w			
10	DQSn center-to-center spacing(12)				
11	DQSn center-to-center spacing to other net(9)	4w			

(1) External termination disallowed. Data termination should use built-in ODT functionality.
(2) DQLMn is the longest Manhattan distance of a byte. r definition, see Section 8.12.3.16.2 and Figure 8-71.
(3) DQLM0 is the longest Manhattan length for the net classes of Byte 0.
(4) DQLM1 is the longest Manhattan length for the net classes of Byte 1.
(5) DQLM2 is the longest Manhattan length for the net classes of Byte 2.
(6) DQLM3 is the longest Manhattan length for the net classes of Byte 3.
(7) Length matching is only done within a byte. Length matching across bytes is neither required nor recommended.
(8) Each DQS pair is length matched to its associated byte.
(9) Center-to-center spacing is allowed to fall to minimum (2w) for up to 1250 mils of routed length.
(10) Other DDR3 trace spacing means other DDR3 net classes not within the byte.
(11) This applies to spacing within the net classes of a byte.
(12) DQS pair spacing is set to ensure proper differential impedance.

8.13 Multichannel Audio Serial Port (McASP)

The multichannel audio serial port (McASP) functions as a general-purpose audio serial port optimized for the needs of multichannel audio applications. The McASP is useful for time-division multiplexed (TDM) stream, Inter-Integrated Sound (I2S) protocols, and inter-component digital audio interface transmission (DIT).

8.13.1 McASP Device-Specific Information

The device includes two multichannel audio serial port (McASP) interface peripherals (McASP0 and McASP1). The McASP module consists of a transmit and receive section. These sections can operate completely independently with different data formats, separate master clocks, bit clocks, and frame syncs or, alternatively, the transmit and receive sections may be synchronized. The McASP module also includes shift registers that may be configured to operate as either transmit data or receive data.

The transmit section of the McASP can transmit data in either a time-division-multiplexed (TDM) synchronous serial format or in a digital audio interface (DIT) format where the bit stream is encoded for S/PDIF, AES-3, IEC-60958, CP-430 transmission. The receive section of the McASP peripheral supports the TDM synchronous serial format.

The McASP module can support one transmit data format (either a TDM format or DIT format) and one receive format at a time. All transmit shift registers use the same format and all receive shift registers use the same format; however, the transmit and receive formats need not be the same. Both the transmit and receive sections of the McASP also support burst mode, which is useful for non-audio data (for example, passing control information between two devices).

The McASP peripheral has additional capability for flexible clock generation and error detection/handling, as well as error management.

The device McASP0 module has up to 6 serial data pins, while McASP1 has 2 serial data pins. The McASP FIFO size is 256 bytes and two DMA and two interrupt requests are supported. Buffers are used transparently to better manage DMA, which can be leveraged to manage data flow more efficiently.

For more detailed information on and the functionality of the McASP peripheral, see the *Multichannel Audio Serial Port (McASP)* chapter in the device-specific Technical Reference Manual.

8.13.2 McASP0 and McASP1 Peripheral Registers Descriptions

The McASP0 and McASP1 peripheral registers are described in the device-specific Technical Reference Manual. Each register is documented as an offset from a base address for the peripheral. The base addresses for all of the peripherals are in the device memory map (see Section 2.10).

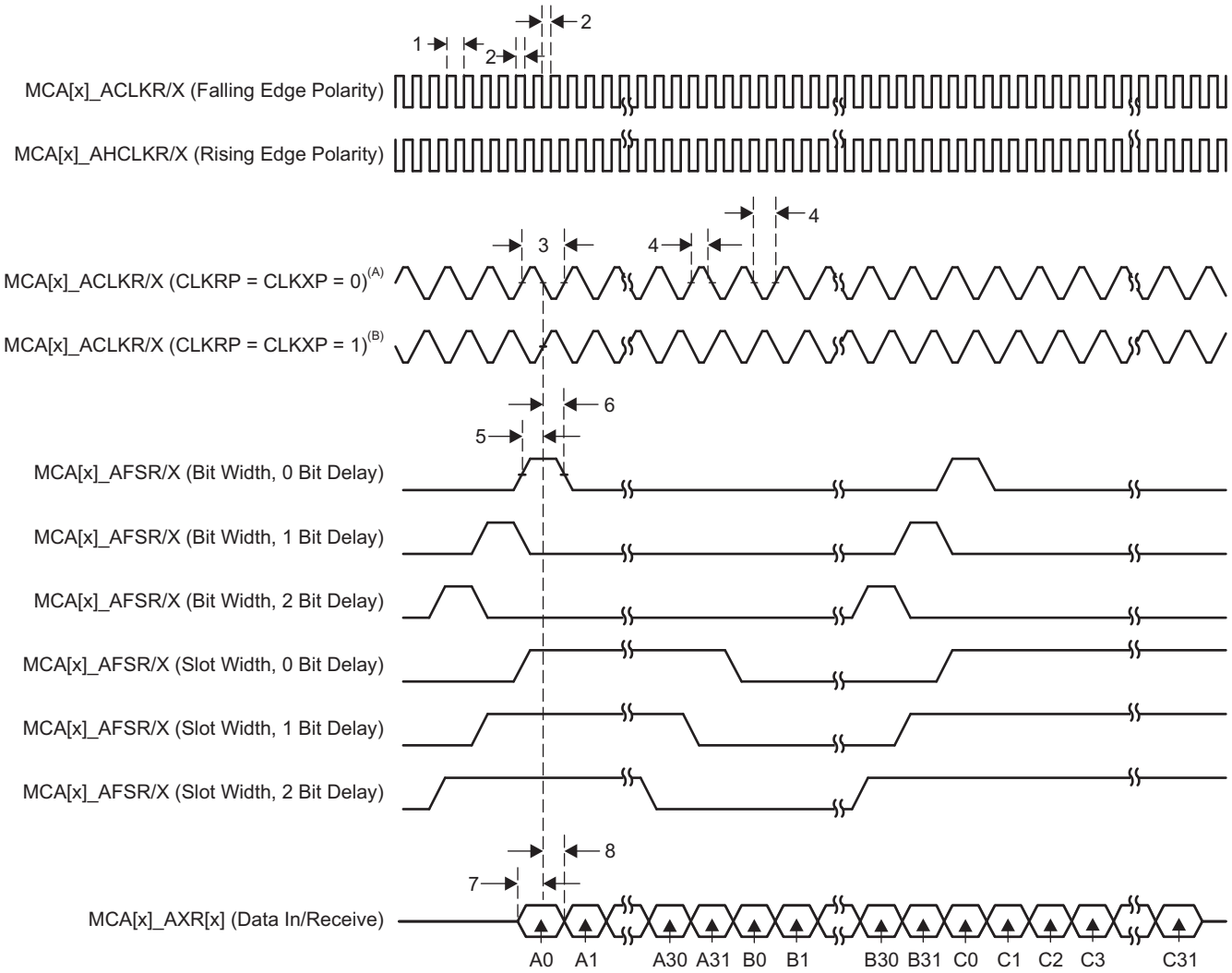
8.13.3 McASP (McASP[1:0]) Electrical Data/Timing

Table 8-59. Timing Requirements for McASP(1)

(see Figure 8-72)

NO.				OPP100/OPP120/ Turbo/Nitro		UNIT
				MIN	MAX	
1	$t_{c(AHCLKRX)}$	Cycle time, MCA[x]_AHCLKR/X		20		ns
2	$t_{w(AHCLKRX)}$	Pulse duration, MCA[x]_AHCLKR/X high or low		0.5P - 2.5(2)		ns
3	$t_{c(ACLKRX)}$	Cycle time, MCA[x]_ACLKR/X		20		ns
4	$t_{w(ACLKRX)}$	Pulse duration, MCA[x]_ACLKR/X high or low		0.5R - 2.5(3)		ns
5	$t_{su(AFSRX-ACLKRX)}$	Setup time, MCA[x]_AFSR/X input valid before MCA[X]_ACLKR/X	ACLKR/X int	10.5		ns
			ACLKR/X ext in	4		
			ACLKR/X ext out	4		
6	$t_{h(ACLKRX-AFSRX)}$	Hold time, MCA[x]_AFSR/X input valid after MCA[X]_ACLKR/X	ACLKR/X int	-1		ns
			ACLKR/X ext in	1		
			ACLKR/X ext out	1		
7	$t_{su(AXR-ACLKRX)}$	Setup time, MCA[x]_AXR input valid before MCA[X]_ACLKR/X	ACLKR/X int	10.5		ns
			ACLKR/X ext in	4		
			ACLKR/X ext out	4		
8	$t_{h(ACLKRX-AXR)}$	Hold time, MCA[x]_AXR input valid after MCA[X]_ACLKR/X	ACLKR/X int	-1		ns
			ACLKR/X ext in	1		
			ACLKR/X ext out	1		

(1) ACLKR internal: ACLKRCTL.CLKRM=1, PDIR.ACLKR = 1
ACLKR external input: ACLKRCTL.CLKRM=0, PDIR.ACLKR=0
ACLKR external output: ACLKRCTL.CLKRM=0, PDIR.ACLKR=1
ACLKX internal: ACLKXCTL.CLKXM=1, PDIR.ACLKX = 1
ACLKX external input: ACLKXCTL.CLKXM=0, PDIR.ACLKX=0
ACLKX external output: ACLKXCTL.CLKXM=0, PDIR.ACLKX=1
(2) P = MCA[x]_AHCLKR/X period in nano seconds (ns).
(3) R = MCA[x]_ACLKR/X period in ns.



A. For CLKRP = CLKXP = 0, the McASP transmitter is configured for rising edge (to shift data out) and the McASP receiver is configured for falling edge (to shift data in).

B. For CLKRP = CLKXP = 1, the McASP transmitter is configured for falling edge (to shift data out) and the McASP receiver is configured for rising edge (to shift data in).

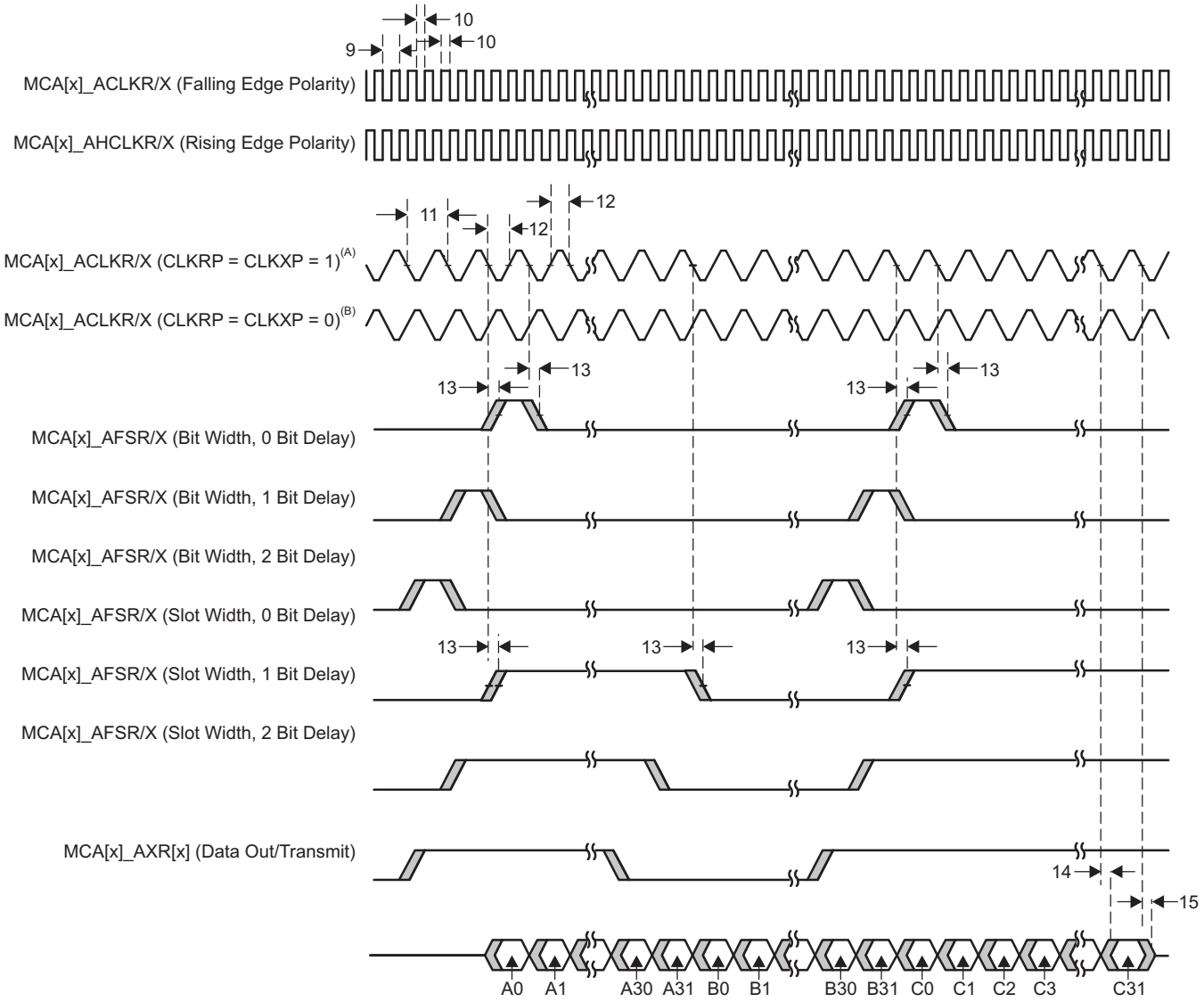
Figure 8-72. McASP Input Timing

Table 8-60. Switching Characteristics Over Recommended Operating Conditions for McASP[1]

(see Figure 8-73)

NO.	PARAMETER			OPP100/OPP120/ Turbo/Nitro		UNIT
				MIN	MAX	
9	$t_{c(AHCLKRX)}$	Cycle time, MCA[X]_AHCLKR/X		20[2]		ns
10	$t_{w(AHCLKRX)}$	Pulse duration, MCA[X]_AHCLKR/X high or low		0.5P - 2.5[3]		ns
11	$t_{c(ACLKRX)}$	Cycle time, MCA[X]_ACLKR/X		20		ns
12	$t_{w(ACLKRX)}$	Pulse duration, MCA[X]_ACLKR/X high or low		0.5P - 2.5[3]		ns
13	$t_{d(ACLKRX-AFSRX)}$	Delay time, MCA[X]_ACLKR/X transmit edge to MCA[X]_AFSR/X output valid	ACLKR/X int	-2	5	ns
			ACLKR/X ext in	1	11.5	
		Delay time, MCA[X]_ACLKR/X transmit edge to MCA[X]_AFSR/X output valid with Pad Loopback	ACLKR/X ext out	1	11.5	
14	$t_{d(ACLKX-AXR)}$	Delay time, MCA[X]_ACLKX transmit edge to MCA[X]_AXR output valid	ACLKX int	-2	5	ns
			ACLKX ext in	1	11.5	
		Delay time, MCA[X]_ACLKX transmit edge to MCA[X]_AXR output valid with Pad Loopback	ACLKX ext out	1	11.5	
15	$t_{dis(ACLKX-AXR)}$	Disable time, MCA[X]_ACLKX transmit edge to MCA[X]_AXR output high impedance	ACLKX int	-2	5	ns
			ACLKX ext in	1	11.5	
		Disable time, MCA[X]_ACLKX transmit edge to MCA[X]_AXR output high impedance with Pad Loopback	ACLKX ext out	1	11.5	

(1) ACLKR internal: ACLKRCTL.CLKRM=1, PDIR.ACLKR = 1
ACLKR external input: ACLKRCTL.CLKRM=0, PDIR.ACLKR=0
ACLKR external output: ACLKRCTL.CLKRM=0, PDIR.ACLKR=1
ACLKX internal: ACLKXCTL.CLKXM=1, PDIR.ACLKX = 1
ACLKX external input: ACLKXCTL.CLKXM=0, PDIR.ACLKX=0
ACLKX external output: ACLKXCTL.CLKXM=0, PDIR.ACLKX=1
(2) 50 MHz
(3) P = AHCLKR/X period.



A. For CLKRP = CLKXP = 1, the McASP transmitter is configured for falling edge (to shift data out) and the McASP receiver is configured for rising edge (to shift data in).

B. For CLKRP = CLKXP = 0, the McASP transmitter is configured for rising edge (to shift data out) and the McASP receiver is configured for falling edge (to shift data in).

Figure 8-73. McASP Output Timing

8.14 MultiMedia Card/Secure Digital/Secure Digital Input Output (MMC/SD/SDIO)

The device includes 3 MMC/SD/SDIO Controllers which are compliant with MMC V4.3, Secure Digital Part 1 Physical Layer Specification V2.00 and Secure Digital Input Output (SDIO) V2.00 specifications.

The device MMC/SD/SDIO Controller has the following features:

- MultiMedia card (MMC)
- Secure Digital (SD) memory card
- MMC/SD protocol support
- SDIO protocol support
- Programmable clock frequency
- 1024 byte read/write FIFO to lower system overhead
- Slave EDMA transfer capability
- SD High capacity support
- SDXC card support
  - Supports only SDHC clock rates
  - Booting from SDXC cards is not supported

8.14.1 MMC/SD/SDIO Peripheral Register Descriptions

The MMC/SD/SDIO peripheral registers are described in the device-specific Technical Reference Manual. Each register is documented as an offset from a base address for the peripheral. The base addresses for all of the peripherals are in the device memory map (see Section 2.10).

8.14.2 MMC/SD/SDIO Electrical Data/Timing

Table 8-61. Timing Requirements for MMC/SD/SDIO

(see Figure 8-75, Figure 8-77)

NO.			OPP100/OPP120/ Turbo/Nitro ALL MODES		UNIT
			MIN	MAX	
1	$t_{su(CMDV-CLKH)}$	Setup time, SD_CMD valid before SD_CLK rising clock edge	4.1		ns
2	$t_{h(CLKH-CMDV)}$	Hold time, SD_CMD valid after SD_CLK rising clock edge	1.9		ns
3	$t_{su(DATV-CLKH)}$	Setup time, SD_DATx valid before SD_CLK rising clock edge	4.1		ns
4	$t_{h(CLKH-DATV)}$	Hold time, SD_DATx valid after SD_CLK rising clock edge	1.9		ns

Table 8-62. Switching Characteristics Over Recommended Operating Conditions for MMC/SD/SDIO

(see Figure 8-74 through Figure 8-77)

NO.	PARAMETER		OPP100/OPP120/ Turbo/Nitro MODES				UNIT
			3.3 V STD 1.8 V SDR12		3.3 V HS 1.8 V SDR25		
			MIN	MAX	MIN	MAX	
7	$f_{op(CLK)}$	Operating frequency, SD_CLK		24		48	MHz
	$t_{c(CLK)}$	Operating period: SD_CLK	41.7		20.8		ns
8	$f_{op(CLKID)}$	Identification mode frequency, SD_CLK		400		400	kHz
	$t_{c(CLKID)}$	Identification mode period: SD_CLK	2500.0		2500.0		ns
9	$t_{w(CLKL)}$	Pulse duration, SD_CLK low	0.5*P(1)		0.5*P(1)		ns
10	$t_{w(CLKH)}$	Pulse duration, SD_CLK high	0.5*P(1)		0.5*P(1)		ns

(1) P = SD_CLK period.

Table 8-62. Switching Characteristics Over Recommended Operating Conditions for MMC/SD/SDIO (continued)

(see Figure 8-74 through Figure 8-77)

NO.	PARAMETER		OPP100/OPP120/ Turbo/Nitro MODES				UNIT
			3.3 V STD 1.8 V SDR12		3.3 V HS 1.8 V SDR25		
			MIN	MAX	MIN	MAX	
11	$t_{r(CLK)}$	Rise time, All Signals (10% to 90%)		2.2		2.2	ns
12	$t_{f(CLK)}$	Fall time, All Signals (10% to 90%)		2.2		2.2	ns
13	$t_{d(CLKL-CMD)}$	Delay time, SD_CLK rising clock edge to SD_CMD transition	-4	4	2.3	14	ns
14	$t_{d(CLKL-DAT)}$	Delay time, SD_CLK rising clock edge to SD_DATx transition	-4	4	2.3	14	ns

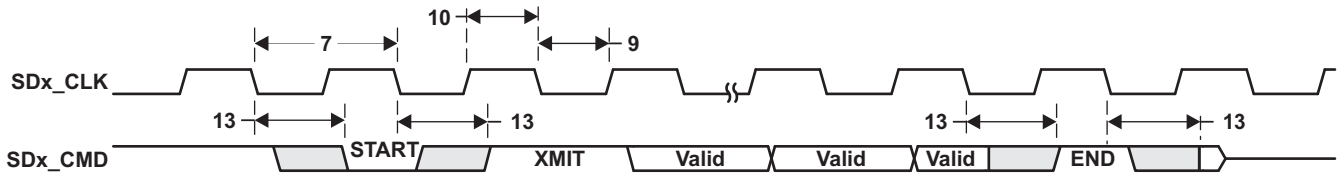


Figure 8-74. MMC/SD/SDIO Host Command Timing

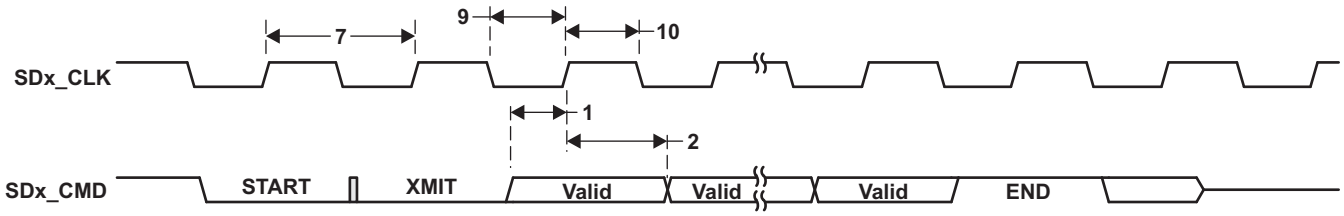


Figure 8-75. MMC/SD/SDIO Card Response Timing

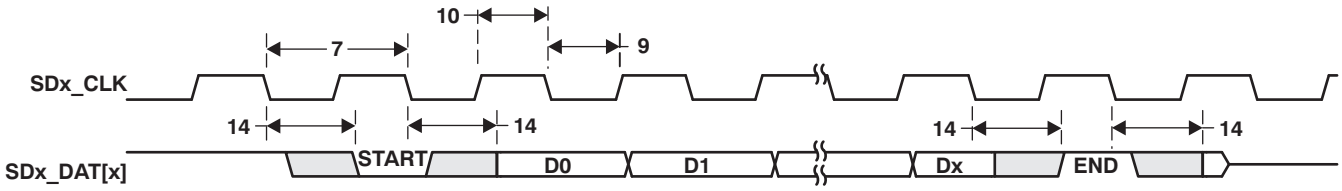


Figure 8-76. MMC/SD/SDIO Host Write Timing

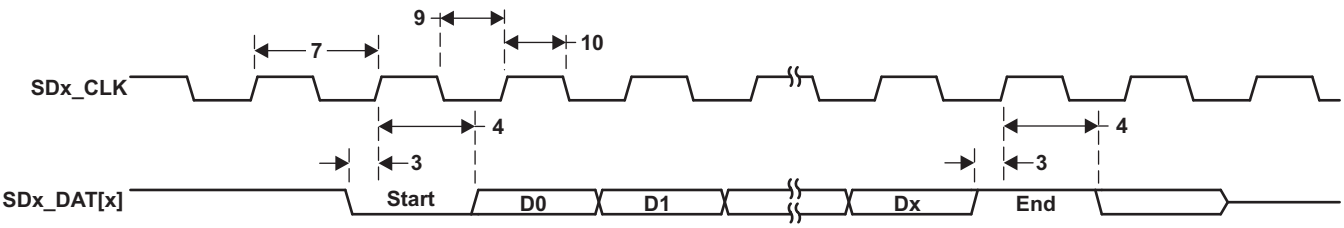


Figure 8-77. MMC/SD/SDIO Host Read and Card CRC Status Timing

8.15 Serial ATA Controller (SATA)

The Serial ATA (SATA) peripheral provides a direct interface to one hard disk drive (SATA) or multiple hard disk drives using a Port Multiplier and supports the following features:

- Serial ATA 1.5 Gbps and 3 Gbps speeds
- Integrated PHYs
- Integrated Rx and Tx data buffers
- Supports all SATA power management features
- Hardware-assisted native command queuing (NCQ) for up to 32 entries
- Supports port multiplier with command-based switching
- Activity LED support.

8.15.1 SATA Peripheral Register Descriptions

The SATA peripheral registers are described in the device-specific Technical Reference Manual. Each register is documented as an offset from a base address for the peripheral. The base addresses for all of the peripherals are in the device memory map (see Section 2.10).

8.15.2 SATA Interface Design Guidelines

This section provides PCB design and layout guidelines for the SATA interface. The design rules constrain PCB trace length, PCB trace skew, signal integrity, cross-talk, and signal timing. Simulation and system design work has been done to ensure the SATA interface requirements are met.

A standard 100-MHz differential clock source must be used for SATA operation (for details, see Section 7.4.2, *SERDES_CLKN/P Input Clock*).

8.15.2.1 SATA Interface Schematic

Figure 8-78 shows the data portion of the SATA interface schematic.

The specific pin numbers can be obtained from Section 3.3.18, *Serial ATA (SATA) Signals*.

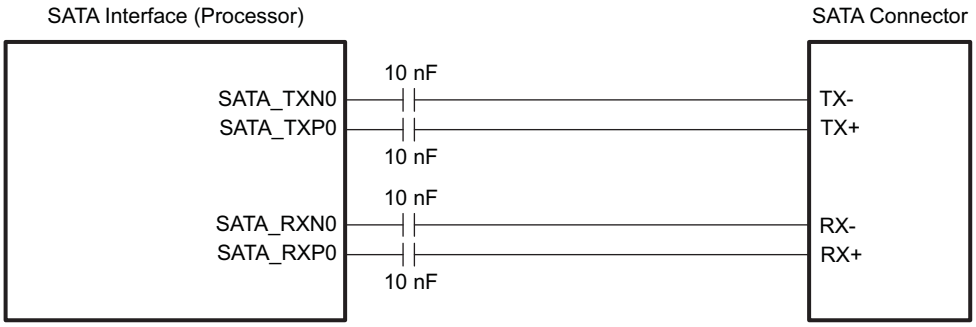


Figure 8-78. SATA Interface High-Level Schematic

8.15.2.2 Compatible SATA Components and Modes

Table 8-63 shows the compatible SATA components and supported modes. Note that the only supported configuration is an internal cable from the processor host to the SATA device.

Table 8-63. SATA Supported Modes

PARAMETER	MIN	MAX	UNIT	SUPPORTED
Transfer Rates	1.5	3.0	Gbps	
xSATA	-	-	-	No
Backplane	-	-	-	No

Table 8-63. SATA Supported Modes (continued)

PARAMETER	MIN	MAX	UNIT	SUPPORTED
Internal Cable (iSATA)	-	-	-	Yes

8.15.2.3 PCB Stackup Specifications

Table 8-64 shows the PCB stackup and feature sizes required for SATA.

Table 8-64. SATA PCB Stackup Specifications

PARAMETER	MIN	TYP	MAX	UNIT
PCB routing/plane layers	4	6	-	Layers
Signal routing layers	2	3	-	Layers
Number of ground plane cuts allowed within SATA routing region	-	-	0	Cuts
Number of layers between SATA routing region and reference ground plane	-	-	0	Layers
PCB trace width, w	-	4	-	Mils
PCB BGA escape via pad size	-	20	-	Mils
PCB BGA escape via hole size	-	10		Mils
Processor BGA pad size(1)		0.4		mm

(1) NSMD pad, per IPC-7351A BGA pad size guideline.

8.15.2.4 Routing Specifications

The SATA data signal traces must be routed to achieve 100 Ω (±20%) differential impedance and 60 Ω (±15%) single-ended impedance. The single-ended impedance is required because differential signals are extremely difficult to closely couple on PCBs and, therefore, single-ended impedance becomes important. 60 Ω is chosen for the single-ended impedance to minimize problems caused by too low an impedance.

These impedances are impacted by trace width, trace spacing, distance to reference planes, and dielectric material. Verify with a PCB design tool that the trace geometry for both data signal pairs results in as close to 100 Ω differential impedance and 60 Ω single-ended impedance traces as possible. For best accuracy, work with your PCB fabricator to ensure this impedance is met.

When routing SATA on the top (or any single) layer, the pin assignment will not allow a straight routing for the SATAx_RXP0 and SATAx_RXN0 signals. There are two ways to overcome this:

1. Swap the SATA pin assignment in the software registers to allow straight, single layer routing.
2. Use the method pictured below in Figure 8-79 and Figure 8-80 to route to the SATA connector. This method results in lines that are still length matched, and still on just one single layer.

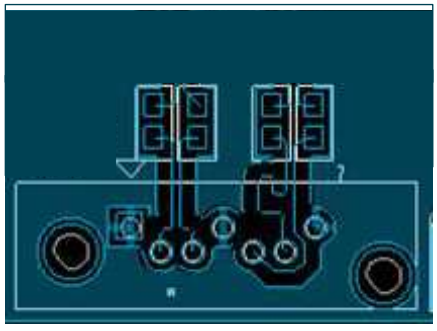


Figure 8-79. SATA Routing

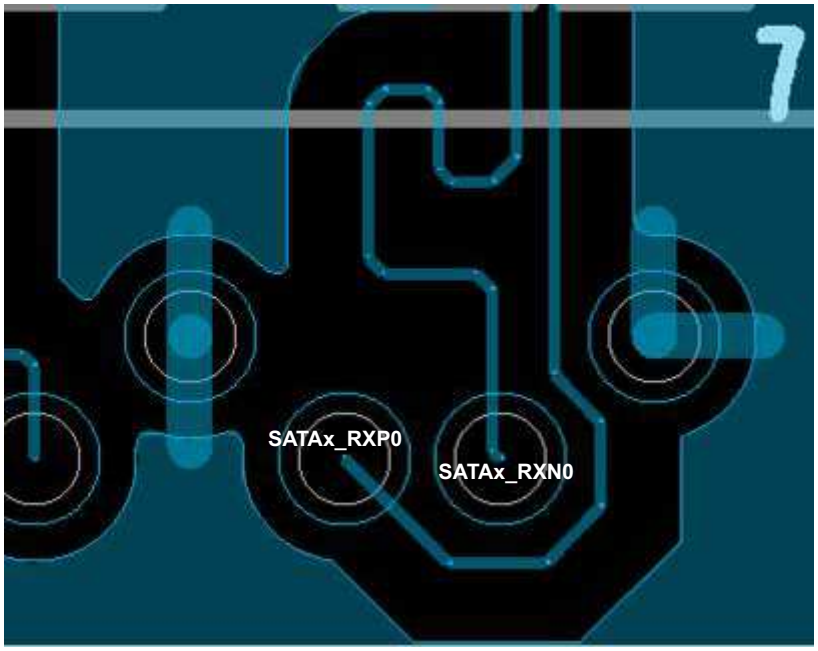


Figure 8-80. Close Up of SATA Routing

Table 8-65 shows the routing specifications for the SATA data signals.

Table 8-65. SATA Routing Specifications

PARAMETER	MIN	TYP	MAX	UNIT
Processor-to-SATA header trace length			10 (1)	Inches
Number of stubs allowed on SATA traces (2)			0	Stubs
TX/RX pair differential impedance	80	100	120	Ω
TX/RX single ended impedance	51	60	69	Ω
Number of vias on each SATA trace			3	Vias (3)
SATA differential pair to any other trace spacing	2*DS (4)			

(1) Beyond this, signal integrity may suffer.
(2) In-line pads may be used for probing.
(3) Vias must be used in pairs with their distance minimized.
(4) DS = differential spacing of the SATA traces.

8.15.2.5 Coupling Capacitors

AC coupling capacitors are required on the receive data pair. Table 8-66 shows the requirements for these capacitors.

Table 8-66. SATA AC Coupling Capacitors Requirements

PARAMETER	MIN	TYP	MAX	UNIT
SATA AC coupling capacitor value	1	10	12	nF
SATA AC coupling capacitor package size (1)		0402	0603	EIA (2)

(1) The physical size of the capacitor should be as small as practical. Use the same size on both lines in each pair, placed side by side.
(2) EIA LxW units; that is, a 0402 is a 40 x 20 mil surface-mount capacitor.

8.16 Serial Peripheral Interface (SPI)

The SPI is a high-speed synchronous serial input/output port that allows a serial bit stream of programmed length (4 to 32 bits) to be shifted into and out of the device at a programmed bit-transfer rate. The SPI is normally used for communication between the device and external peripherals. Typical applications include an interface-to-external I/O or peripheral expansion via devices such as shift registers, display drivers, SPI EEPROMs, and Analog-to-Digital Converters (ADCs).

The SPI supports the following features:

- Master/Slave operation
- Four chip selects for interfacing/control to up to four SPI Slave devices and connection to a single external Master
- 32-bit shift register
- Buffered receive/transmit data register per channel (1 word deep), FIFO size is 64 bytes
- Programmable SPI configuration per channel (clock definition, enable polarity and word width)
- Supports one interrupt request and two DMA requests per channel.

For more detailed information on the SPI, see the *Multichannel Serial Port Interface (McSPI)* chapter in the device-specific Technical Reference Manual.

8.16.1 SPI Peripheral Register Descriptions

The SPI peripheral registers are described in the device-specific Technical Reference Manual. Each register is documented as an offset from a base address for the peripheral. The base addresses for all of the peripherals are in the device memory map (see Section 2.10).

8.16.2 SPI Electrical Data/Timing

Table 8-67. Timing Requirements for SPI - Master Mode

(see Figure 8-81 and Figure 8-82)

NO.				OPP100/OPP120/ Turbo/Nitro		UNIT
				MIN	MAX	
MASTER: SPI0, SPI1, SPI2 (M0) and SPI3 (M0)1 LOAD AT A MAXIMUM OF 5 pF						
1	$t_{c(SPICLK)}$	Cycle time, SPI_CLK(1)(2)		20.8(3)		ns
2	$t_{w(SPICLKL)}$	Pulse duration, SPI_CLK low(1)		0.5*P - 1(4)		ns
3	$t_{w(SPICLKH)}$	Pulse duration, SPI_CLK high(1)		0.5*P - 1(4)		ns
4	$t_{su(MISO-SPICLK)}$	Setup time, SPI_D[x] valid before SPI_CLK active edge(1)	SPI0, SPI1	2.29		ns
			SPI2, SPI3	4		
5	$t_{h(SPICLK-MISO)}$	Hold time, SPI_D[x] valid after SPI_CLK active edge(1)		2.67		ns
6	$t_{d(SPICLK-MOSI)}$	Delay time, SPI_CLK active edge to SPI_D[x] transition(1)			3.57	ns
7	$t_{d(SCS-MOSI)}$	Delay time, $\overline{\text{SPI\_SCS[x]}}$ active edge to SPI_D[x] transition			3.57	ns
8	$t_{d(SCS-SPICLK)}$	Delay time, $\overline{\text{SPI\_SCS[x]}}$ active to SPI_CLK first edge(1)	MASTER_PHA0(5)	B-4.2(6)		ns
			MASTER_PHA1(5)	A-4.2(7)		ns
9	$t_{d(SPICLK-SCS)}$	Delay time, SPI_CLK last edge to $\overline{\text{SPI\_SCS[x]}}$ inactive(1)	MASTER_PHA0(5)	A-4.2(7)		ns
			MASTER_PHA1(5)	B-4.2(6)		ns
MASTER: SPI0, SPI1, SPI2 (M0) and SPI3 (M0) LOAD AT MAX 25pF MASTER: SPI2 (M1, M2, M3) and SPI3 (M1, M2, M3) 1 to 4 LOAD AT 5 to 25pF						
1	$t_{c(SPICLK)}$	Cycle time, SPI_CLK(1)(2)		41.7(8)		ns
2	$t_{w(SPICLKL)}$	Pulse duration, SPI_CLK low(1)		0.5*P - 2(4)		ns
3	$t_{w(SPICLKH)}$	Pulse duration, SPI_CLK high(1)		0.5*P - 2(4)		ns
4	$t_{su(MISO-SPICLK)}$	Setup time, SPI_D[x] valid before SPI_CLK active edge(1)	SPI0, SPI1	4		ns
			SPI2, SPI3	6		
5	$t_{h(SPICLK-MISO)}$	Hold time, SPI_D[x] valid after SPI_CLK active edge(1)		3.8		ns
6	$t_{d(SPICLK-MOSI)}$	Delay time, SPI_CLK active edge to SPI_D[x] transition(1)		-5.5	5.5	ns
7	$t_{d(SCS-MOSI)}$	Delay time, $\overline{\text{SPI\_SCS[x]}}$ active edge to SPI_D[x] transition			5.5	ns
8	$t_{d(SCS-SPICLK)}$	Delay time, $\overline{\text{SPI\_SCS[x]}}$ active to SPI_CLK first edge(1)	MASTER_PHA0(5)	B-3.5(6)		ns
			MASTER_PHA1(5)	A-3.5(7)		ns
9	$t_{d(SPICLK-SCS)}$	Delay time, SPI_CLK last edge to $\overline{\text{SPI\_SCS[x]}}$ inactive(1)	MASTER_PHA0(5)	A-3.5(7)		ns
			MASTER_PHA1(5)	B-3.5(6)		ns

(1) This timing applies to all configurations regardless of SPI_CLK polarity and which clock edges are used to drive output data and capture input data.
(2) Related to the SPI_CLK maximum frequency.
(3) Maximum frequency = 48 MHz
(4) P = SPICLK period.
(5) SPI_CLK phase is programmable with the PHA bit of the SPI_CH(i)CONF register.
(6) B = (TCS + 0.5) * TSPICLKREF * F_{ratio}, where TCS is a bit field of the SPI_CH(i)CONF register and F_{ratio} = Even ≥2.
(7) When P = 20.8 ns, A = (TCS + 1) * TSPICLKREF, where TCS is a bit field of the SPI_CH(i)CONF register. When P > 20.8 ns, A = (TCS + 0.5) * F_{ratio} * TSPICLKREF, where TCS is a bit field of the SPI_CH(i)CONF register.
(8) Maximum frequency = 24 MHz

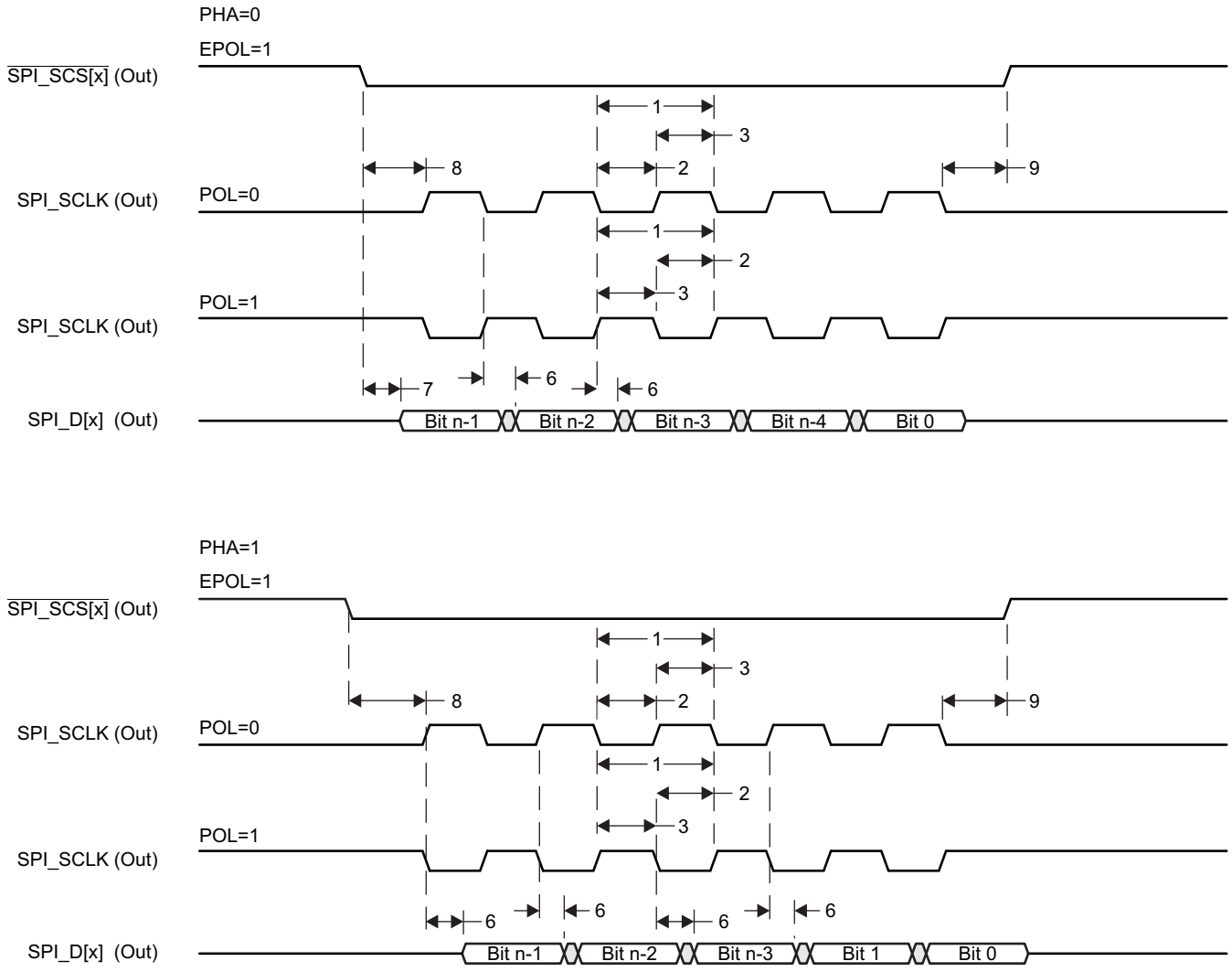


Figure 8-81. SPI Master Mode Transmit Timing

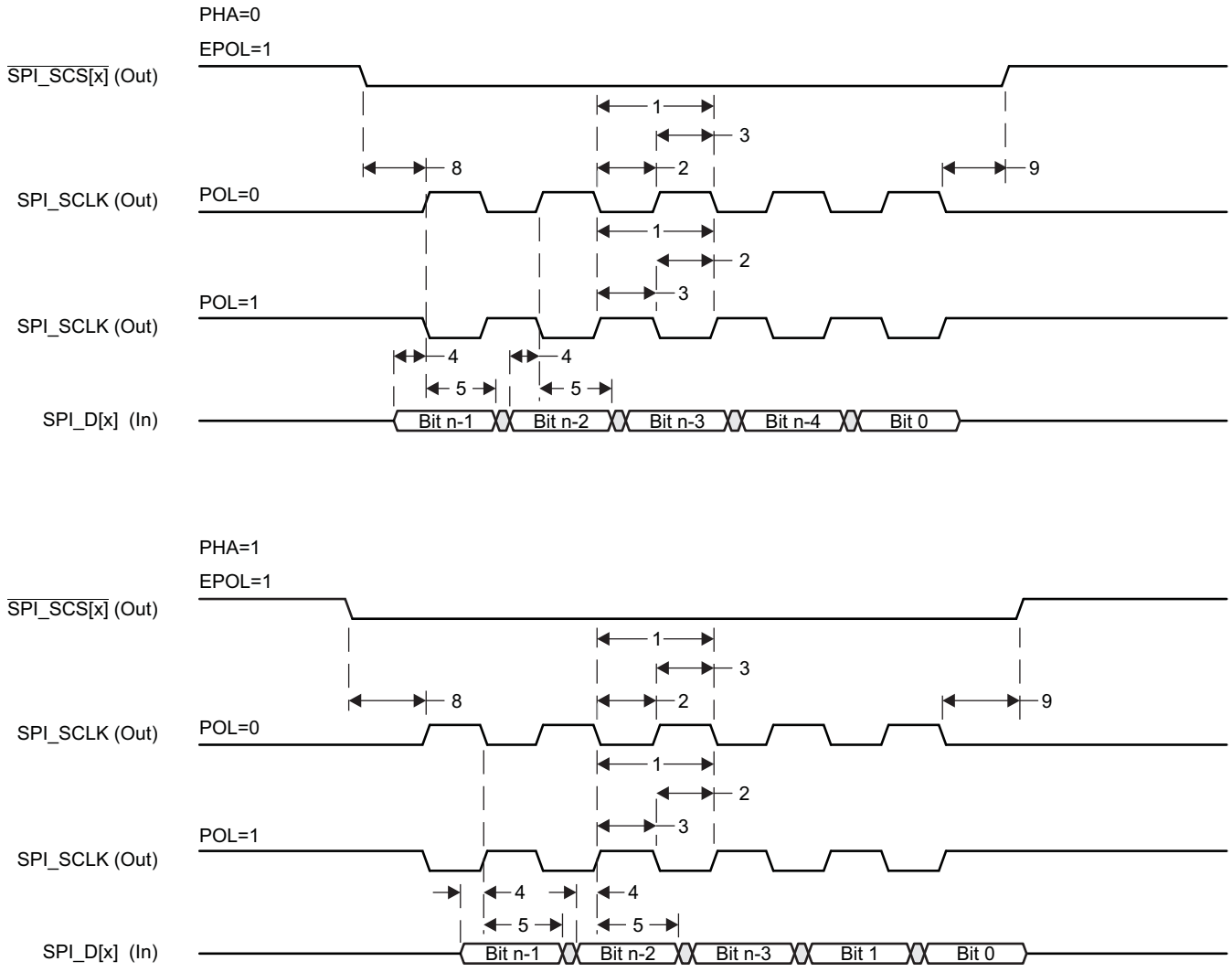


Figure 8-82. SPI Master Mode Receive Timing

Table 8-68. Timing Requirements for SPI - Slave Mode

(see Figure 8-83 and Figure 8-84)

NO.			OPP100/OPP120/Turbo/Nitro		UNIT
			MIN	MAX	
1	$t_{c(SPICLK)}$	Cycle time, SPI_CLK (1) (2)	62.5 (3)		ns
2	$t_{w(SPICLKL)}$	Pulse duration, SPI_CLK low (1)	0.5*P - 3 (4)		ns
3	$t_{w(SPICLKH)}$	Pulse duration, SPI_CLK high (1)	0.5*P - 3 (4)		ns
4	$t_{su(MOSI-SPICLK)}$	Setup time, SPI_D[x] valid before SPI_CLK active edge (1)	12.92		ns
5	$t_{h(SPICLK-MOSI)}$	Hold time, SPI_D[x] valid after SPI_CLK active edge (1)	12.92		ns
6	$t_{d(SPICLK-MISO)}$	Delay time, SPI_CLK active edge to SPI_D[x] transition (1)	-4.00	17.1	ns
7	$t_{d(SCS-MISO)}$	Delay time, $\overline{\text{SPI\_SCS[x]}}$ active edge to SPI_D[x] transition (5)		17.1	ns

(1) This timing applies to all configurations regardless of SPI_CLK polarity and which clock edges are used to drive output data and capture input data.
(2) Related to the input maximum frequency supported by the SPI module.
(3) Maximum frequency = 16 MHz
(4) P = SPICLK period.
(5) PHA = 0; SPI_CLK phase is programmable with the PHA bit of the SPI_CH(i)CONF register.

Table 8-68. Timing Requirements for SPI - Slave Mode (continued)

(see Figure 8-83 and Figure 8-84)

NO.			OPP100/OPP120/Turbo/Nitro		UNIT
			MIN	MAX	
8	$t_{su(SCS-SPICLK)}$	Setup time, $\overline{SPI\_SCS[x]}$ valid before SPI_CLK first edge(1)	12.92		ns
9	$t_{h(SPICLK-SCS)}$	Hold time, $\overline{SPI\_SCS[x]}$ valid after SPI_CLK last edge(1)	12.92		ns

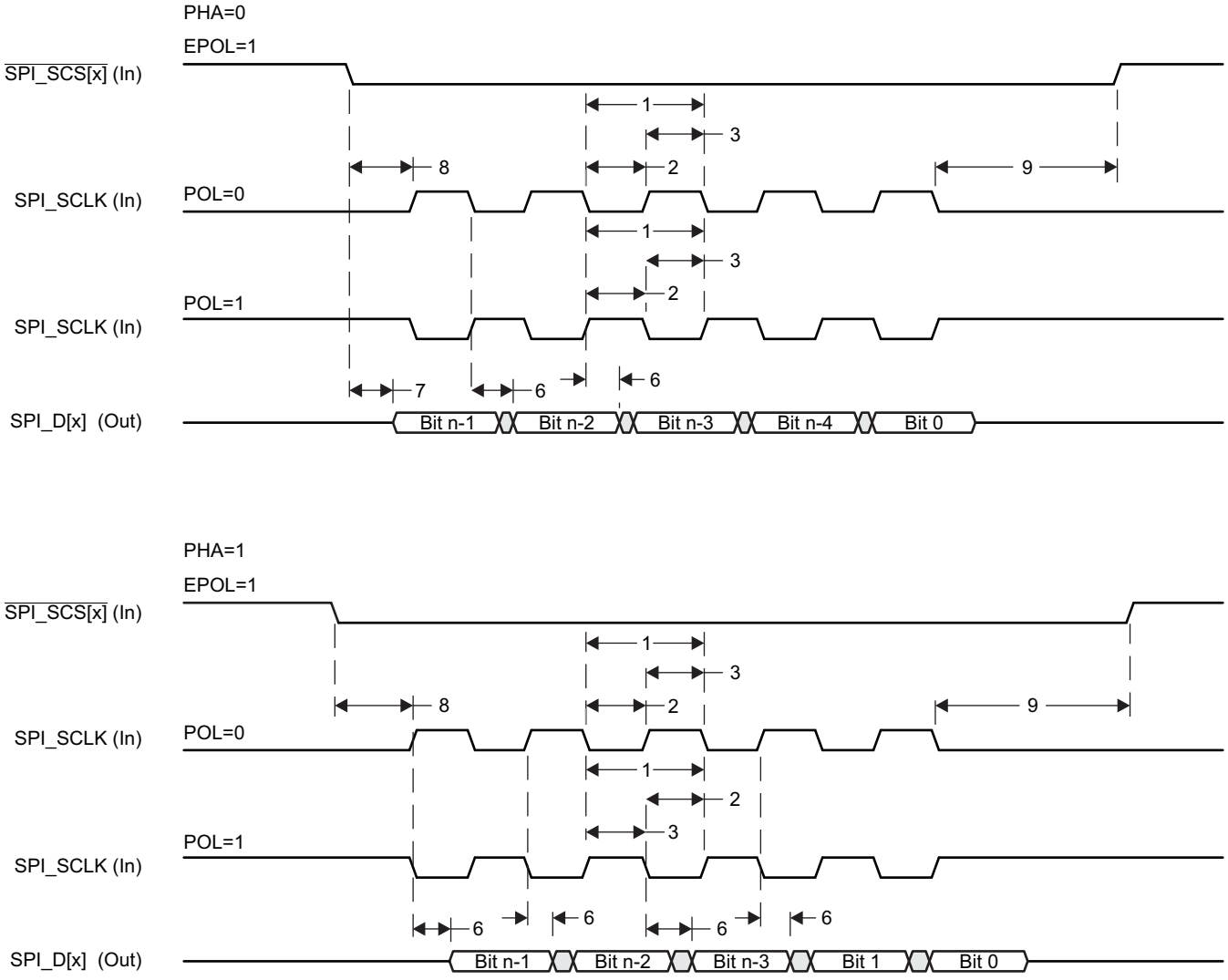


Figure 8-83. SPI Slave Mode Transmit Timing

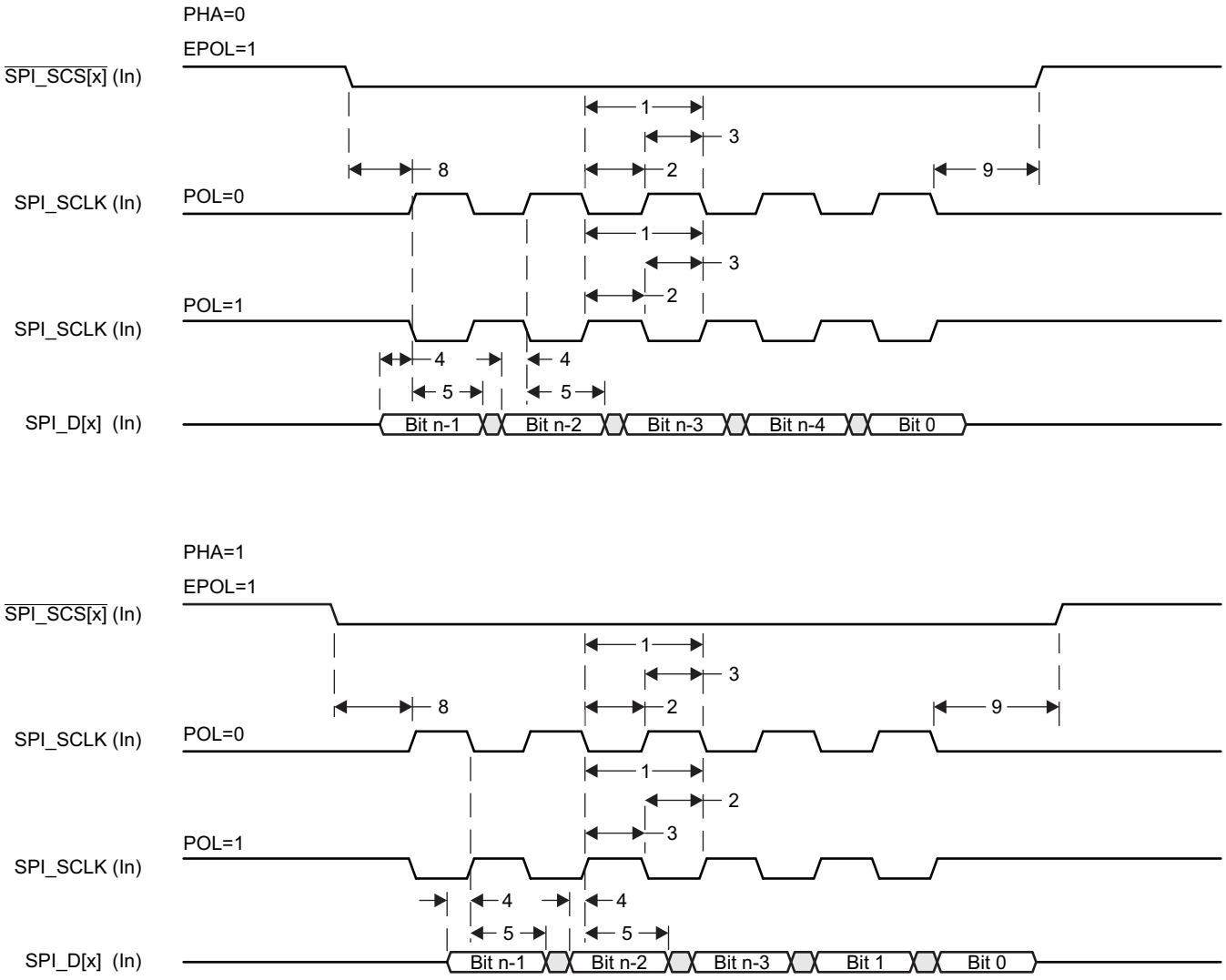


Figure 8-84. SPI Slave Mode Receive Timing

8.17 Timers

The device has eight 32-bit general-purpose (GP) timers (TIMER8 - TIMER1) that have the following features:

- TIMER8, TIMER1 are for software use and do not have an external connection
- Dedicated input trigger for capture mode and dedicated output trigger/pulse width modulation (PWM) signal
- Interrupts generated on overflow, compare, and capture
- Free-running 32-bit upward counter
- Supported modes:
  - Compare and capture modes
  - Auto-reload mode
  - Start-stop mode
- TIMER[8:1] functional clock is sourced from either the DEVOSC, AUXOSC, AUD_CLK2/1/0, TCLKIN, or SYSCLK18 27 MHz as selected by the timer clock multiplexers.
- On-the-fly read/write register (while counting)
- Generates interrupts to the ARM and Media Controller.

The device has one system watchdog timer that have the following features:

- Free-running 32-bit upward counter
- On-the-fly read/write register (while counting)
- Reset upon occurrence of a timer overflow condition
- The system watchdog timer has two possible clock sources:
  - RCOSC32K oscillator
  - RTCDIVIDER
- The watchdog timer is used to provide a recovery mechanism for the device in the event of a fault condition, such as a non-exiting code loop.

For more detailed information on the GP and Watchdog Timers, see the *Timers* and *Watchdog Timer* chapters in the device-specific Technical Reference Manual.

8.17.1 Timer Peripheral Register Descriptions

The Timer peripheral registers are described in the device-specific Technical Reference Manual. Each register is documented as an offset from a base address for the peripheral. The base addresses for all of the peripherals are in the device memory map (see Section 2.10).

8.17.2 Timer Electrical/Data Timing

Table 8-69. Timing Requirements for Timer

(see Figure 8-85)

NO.			OPP100/OPP120/ Turbo/Nitro		UNIT
			MIN	MAX	
1	$t_{w(EVTIH)}$	Pulse duration, high	4P(1)		ns
2	$t_{w(EVTIL)}$	Pulse duration, low	4P(1)		ns

(1) P = module clock.

Table 8-70. Switching Characteristics Over Recommended Operating Conditions for Timer

(see Figure 8-85)

NO.	PARAMETER		OPP100/OPP120/ Turbo/Nitro		UNIT
			MIN	MAX	
3	$t_{w(EVTOH)}$	Pulse duration, high	4P-3(1)		ns
4	$t_{w(EVTOL)}$	Pulse duration, low	4P-3(1)		ns

(1) P = module clock.

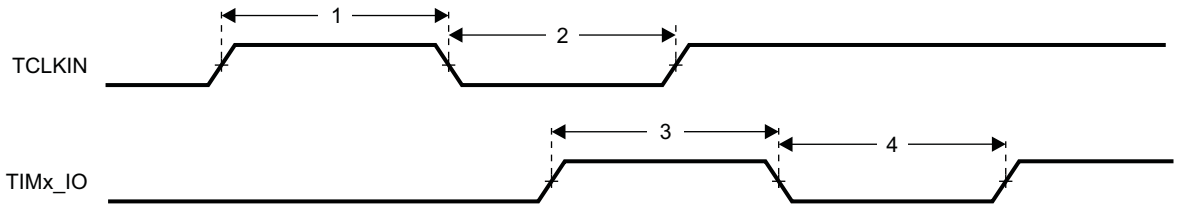


Figure 8-85. Timer Timing

8.18 Universal Asynchronous Receiver/Transmitter (UART)

The UART performs serial-to-parallel conversions on data received from a peripheral device and parallel-to-serial conversion on data received from the CPU. The device provides up to three UART peripheral interfaces, depending on the selected pin multiplexing.

Each UART has the following features:

- Selectable UART/IrDA (SIR/MIR)/CIR modes
- Dual 64-entry FIFOs for received and transmitted data payload
- Programmable and selectable transmit and receive FIFO trigger levels for DMA and interrupt generation
- Baud-rate generation based upon programmable divisors N (N=1…16384)
- Two DMA requests and one interrupt request to the system
- Can connect to any RS-232 compliant device.

UART functions include:

- Baud-rate up to 3.6 Mbit/s on UART0, UART1, and UART2
- Programmable serial interfaces characteristics
  - 5, 6, 7, or 8-bit characters
  - Even, odd, or no parity-bit generation and detection
  - 1, 1.5, or 2 stop-bit generation
  - Flow control: hardware (RTS/CTS) or software (XON/XOFF)
- Additional modem control functions (UART0_DTR, UART0_DSR, UART0_DCD, and UART0_RIN) for UART0 only; UART1 and UART2 do not support full-flow control signaling.

IR-IrDA functions include:

- Support of IrDA 1.4 slow infrared (SIR, baud-rate up to 115.2 Kbits/s), medium infrared (MIR, baud-rate up to 1.152 Mbits/s) and fast infrared (FIR baud-rate up to 4.0 Mbits/s) communications
- Supports framing error, cyclic redundancy check (CRC) error, illegal symbol (FIR), and abort pattern (SIR, MIR) detection
- 8-entry status FIFO (with selectable trigger levels) available to monitor frame length and frame errors.

IR-CIR functions include:

- Consumer infrared (CIR) remote control mode with programmable data encoding
- Free data format (supports any remote control private standards)
- Selectable bit rate and configurable carrier frequency.

For more detailed information on the UART peripheral, see the *UART/IrDA/CIR Module* chapter in the device-specific Technical Reference Manual.

8.18.1 UART Peripheral Register Descriptions

The UART peripheral registers are described in the device-specific Technical Reference Manual. Each register is documented as an offset from a base address for the peripheral. The base addresses for all of the peripherals are in the device memory map (see Section 2.10).

8.18.2 UART Electrical/Data Timing

Table 8-71. Timing Requirements for UART

(see Figure 8-86)

NO.			OPP100/OPP120/ Turbo/Nitro		UNIT
			MIN	MAX	
4	$t_{w(RX)}$	Pulse width, receive data bit, 15/30/100pF high or low	0.96U(1)	1.05U(1)	ns
5	$t_{w(CTS)}$	Pulse width, receive start bit, 15/30/100pF high or low	0.96U(1)	1.05U(1)	ns
	$t_{d(RTS-TX)}$	Delay time, transmit start bit to transmit data	P(2)		ns
	$t_{d(CTS-TX)}$	Delay time, receive start bit to transmit data	P(2)		ns

(1) U = UART baud time = 1/programmed baud rate
(2) P = Clock period of the reference clock (FCLK, usually 48 MHz).

Table 8-72. Switching Characteristics Over Recommended Operating Conditions for UART

(see Figure 8-86)

NO.	PARAMETER			OPP100/OPP120/ Turbo/Nitro		UNIT
				MIN	MAX	
	$f_{(baud)}$	Maximum programmable baud rate	15 pF		5	MHz
			30 pF		0.23	
			100 pF		0.115	
2	$t_{w(TX)}$	Pulse width, transmit data bit, 15/30/100 pF high or low		U - 2(1)	U + 2(1)	ns
3	$t_{w(RTS)}$	Pulse width, transmit start bit, 15/30/100 pF high or low		U - 2(1)	U + 2(1)	ns

(1) U = UART baud time = 1/programmed baud rate

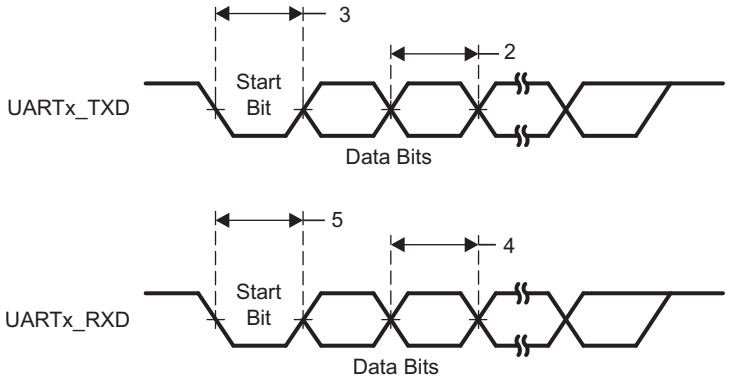


Figure 8-86. UART Timing

8.19 Universal Serial Bus (USB2.0)

The device includes two USB2.0 modules which support the *Universal Serial Bus Specification Revision 2.0.* The following are some of the major USB features that are supported:

- USB 2.0 peripheral at high speed (HS: 480 Mbps) and full speed (FS: 12 Mbps)
- USB 2.0 host at HS, FS, and low speed (LS: 1.5 Mbps)
- Each endpoint (other than endpoint 0, control only) can support all transfer modes (control, bulk, interrupt, and isochronous)
- Supports high-bandwidth ISO mode
- Supports 15 Transmit (TX) and 15 Receive (RX) endpoints including endpoint 0
- FIFO RAM
  - 32K endpoint
  - Programmable size
- Includes two integrated PHYs
- RNDIS-like mode for terminating RNDIS-type protocols without using short-packet termination for support of MSC applications.
- USB Dual Role Device: Host Negotiation Protocol (HNP)

The USB2.0 peripherals do not support the following features:

- On-chip charge pump (VBUS Power must be generated external to the device.)
- RNDIS mode acceleration for USB sizes that are not multiples of 64 bytes
- Endpoint max USB packet sizes that do not conform to the USB 2.0 spec (for FS/LS: 8, 16, 32, 64, – and 1023 are defined; for HS: 64, 128, 512, and 1024 are defined
- USB OTG extension: Session Request Protocol (SRP)

For more detailed information on the USB2.0 peripheral, see the *Universal Serial Bus (USB)* chapter in the device-specific Technical Reference Manual.

8.19.1 USB2.0 Peripheral Register Descriptions

The USB peripheral registers are described in the device-specific Technical Reference Manual. Each register is documented as an offset from a base address for the peripheral. The base addresses for all of the peripherals are in the device memory map (see Section 2.10).

8.19.2 USB2.0 Electrical Data/Timing

Table 8-73. Switching Characteristics Over Recommended Operating Conditions for USB2.0

(see Figure 8-87)

NO.	PARAMETER		OPP100/OPP120/ Turbo/Nitro						UNIT
			LOW SPEED 1.5 Mbps		FULL SPEED 12 Mbps		HIGH SPEED 480 Mbps		
			MIN	MAX	MIN	MAX	MIN	MAX	
1	$t_{r(D)}$	Rise time, USBx_DP and USBx_DM signals(1)	75	300	4	20	0.5		ns
2	$t_{f(D)}$	Fall time, USBx_DP and USBx_DM signals(1)	75	300	4	20	0.5		ns
3	t_{rfM}	Rise/Fall time, matching(2)	80	125	90	111	–	–	%
4	V_{CRS}	Output signal cross-over voltage(1)	1.3	2	1.3	2	–	–	V
5	$t_{jr(source)NT}$	Source (Host) Driver jitter, next transition		2		2		(3)	ns
	$t_{jr(FUNC)NT}$	Function Driver jitter, next transition		25		2		(3)	ns
6	$t_{jr(source)PT}$	Source (Host) Driver jitter, paired transition(4)		1		1		(3)	ns
	$t_{jr(FUNC)PT}$	Function Driver jitter, paired transition		10		1		(3)	ns
7	$t_{w(EOPT)}$	Pulse duration, EOP transmitter	1250	1500	160	175	–	–	ns
8	$t_{w(EOPR)}$	Pulse duration, EOP receiver(5)	670		82		–		ns
9	$t_{(DRATE)}$	Data Rate		1.5		12		480	Mb/s
10	Z_{DRV}	Driver Output Resistance	–	–	28	49.5	40.5	49.5	Ω
11	Z_{INP}	Receiver Input Impedance	300		300	–	–	–	kΩ

(1) Low Speed: C_L = 200 pF, Full Speed: C_L = 50 pF, High Speed: C_L = 50 pF
(2) $t_{RFM} = (t_r/t_f) \times 100$. [Excluding the first transaction from the Idle state.]
(3) For more detailed information, see the Universal Serial Bus Specification Revision 2.0, Chapter 7, *Electrical*.
(4) $t_{jr} = t_{px(1)} - t_{px(0)}$
(5) Must accept as valid EOP.

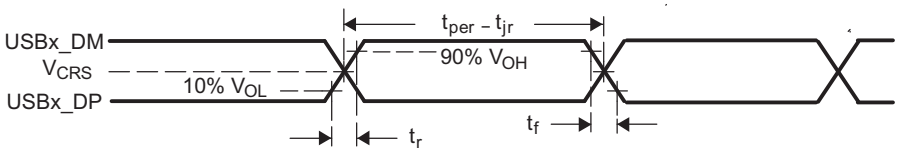


Figure 8-87. USB2.0 Integrated Transceiver Interface Timing

For more detailed information on USB2.0 board design, routing, and layout guidelines, see the *USB 2.0 Board Design and Layout Guidelines* Application Report (Literature Number: SPRAAR7).

9 Device and Documentation Support

9.1 Device Support

9.1.1 Development Support

TI offers an extensive line of development tools, including tools to evaluate the performance of the processors, generate code, develop algorithm implementations, and fully integrate and debug software and hardware modules. The tool's support documentation is electronically available within the Code Composer Studio™ Integrated Development Environment (IDE).

The following products support development of DM383 processor applications:

Software Development Tools: Code Composer Studio™ Integrated Development Environment (IDE): including Editor C/C++/Assembly Code Generation, and Debug plus additional development tools Scalable, Real-Time Foundation Software (Device/BIOS™), which provides the basic run-time target software needed to support any DM383 processor application.

Reference Design Kits: Production ready reference kits including hardware collaterals and software, for a faster time-to-market.

Hardware Development Tools: Extended Development System (XDS™) Emulator

For a complete listing of development-support tools for the DM383 processor platform, visit the Texas Instruments website at www.ti.com. For information on pricing and availability, contact the nearest TI field sales office or authorized distributor.

9.1.2 Device and Development Support-Tool Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all MPUs and support tools. Each device has one of three prefixes: X, P, or null (no prefix). Texas Instruments recommends two of three possible prefix designators for its support tools: TMDX and TMDS. These prefixes represent evolutionary stages of product development from engineering prototypes (TMDX) through fully qualified production devices/tools (TMDS).

Device development evolutionary flow:

X Pre-production device that is not necessarily representative of the final device's electrical specifications and may not use production assembly flow.

P Prototype device that is not necessarily the final silicon die and may not necessarily meet final electrical specifications.

null Production version of the silicon die that is fully qualified.

Support tool development evolutionary flow:

TMDX Development-support product that has not yet completed Texas Instruments internal qualification testing.

TMDS Fully-qualified development-support product.

X and P devices and TMDX development-support tools are shipped against the following disclaimer:

"Developmental product is intended for internal evaluation purposes."

Production devices and TMDS development-support tools have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies.

Predictions show that prototype devices (X or P) have a greater failure rate than the standard production devices. Texas Instruments recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

9.1.3 Device Nomenclature

TI device nomenclature also includes a suffix with the device family name. This suffix indicates the package type (for example, AAR), the temperature range (for example, blank is the default commercial temperature range), and the device speed range (for example, 01 is the 720 MHz ARM device). Figure 9-1 provides a legend for reading the complete device name for any DM383 device.

For device part numbers and further ordering information of DM383 devices in the AAR package type, see the TI website (www.ti.com) or contact your TI sales representative.

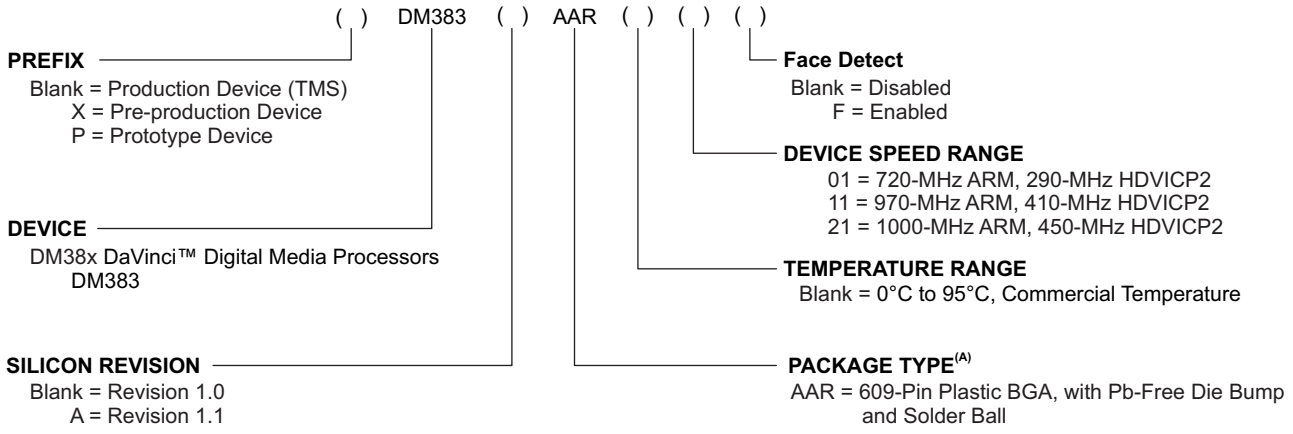


Figure 9-1. Device Nomenclature

9.2 Documentation Support

Contact your TI sales representative for support documents.

For additional peripheral information, see the latest version of the *DM38x DaVinci™ Digital Media Processor Technical Reference Manual* (Literature Number: SPRUHG1).

9.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

TI Embedded Processors Wiki ***Texas Instruments Embedded Processors Wiki.*** Established to help developers get started with Embedded Processors from Texas Instruments and to foster innovation and growth of general knowledge about the hardware and software surrounding these devices.

10 Mechanical

Table 10-1 shows the thermal resistance characteristics for the PBGA–AAR mechanical package.

The device package has been specially engineered with a new technology called Via Channel™, allowing 0.8 mm PCB design rules to be employed. This allows larger than normal PCB via and trace sizes and reduced PCB signal layers to be used in a PCB design with this 0.5 mm pitch package, and will substantially reduce PCB costs. It also allows PCB routing in only two signal layers (four layers total deleted) due to the increased layer efficiency of the Via Channel™ BGA technology.

10.1 Thermal Data for the AAR

Table 10-1. Thermal Resistance Characteristics (PBGA Package) [AAR]

		Air Flow (m/s)(1)	°C/W(2)
$\Theta_{JA/JMA}$	Junction-to-air/ Junction-to-moving air	still air	17.79
		1.0 m/s	13.36
		2.0 m/s	12.54
		3.0 m/s	12.04
Psi_{JT}	Junction-to-package top	still air	0.08
		1.0 m/s	0.16
		2.0 m/s	0.20
		3.0 m/s	0.23
Psi_{JB}	Junction-to-board	still air	4.90
		1.0 m/s	4.81
		2.0 m/s	4.78
		3.0 m/s	4.76
Θ_{JB}	Junction-to-board		4.86
$\Theta_{JC\ (1SOP\ board)}$	Junction-to-case		3.84

(1) m/s = meters per second.
(2) These measurements were conducted in a JEDEC defined 2S2P system (with the exception of the Theta JC [ΘJC] measurement, which was conducted in a JEDEC defined 1S0P system) and will change based on environment as well as application. For more information, see these EIA/JEDEC standards:
- JESD51-2, *Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air)*.
- JESD51-3, *Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*.
- JESD51-7, *High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*.
- JESD51-9, *Test Boards for Area Array Surface Mount Packages*.

10.2 Packaging Information

The following packaging information and addendum reflect the most current data available for the designated device(s). This data is subject to change without notice and without revision of this document.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DM383AAAR11	ACTIVE	FCBGA	AAR	609	90	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	0 to 0	DM383AAAR11	Samples
DM383AAAR21	ACTIVE	FCBGA	AAR	609	90	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR		DM383AAAR21	Samples
DM383AAAR21F	ACTIVE	FCBGA	AAR	609	90	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR		DM383AAAR21F	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

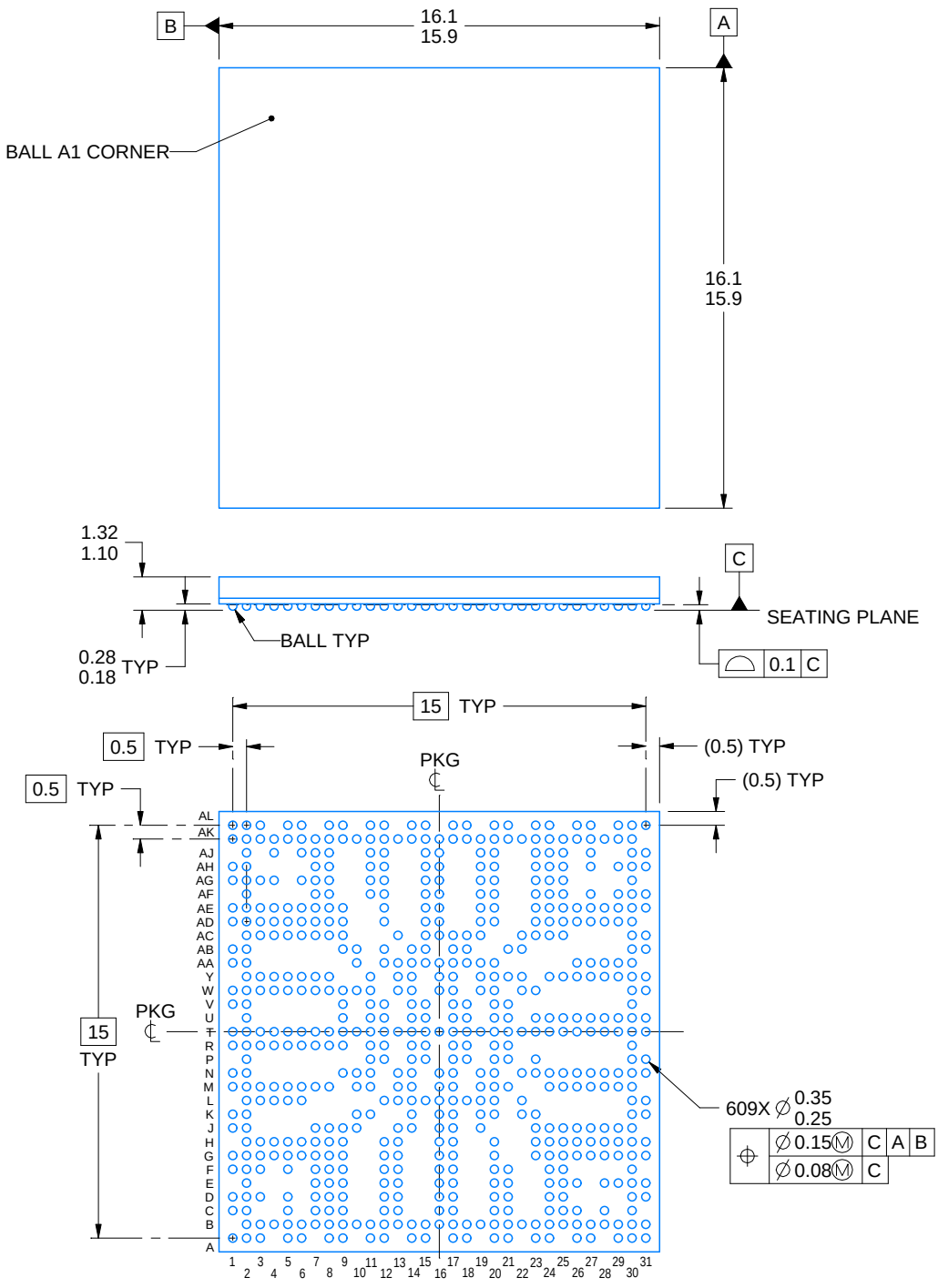
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

PACKAGE OUTLINE

AAR0609A

FCBGA - 1.32 mm max height

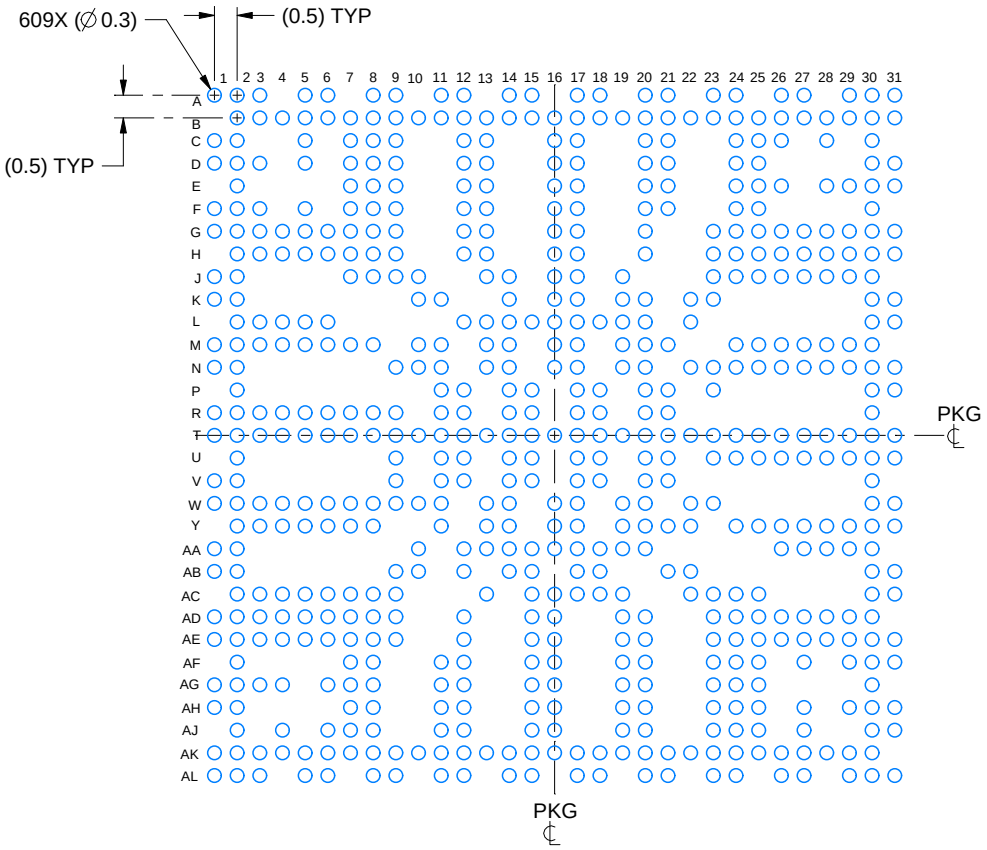
BALL GRID ARRAY



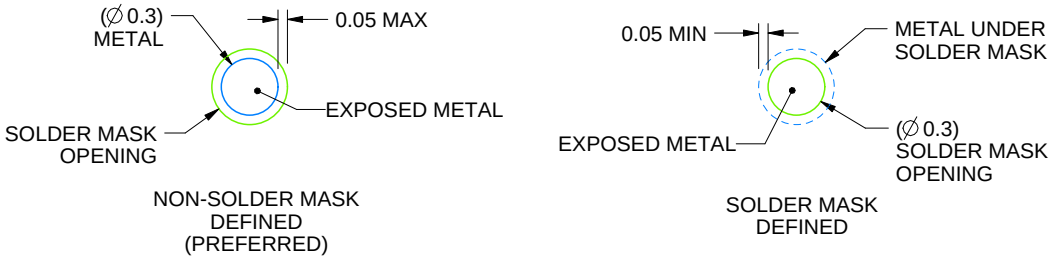
4224431/A 10/2018

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Pb-free solder ball design.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:6X

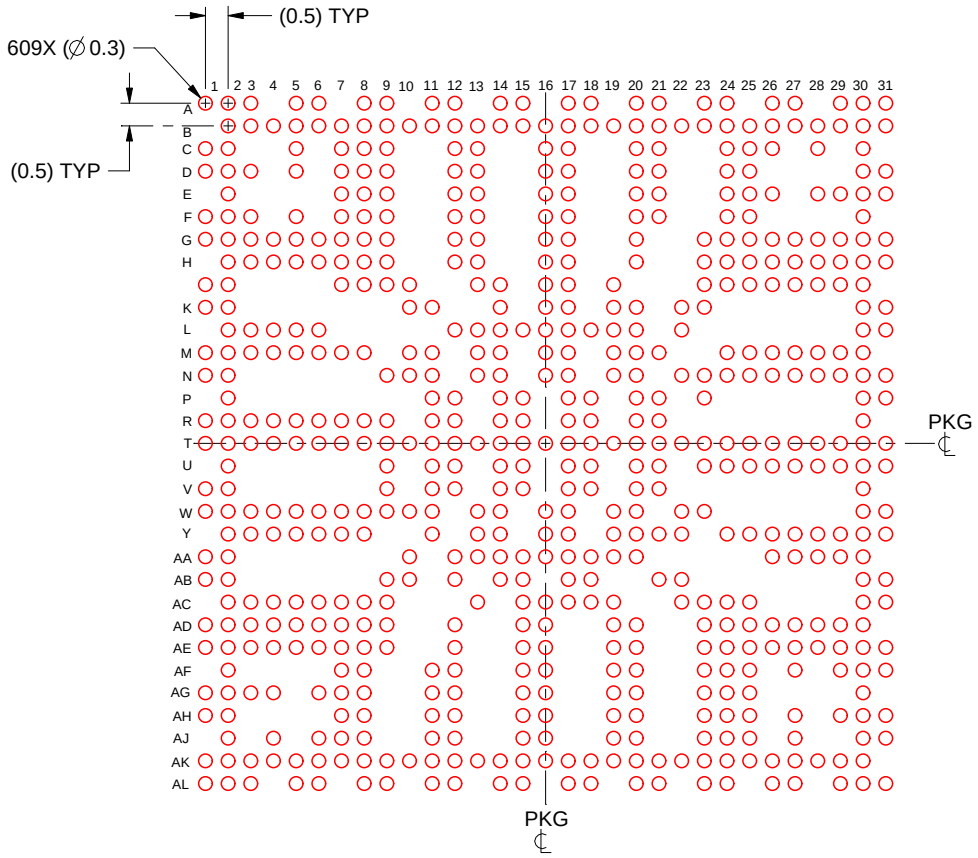


SOLDER MASK DETAILS
NOT TO SCALE

4224431/A 10/2018

NOTES: (continued)

5. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SPRU811 (www.ti.com/lit/spru811).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:6X

4224431/A 10/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale (www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265