

CSD88539ND, Dual 60 V N-Channel NexFET™ Power MOSFETs

1 Features

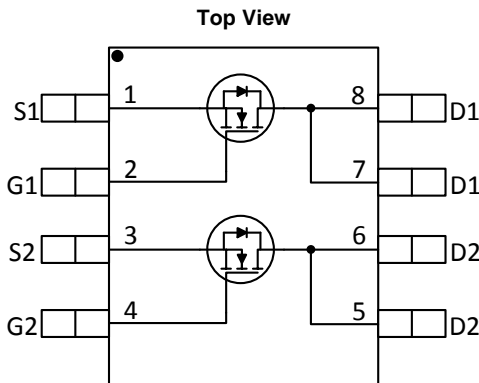
- Ultra-Low Q_g and Q_{gd}
- Avalanche Rated
- Pb Free
- RoHS Compliant
- Halogen Free

2 Applications

- Half Bridge for Motor Control
- Synchronous Buck Converter

3 Description

This dual SO-8, 60 V, 23 mΩ NexFET™ power MOSFET is designed to serve as a half bridge in low-current motor control applications.



Product Summary

$T_A = 25^\circ\text{C}$		TYPICAL VALUE		UNIT
V_{DS}	Drain-to-Source Voltage	60		V
Q_g	Gate Charge Total (10 V)	7.2		nC
Q_{gd}	Gate Charge Gate to Drain	1.1		nC
$R_{DS(on)}$	Drain-to-Source On Resistance	$V_{GS} = 6\text{ V}$	27	mΩ
		$V_{GS} = 10\text{ V}$	23	mΩ
$V_{GS(th)}$	Threshold Voltage	3.0		V

Ordering Information

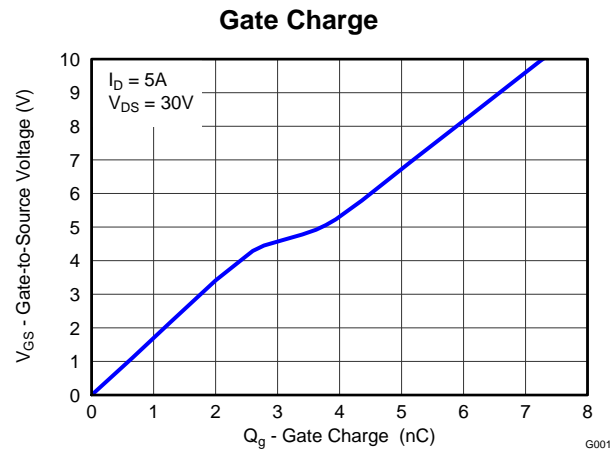
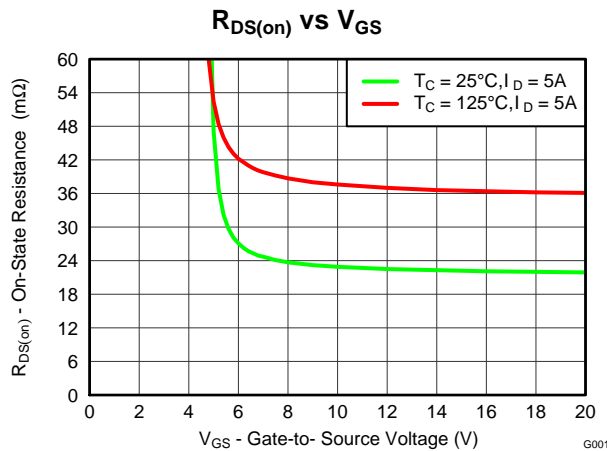
Device	Qty	Media	Package	Ship
CSD88539ND	2500	13-Inch Reel	SO-8 Plastic Package	Tape and Reel
CSD88539NDT	250	7-Inch Reel		

Absolute Maximum Ratings

$T_A = 25^\circ\text{C}$		VALUE	UNIT
V_{DS}	Drain-to-Source Voltage	60	V
V_{GS}	Gate-to-Source Voltage	± 20	V
I_D	Continuous Drain Current (Package limited)	15	A
	Continuous Drain Current (Silicon limited), $T_C = 25^\circ\text{C}$	11.7	
	Continuous Drain Current ⁽¹⁾	6.3	
I_{DM}	Pulsed Drain Current ⁽²⁾	46	A
P_D	Power Dissipation ⁽¹⁾	2.1	W
T_J, T_{STG}	Operating Junction and Storage Temperature Range	-55 to 150	$^\circ\text{C}$
E_{AS}	Avalanche Energy, single pulse $I_D = 22\text{ A}, L = 0.1\text{ mH}, R_G = 25\ \Omega$	24	mJ

(1) Typical $R_{\theta JA} = 60^\circ\text{C/W}$ on a 1-inch², 2-oz. Cu pad on a 0.06-inch thick FR4 PCB

(2) Pulse duration $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$



4 Specifications

4.1 Electrical Characteristics

($T_A = 25^\circ\text{C}$ unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Static Characteristics						
V_{DSS}	Drain-to-Source Voltage	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	60			V
I_{DSS}	Drain-to-Source Leakage Current	$V_{GS} = 0\text{ V}, V_{DS} = 48\text{ V}$			1	μA
I_{GSS}	Gate-to-Source Leakage Current	$V_{DS} = 0\text{ V}, V_{GS} = 20\text{ V}$			100	nA
$V_{GS(th)}$	Gate-to-Source Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	2.6	3.0	3.6	V
$R_{DS(on)}$	Drain-to-Source On Resistance	$V_{GS} = 6\text{ V}, I_D = 5\text{ A}$		27	34	m Ω
		$V_{GS} = 10\text{ V}, I_D = 5\text{ A}$		23	28	m Ω
g_{fs}	Transconductance	$V_{DS} = 30\text{ V}, I_D = 5\text{ A}$		19		S
Dynamic Characteristics						
C_{iss}	Input Capacitance	$V_{GS} = 0\text{ V}, V_{DS} = 30\text{ V}, f = 1\text{ MHz}$		570	741	pF
C_{oss}	Output Capacitance			70	91	pF
C_{rss}	Reverse Transfer Capacitance			2.0	2.6	pF
R_G	Series Gate Resistance			6.6	13.2	Ω
Q_g	Gate Charge Total (10 V)	$V_{DS} = 30\text{ V}, I_D = 5\text{ A}$		7.2	9.4	nC
Q_{gd}	Gate Charge Gate to Drain			1.1		nC
Q_{gs}	Gate Charge Gate to Source			2.7		nC
$Q_{g(th)}$	Gate Charge at V_{th}			1.8		nC
Q_{oss}	Output Charge	$V_{DS} = 30\text{ V}, V_{GS} = 0\text{ V}$		9.6		nC
$t_{d(on)}$	Turn On Delay Time	$V_{DS} = 30\text{ V}, V_{GS} = 10\text{ V}, I_{DS} = 5\text{ A}, R_G = 0\ \Omega$		5		ns
t_r	Rise Time			9		ns
$t_{d(off)}$	Turn Off Delay Time			14		ns
t_f	Fall Time			4		ns
Diode Characteristics						
V_{SD}	Diode Forward Voltage	$I_{SD} = 5\text{ A}, V_{GS} = 0\text{ V}$		0.8	1	V
Q_{rr}	Reverse Recovery Charge	$V_{DS} = 30\text{ V}, I_F = 5\text{ A}, di/dt = 300\text{A}/\mu\text{s}$		37		nC
t_{rr}	Reverse Recovery Time			21		ns

4.2 Thermal Characteristics

($T_A = 25^\circ\text{C}$ unless otherwise stated)

PARAMETER		MIN	TYP	MAX	UNIT
$R_{\theta JL}$	Junction-to-Lead Thermal Resistance ⁽¹⁾			20	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Junction-to-Ambient Thermal Resistance ⁽¹⁾⁽²⁾			75	$^\circ\text{C}/\text{W}$

- (1) $R_{\theta JC}$ is determined with the device mounted on a 1-inch² (6.45-cm²), 2-oz. (0.071-mm thick) Cu pad on a 1.5-inch x 1.5-inch (3.81-cm x 3.81-cm), 0.06-inch (1.52-mm) thick FR4 PCB. $R_{\theta JC}$ is specified by design, whereas $R_{\theta JA}$ is determined by the user's board design.
- (2) Device mounted on FR4 material with 1-inch² (6.45-cm²), 2-oz. (0.071-mm thick) Cu.

4.3 Typical MOSFET Characteristics

($T_A = 25^\circ\text{C}$ unless otherwise stated)

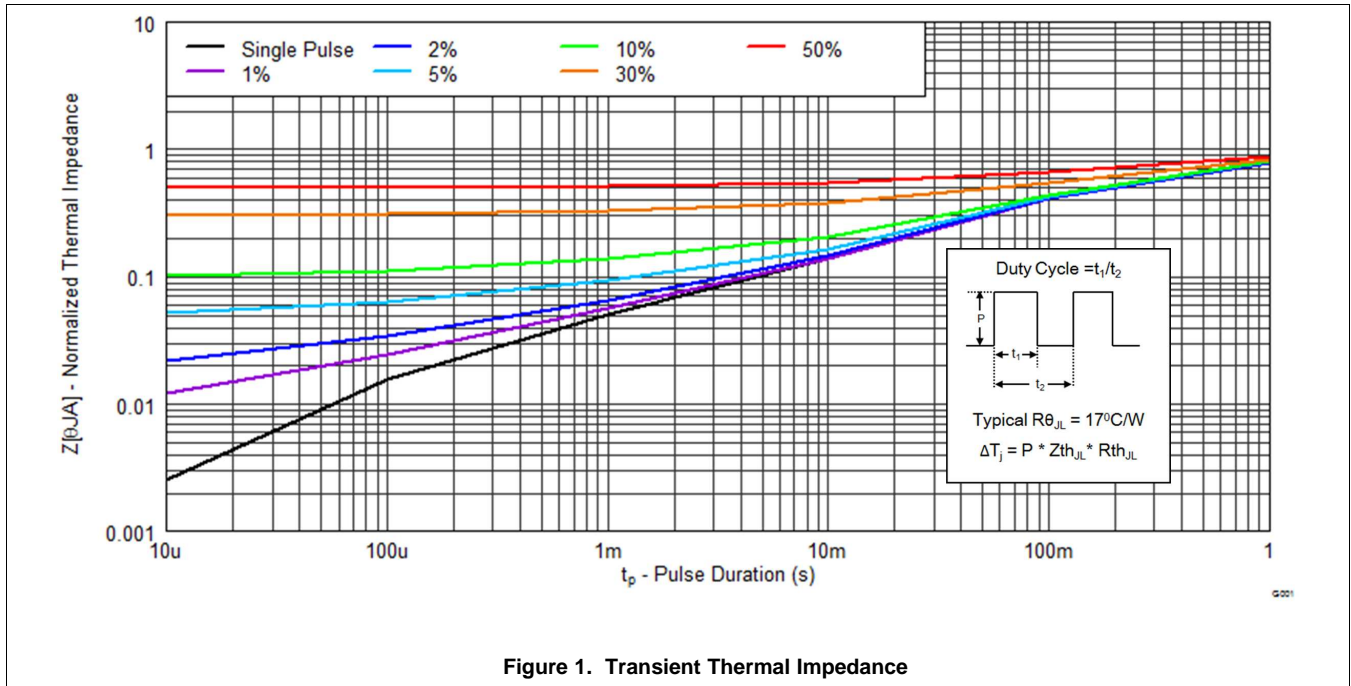


Figure 1. Transient Thermal Impedance

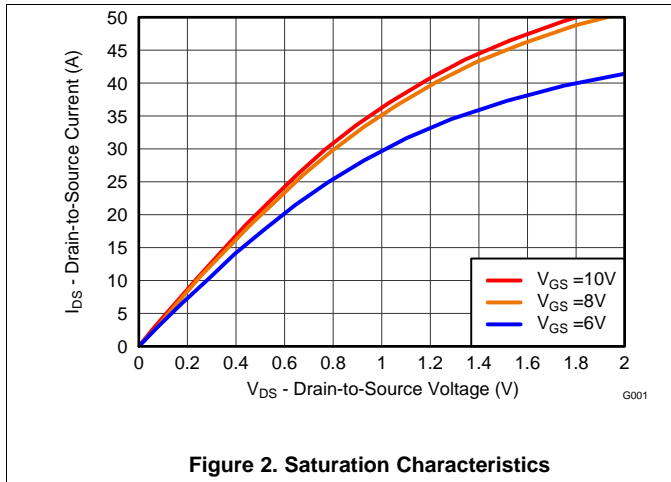


Figure 2. Saturation Characteristics

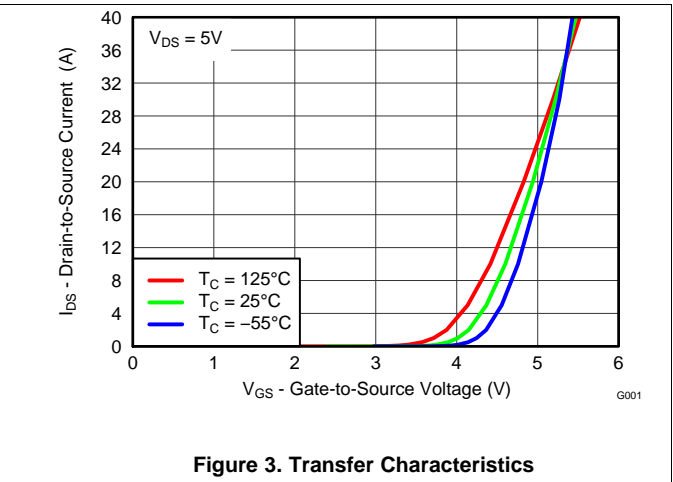
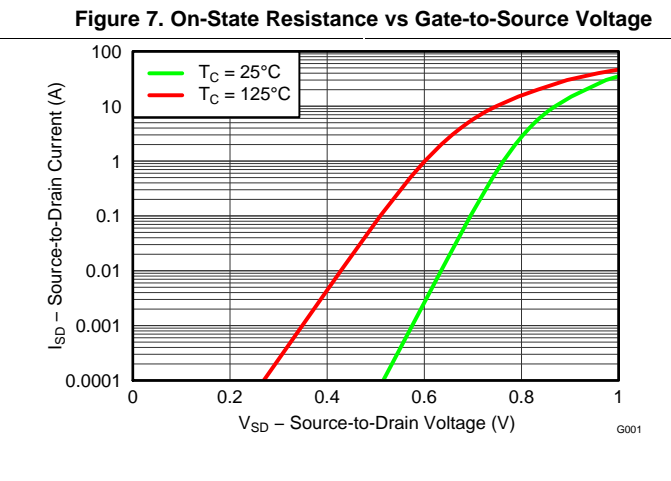
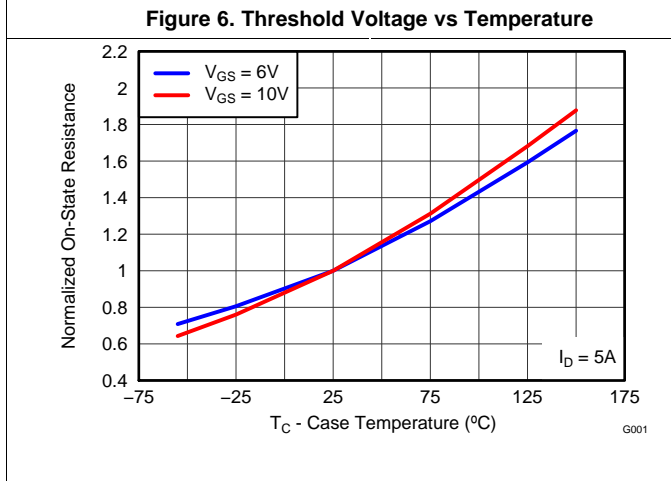
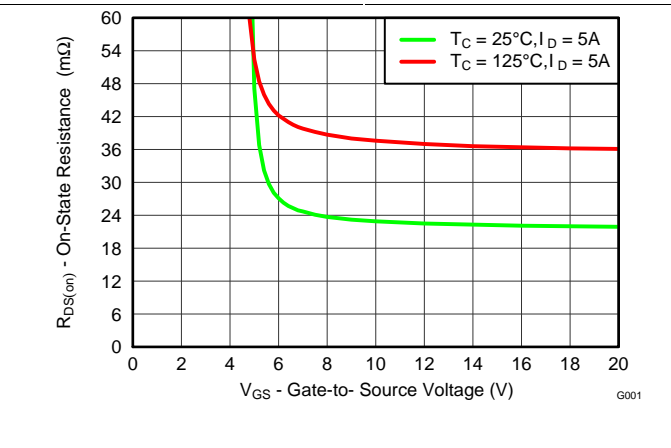
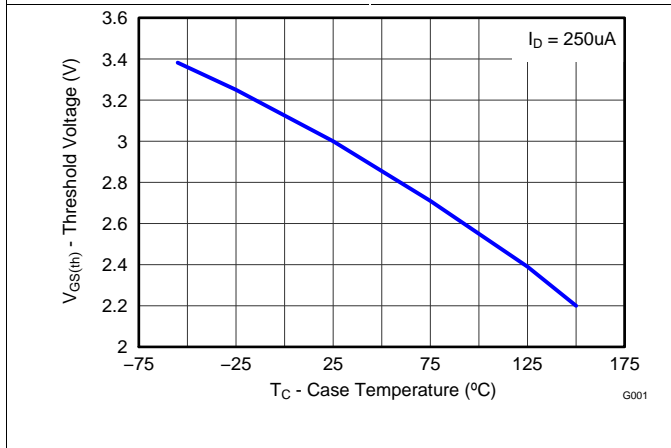
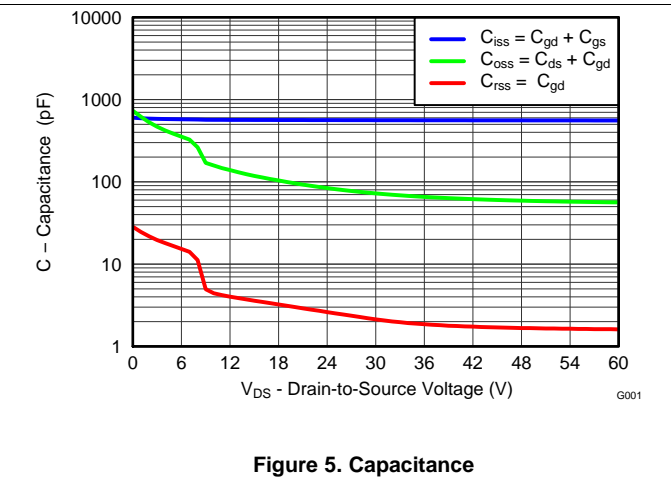
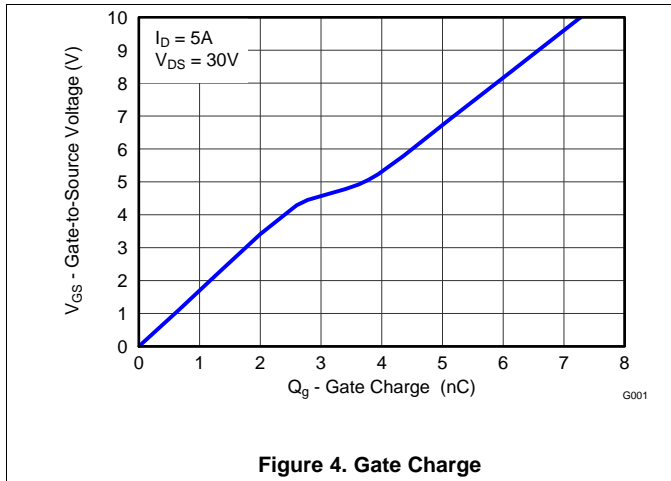


Figure 3. Transfer Characteristics

Typical MOSFET Characteristics (continued)

($T_A = 25^\circ\text{C}$ unless otherwise stated)



Typical MOSFET Characteristics (continued)

($T_A = 25^\circ\text{C}$ unless otherwise stated)

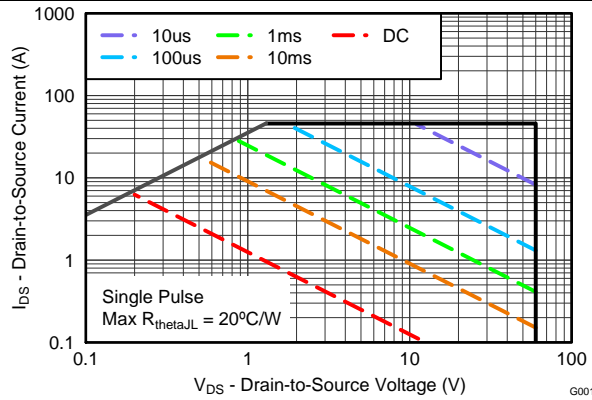


Figure 10. Maximum Safe Operating Area

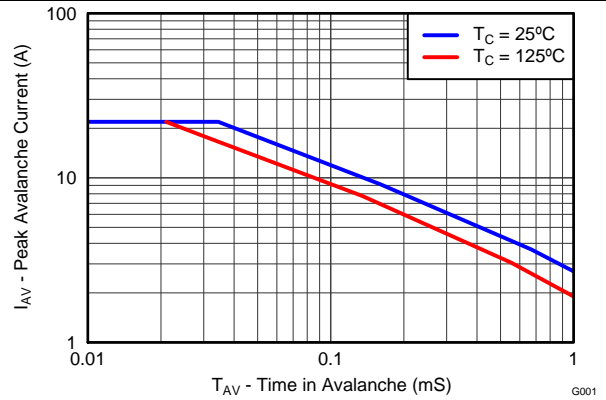


Figure 11. Single Pulse Unclamped Inductive Switching

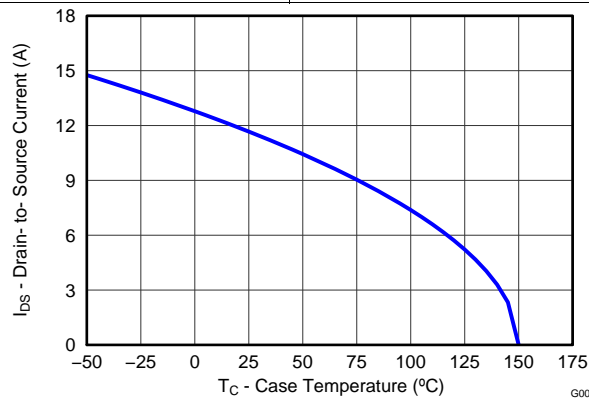
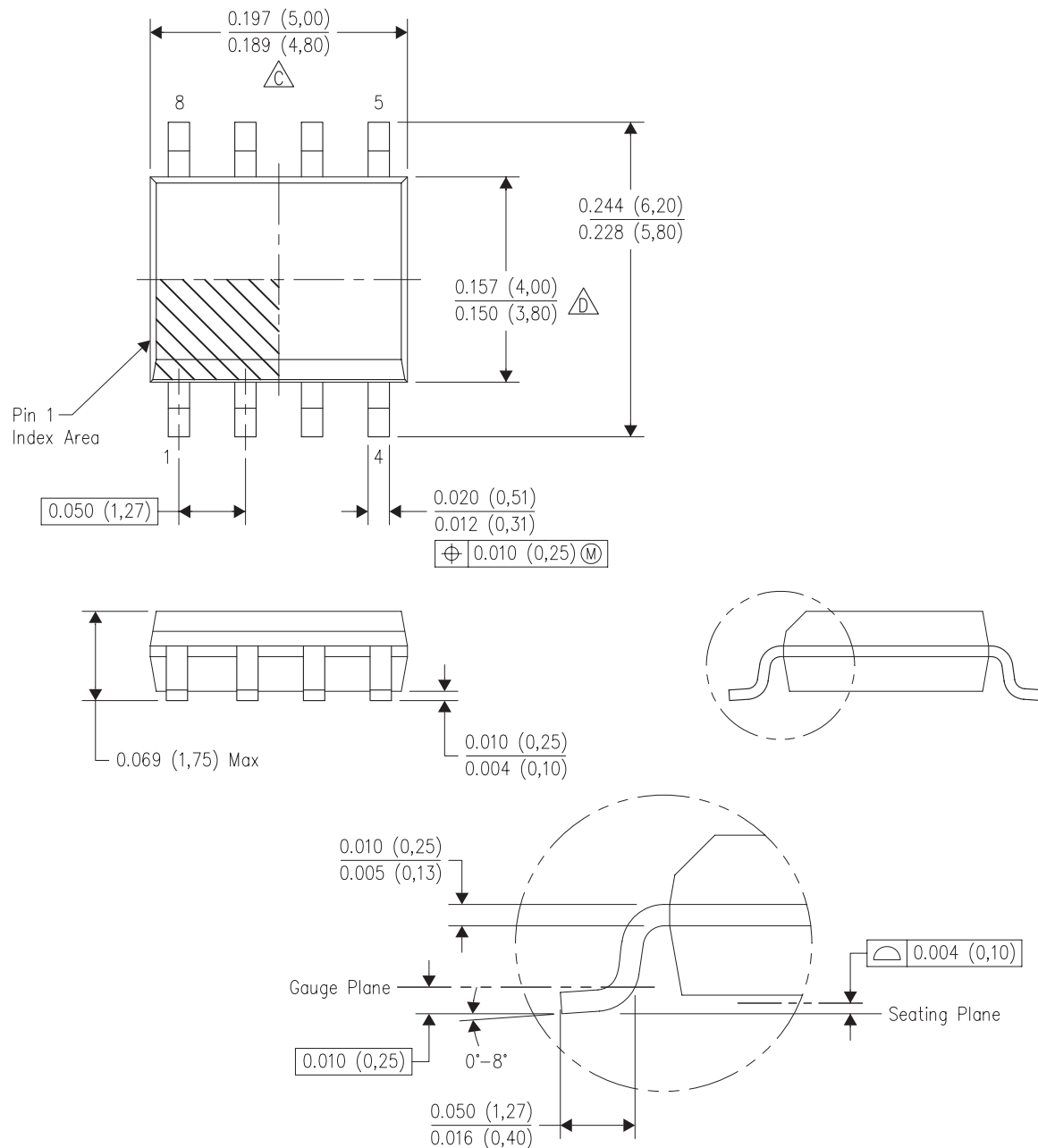


Figure 12. Maximum Drain Current vs Temperature

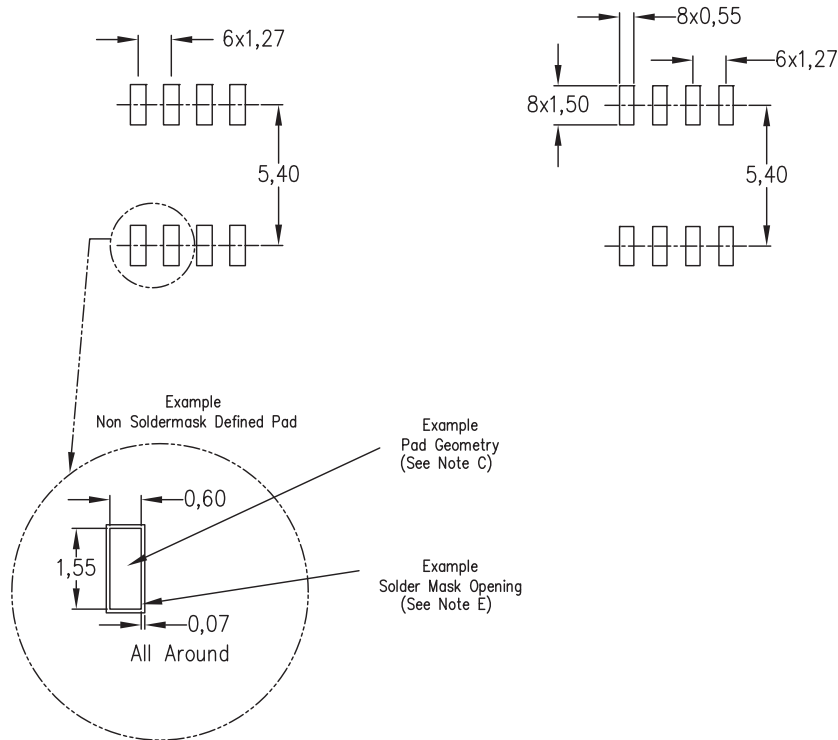
5 Mechanical Data

5.1 SO-8 Package Dimensions



1. All linear dimensions are in inches (millimeters).
2. This drawing is subject to change without notice.
3. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
4. Body width does not include interlead flash. Interlead flas shall not exceed 0.017 (0,43) each side.
5. Reference JEDEC MS-012 variation AA.

5.2 Recommended PCB Pattern and Stencil Opening



1. All linear dimensions are in millimeters.
2. This drawing is subject to change without notice.
3. Publication IPC-7351 is recommended for alternate designs.
4. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
5. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

6 Device and Documentation Support

6.1 Trademarks

NexFET is a trademark of Texas Instruments.

6.2 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD88539ND	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-55 to 150	88539N	Samples
CSD88539NDT	ACTIVE	SOIC	D	8	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-55 to 150	88539N	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CSD88539ND	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
CSD88539NDT	SOIC	D	8	250	178.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CSD88539ND	SOIC	D	8	2500	336.6	336.6	41.3
CSD88539NDT	SOIC	D	8	250	210.0	210.0	52.0

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