

# CSD17578Q5A 30 V N-Channel NexFET™ Power MOSFETs

## 1 Features

- Low  $Q_g$  and  $Q_{gd}$
- Low  $R_{DS(on)}$
- Low Thermal Resistance
- Avalanche Rated
- Pb-Free Terminal Plating
- RoHS Compliant
- Halogen Free
- SON 5 mm x 6 mm Plastic Package

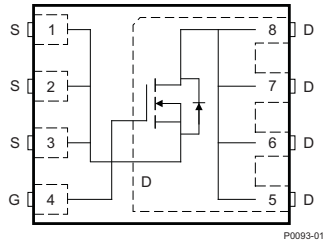
## 2 Applications

- Point-of-Load Synchronous Buck Converter for Applications in Networking, Telecom, and Computing Systems
- Optimized for Control FET Applications

## 3 Description

This 30 V, 5.9 mΩ, SON 5 mm x 6 mm NexFET™ power MOSFET is designed to minimize losses in power conversion applications.

Top View



## Product Summary

$T_A = 25^\circ\text{C}$		TYPICAL VALUE		UNIT
$V_{DS}$	Drain-to-Source Voltage	30		V
$Q_g$	Gate Charge Total (4.5 V)	7.9		nC
$Q_{gd}$	Gate Charge Gate-to-Drain	2.0		nC
$R_{DS(on)}$	Drain-to-Source On-Resistance	$V_{GS} = 4.5\text{ V}$	7.9	mΩ
		$V_{GS} = 10\text{ V}$	5.9	mΩ
$V_{GS(th)}$	Threshold Voltage	1.5		V

## Ordering Information<sup>(1)</sup>

Device	Media	Qty	Package	Ship
CSD17578Q5A	13-Inch Reel	2500	SON 5 x 6 mm Plastic Package	Tape and Reel
CSD17578Q5AT	7-Inch Reel	250		

(1) For all available packages, see the orderable addendum at the end of the data sheet.

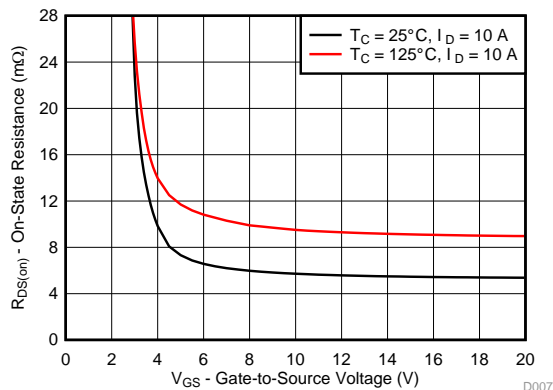
## Absolute Maximum Ratings

$T_A = 25^\circ\text{C}$		VALUE	UNIT
$V_{DS}$	Drain-to-Source Voltage	30	V
$V_{GS}$	Gate-to-Source Voltage	±20	V
$I_D$	Continuous Drain Current (Package limited)	25	A
	Continuous Drain Current (Silicon limited), $T_C = 25^\circ\text{C}$	59	
	Continuous Drain Current <sup>(1)</sup>	16	
$I_{DM}$	Pulsed Drain Current <sup>(2)</sup>	132	A
$P_D$	Power Dissipation <sup>(1)</sup>	3.1	W
	Power Dissipation, $T_C = 25^\circ\text{C}$	42	
$T_J, T_{stg}$	Operating Junction and Storage Temperature Range	-55 to 150	°C
$E_{AS}$	Avalanche Energy, single pulse $I_D = 22\text{ A}, L = 0.1\text{ mH}$	23	mJ

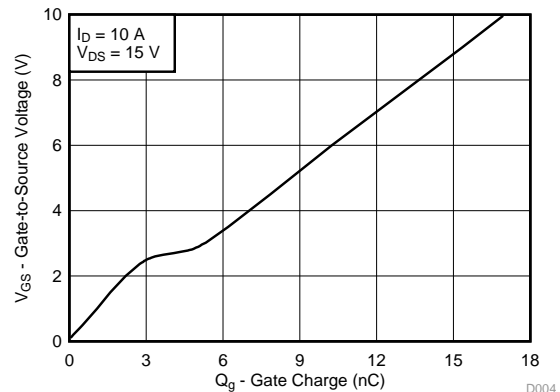
(1) Typical  $R_{\theta JA} = 40^\circ\text{C/W}$  on a 1 inch<sup>2</sup>, 2 oz. Cu pad on a 0.06 inch thick FR4 PCB.

(2) Max  $R_{\theta JC} = 3.8^\circ\text{C/W}$ , pulse duration ≤100 μs, duty cycle ≤1%

$R_{DS(on)}$  vs  $V_{GS}$



Gate Charge



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## 4 Revision History

DATE	REVISION	NOTES
March 2015	*	Initial release.

## 5 Specifications

### 5.1 Electrical Characteristics

( $T_A = 25^\circ\text{C}$  unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>STATIC CHARACTERISTICS</b>						
$V_{DSS}$	Drain-to-Source Voltage	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	30			V
$I_{DSS}$	Drain-to-Source Leakage Current	$V_{GS} = 0\text{ V}, V_{DS} = 24\text{ V}$			1	$\mu\text{A}$
$I_{GSS}$	Gate-to-Source Leakage Current	$V_{DS} = 0\text{ V}, V_{GS} = 20\text{ V}$			100	nA
$V_{GS(th)}$	Gate-to-Source Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	1.1	1.5	1.9	V
$R_{DS(on)}$	Drain-to-Source On-Resistance	$V_{GS} = 4.5\text{ V}, I_D = 10\text{ A}$		7.9	9.3	m $\Omega$
		$V_{GS} = 10\text{ V}, I_D = 10\text{ A}$		5.9	6.9	m $\Omega$
$g_{fs}$	Transconductance	$V_{DS} = 3\text{ V}, I_D = 10\text{ A}$		44		S
<b>DYNAMIC CHARACTERISTICS</b>						
$C_{iss}$	Input Capacitance	$V_{GS} = 0\text{ V}, V_{DS} = 15\text{ V}, f = 1\text{ MHz}$		1170	1510	pF
$C_{oss}$	Output Capacitance			136	177	pF
$C_{rss}$	Reverse Transfer Capacitance			58	75	pF
$R_G$	Series Gate Resistance			1.8	3.6	$\Omega$
$Q_g$	Gate Charge Total (4.5 V)	$V_{DS} = 15\text{ V}, I_D = 10\text{ A}$		7.9	10.3	nC
$Q_g$	Gate Charge Total (10 V)			17.2	22.3	nC
$Q_{gd}$	Gate Charge Gate-to-Drain			2.0		nC
$Q_{gs}$	Gate Charge Gate-to-Source			3.1		nC
$Q_{g(th)}$	Gate Charge at $V_{th}$			1.7		nC
$Q_{oss}$	Output Charge		$V_{DS} = 15\text{ V}, V_{GS} = 0\text{ V}$		4.2	
$t_{d(on)}$	Turn On Delay Time	$V_{DS} = 15\text{ V}, V_{GS} = 10\text{ V}, I_{DS} = 10\text{ A}, R_G = 0\ \Omega$		4		ns
$t_r$	Rise Time			22		ns
$t_{d(off)}$	Turn Off Delay Time			17		ns
$t_f$	Fall Time			2		ns
<b>DIODE CHARACTERISTICS</b>						
$V_{SD}$	Diode Forward Voltage	$I_{SD} = 10\text{ A}, V_{GS} = 0\text{ V}$		0.8	1.0	V
$Q_{rr}$	Reverse Recovery Charge	$V_{DS} = 15\text{ V}, I_F = 10\text{ A}, di/dt = 300\text{ A}/\mu\text{s}$		6.5		nC
$t_{rr}$	Reverse Recovery Time			6.8		ns

### 5.2 Thermal Information

( $T_A = 25^\circ\text{C}$  unless otherwise stated)

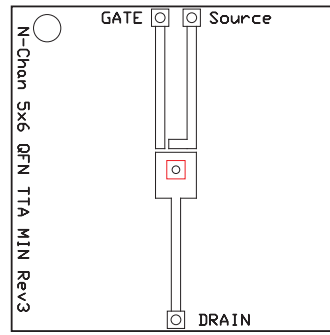
THERMAL METRIC		MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Junction-to-Case Thermal Resistance <sup>(1)</sup>			3.8	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Junction-to-Ambient Thermal Resistance <sup>(1)(2)</sup>			50	

- (1)  $R_{\theta JC}$  is determined with the device mounted on a 1 inch<sup>2</sup> (6.45 cm<sup>2</sup>), 2 oz. (0.071 mm thick) Cu pad on a 1.5 inch x 1.5 inch (3.81 cm x 3.81 cm), 0.06 inch (1.52 mm) thick FR4 PCB.  $R_{\theta JC}$  is specified by design, whereas  $R_{\theta JA}$  is determined by the user's board design.
- (2) Device mounted on FR4 material with 1 inch<sup>2</sup> (6.45 cm<sup>2</sup>), 2 oz. (0.071 mm thick) Cu.



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Max  $R_{\theta JA} = 50^{\circ}\text{C/W}$   
when mounted on  
1 inch<sup>2</sup> (6.45 cm<sup>2</sup>) of  
2 oz. (0.071 mm thick)  
Cu.



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Max  $R_{\theta JA} = 140^{\circ}\text{C/W}$   
when mounted on a  
minimum pad area of  
2 oz. (0.071 mm thick)  
Cu.

### 5.3 Typical MOSFET Characteristics

( $T_A = 25^{\circ}\text{C}$  unless otherwise stated)

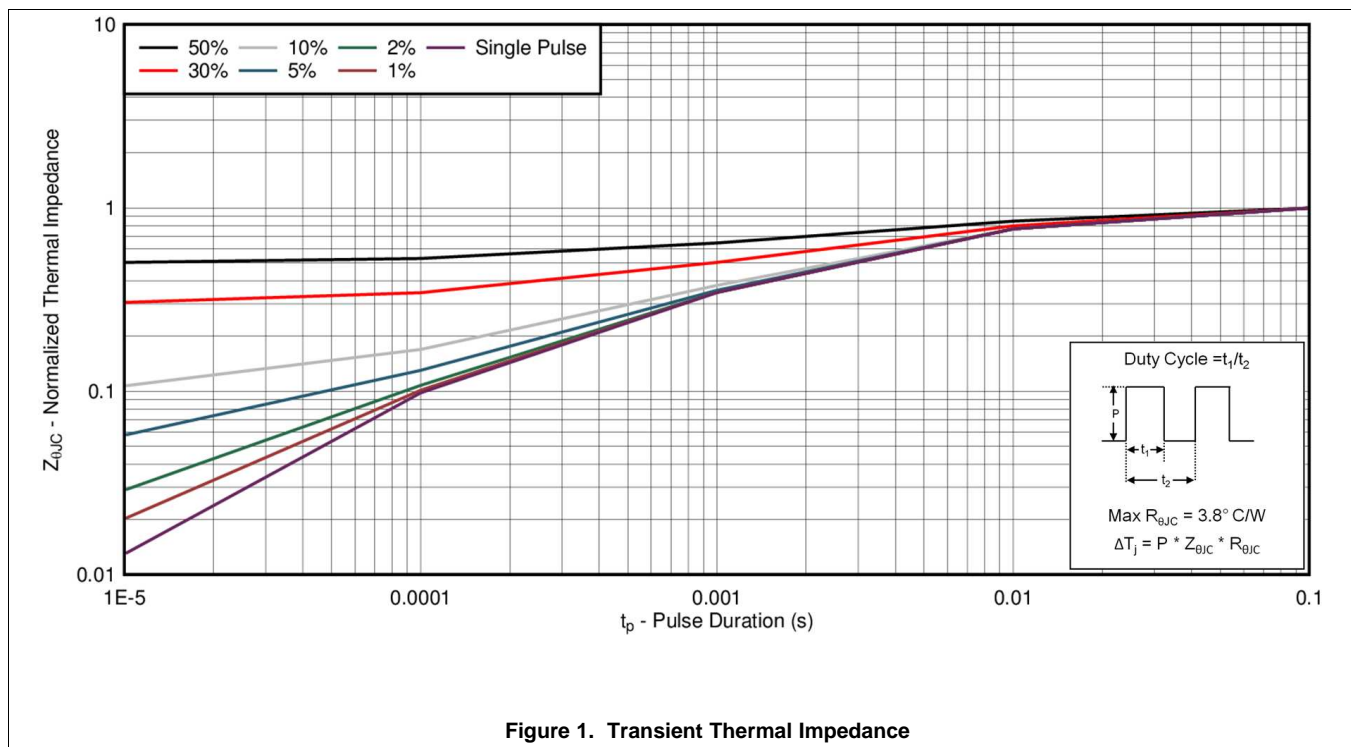


Figure 1. Transient Thermal Impedance

Typical MOSFET Characteristics (continued)

( $T_A = 25^\circ\text{C}$  unless otherwise stated)

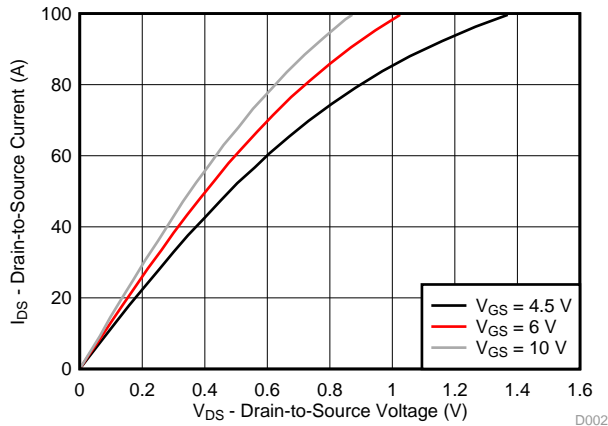


Figure 2. Saturation Characteristics

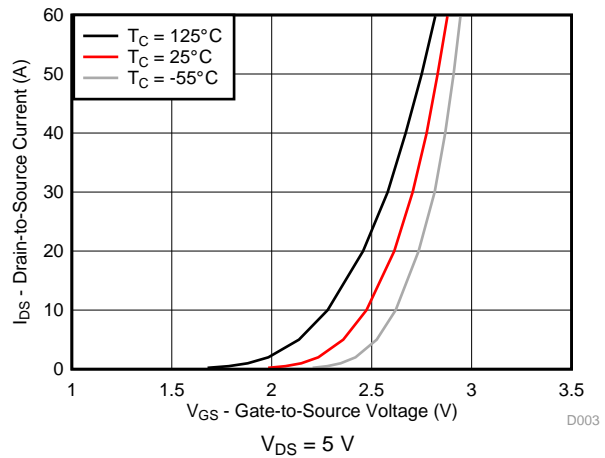


Figure 3. Transfer Characteristics

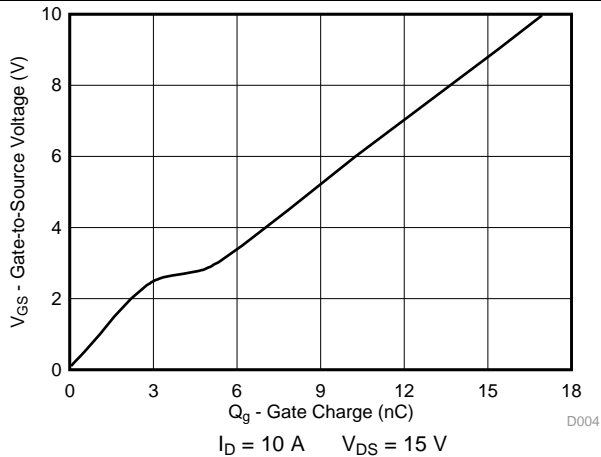


Figure 4. Gate Charge

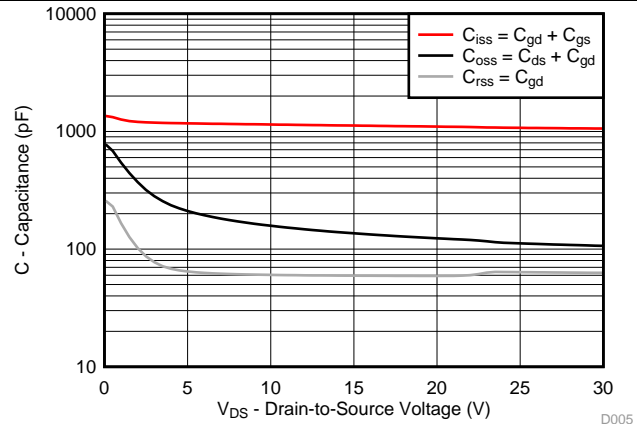


Figure 5. Capacitance

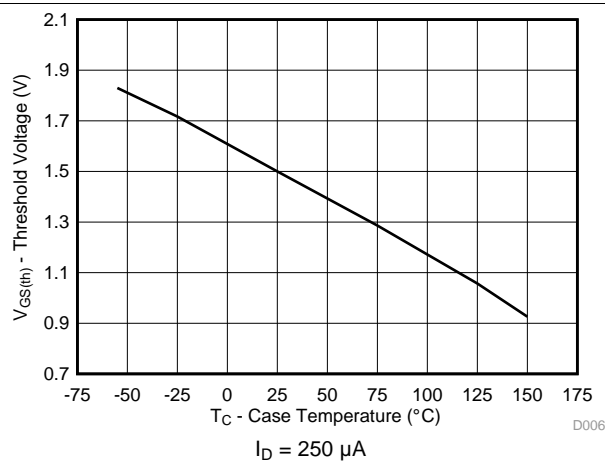


Figure 6. Threshold Voltage vs Temperature

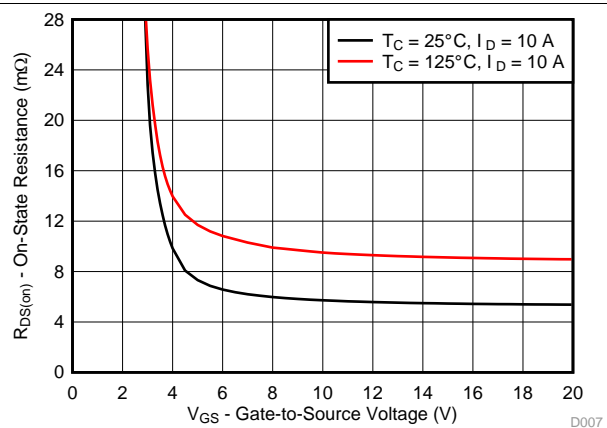


Figure 7. On-State Resistance vs Gate-to-Source Voltage

Typical MOSFET Characteristics (continued)

( $T_A = 25^\circ\text{C}$  unless otherwise stated)

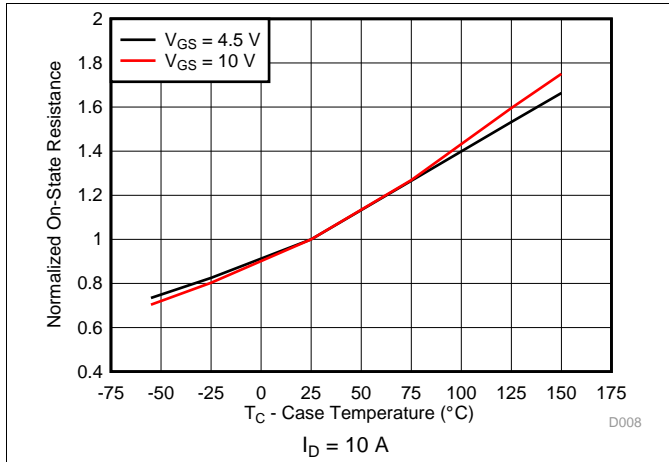


Figure 8. Normalized On-State Resistance vs Temperature

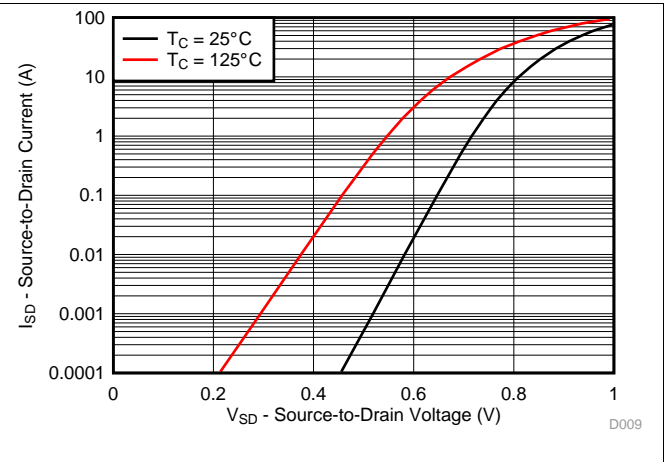


Figure 9. Typical Diode Forward Voltage

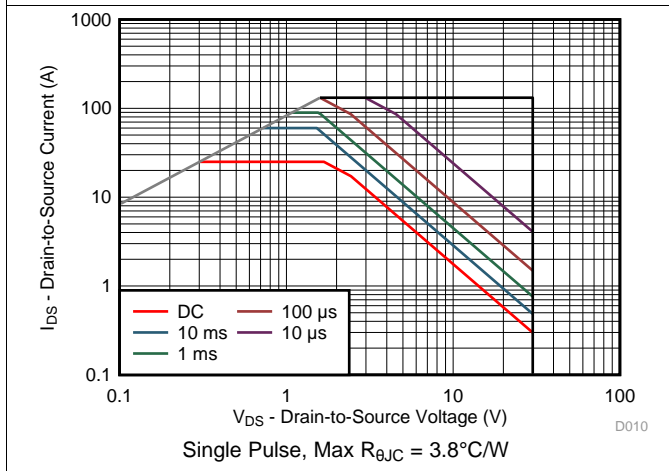


Figure 10. Maximum Safe Operating Area

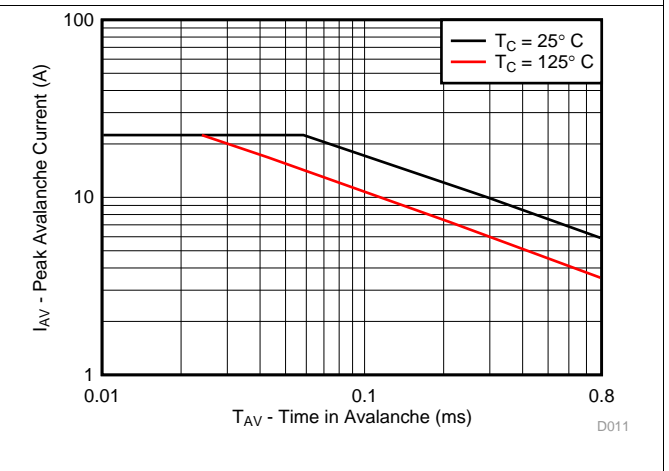


Figure 11. Single Pulse Unclamped Inductive Switching

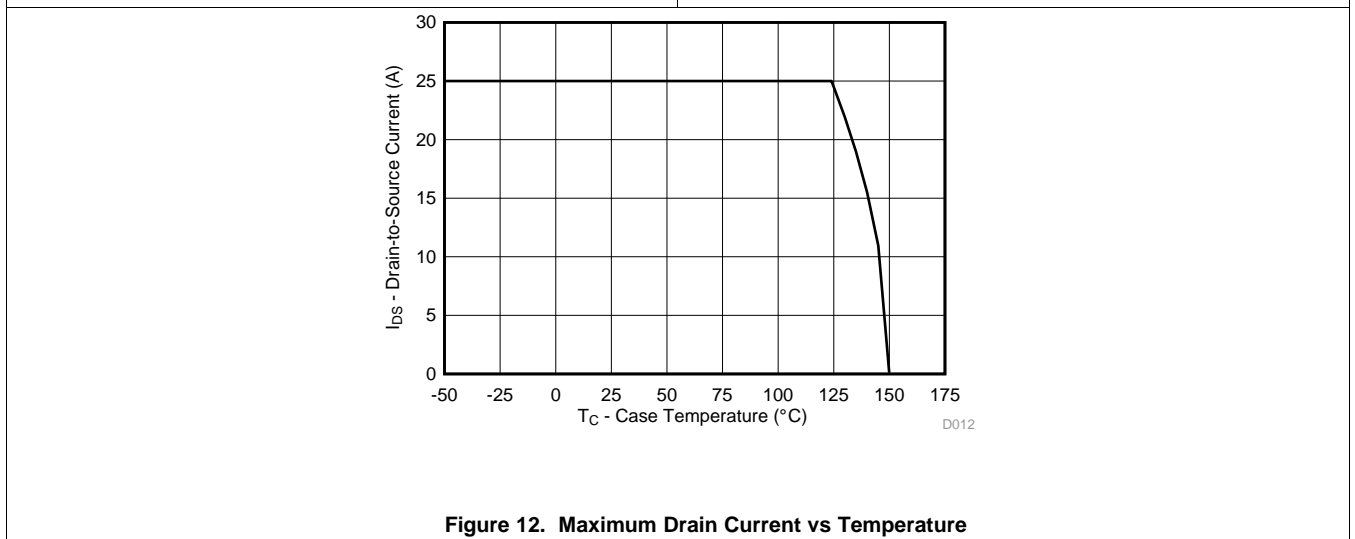


Figure 12. Maximum Drain Current vs Temperature

## 6 Device and Documentation Support

### 6.1 Trademarks

NexFET is a trademark of Texas Instruments.  
All other trademarks are the property of their respective owners.

### 6.2 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 6.3 Glossary

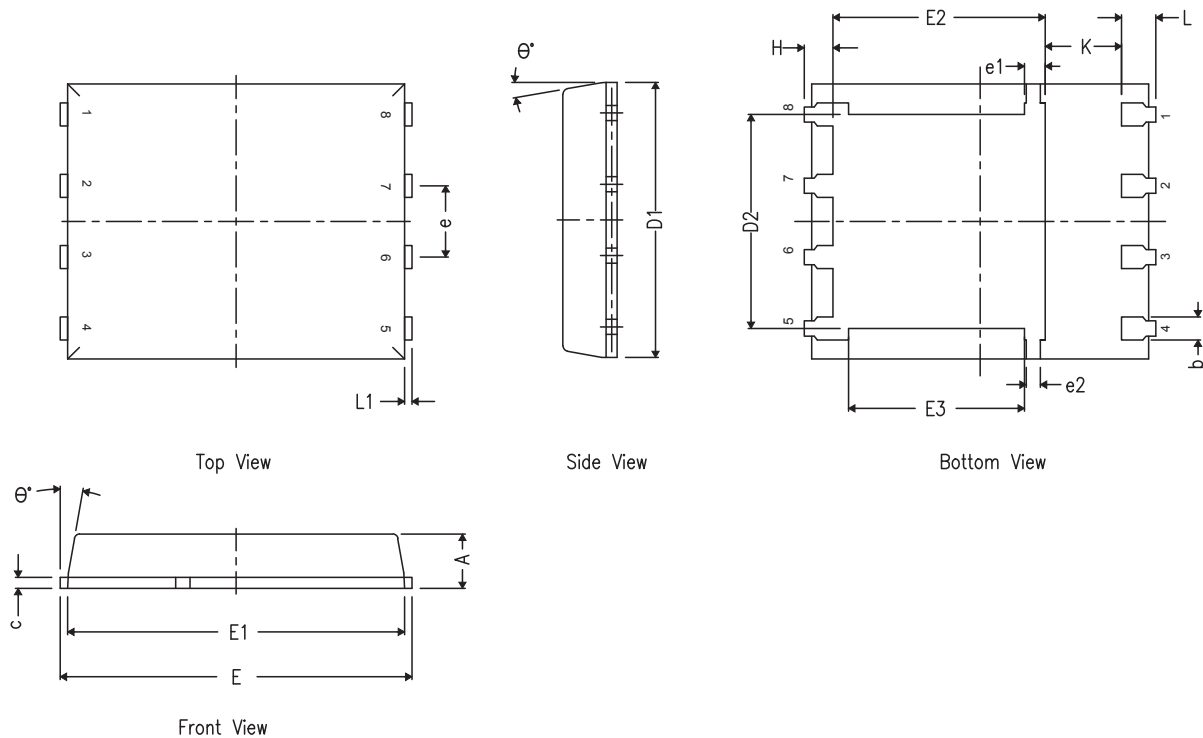
[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 7 Mechanical, Packaging, and Orderable Information

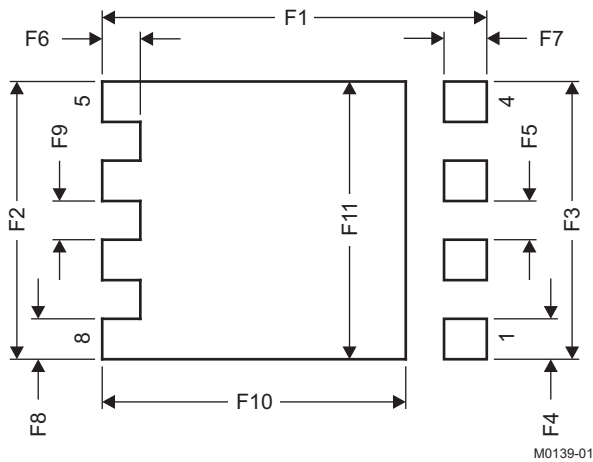
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

### 7.1 Q5A Package Dimensions



DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.90	1.00	1.10
b	0.33	0.41	0.51
c	0.20	0.25	0.34
D1	4.80	4.90	5.00
D2	3.61	3.81	4.02
E	5.90	6.00	6.10
E1	5.70	5.75	5.80
E2	3.38	3.58	3.78
E3	3.03	3.13	3.23
e	1.17	1.27	1.37
e1	0.27	0.37	0.47
e2	0.15	0.25	0.35
H	0.41	0.56	0.71
K	1.10		
L	0.51	0.61	0.71
L1	0.06	0.13	0.20
$\theta$	0°		12°

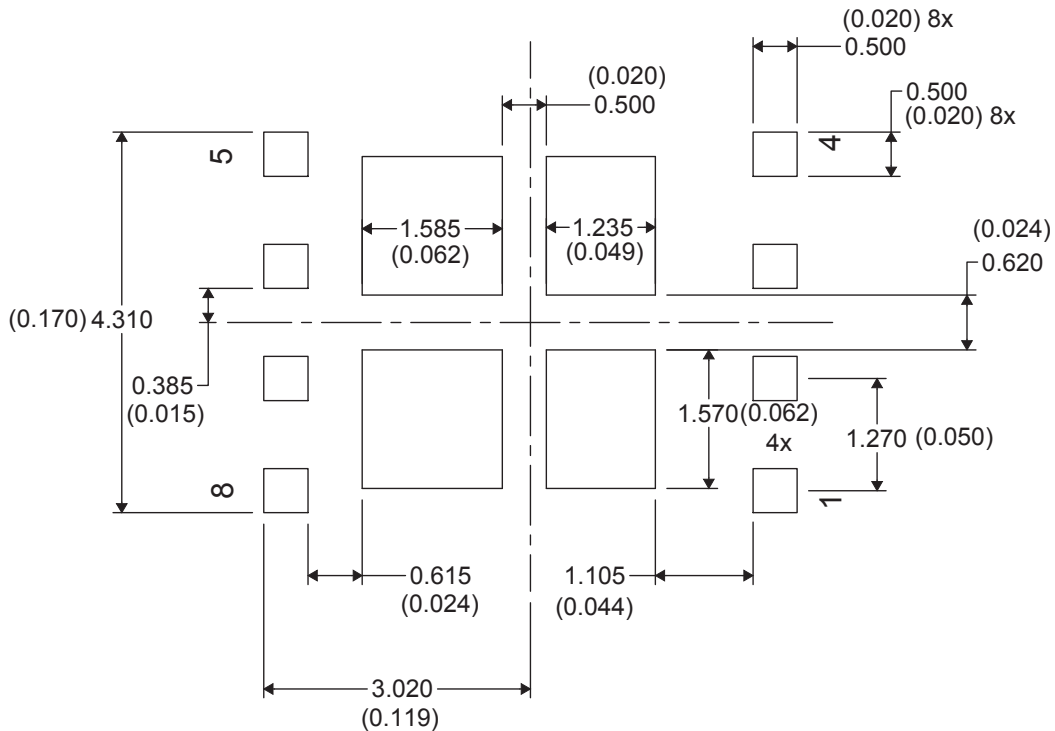
## 7.2 Recommended PCB Pattern



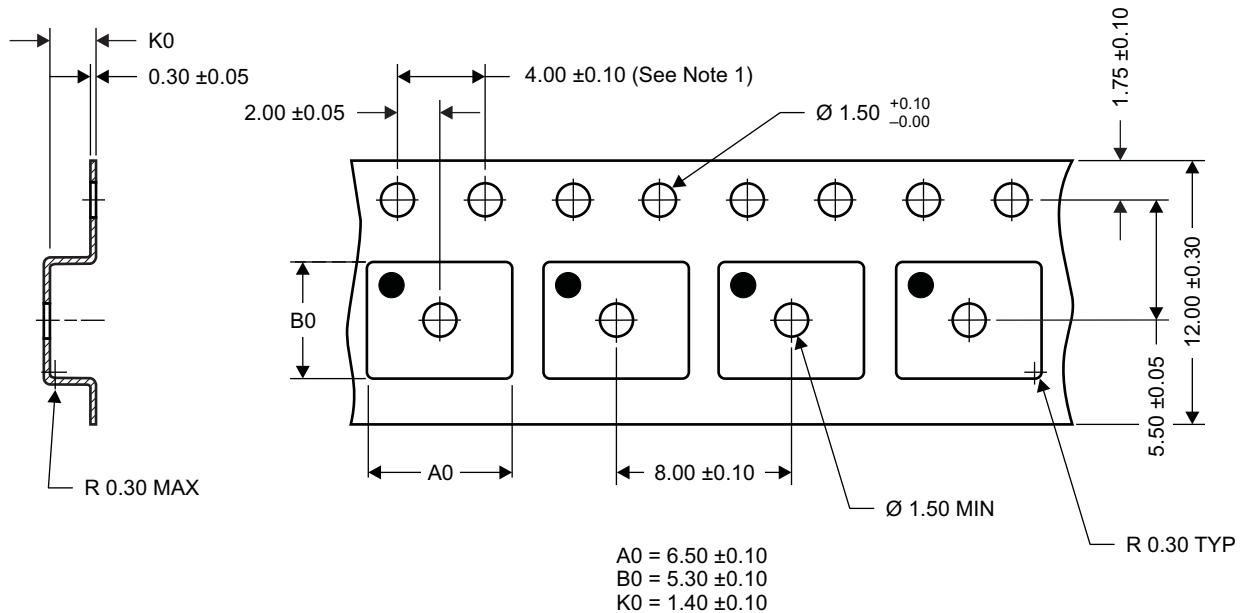
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
F1	6.205	6.305	0.244	0.248
F2	4.46	4.56	0.176	0.18
F3	4.46	4.56	0.176	0.18
F4	0.65	0.7	0.026	0.028
F5	0.62	0.67	0.024	0.026
F6	0.63	0.68	0.025	0.027
F7	0.7	0.8	0.028	0.031
F8	0.65	0.7	0.026	0.028
F9	0.62	0.67	0.024	0.026
F10	4.9	5	0.193	0.197
F11	4.46	4.56	0.176	0.18

For recommended circuit layout for PCB designs, see application note [SLPA005](#) – *Reducing Ringing Through PCB Layout Techniques*.

### 7.3 Recommended Stencil Opening



### 7.4 Q5A Tape and Reel Information



#### Notes:

- 10-sprocket hole-pitch cumulative tolerance ±0.2
- Camber not to exceed 1 mm in 100 mm, noncumulative over 250 mm
- Material: black static-dissipative polystyrene
- All dimensions are in mm (unless otherwise specified)
- A0 and B0 measured on a plane 0.3 mm above the bottom of the pocket

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**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD17578Q5A	ACTIVE	VSONP	DQJ	8	2500	Pb-Free (RoHS Exempt)	SN	Level-1-260C-UNLIM		CSD17578	<a href="#">Samples</a>
CSD17578Q5AT	ACTIVE	VSONP	DQJ	8	250	Pb-Free (RoHS Exempt)	SN	Level-1-260C-UNLIM	-55 to 150	CSD17578	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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