MICROPOWER DC VOLTAGE DETECTOR

GENERAL DESCRIPTION

The PCF1251 is a CMOS micropower DC voltage detector and it is especially designed for power-on/off voltage detection monitoring and reset. The IC has an extremely low current consumption and is therefore particularly suited for battery operated applications. The internal bandgap reference voltage is stable with temperature variations. The voltage trip-point and the hysteresis can be set independently with external resistors. Two of the four outputs can be delayed with an external capacitor.

Features

- Extremely low current consumption
- Built-in bandgap voltage reference
- Wide range of voltage trip-points
- Two pairs of outputs; one pair with delay possibility
- 8-lead DIL or SO8 mini-pack (plastic packages).

QUICK REFERENCE DATA

parameter	symbol	min.	typ.	max.	unit
Supply voltage range with respect to V_{SS}	V_{DD}	1	–	6	V
Supply current	I_{DD}	–	1	–	μA
Output currents at V_{DD} = 1 V	I_O	–	2	–	mA
Bandgap voltage reference at 25 °C	V_{REF}	1,05	1,15	1,25	V

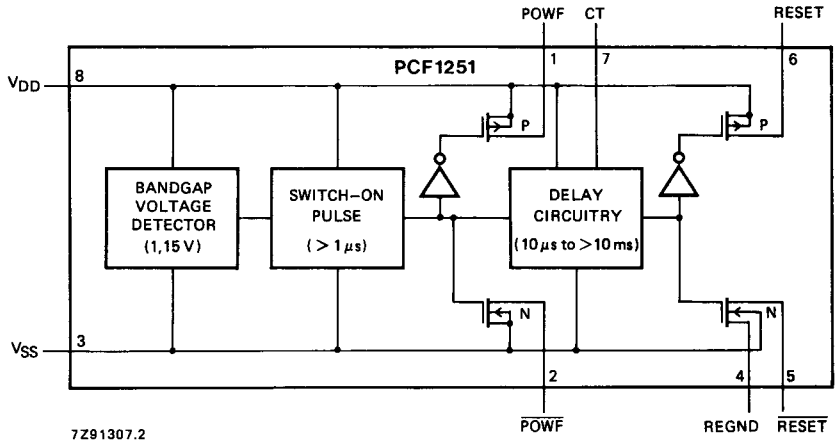


Fig. 1 Block diagram.

PACKAGE OUTLINES

PCF1251P: 8-lead DIL; plastic (SOT97).
PCF1251T: 8-lead mini-pack; plastic (SO8; SOT96A).

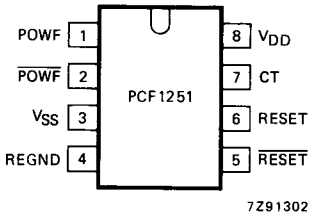


Fig. 2 Pinning diagram.

PINNING

1	POWF	power-fail output
2	$\overline{\text{POWF}}$	power-fail output (inverted)
3	V_{SS}	negative supply voltage
4	REGND	reset ground
5	$\overline{\text{RESET}}$	reset output (inverted; delayed)
6	RESET	reset output (delayed)
7	CT	capacitor for additional delay
8	V_{DD}	positive supply voltage

FUNCTIONAL DESCRIPTION

The PCF1251 consists of a bandgap voltage reference, a comparator and delay circuitry (see Fig. 1). The supply voltage of the circuit (V_{DD} with respect to V_{SS}) is compared with an internal bandgap voltage reference by means of a special comparator. This comparator is connected to the circuit supply voltage. As long as the supply voltage is above the reference voltage level, the four open-drain outputs are all switched off and an extended drain-source voltage of up to 6 V is allowed. When the supply voltage is reduced and reaches the reference voltage level (V_{REF}), the power-fail outputs are switched on (p-channel for POWF and n-channel for $\overline{\text{POWF}}$ outputs). After a delay, determined by an external capacitor between pins CT and V_{DD}, the outputs RESET and $\overline{\text{RESET}}$ are switched on. The same delay will be active when the supply voltage is increased again and exceeds the internal voltage reference, resulting in switching off the outputs.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage with respect to V_{SS}	V_{DD}	–	8	V
Output voltage at pin 2 V_{DD} with respect to V_2	V_2	–	8	V
Output voltage at pin 5 (pin 4 at V_{SS}) V_{DD} with respect to V_5	V_5	–	8	V
Output voltage at pin 1 V_1 with respect to V_{SS}	V_1	–	8	V
Output voltage at pin 6 V_6 with respect to V_{SS}	V_6	–	8	V
Voltage at pin 7 (CT)	V_7	−0,5	V_{DD} + 0,5	V
Current at pin 7 (CT)	I_7	–	20	mA
Output currents at pins 1, 2, 5 and 6	$\lvert I_O \rvert$	–	25	mA
Total power dissipation	P_{tot}	–	150	mW
Operating ambient temperature range	T_{amb}	−40	+85	°C
Storage temperature range	T_{stg}	−55	+125	°C

HANDLING

Inputs and outputs are protected against electrostatic charge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see 'Handling MOS Devices').

CHARACTERISTICS

V_{DD} = 1 to 6 V; V_{SS} = 0 V; T_{amb} = −40 to + 85 °C; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Operating supply voltage	V_{DD}	1	–	6	V
Operating supply current V_{DD} = 6 V; all outputs open	I_{DD}	–	1	3	μA
Bandgap voltage reference; T_{amb} = 25 °C	V_{REF}	1,05	1,15	1,25	V
V_{REF} temperature coefficient	$\Delta V_{REF}/\Delta T$	–	−0,4	–	mV/K
Output current at pins 2 and 5 T_{amb} = 25 °C; $V_{DD} < V_{REF}$; V_O = 0,4 V with respect to V_{SS}	I_O	1	2	–	mA
Output current at pins 1 and 6 T_{amb} = 25 °C; $V_{DD} < V_{REF}$; $-V_O$ = 0,4 V with respect to V_{DD}	$-I_O$	1	2	–	mA

(1) For correct switching of the outputs the slew rate of the supply voltage should be less than 1 V/ms.

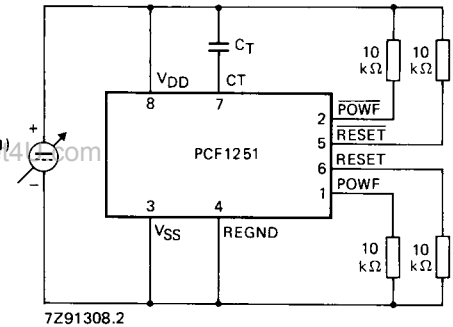


Fig. 3 Test circuit for timing measurements.

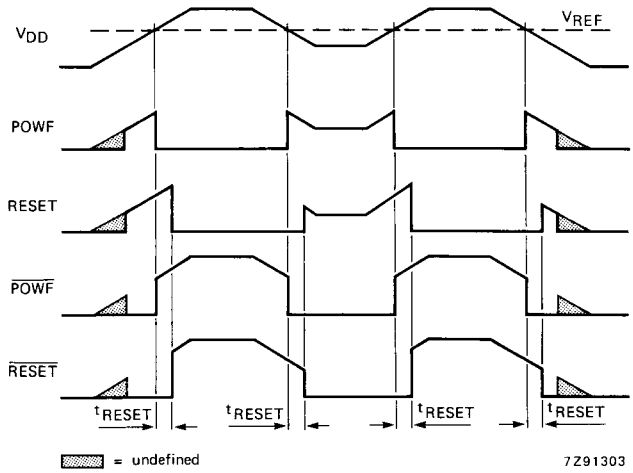


Fig. 4 Timing diagram for slow supply voltage changes.

(1) at T_{amb} = 25 °C

a) $C_T < 0.1$ nF: 10 µs < t_{RESET} < 750 µs

b) $C_T \geqslant 0.1$ nF: t_{RESET} = $\left[0{,}1 + 3{,}2 \text{ ms} \times C_T\left(\frac{\text{nF}}{\text{nF}}\right)\right]^{+75\%}_{-50\%}$

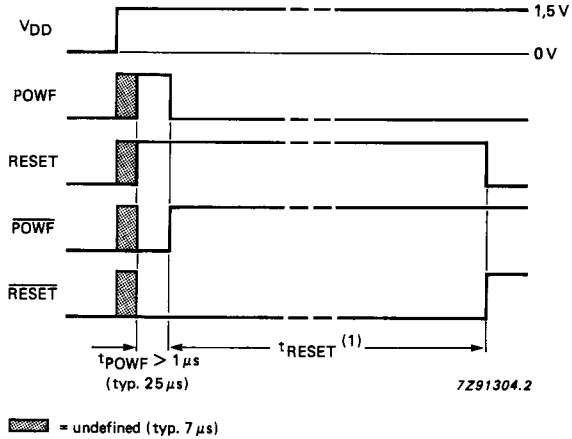


Fig. 5 Timing diagram for fast supply voltage switching on (non-repetitive).

APPLICATION INFORMATION

(1) The value of capacitor C is chosen to limit the slew rate of the supply voltage to less than 1 V/ms (e.g. the hysteresis voltage step on resistor R3).

(2) CT (pin 7) is a high-impedance connection for the capacitor C_T. This capacitor adds to the reset delay time provided by an internal current source (120 nA) and capacitor. Care must be taken to avoid external leakage current at this pin but the pin should not be left open circuit as stray capacitances to V_{SS} can then disturb the delay function.

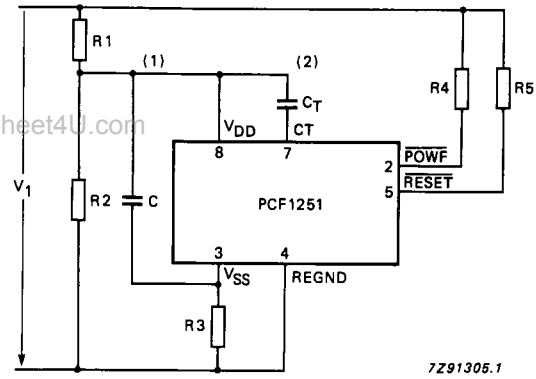
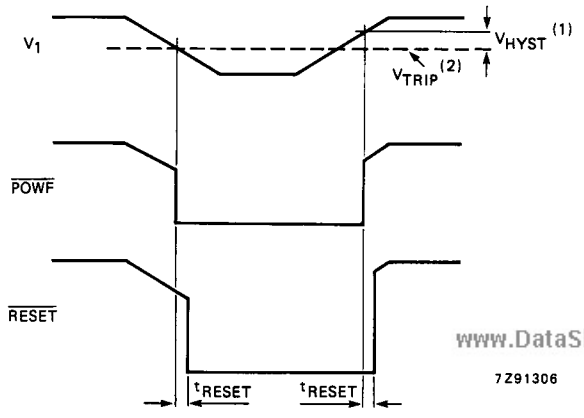


Fig. 6 Application circuit diagram.



(1) $V_{HYST} = V_{TRIP} \times \frac{R3}{R3 + R4}$; (0,2 V max.)

(2) $V_{TRIP} = V_{REF} \times \frac{R1 + R2}{R2}$

Fig. 7 Timing diagram for the circuit of Fig. 6.