

# SN54HCT541, SN74HCT541 OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

SCLS306C – JANUARY 1996 – REVISED AUGUST 2003

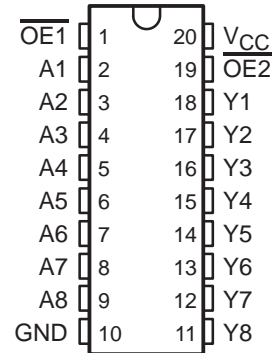
- Operating Voltage Range of 4.5 V to 5.5 V
- High-Current 3-State Outputs Interface Directly With System Bus or Can Drive Up To 15 LSTTL Loads
- Low Power Consumption, 80- $\mu$ A Max  $I_{CC}$
- Typical  $t_{pd} = 12$  ns
- $\pm 6$ -mA Output Drive at 5 V
- Low Input Current of 1  $\mu$ A Max
- Inputs Are TTL-Voltage Compatible
- Data Flow-Through Pinout (All Inputs on Opposite Side From Outputs)

## description/ordering information

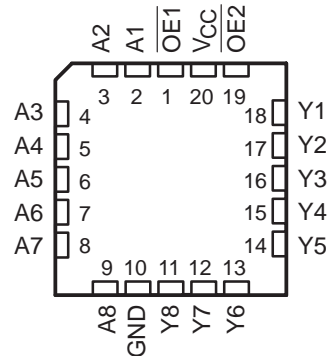
These octal buffers and line drivers are designed to have the performance of the popular 'HC240 series devices and to offer a pinout with inputs and outputs on opposite sides of the package. This arrangement greatly facilitates printed circuit board layout.

The 3-state control gate is a 2-input NOR. If either output-enable ( $\overline{OE}1$  or  $\overline{OE}2$ ) input is high, all eight outputs are in the high-impedance state. The 'HCT541 devices provide true data at the outputs.

## SN54HCT541 . . . J OR W PACKAGE SN74HCT541 . . . DB, DW, N, NS, OR PW PACKAGE (TOP VIEW)



## SN54HCT541 . . . FK PACKAGE (TOP VIEW)



## ORDERING INFORMATION

| TA             | PACKAGE†   |               | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|----------------|------------|---------------|-----------------------|------------------|
| -40°C to 85°C  | PDIP – N   | Tube of 20    | SN74HCT541N           | SN74HCT541N      |
|                | SOIC – DW  | Tube of 25    | SN74HCT541DW          | HCT541           |
|                |            | Reel of 2000  | SN74HCT541DWR         |                  |
|                | SOP – NS   | Reel of 2000  | SN74HCT541NSR         | HCT541           |
|                | SSOP – DB  | Reel of 2000  | SN74HCT541DBR         | HT541            |
|                | TSSOP – PW | Tube of 70    | SN74HCT541PW          | HT541            |
| Reel of 2000   |            | SN74HCT541PWR |                       |                  |
| Reel of 250    |            | SN74HCT541PWT |                       |                  |
| -55°C to 125°C | CDIP – J   | Tube of 20    | SNJ54HCT541J          | SNJ54HCT541J     |
|                | CFP – W    | Tube of 85    | SNJ54HCT541W          | SNJ54HCT541W     |
|                | LCCC – FK  | Tube of 55    | SNJ54HCT541FK         | SNJ54HCT541FK    |

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS  
INSTRUMENTS**

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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

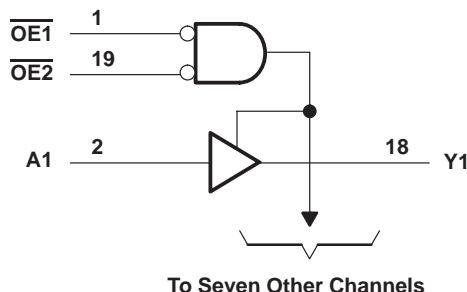
# SN54HCT541, SN74HCT541 OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

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FUNCTION TABLE  
(each buffer/driver)

| INPUTS           |                  |   | OUTPUT |
|------------------|------------------|---|--------|
| $\overline{OE1}$ | $\overline{OE2}$ | A | Y      |
| L                | L                | L | L      |
| L                | L                | H | H      |
| H                | X                | X | Z      |
| X                | H                | X | Z      |

## logic diagram (positive logic)



## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

|   |                |
|---|----------------|
| Supply voltage range, $V_{CC}$ .....  | -0.5 V to 7 V  |
| Input clamp current, $I_{IK}$ ( $V_I < 0$ or $V_I > V_{CC}$ ) (see Note 1) .....  | $\pm 20$ mA    |
| Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ ) (see Note 1) ..... | $\pm 20$ mA    |
| Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ ) .....                  | $\pm 35$ mA    |
| Continuous current through $V_{CC}$ or GND .....                                  | $\pm 70$ mA    |
| Package thermal impedance, $\theta_{JA}$ (see Note 2):                            |                |
| DB package .....  | 70°C/W         |
| DW package .....  | 58°C/W         |
| N package .....   | 69°C/W         |
| NS package .....  | 60°C/W         |
| PW package .....  | 83°C/W         |
| Storage temperature range, $T_{stg}$ .....  | -65°C to 150°C |

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.  
2. The package thermal impedance is calculated in accordance with JESD 51-7.

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## recommended operating conditions (see Note 3)

|                 |                                 | SN54HCT541                       |                 |     | SN74HCT541 |                 |     | UNIT |
|-----------------|---------------------------------|----------------------------------|-----------------|-----|------------|-----------------|-----|------|
|                 |                                 | MIN                              | NOM             | MAX | MIN        | NOM             | MAX |      |
| V <sub>CC</sub> | Supply voltage                  | 4.5                              | 5               | 5.5 | 4.5        | 5               | 5.5 | V    |
| V <sub>IH</sub> | High-level input voltage        | V <sub>CC</sub> = 4.5 V to 5.5 V |                 |     | 2          |                 |     | V    |
| V <sub>IL</sub> | Low-level input voltage         | V <sub>CC</sub> = 4.5 V to 5.5 V |                 |     | 0.8        |                 |     | V    |
| V <sub>I</sub>  | Input voltage                   | 0                                | V <sub>CC</sub> |     | 0          | V <sub>CC</sub> |     | V    |
| V <sub>O</sub>  | Output voltage                  | 0                                | V <sub>CC</sub> |     | 0          | V <sub>CC</sub> |     | V    |
| Δt/Δv           | Input transition rise/fall time | 500                              |                 |     | 500        |                 |     | ns   |
| T <sub>A</sub>  | Operating free-air temperature  | -55                              | 125             |     | -40        | 85              |     | °C   |

NOTE 3: All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER          | TEST CONDITIONS  |                          | V <sub>CC</sub> | T <sub>A</sub> = 25°C |       |      | SN54HCT541 |       | SN74HCT541 |       | UNIT |
|--------------------|--|--------------------------|-----------------|-----------------------|-------|------|------------|-------|------------|-------|------|
|                    |  |                          |                 | MIN                   | TYP   | MAX  | MIN        | MAX   | MIN        | MAX   |      |
| V <sub>OH</sub>    | V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>  | I <sub>OH</sub> = -20 μA | 4.5 V           | 4.4                   | 4.499 |      | 4.4        |       | 4.4        | V     |      |
|                    |  | I <sub>OH</sub> = -6 mA  |                 | 3.98                  | 4.3   |      | 3.7        |       | 3.84       |       |      |
| V <sub>OL</sub>    | V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>  | I <sub>OL</sub> = 20 μA  | 4.5 V           |                       | 0.001 | 0.1  |            | 0.1   |            | 0.1   | V    |
|                    |  | I <sub>OL</sub> = 6 mA   |                 |                       | 0.17  | 0.26 |            | 0.4   |            | 0.33  |      |
| I <sub>I</sub>     | V <sub>I</sub> = V <sub>CC</sub> or 0  |                          | 5.5 V           |                       | ±0.1  | ±100 |            | ±1000 |            | ±1000 | nA   |
| I <sub>OZ</sub>    | V <sub>O</sub> = V <sub>CC</sub> or 0, V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> |                          | 5.5 V           |                       | ±0.01 | ±0.5 |            | ±10   |            | ±5    | μA   |
| I <sub>CC</sub>    | V <sub>I</sub> = V <sub>CC</sub> or 0, I <sub>O</sub> = 0                                  |                          | 5.5 V           |                       |       | 8    |            | 160   |            | 80    | μA   |
| ΔI <sub>CC</sub> † | One input at 0.5 V or 2.4 V, Other inputs at 0 or V <sub>CC</sub>                          |                          | 5.5 V           |                       | 1.4   | 2.4  |            | 3     |            | 2.9   | mA   |
| C <sub>i</sub>     |  |                          | 4.5 V to 5.5 V  |                       | 3     | 10   |            | 10    |            | 10    | pF   |

† This is the increase in supply current for each input that is at one of the specified TTL voltage levels, rather than 0 V or V<sub>CC</sub>.

## switching characteristics over recommended operating free-air temperature range, C<sub>L</sub> = 50 pF (unless otherwise noted) (see Figure 1)

| PARAMETER        | FROM (INPUT)           | TO (OUTPUT) | V <sub>CC</sub> | T <sub>A</sub> = 25°C |     |     | SN54HCT541 |     | SN74HCT541 |     | UNIT |
|------------------|------------------------|-------------|-----------------|-----------------------|-----|-----|------------|-----|------------|-----|------|
|                  |                        |             |                 | MIN                   | TYP | MAX | MIN        | MAX | MIN        | MAX |      |
| t <sub>pd</sub>  | A                      | Y           | 4.5 V           |                       | 13  | 23  |            | 34  |            | 29  | ns   |
|                  |                        |             | 5.5 V           |                       | 12  | 21  |            | 31  |            | 26  |      |
| t <sub>en</sub>  | $\overline{\text{OE}}$ | Y           | 4.5 V           |                       | 21  | 30  |            | 45  |            | 38  | ns   |
|                  |                        |             | 5.5 V           |                       | 19  | 27  |            | 41  |            | 34  |      |
| t <sub>dis</sub> | $\overline{\text{OE}}$ | Y           | 4.5 V           |                       | 19  | 30  |            | 45  |            | 38  | ns   |
|                  |                        |             | 5.5 V           |                       | 18  | 27  |            | 41  |            | 34  |      |
| t <sub>t</sub>   |                        | Y           | 4.5 V           |                       | 8   | 12  |            | 18  |            | 15  | ns   |
|                  |                        |             | 5.5 V           |                       | 7   | 11  |            | 16  |            | 14  |      |



**SN54HCT541, SN74HCT541**  
**OCTAL BUFFERS AND LINE DRIVERS**  
**WITH 3-STATE OUTPUTS**

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switching characteristics over recommended operating free-air temperature range,  $C_L = 150 \text{ pF}$   
(unless otherwise noted) (see Figure 1)

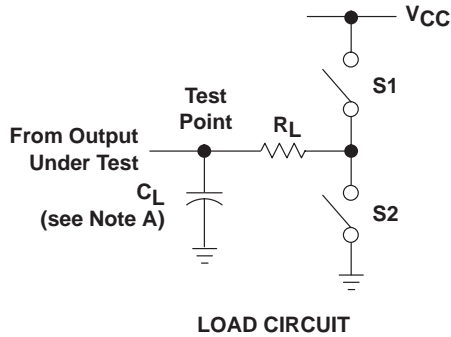
| PARAMETER | FROM<br>(INPUT) | TO<br>(OUTPUT) | $V_{CC}$ | $T_A = 25^\circ\text{C}$ |     |     | SN54HCT541 |     | SN74HCT541 |     | UNIT |
|-----------|-----------------|----------------|----------|--------------------------|-----|-----|------------|-----|------------|-----|------|
|           |                 |                |          | MIN                      | TYP | MAX | MIN        | MAX | MIN        | MAX |      |
| $t_{pd}$  | A               | Y              | 4.5 V    | 20                       | 33  | 49  | 42         | ns  |            |     |      |
|           |                 |                | 5.5 V    | 19                       | 30  | 45  | 38         |     |            |     |      |
| $t_{en}$  | $\overline{OE}$ | Y              | 4.5 V    | 26                       | 40  | 60  | 50         | ns  |            |     |      |
|           |                 |                | 5.5 V    | 25                       | 36  | 54  | 45         |     |            |     |      |
| $t_t$     |                 | Y              | 4.5 V    | 17                       | 42  | 63  | 53         | ns  |            |     |      |
|           |                 |                | 5.5 V    | 14                       | 38  | 57  | 48         |     |            |     |      |

operating characteristics,  $T_A = 25^\circ\text{C}$

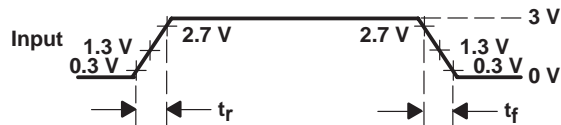
| PARAMETER  | TEST CONDITIONS | TYP | UNIT |
|--|-----------------|-----|------|
| $C_{pd}$ Power dissipation capacitance per buffer/driver | No load         | 35  | pF   |



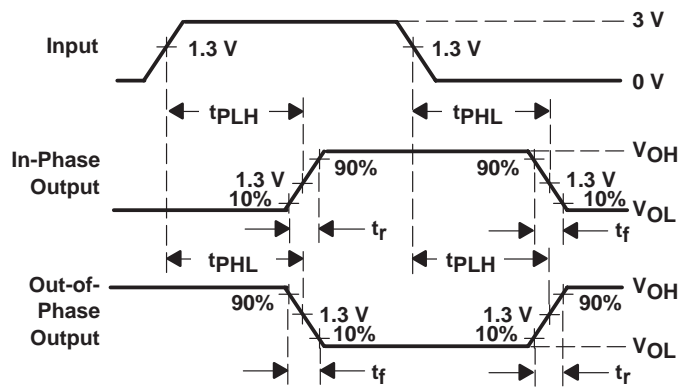
PARAMETER MEASUREMENT INFORMATION



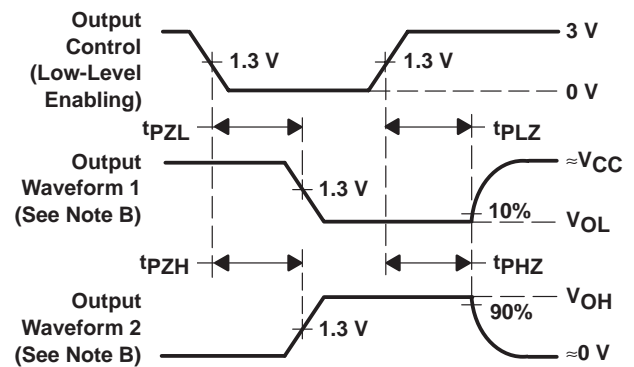
| PARAMETER         | $R_L$        | $C_L$                 | S1     | S2     |
|-------------------|--------------|-----------------------|--------|--------|
| $t_{en}$          | 1 k $\Omega$ | 50 pF<br>or<br>150 pF | Open   | Closed |
|                   |              |                       | Closed | Open   |
| $t_{dis}$         | 1 k $\Omega$ | 50 pF                 | Open   | Closed |
|                   |              |                       | Closed | Open   |
| $t_{pd}$ or $t_t$ | --           | 50 pF<br>or<br>150 pF | Open   | Open   |



VOLTAGE WAVEFORM  
INPUT RISE AND FALL TIMES



VOLTAGE WAVEFORMS  
PROPAGATION DELAY AND OUTPUT RISE AND FALL TIMES



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES FOR 3-STATE OUTPUTS

- NOTES: A.  $C_L$  includes probe and test-fixture capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 C. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  1 MHz,  $Z_O = 50 \Omega$ ,  $t_r = 6$  ns,  $t_f = 6$  ns.  
 D. The outputs are measured one at a time with one input transition per measurement.  
 E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .  
 F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .  
 G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

Figure 1. Load Circuit and Voltage Waveforms

**PACKAGING INFORMATION**

| Orderable Device | Status<br>(1) | Package Type | Package<br>Drawing | Pins | Package<br>Qty | Eco Plan<br>(2)            | Lead finish/<br>Ball material<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples                 |
|------------------|---------------|--------------|--------------------|------|----------------|----------------------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| JM38510/65761BRA | ACTIVE        | CDIP         | J                  | 20   | 1              | TBD                        | SNPB                                 | N / A for Pkg Type   | -55 to 125   | JM38510/<br>65761BRA    | <a href="#">Samples</a> |
| M38510/65761BRA  | ACTIVE        | CDIP         | J                  | 20   | 1              | TBD                        | SNPB                                 | N / A for Pkg Type   | -55 to 125   | JM38510/<br>65761BRA    | <a href="#">Samples</a> |
| SN54HCT541J      | ACTIVE        | CDIP         | J                  | 20   | 1              | TBD                        | SNPB                                 | N / A for Pkg Type   | -55 to 125   | SN54HCT541J             | <a href="#">Samples</a> |
| SN74HCT541DBR    | ACTIVE        | SSOP         | DB                 | 20   | 2000           | Green (RoHS<br>& no Sb/Br) | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 85    | HT541                   | <a href="#">Samples</a> |
| SN74HCT541DW     | ACTIVE        | SOIC         | DW                 | 20   | 25             | Green (RoHS<br>& no Sb/Br) | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 85    | HCT541                  | <a href="#">Samples</a> |
| SN74HCT541DWE4   | ACTIVE        | SOIC         | DW                 | 20   | 25             | Green (RoHS<br>& no Sb/Br) | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 85    | HCT541                  | <a href="#">Samples</a> |
| SN74HCT541DWG4   | ACTIVE        | SOIC         | DW                 | 20   | 25             | Green (RoHS<br>& no Sb/Br) | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 85    | HCT541                  | <a href="#">Samples</a> |
| SN74HCT541DWR    | ACTIVE        | SOIC         | DW                 | 20   | 2000           | Green (RoHS<br>& no Sb/Br) | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 85    | HCT541                  | <a href="#">Samples</a> |
| SN74HCT541DWRE4  | ACTIVE        | SOIC         | DW                 | 20   | 2000           | Green (RoHS<br>& no Sb/Br) | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 85    | HCT541                  | <a href="#">Samples</a> |
| SN74HCT541DWRG4  | ACTIVE        | SOIC         | DW                 | 20   | 2000           | Green (RoHS<br>& no Sb/Br) | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 85    | HCT541                  | <a href="#">Samples</a> |
| SN74HCT541N      | ACTIVE        | PDIP         | N                  | 20   | 20             | Pb-Free<br>(RoHS)          | NIPDAU                               | N / A for Pkg Type   | -40 to 85    | SN74HCT541N             | <a href="#">Samples</a> |
| SN74HCT541NSR    | ACTIVE        | SO           | NS                 | 20   | 2000           | Green (RoHS<br>& no Sb/Br) | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 85    | HCT541                  | <a href="#">Samples</a> |
| SN74HCT541NSRE4  | ACTIVE        | SO           | NS                 | 20   | 2000           | Green (RoHS<br>& no Sb/Br) | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 85    | HCT541                  | <a href="#">Samples</a> |
| SN74HCT541NSRG4  | ACTIVE        | SO           | NS                 | 20   | 2000           | Green (RoHS<br>& no Sb/Br) | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 85    | HCT541                  | <a href="#">Samples</a> |
| SN74HCT541PW     | ACTIVE        | TSSOP        | PW                 | 20   | 70             | Green (RoHS<br>& no Sb/Br) | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 85    | HT541                   | <a href="#">Samples</a> |
| SN74HCT541PWG4   | ACTIVE        | TSSOP        | PW                 | 20   | 70             | Green (RoHS<br>& no Sb/Br) | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 85    | HT541                   | <a href="#">Samples</a> |
| SN74HCT541PWR    | ACTIVE        | TSSOP        | PW                 | 20   | 2000           | Green (RoHS<br>& no Sb/Br) | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 85    | HT541                   | <a href="#">Samples</a> |

| Orderable Device | Status<br>(1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan<br>(2)         | Lead finish/<br>Ball material<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples                 |
|------------------|---------------|--------------|-----------------|------|-------------|-------------------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| SN74HCT541PWRE4  | ACTIVE        | TSSOP        | PW              | 20   | 2000        | Green (RoHS & no Sb/Br) | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 85    | HT541                   | <a href="#">Samples</a> |
| SN74HCT541PWRG4  | ACTIVE        | TSSOP        | PW              | 20   | 2000        | Green (RoHS & no Sb/Br) | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 85    | HT541                   | <a href="#">Samples</a> |
| SN74HCT541PWT    | ACTIVE        | TSSOP        | PW              | 20   | 250         | Green (RoHS & no Sb/Br) | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 85    | HT541                   | <a href="#">Samples</a> |
| SNJ54HCT541FK    | ACTIVE        | LCCC         | FK              | 20   | 1           | TBD                     | POST-PLATE                           | N / A for Pkg Type   | -55 to 125   | SNJ54HCT<br>541FK       | <a href="#">Samples</a> |
| SNJ54HCT541J     | ACTIVE        | CDIP         | J               | 20   | 1           | TBD                     | SNPB                                 | N / A for Pkg Type   | -55 to 125   | SNJ54HCT541J            | <a href="#">Samples</a> |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF SN54HCT541, SN74HCT541 :**

- Catalog: [SN74HCT541](#)
- Military: [SN54HCT541](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

| Device        | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74HCT541DBR | SSOP         | DB              | 20   | 2000 | 330.0              | 16.4               | 8.2     | 7.5     | 2.5     | 12.0    | 16.0   | Q1            |
| SN74HCT541DWR | SOIC         | DW              | 20   | 2000 | 330.0              | 24.4               | 10.8    | 13.3    | 2.7     | 12.0    | 24.0   | Q1            |
| SN74HCT541NSR | SO           | NS              | 20   | 2000 | 330.0              | 24.4               | 8.4     | 13.0    | 2.5     | 12.0    | 24.0   | Q1            |
| SN74HCT541PWR | TSSOP        | PW              | 20   | 2000 | 330.0              | 16.4               | 6.95    | 7.0     | 1.4     | 8.0     | 16.0   | Q1            |
| SN74HCT541PWT | TSSOP        | PW              | 20   | 250  | 330.0              | 16.4               | 6.95    | 7.1     | 1.6     | 8.0     | 16.0   | Q1            |

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

| Device        | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|---------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74HCT541DBR | SSOP         | DB              | 20   | 2000 | 367.0       | 367.0      | 38.0        |
| SN74HCT541DWR | SOIC         | DW              | 20   | 2000 | 367.0       | 367.0      | 45.0        |
| SN74HCT541NSR | SO           | NS              | 20   | 2000 | 367.0       | 367.0      | 45.0        |
| SN74HCT541PWR | TSSOP        | PW              | 20   | 2000 | 367.0       | 367.0      | 38.0        |
| SN74HCT541PWT | TSSOP        | PW              | 20   | 250  | 367.0       | 367.0      | 38.0        |

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - $\triangle C$  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - $\triangle D$  The 20 pin end lead shoulder width is a vendor option, either half or full width.

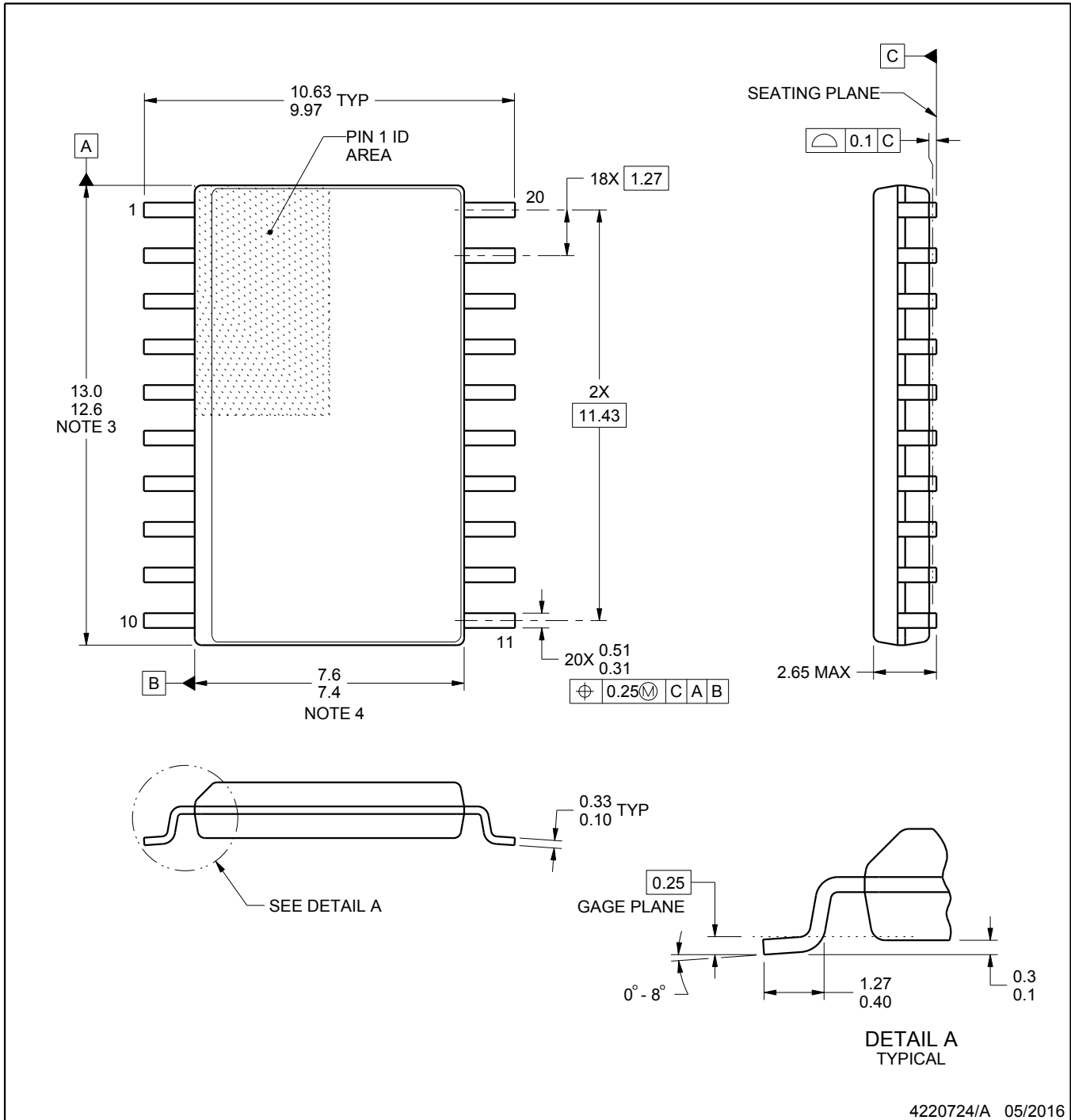
# DW0020A



# PACKAGE OUTLINE

## SOIC - 2.65 mm max height

SOIC



4220724/A 05/2016

### NOTES:

- All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
- This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
- Reference JEDEC registration MS-013.

# EXAMPLE BOARD LAYOUT

DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE  
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

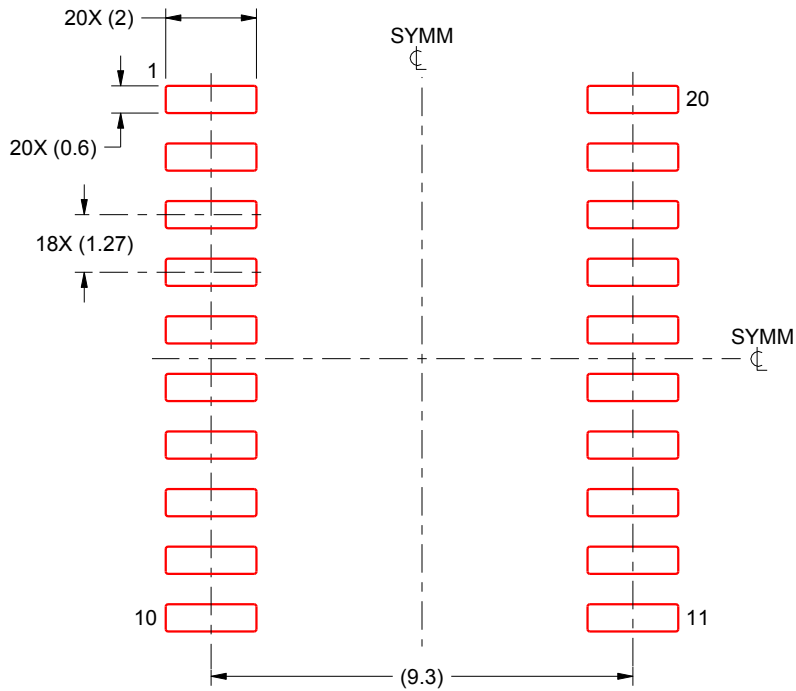
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

FK (S-CQCC-N\*\*)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



| NO. OF TERMINALS ** | A                |                  | B                |                  |
|---------------------|------------------|------------------|------------------|------------------|
|                     | MIN              | MAX              | MIN              | MAX              |
| 20                  | 0.342<br>(8,69)  | 0.358<br>(9,09)  | 0.307<br>(7,80)  | 0.358<br>(9,09)  |
| 28                  | 0.442<br>(11,23) | 0.458<br>(11,63) | 0.406<br>(10,31) | 0.458<br>(11,63) |
| 44                  | 0.640<br>(16,26) | 0.660<br>(16,76) | 0.495<br>(12,58) | 0.560<br>(14,22) |
| 52                  | 0.740<br>(18,78) | 0.761<br>(19,32) | 0.495<br>(12,58) | 0.560<br>(14,22) |
| 68                  | 0.938<br>(23,83) | 0.962<br>(24,43) | 0.850<br>(21,6)  | 0.858<br>(21,8)  |
| 84                  | 1.141<br>(28,99) | 1.165<br>(29,59) | 1.047<br>(26,6)  | 1.063<br>(27,0)  |



4040140/D 01/11

- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package can be hermetically sealed with a metal lid.
  - Falls within JEDEC MS-004

# DB0020A



# PACKAGE OUTLINE

## SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



4214851/B 08/2019

### NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.

# EXAMPLE BOARD LAYOUT

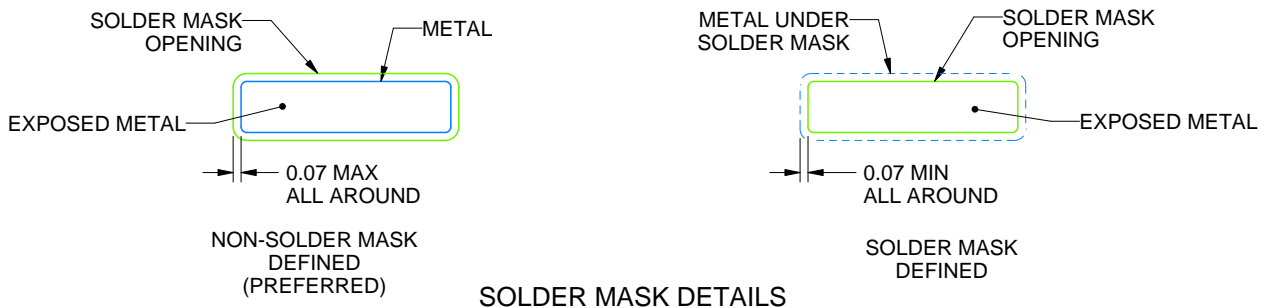
DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



4214851/B 08/2019

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4214851/B 08/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

J (R-GDIP-T\*\*)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



| DIM \ PINS ** | 14                     | 16                     | 18                     | 20                     |
|---------------|------------------------|------------------------|------------------------|------------------------|
| A             | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC |
| B MAX         | 0.785<br>(19,94)       | .840<br>(21,34)        | 0.960<br>(24,38)       | 1.060<br>(26,92)       |
| B MIN         | —                      | —                      | —                      | —                      |
| C MAX         | 0.300<br>(7,62)        | 0.300<br>(7,62)        | 0.310<br>(7,87)        | 0.300<br>(7,62)        |
| C MIN         | 0.245<br>(6,22)        | 0.245<br>(6,22)        | 0.220<br>(5,59)        | 0.245<br>(6,22)        |



4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package is hermetically sealed with a ceramic lid using glass frit.
  - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

PW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



4040064-5/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
  - E. Falls within JEDEC MO-153

PW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate design.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
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