# DATA SHEET



# 74AHC2G00; 74AHCT2G00
## 2-input NAND gate

Product specification

2004 Jan 21

Philips
Semiconductors

# 2-input NAND gate 74AHC2G00; 74AHCT2G00

## FEATURES

- Symmetrical output impedance
- High noise immunity
- ESD protection:
  - HBM EIA/JESD22-A114-A exceeds 2000 V
  - MM EIA/JESD22-A115-A exceeds 200 V
  - CDM EIA/JESD22-C101 exceeds 500 V.
- Low power dissipation
- Balanced propagation delays
- SOT505-2 and SOT765-1 package
- Specified from –40 to +85 °C and –40 to +125 °C.



## DESCRIPTION

The 74AHC2G/AHCT2G00 is a high-speed Si-gate CMOS device.

The 74AHC2G/AHCT2G00 provides the 2-input NAND gate function.

## QUICK REFERENCE DATA

GND = 0 V; $T_{amb}$ = 25 °C; $t_r = t_f \leq 3.0$ ns.

| SYMBOL | PARAMETER | CONDITIONS | TYPICAL | | UNIT |
|---|---|---|---|---|---|
| | | | AHC2G | AHCT2G | |
| $t_{PHL}/t_{PLH}$ | propagation delay nA and nB to nY | $C_L$ = 15 pF; $V_{CC}$ = 5 V | 3.5 | 3.6 | ns |
| $C_I$ | input capacitance | | 1.5 | 1.5 | pF |
| $C_{PD}$ | power dissipation capacitance per gate | $C_L$ = 50 pF; f = 1 MHz; notes 1 and 2 | 17 | 18 | pF |

### Notes

1. $C_{PD}$ is used to determine the dynamic power dissipation ($P_D$ in μW).
   $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
   $f_i$ = input frequency in MHz;
   $f_o$ = output frequency in MHz;
   $C_L$ = output load capacitance in pF;
   $V_{CC}$ = supply voltage in Volts;
   N = total load switching outputs;
   $\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is $V_I$ = GND to $V_{CC}$.

### FUNCTION TABLE

See note 1.

| INPUT | | OUTPUT |
|---|---|---|
| nA | nB | nY |
| L | L | H |
| L | H | H |
| H | L | H |
| H | H | L |



**Note**

1. H = HIGH voltage level;
   L = LOW voltage level.

### ORDERING INFORMATION

| TYPE NUMBER | PACKAGE | | | | | |
|---|---|---|---|---|---|---|
| | TEMPERATURE RANGE | PINS | PACKAGE | MATERIAL | CODE | MARKING |
| 74AHC2G00DP | –40 to +125 °C | 8 | TSSOP8 | plastic | SOT505-2 | A00 |
| 74AHCT2G00DP | –40 to +125 °C | 8 | TSSOP8 | plastic | SOT505-2 | C00 |
| 74AHC2G00DC | –40 to +125 °C | 8 | VSSOP8 | plastic | SOT765-1 | A00 |
| 74AHCT2G00DC | –40 to +125 °C | 8 | VSSOP8 | plastic | SOT765-1 | C00 |

### PINNING

| PIN | SYMBOL | DESCRIPTION |
|---|---|---|
| 1 | 1A | data input |
| 2 | 1B | data input |
| 3 | 2Y | data output |
| 4 | GND | ground (0 V) |
| 5 | 2A | data input |
| 6 | 2B | data input |
| 7 | 1Y | data output |
| 8 | $V_{CC}$ | supply voltage |

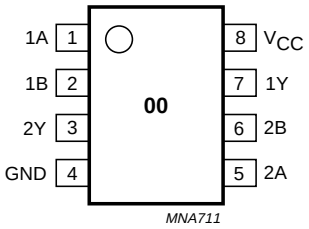



Fig.1 Pin configuration.

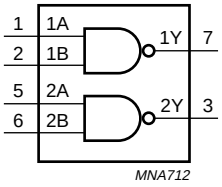



Fig.2 Logic symbol.

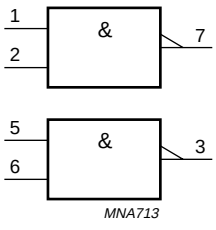



Fig.3 IEC logic symbol.

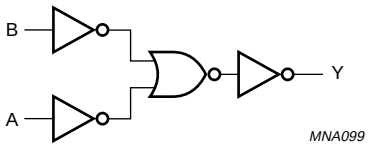



Fig.4 Logic diagram.

## RECOMMENDED OPERATING CONDITIONS

| SYMBOL | PARAMETER | CONDITIONS | 74AHC2G00 | | | 74AHCT2G00 | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN. | TYP. | MAX. | MIN. | TYP. | MAX. | |
| $V_{CC}$ | supply voltage | | 2.0 | 5.0 | 5.5 | 4.5 | 5.0 | 5.5 | V |
| $V_I$ | input voltage | | 0 | – | 5.5 | 0 | – | 5.5 | V |
| $V_O$ | output voltage | | 0 | – | $V_{CC}$ | 0 | – | $V_{CC}$ | V |
| $T_{amb}$ | operating ambient temperature | see DC and AC characteristics per device | –40 | +25 | +125 | –40 | +25 | +125 | °C |
| $t_r$, $t_f$ | input rise and fall times | $V_{CC}$ = 3.3 ± 0.3 V | – | – | 100 | – | – | – | ns/V |
| | | $V_{CC}$ = 5 ± 0.5 V | – | – | 20 | – | – | 20 | ns/V |



## LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134); voltages are referenced to GND (ground = 0 V).

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | supply voltage | | –0.5 | +7.0 | V |
| $V_I$ | input voltage | | –0.5 | +7.0 | V |
| $I_{IK}$ | input diode current | $V_I$ < –0.5 V | – | –20 | mA |
| $I_{OK}$ | output diode current | $V_O$ < –0.5 V or $V_O$ > $V_{CC}$ + 0.5 V; note 1 | – | ±20 | mA |
| $I_O$ | output source or sink current | –0.5 V < $V_O$ < $V_{CC}$ + 0.5 V | – | ±25 | mA |
| $I_{CC}$, $I_{GND}$ | $V_{CC}$ or GND current | | – | ±75 | mA |
| $T_{stg}$ | storage temperature | | –65 | +150 | °C |
| $P_D$ | power dissipation | $T_{amb}$ = –40 to +125 °C | – | 250 | mW |

**Note**

1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

## DC CHARACTERISTICS

### Type 74AHC2G00

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

| SYMBOL | PARAMETER | CONDITIONS | | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|---|
| | | OTHER | $V_{CC}$ (V) | | | | |
| **$T_{amb}$ = 25 °C** | | | | | | | |
| $V_{IH}$ | HIGH-level input voltage | | 2.0 | 1.5 | – | – | V |
| | | | 3.0 | 2.1 | – | – | V |
| | | | 5.5 | 3.85 | – | – | V |
| $V_{IL}$ | LOW-level input voltage | | 2.0 | – | – | 0.5 | V |
| | | | 3.0 | – | – | 0.9 | V |
| | | | 5.5 | – | – | 1.65 | V |
| $V_{OH}$ | HIGH-level output voltage | $V_I$ = $V_{IH}$ or $V_{IL}$ | | | | | |
| | | $I_O$ = –50 μA | 2.0 | 1.9 | 2.0 | – | V |
| | | $I_O$ = –50 μA | 3.0 | 2.9 | 3.0 | – | V |
| | | $I_O$ = –50 μA | 4.5 | 4.4 | 4.5 | – | V |
| | | $I_O$ = –4.0 mA | 3.0 | 2.58 | – | – | V |
| | | $I_O$ = –8.0 mA | 4.5 | 3.94 | – | – | V |
| $V_{OL}$ | LOW-level output voltage | $V_I$ = $V_{IH}$ or $V_{IL}$ | | | | | |
| | | $I_O$ = 50 μA | 2.0 | – | 0 | 0.1 | V |
| | | $I_O$ = 50 μA | 3.0 | – | 0 | 0.1 | V |
| | | $I_O$ = 50 μA | 4.5 | – | 0 | 0.1 | V |
| | | $I_O$ = 4.0 mA | 3.0 | – | – | 0.36 | V |
| | | $I_O$ = 8.0 mA | 4.5 | – | – | 0.36 | V |
| $I_{LI}$ | input leakage current | $V_I$ = $V_{CC}$ or GND | 5.5 | – | – | 0.1 | μA |
| $I_{CC}$ | quiescent supply current | $V_I$ = $V_{CC}$ or GND; $I_O$ = 0 | 5.5 | – | – | 10 | μA |
| $C_I$ | input capacitance | | – | – | 1.5 | 10 | pF |

| SYMBOL | PARAMETER | CONDITIONS | | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|---|
| | | OTHER | $V_{CC}$ (V) | | | | |
| **$T_{amb}$ = −40 to +85 °C** | | | | | | | |
| $V_{IH}$ | HIGH-level input voltage | | 2.0 | 1.5 | – | – | V |
| | | | 3.0 | 2.1 | – | – | V |
| | | | 5.5 | 3.85 | – | – | V |
| $V_{IL}$ | LOW-level input voltage | | 2.0 | – | – | 0.5 | V |
| | | | 3.0 | – | – | 0.9 | V |
| | | | 5.5 | – | – | 1.65 | V |
| $V_{OH}$ | HIGH-level output voltage | $V_I$ = $V_{IH}$ or $V_{IL}$ | | | | | |
| | | $I_O$ = –50 μA | 2.0 | 1.9 | – | – | V |
| | | $I_O$ = –50 μA | 3.0 | 2.9 | – | – | V |
| | | $I_O$ = –50 μA | 4.5 | 4.4 | – | – | V |
| | | $I_O$ = –4.0 mA | 3.0 | 2.48 | – | – | V |
| | | $I_O$ = –8.0 mA | 4.5 | 3.8 | – | – | V |
| $V_{OL}$ | LOW-level output voltage | $V_I$ = $V_{IH}$ or $V_{IL}$ | | | | | |
| | | $I_O$ = 50 μA | 2.0 | – | – | 0.1 | V |
| | | $I_O$ = 50 μA | 3.0 | – | – | 0.1 | V |
| | | $I_O$ = 50 μA | 4.5 | – | – | 0.1 | V |
| | | $I_O$ = 4.0 mA | 3.0 | – | – | 0.44 | V |
| | | $I_O$ = 8.0 mA | 4.5 | – | – | 0.44 | V |
| $I_{LI}$ | input leakage current | $V_I$ = $V_{CC}$ or GND | 5.5 | – | – | 1.0 | μA |
| $I_{CC}$ | quiescent supply current | $V_I$ = $V_{CC}$ or GND; $I_O$ = 0 | 5.5 | – | – | 10 | μA |
| $C_I$ | input capacitance | | – | – | – | 10 | pF |

| SYMBOL | PARAMETER | CONDITIONS | | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|---|
| | | OTHER | $V_{CC}$ (V) | | | | |
| **$T_{amb}$ = −40 to +125 °C** | | | | | | | |
| $V_{IH}$ | HIGH-level input voltage | | 2.0 | 1.5 | – | – | V |
| | | | 3.0 | 2.1 | – | – | V |
| | | | 5.5 | 3.85 | – | – | V |
| $V_{IL}$ | LOW-level input voltage | | 2.0 | – | – | 0.5 | V |
| | | | 3.0 | – | – | 0.9 | V |
| | | | 5.5 | – | – | 1.65 | V |
| $V_{OH}$ | HIGH-level output voltage | $V_I$ = $V_{IH}$ or $V_{IL}$ | | | | | |
| | | $I_O$ = –50 μA | 2.0 | 1.9 | – | – | V |
| | | $I_O$ = –50 μA | 3.0 | 2.9 | – | – | V |
| | | $I_O$ = –50 μA | 4.5 | 4.4 | – | – | V |
| | | $I_O$ = –4.0 mA | 3.0 | 2.40 | – | – | V |
| | | $I_O$ = –8.0 mA | 4.5 | 3.70 | – | – | V |
| $V_{OL}$ | LOW-level output voltage | $V_I$ = $V_{IH}$ or $V_{IL}$ | | | | | |
| | | $I_O$ = 50 μA | 2.0 | – | – | 0.1 | V |
| | | $I_O$ = 50 μA | 3.0 | – | – | 0.1 | V |
| | | $I_O$ = 50 μA | 4.5 | – | – | 0.1 | V |
| | | $I_O$ = 4.0 mA | 3.0 | – | – | 0.55 | V |
| | | $I_O$ = 8.0 mA | 4.5 | – | – | 0.55 | V |
| $I_{LI}$ | input leakage current | $V_I$ = $V_{CC}$ or GND | 5.5 | – | – | 2.0 | μA |
| $I_{CC}$ | quiescent supply current | $V_I$ = $V_{CC}$ or GND; $I_O$ = 0 | 5.5 | – | – | 40 | μA |
| $C_I$ | input capacitance | | – | – | – | 10 | pF |

**Type 74AHCT2G00**

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

| SYMBOL | PARAMETER | CONDITIONS | | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|---|
| | | OTHER | $V_{CC}$ (V) | | | | |
| **$T_{amb}$ = 25 °C** | | | | | | | |
| $V_{IH}$ | HIGH-level input voltage | | 4.5 to 5.5 | 2.0 | – | – | V |
| $V_{IL}$ | LOW-level input voltage | | 4.5 to 5.5 | – | – | 0.8 | V |
| $V_{OH}$ | HIGH-level output voltage | $V_I$ = $V_{IH}$ or $V_{IL}$ | | | | | |
| | | $I_O$ = –50 μA | 4.5 | 4.4 | 4.5 | – | V |
| | | $I_O$ = –8.0 mA | 4.5 | 3.94 | – | – | V |
| $V_{OL}$ | LOW-level output voltage | $V_I$ = $V_{IH}$ or $V_{IL}$ | | | | | |
| | | $I_O$ = 50 μA | 4.5 | – | 0 | 0.1 | V |
| | | $I_O$ = 8.0 mA | 4.5 | – | – | 0.36 | V |
| $I_{LI}$ | input leakage current | $V_I$ = $V_{IH}$ or $V_{IL}$ | 5.5 | – | – | 0.1 | μA |
| $I_{CC}$ | quiescent supply current | $V_I$ = $V_{CC}$ or GND; $I_O$ = 0 | 5.5 | – | – | 1.0 | μA |
| $\Delta I_{CC}$ | additional quiescent supply current per input pin | $V_I$ = 3.4 V; other inputs at $V_{CC}$ or GND; $I_O$ = 0 | 5.5 | – | – | 1.35 | mA |
| $C_I$ | input capacitance | | | – | 1.5 | 10 | pF |
| **$T_{amb}$ = –40 to +85 °C** | | | | | | | |
| $V_{IH}$ | HIGH-level input voltage | | 4.5 to 5.5 | 2.0 | – | – | V |
| $V_{IL}$ | LOW-level input voltage | | 4.5 to 5.5 | – | – | 0.8 | V |
| $V_{OH}$ | HIGH-level output voltage | $V_I$ = $V_{IH}$ or $V_{IL}$ | | | | | |
| | | $I_O$ = –50 μA | 4.5 | 4.4 | – | – | V |
| | | $I_O$ = –8.0 mA | 4.5 | 3.8 | – | – | V |
| $V_{OL}$ | LOW-level output voltage | $V_I$ = $V_{IH}$ or $V_{IL}$ | | | | | |
| | | $I_O$ = 50 μA | 4.5 | – | – | 0.1 | V |
| | | $I_O$ = 8.0 mA | 4.5 | – | – | 0.44 | V |
| $I_{LI}$ | input leakage current | $V_I$ = $V_{IH}$ or $V_{IL}$ | 5.5 | – | – | 1.0 | μA |
| $I_{CC}$ | quiescent supply current | $V_I$ = $V_{CC}$ or GND; $I_O$ = 0 | 5.5 | – | – | 10 | μA |
| $\Delta I_{CC}$ | additional quiescent supply current per input pin | $V_I$ = 3.4 V; other inputs at $V_{CC}$ or GND; $I_O$ = 0 | 5.5 | – | – | 1.5 | mA |
| $C_I$ | input capacitance | | – | – | – | 10 | pF |

| SYMBOL | PARAMETER | CONDITIONS | | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|---|
| | | OTHER | $V_{CC}$ (V) | | | | |
| **$T_{amb}$ = −40 to +125 °C** | | | | | | | |
| $V_{IH}$ | HIGH-level input voltage | | 4.5 to 5.5 | 2.0 | – | – | V |
| $V_{IL}$ | LOW-level input voltage | | 4.5 to 5.5 | – | – | 0.8 | V |
| $V_{OH}$ | HIGH-level output voltage | $V_I$ = $V_{IH}$ or $V_{IL}$ | | | | | |
| | | $I_O$ = –50 μA | 4.5 | 4.4 | – | – | V |
| | | $I_O$ = –8.0 mA | 4.5 | 3.70 | – | – | V |
| $V_{OL}$ | LOW-level output voltage | $V_I$ = $V_{IH}$ or $V_{IL}$ | | | | | |
| | | $I_O$ = 50 μA | 4.5 | – | – | 0.1 | V |
| | | $I_O$ = 8.0 mA | 4.5 | – | – | 0.55 | V |
| $I_{LI}$ | input leakage current | $V_I$ = $V_{IH}$ or $V_{IL}$ | 5.5 | – | – | 2.0 | μA |
| $I_{CC}$ | quiescent supply current | $V_I$ = $V_{CC}$ or GND; $I_O$ = 0 | 5.5 | – | – | 40 | μA |
| $\Delta I_{CC}$ | additional quiescent supply current per input pin | $V_I$ = 3.4 V; other inputs at $V_{CC}$ or GND; $I_O$ = 0 | 5.5 | – | – | 1.5 | mA |
| $C_I$ | input capacitance | | – | – | – | 10 | pF |

## AC CHARACTERISTICS

### Type 74AHC2G00

GND = 0 V; $t_r = t_f \leq 3.0$ ns.

| SYMBOL | PARAMETER | TEST CONDITIONS | | | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | WAVEFORMS | $C_L$ (pF) | $V_{CC}$ (V) | | | | |
| **$T_{amb}$ = 25 °C** | | | | | | | | |
| $t_{PHL}/t_{PLH}$ | propagation delay input nA and nB to output nY | see Figs 5 and 6 | 15 | 3.0 to 3.6 | – | 4.5[1] | 7.9 | ns |
| | | | | 4.5 to 5.5 | – | 3.5[2] | 5.5 | ns |
| | | | 50 | 3.0 to 3.6 | – | 6.5[1] | 11.4 | ns |
| | | | | 4.5 to 5.5 | – | 4.9[2] | 7.5 | ns |
| **$T_{amb}$ = −40 to +85 °C** | | | | | | | | |
| $t_{PHL}/t_{PLH}$ | propagation delay input nA and nB to output nY | see Figs 5 and 6 | 15 | 3.0 to 3.6 | 1.0 | – | 9.5 | ns |
| | | | | 4.5 to 5.5 | 1.0 | – | 6.5 | ns |
| | | | 50 | 3.0 to 3.6 | 1.0 | – | 13.0 | ns |
| | | | | 4.5 to 5.5 | 1.0 | – | 8.5 | ns |
| **$T_{amb}$ = −40 to +125 °C** | | | | | | | | |
| $t_{PHL}/t_{PLH}$ | propagation delay input nA and nB to output nY | see Figs 5 and 6 | 15 | 3.0 to 3.6 | 1.0 | – | 10.5 | ns |
| | | | | 4.5 to 5.5 | 1.0 | – | 7.0 | ns |
| | | | 50 | 3.0 to 3.6 | 1.0 | – | 14.5 | ns |
| | | | | 4.5 to 5.5 | 1.0 | – | 9.5 | ns |

**Notes**

1. Typical values are measured at VCC = 3.3 V.
2. Typical values are measured at VCC = 5.0 V.

**Type 74AHCT2G00**

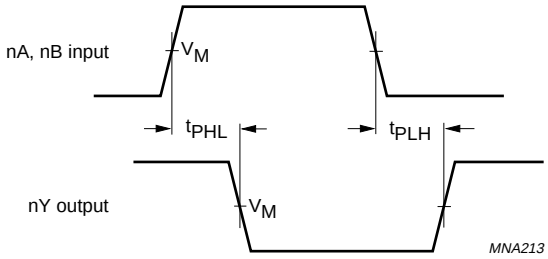
GND = 0 V; $t_r = t_f \leq 3.0$ ns.

| SYMBOL | PARAMETER | TEST CONDITIONS | | | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | WAVEFORMS | $C_L$ (pF) | $V_{CC}$ (V) | | | | |
| **$T_{amb}$ = 25 °C** | | | | | | | | |
| $t_{PHL}/t_{PLH}$ | propagation delay input nA and nB to output nY | see Figs 5 and 6 | 15 | 4.5 to 5.5 | 1.0 | 3.6[1] | 6.2 | ns |
| | | | 50 | 4.5 to 5.5 | 1.0 | 5.0[1] | 7.9 | ns |
| **$T_{amb}$ = −40 to +85 °C** | | | | | | | | |
| $t_{PHL}/t_{PLH}$ | propagation delay input nA and nB to output nY | see Figs 5 and 6 | 15 | 4.5 to 5.5 | 1.0 | – | 7.1 | ns |
| | | | 50 | 4.5 to 5.5 | 1.0 | – | 9.0 | ns |
| **$T_{amb}$ = −40 to +125 °C** | | | | | | | | |
| $t_{PHL}/t_{PLH}$ | propagation delay input nA and nB to output nY | see Figs 5 and 6 | 15 | 4.5 to 5.5 | 1.0 | – | 8.0 | ns |
| | | | 50 | 4.5 to 5.5 | 1.0 | – | 10.0 | ns |

**Note**

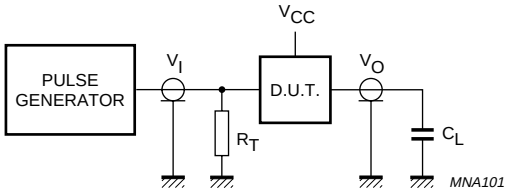
1. Typical values are measured at VCC = 5.0 V.

**AC WAVEFORMS**




| FAMILY | $V_M$ INPUT | $V_M$ OUTPUT |
|---|---|---|
| AHC2G00 | 50% $V_{CC}$ | 50% $V_{CC}$ |
| AHCT2G00 | 1.5 V | 50% $V_{CC}$ |

Fig.5 The inputs (nA and nB) to output (nY) propagation delays.




| FAMILY | $V_I$ INPUT REQUIREMENTS |
|---|---|
| AHC2G00 | GND to $V_{CC}$ |
| AHCT2G00 | GND to 3.0 V |

Definitions for test circuit:

$C_L$ = Load capacitance including jig and probe capacitance (See “AC characteristics” for the value).

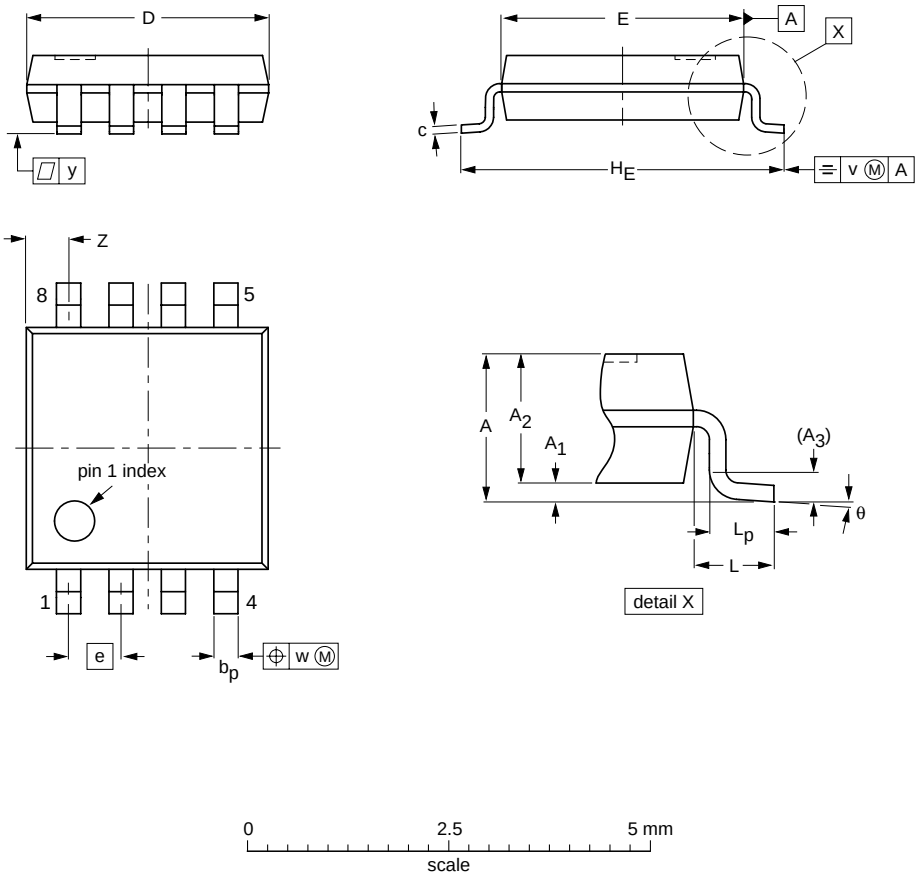
$R_T$ = Termination resistance should be equal to the output impedance $Z_0$ of the pulse generator.

Fig.6 Load circuitry for switching times.

## PACKAGE OUTLINES

**TSSOP8: plastic thin shrink small outline package; 8 leads; body width 3 mm; lead length 0.5 mm SOT505-2**






**DIMENSIONS (mm are the original dimensions)**

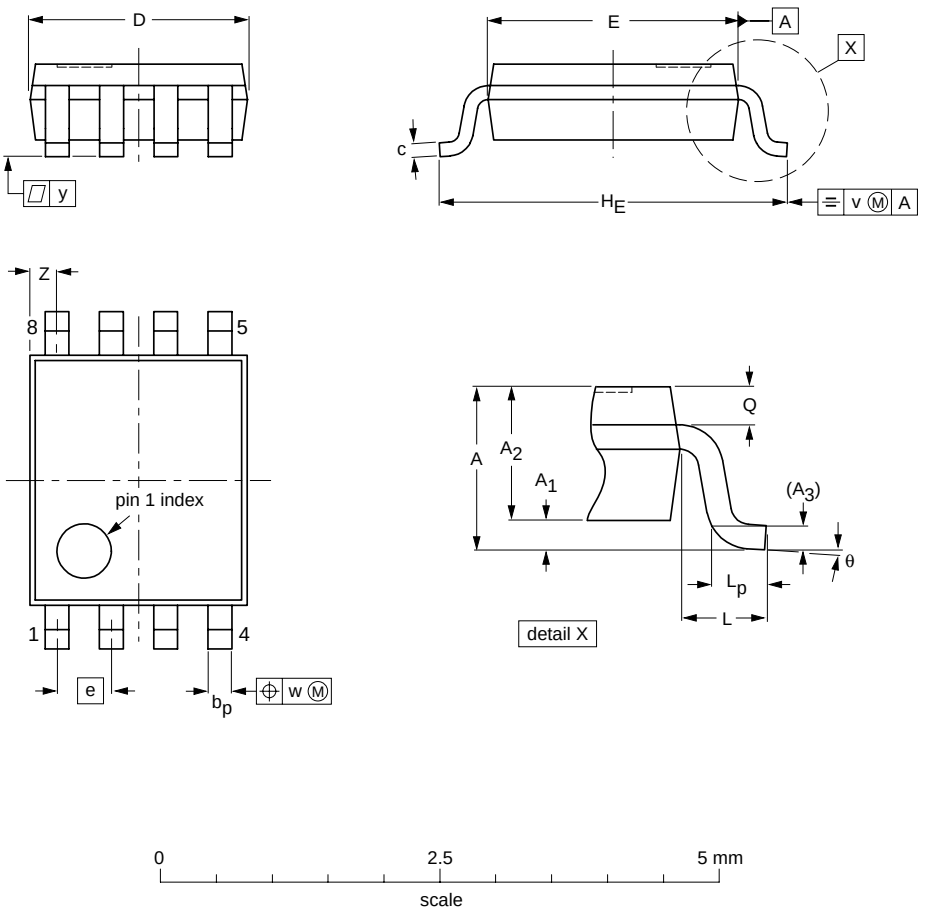
| UNIT | A max. | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | $D^{(1)}$ | $E^{(1)}$ | e | $H_E$ | L | $L_p$ | v | w | y | $Z^{(1)}$ | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 1.1 | 0.15<br>0.00 | 0.95<br>0.75 | 0.25 | 0.38<br>0.22 | 0.18<br>0.08 | 3.1<br>2.9 | 3.1<br>2.9 | 0.65 | 4.1<br>3.9 | 0.5 | 0.47<br>0.33 | 0.2 | 0.13 | 0.1 | 0.70<br>0.35 | 8°<br>0° |

**Note**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT505-2 | | - - - | | | | 02-01-16 |

**VSSOP8: plastic very thin shrink small outline package; 8 leads; body width 2.3 mm** **SOT765-1**




**DIMENSIONS (mm are the original dimensions)**

| UNIT | A max. | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | $D^{(1)}$ | $E^{(2)}$ | e | $H_E$ | L | $L_p$ | Q | v | w | y | $Z^{(1)}$ | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 1 | 0.15<br>0.00 | 0.85<br>0.60 | 0.12 | 0.27<br>0.17 | 0.23<br>0.08 | 2.1<br>1.9 | 2.4<br>2.2 | 0.5 | 3.2<br>3.0 | 0.4 | 0.40<br>0.15 | 0.21<br>0.19 | 0.2 | 0.13 | 0.1 | 0.4<br>0.1 | 8°<br>0° |

**Notes**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT765-1 | | MO-187 | | | | 02-06-07 |

**DATA SHEET STATUS**

| LEVEL | DATA SHEET STATUS(1) | PRODUCT STATUS(2)(3) | DEFINITION |
|---|---|---|---|
| I | Objective data | Development | This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice. |
| II | Preliminary data | Qualification | This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product. |
| III | Product data | Production | This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN). |



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1. Please consult the most recently issued data sheet before initiating or completing a design.
2. The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.
3. For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

**DEFINITIONS**

**Short-form specification** — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

**Limiting values definition** — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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**Contact information**

For additional information please visit **http://www.semiconductors.philips.com**. Fax: **+31 40 27 24825**
For sales offices addresses send e-mail to: **sales.addresses@www.semiconductors.philips.com**.



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