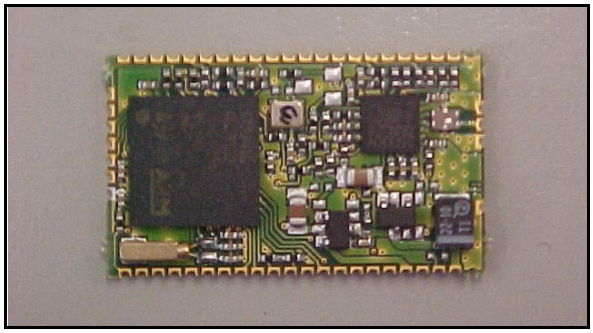
BT-STA2425

Bluetooth® technology module

Features

- Bluetooth® specification V 2.0 compliant
- Transmission rate up to 721 kbit/s (basic rate) and beyond (EDR)
- Output power level: class 2 (0 dBm typical) and class 1.5 (> 4 dBm)
- Power class 1 compatible (with external power amplifier)
- ACL and SCO links
- Full Bluetooth® upper-layer stack including profiles
- Supports USB1.1, UART, I^2C, PCM, SPI, and 15 GPIOs
- Embedded ARM7TDMI® core processor
- Integrated 4-Mbit flash, 64-KByte RAM, 4-Kbyte ROM
- 2.8-V single power supply
- Designed for low power consumption in standby condition
- 13-MHz and 32.768-kHz digital clock outputs
- No external components needed - excluding antenna
- Module size: 29 mm x 17 mm
- Fully programmable solution
- Free development framework (CFWLite, including real-time operating system)
- Reference designs at no additional cost
- Proved for FCC/CE and BQB compliant designs
- Firmware library supporting profiles:
  - A2DP, AVRCP sink and source
  - HFP/HS
  - SPP (up to 7 simultaneous connections
  - Additional profiles under development
- Seamless connection with ST audio codecs and amplifiers (STA529, STA333BW,STA328)



Applications

- Remote speakers
- Bluetooth® plug-in for TV, portable players
- Audio cradle systems
- Wireless audio systems
- Serial port replacement
- Industrial automation
- Wireless peripherals

Description

The BT-STA2425 is a flexible low-power module enabling Bluetooth® connectivity. It is fully programmable and capable of running the whole stack plus custom applications.

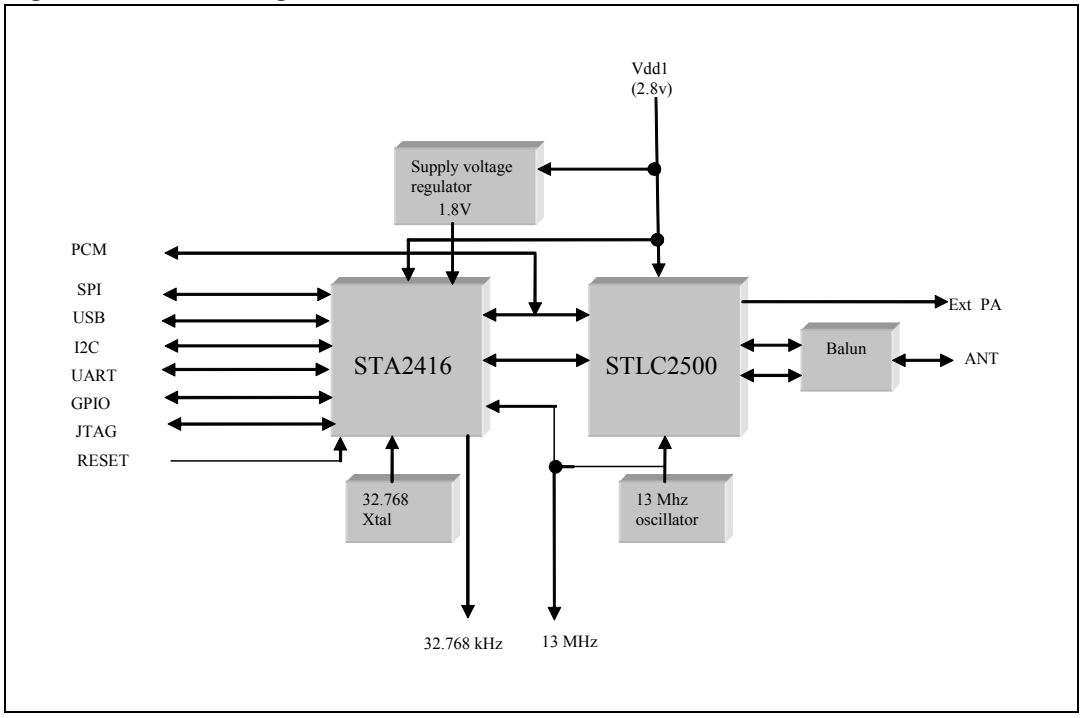
The ARM7® embedded microcontroller can be either programmed by the end-user or flashed with our selection of firmware images, thereby turning the module in a complete solution for wireless audio connectivity or serial port replacement.

A full set of peripherals is also available to allow simple interfacing with other devices in the system.

Order code: BT-STA2425

1 Block diagram

Figure 1. Block diagram



2 Pin connections

Figure 2. Pin connections (component side)

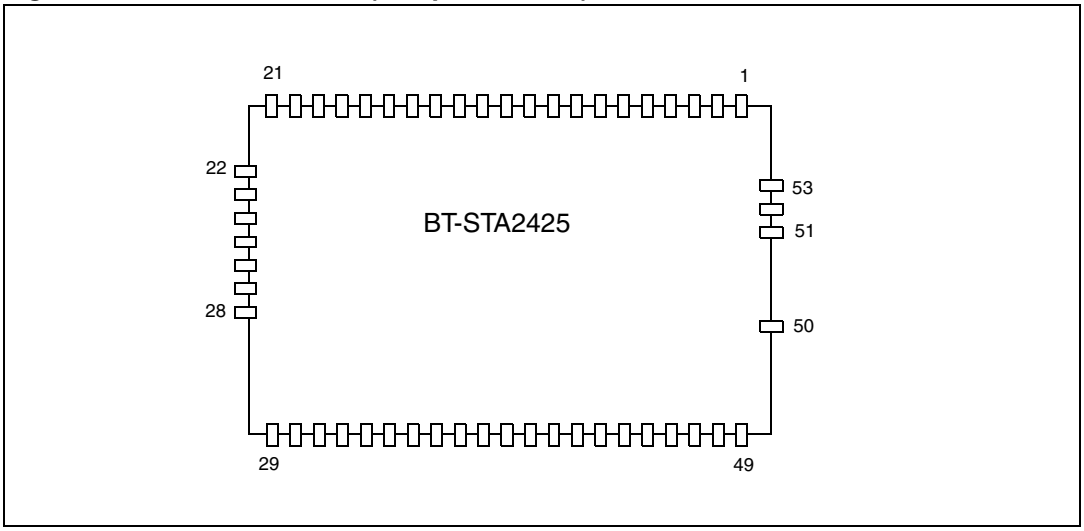


Table 1. Pin description

Number	Name	Type	Description
1 (1)	RX_EN	O	RX Enable *Used in Class1 application*
2 (1)	PA_EN	O	External PA enable *Used in Class1 application*
3 (1)	PA_V1	O	External PA gain setting *Used in Class1 application*
4 (1)	PA_V0	O	External PA gain setting *Used in Class1 application*
5 (1)	ANT_SW	O	Antenna switch *Used in Class1 application*
6	PMC_A	I/O	Synchronous data in/out
7	PMC_B	I/O	Synchronous data out/in
8	PMC_SYNC	I/O	Synchronous data strobe
9	PMC_CLK	I/O	Synchronous data clock
10	NTRST	I	JTAG0 pin
11	TDI	I	JTAG1 pin
12	TMS	I	JTAG2 pin
13	TCK	I	JTAG3 pin (must be connected to ground if not used)
14	TDO	I	JTAG4 pin
15	13M_CK	O	13 MHz oscillator out
16	RESET	I	Reset pin: a low on this pin resets the module. An internal pull-up resistor of 100 kΩ to VDD and a capacitor of 100 nF to GND is built into the module.
17	INT2	I	External interrupt signal, internally connected to GND via 10 kΩ

Table 1. Pin description (continued)

Number	Name	Type	Description
18	UART1_RXD	I	UART data input
19	UART1_TXD	O	UART data output
20	I2C0	I/O	I^2C interface data, to be connected to VDD via 10 kΩ resistor
21	I2C1	I/O	I^2C interface clock, to be connected to VDD by 10 kΩ resistor
22	USB_DN	I/O	USB data - (negative) (connect to GND if not used)
23	USB_DP	I/O	USB data + (positive) (connect to GND if not used)
24	SPI_FRM	I/O	SPI frame sync
25	SPI_CLK	I/O	SPI clock
26	SPI_TXD	O	SPI transmit data
27	SPI_RXD	I	SPI receive data (connect to GND if not used)
28	GND_S	PWR	High-quality signal ground
29	BOOT	I	External downloading enable: when low it allows the firmware to be downloaded into the internal flash at power-up
30	GPIO 0	I/O	General purpose input / output 0
31	GPIO 1	I/O	General purpose input / output 1
32	GPIO 2	I/O	General purpose input / output 2
33	GPIO 3	I/O	General purpose input / output 3
34	GPIO 4	I/O	General purpose input / output 4
35	GPIO 5	I/O	General purpose input / output 5
36	GPIO 6	I/O	General purpose input / output 6 Not to be used, internally used for STLC2500 wake-up
37	GPIO 7	I/O	General purpose input / output 7
38	GPIO 8	I/O	General purpose input / output 8 Not to be used, internally used for STLC2500 reset
39	GPIO 9	I/O	General purpose input / output 9
40	LP_CK	O	32.768 kHz digital output
41	GPIO11	I/O	General purpose input / output 11
42	GPIO12	I/O	General purpose input / output 12
43	GPIO13	I/O	General purpose input / output 13
44	GPIO14	I/O	General purpose input / output 14
45	GPIO15	I/O	General purpose input / output 15
46	1V8	PWR	1.8 V internal regulator output. Not to be used – only for test purposes

Table 1. Pin description (continued)

Number	Name	Type	Description
47	2V8	PWR	2.8-V internal regulator output. Not to be used – only for test purposes
48	NC	I	Not connected
49	VDD	PWR	2.8 V power supply The STA2416 I/Os and STLC2500 supply pins are connected to this pin (the STA2416 supply voltage is internally generated)
50	GND	PWR	Digital ground
51	GND_RF	PWR	RF ground
52	BT_ANTENNA	I/O	RF pad to be connected to the antenna
53	GND_RF	PWR	RF ground

1. Leave unconnected for Class-2/1.5 operation.

3 Electrical specification

3.1 Absolute maximum ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Min	Max	Unit
VDD	Module supply voltage		4	V
Vin	Input voltage on any digital pin	GND - 0.3	VDD + 0.3	V
Tstg	Storage temperature	-40	+85	° C
Tsold	Soldering temperature < 10s		250	° C

3.2 Operating range

Table 3. Operating range

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VDD	Module supply voltage	-20°C < T < 70°C	2.75	2.8	2.85	V
Tstg	Operating ambient temperature		-20		+70	°C
Iop	Operating current.	VDD = 2.8 V		40		mA
Iosb	Standby current.	VDD = 2.8 V, Inhibit = L		100		µA

3.3 DC specifications

The parameters in *Table 4* are specified at VDD = 2.8 V and Tamb = 25° C, unless specified otherwise.

Table 4. DC specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VIL	Low level input voltage				0.8	V
VIH	High level input voltage		2		2.85	V
Vhyst	Schmitt trigger hysteresis		0.4			V
VOL	Low level output voltage				0.2	V
VOH	High level output voltage		2.4		2.85	V
13M_CKH	13 MHz output high level		2.4			V
13M_CKL	13 MHz output low level				0.3	V

3.4 Transmitter / receiver specifications

The parameters in *Table 5* are specified at VDD = 2.8 V and Tamb = 25° C, unless specified otherwise. RF sensitivity and output power parameters are measured on the antenna pad.

For more complete information please refer to the datasheets for STA2416 and STLC2500C

Table 5. Tx/Rx specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
RFin	Input frequency range		2402		2480	MHz
RX sens	Receiver sensitivity	BER = 0.1%		-81		dBm
RFout	Output frequency range		2402		2480	MHz
TXpout	Nominal output power	Frequency = 2402 to 2480 MHz		3		dBm
TXout	Txout spectr at - 20 dBm			930	1000	kHz
ACP	Channel offset = 2			-50		dBm
ACP	Channel offset = 3			-55		dBm
ACP	Channel offset = 4			-57		dBm
Chs	Channel space			1		MHz
ΔF	Initial CF tolerance		-75		+75	kHz
|Δf-p1|	CFD 1 slot packet				25	kHz
|Δf-p3|	CFD 3 slot packet				40	kHz
|Δf-p5|	CFD 5 slot packet				40	kHz
|Δf/50µs|	CFD rate				20	kHz/µs
Hop	Hopping			1600		hop/s
13M_CK	System clock			13		MHz
	System clock precision	Tamb = 25° C	-10		+10	ppm
	System clock stability	Tamb = -20° C to 70° C	-20		+20	ppm
LP_CK	Low-power mode clock			32.768		kHz
	Low-power mode clock accuracy		-200		+200	ppm
Tr	Transmission rate	Asyncronous			1.4	Mbits/s

4 Mechanical information

Figure 3. Module dimensions (component side)

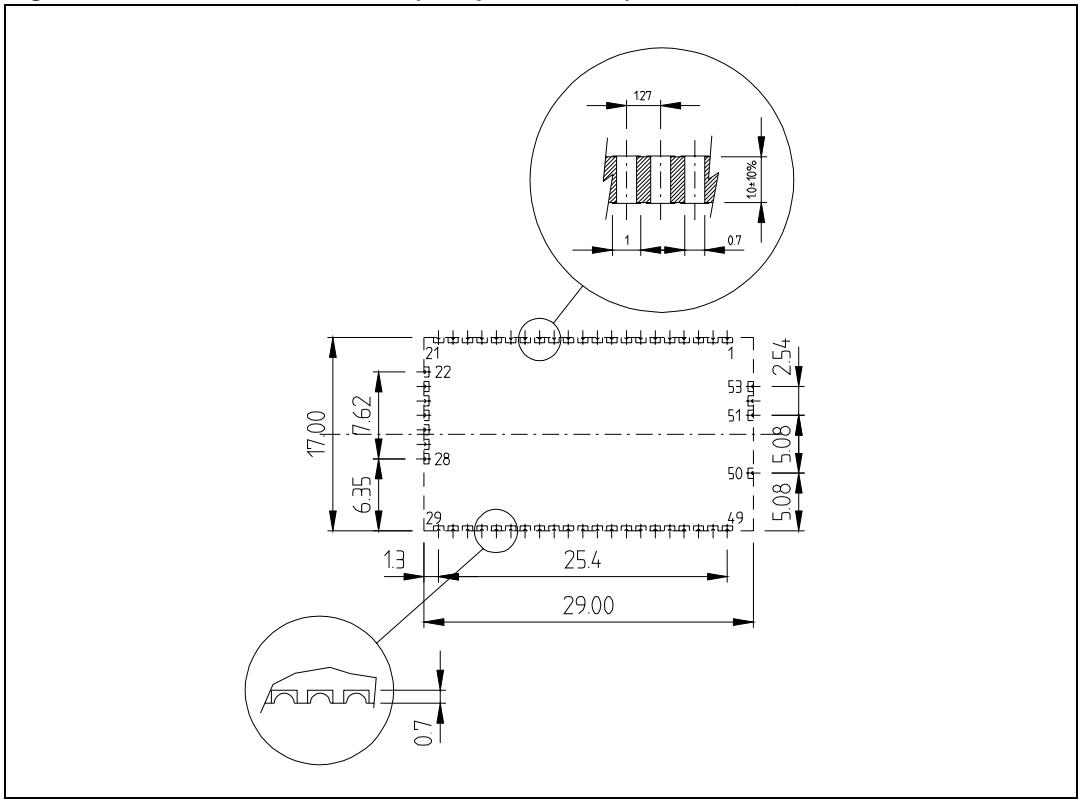
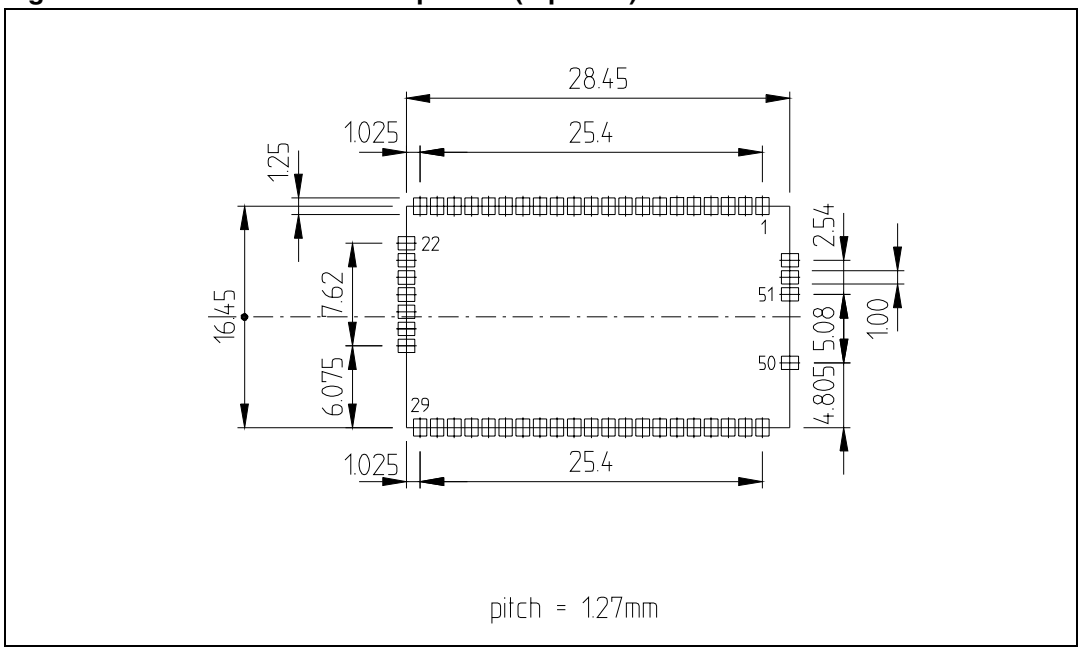


Figure 4. Recommended land pattern (top view)

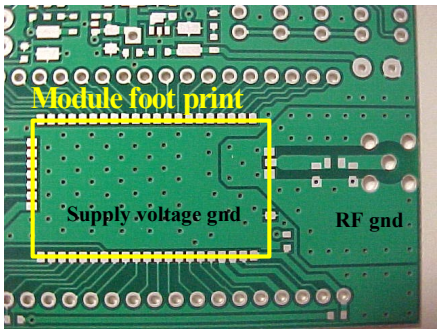


5 Applications information

The following are some suggestions to better implement the BT-STA2425 module in the final application.

- The module is usually mounted on a motherboard, so avoid routing tracks with switching signals below the module. The best would be to have a ground plane beneath the module.
- Connect the power supply ground of the module with the other grounds in a star fashion on the motherboard.
- Keep the RF ground separate from the module power supply ground - the two grounds are already connected at one point inside the module. A possible implementation is shown in *Figure 5*.

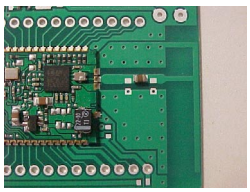
Figure 5. Ground connections



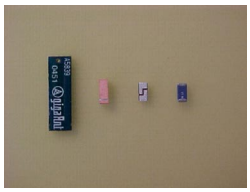
The RF pin must be connected to an antenna which could be one of those shown in *Figure 6* and explained as follows.

- An antenna directly printed on the PCB
- An integrated antenna, such as:
  - Antenova 30-30-A5839-01
  - Murata ANCV12G44SAA127
  - Pulse W3008
  - Yageo CAN4311153002451K
- An external antenna connected by means a SMA connector.

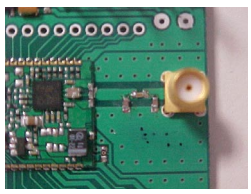
Figure 6. Types of antenna for the BT-STA2425 module



Printed-circuit antenna



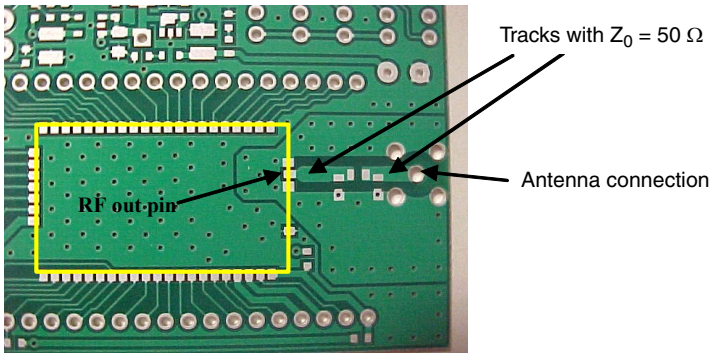
Integrated antenna



External antenna

Whichever type of antenna is chosen, the connection from the RF antenna pin, BT_ANTENNA, must follow good RF design practice and maintain the characteristic impedance (Z_0) of 50 Ω, by careful track layout, for maximum power transfer.

Figure 7. Antenna connection

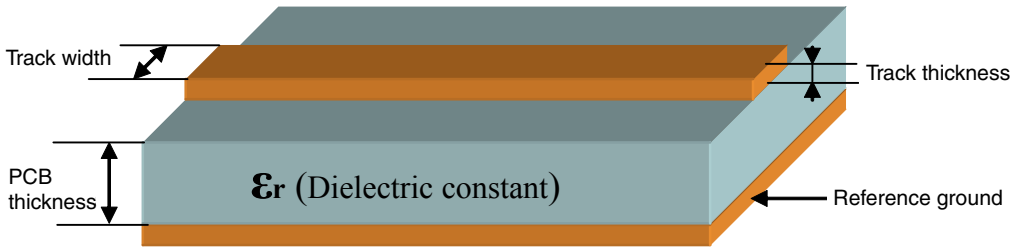


50 Ω matching depends on various factors, for instance:

- the type of board material, for example FR4
- the electrical characteristics of the board, for example the relative permittivity, εr, at 2.4 GHz
- the mechanical dimensions of the board and tracks, for example PCB thickness, track and ground thicknesses, track width.

As an example, using a 1-mm thick FR4 board (εr = 4.3 at 2.4 GHz) with copper thickness of 41 µm, the required track width for 50-Ω strip-line is 1.9 mm (microstrip-type calculation)

Figure 8. Parameters for track matching



Tools for calculating the characteristic impedance based on the physical and mechanical characteristics of the PCB can be easily found on the internet.

6 Trademarks and other acknowledgements

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7 Revision history

Table 6. Document revision history

Date	Revision	Changes
10-Dec-2007	1	Initial release.

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