TPS2592Zx 4.5-V to 18-V eFuse with Blocking FET Control

Not Recommended for New Designs

1 Features

- 4.5-V to 18-V Protection
- Integrated 28-mΩ Pass MOSFET
- Absolute Maximum Voltage of 20 V
- 1-A to 2.1-A Adjustable I_{LIMIT}
- Reverse Current Blocking Support
- Programmable OUT Slew Rate, UVLO
- Built-in Thermal Shutdown
- Safe during Single Point Failure Test (UL60950)
- Small Foot Print – 10L (3 mm x 3 mm) VSON

2 Applications

- HDD and SSD Drives
- Set Top Boxes
- Servers / AUX Supplies
- Fan Control
- PCI/PCIe Cards
- Adapter Powered Devices

3 Description

The TPS2592xx family of eFuses is a highly integrated circuit protection and power management solution in a tiny package. The devices use few external components and provide multiple protection modes. They are a robust defense against overloads, shorts circuits, voltage surges, excessive inrush current, and reverse current.

Current limit level can be set with a single external resistor. Applications with particular voltage ramp requirements can set dV/dT pin with a single capacitor to ensure proper output ramp rates.

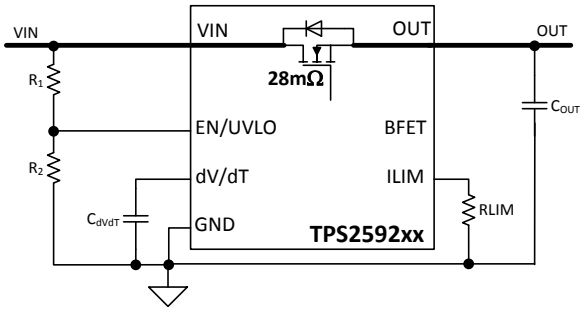
Many systems, such as SSDs, must not allow holdup capacitance energy to dump back through the FET body diode onto a drooping or shorted input bus. The BFET pin is for such systems. An external NFET can be connected “Back to Back (B2B)” with the TPS2592 output and the gate driven by BFET to prevent current flow from load to source.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS2592ZA	VSON (10)	3.00 mm × 3.00 mm
TPS2592ZL		

(1) For all available packages, see the orderable addendum at the end of the datasheet.

4 Application Schematic



Transient: Output Short Circuit

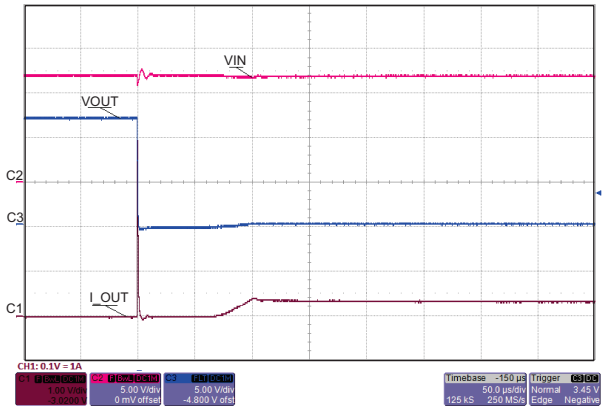


Table of Contents

5 Revision History

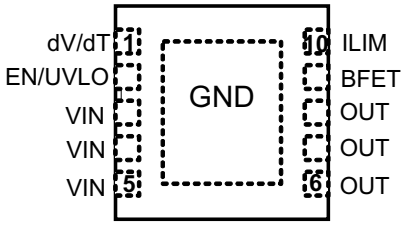
DATE	REVISION	NOTES
December 2014	*	Initial release

6 Device Comparison Table

PART NUMBER	UV	OV CLAMP	FAULT RESPONSE	STATUS
TPS2592ZA	4.3 V	—	Auto-retry	Active
TPS2592ZL	4.3 V	—	Latched	Preview

7 Pin Configuration and Functions

10-Pin VSON
DRC Package
(Top View)



Pin Functions

PIN		DESCRIPTION
NAME	NUMBER	
BFET	9	Connect this pin to the gate of a blocking NFET. See the Feature Description.
dV/dT	1	Tie a capacitor from this pin to GND to control the ramp rate of OUT at device turn-on.
EN/UVLO	2	This is a dual function control pin. When used as an ENABLE pin and pulled down, it shuts off the internal pass MOSFET and pulls BFET to GND. When pulled high, it enables the device and BFET. As an UVLO pin, it can be used to program different UVLO trip point via external resistor divider.
GND	PowerPAD™	GND
ILIM	10	A resistor from this pin to GND will set the overload and short circuit limit.
OUT	6-8	Output of the device
VIN	3-5	Input supply voltage

8 Specifications

8.1 Absolute Maximum Ratings

over operating temperature range (unless otherwise noted) (1) (2)

		MIN	MAX	UNIT
Supply voltage range(1)	VIN	–0.3	20	V
	VIN (10 ms Transient)		22	
Output voltage	OUT	–0.3	VIN + 0.3	V
	OUT (Transient < 1 µs)		-1.2	V
Voltage	ILIM	–0.3	7	V
	EN/UVLO	–0.3	7	
	dV/dT	–0.3	7	
	BFET	–0.3	30	
Continuous power dissipation		See the Thermal Information		
Maximum power dissipation(3), $P_D = (V_{VIN}-V_{OUT})*I_{LIMIT}$	T_A = –40°C to +85°C		40	W
	T_A = 0°C to +85°C		50	
Storage temperature range, T_{stg}		-65	150	°C

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential voltages, are with respect to network ground terminal.
(3) Refer detailed explanation in the application section *Maximum Device Power Dissipation Considerations* .

8.2 ESD Ratings

			MAX	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

8.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	TYP	MAX	UNIT
Input voltage range	VIN	4.5		18(1)	V
	BFET	0		VIN+6	
	dV/dT, EN/UVLO	0		6	
	ILIM	0		3.3	
Continuous output current	I_{OUT}	0		1.7	A
Resistance	ILIM	10		45.3	kΩ
External capacitance	OUT	0.1	1	1000	µF
	dV/dT		1	1000	nF
Operating junction temperature range, T_J		–40	25	125	°C
Operating Ambient temperature range, T_A		–40	25	85	°C

(1) Maximum voltage (including input transients) at VIN pin should not exceed absolute maximum rating as specified in Absolute Maximum Ratings.

8.4 Thermal Information(1)

over operating free-air temperature range (unless otherwise noted)

THERMAL METRIC		TPS2592Zx	UNIT
		DRC (10) PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	45.9	°C/W
$R_{\theta JCtop}$	Junction-to-case (top) thermal resistance	53	
$R_{\theta JB}$	Junction-to-board thermal resistance	21.2	
ψ_{JT}	Junction-to-top characterization parameter	1.2	
ψ_{JB}	Junction-to-board characterization parameter	21.4	
$R_{\theta JCbot}$	Junction-to-case (bottom) thermal resistance	5.9	

(1) For more information about traditional and new thermal metrics, see the IC Package Thermal Metrics application report, SPRA953.

8.5 Electrical Characteristics

–40°C ≤ T_J ≤ 125°C, VIN = 12 V, $V_{EN\ /UVLO}$ = 2 V, R_{ILIM} = 45.3 kΩ, C_{dVdT} = OPEN. All voltages referenced to GND (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VIN (INPUT SUPPLY)						
V_{UVR}	UVLO threshold, rising		4.15	4.3	4.45	V
V_{UVhyst}	UVLO hysteresis(1)			5.4%		
IQ_{ON}	Supply current	Enabled: EN/UVLO = 2 V	0.2	0.42	0.65	mA
IQ_{OFF}		EN/UVLO = 0 V		0.1	0.25	mA
EN/UVLO (ENABLE/UVLO INPUT)						
V_{ENR}	EN Threshold voltage, rising		1.37	1.4	1.44	V
V_{ENF}	EN Threshold voltage, falling		1.32	1.35	1.39	V
I_{EN}	EN Input leakage current	0 V ≤ V_{EN} ≤ 5V	–100	0	100	nA
dV/dT (OUTPUT RAMP CONTROL)						
I_{dVdT}	dV/dT Charging current(1)	V_{dVdT} = 0 V		220		nA
R_{dVdT_disch}	dV/dT Discharging resistance	EN/UVLO = 0 V, I_{dVdT} = 10 mA sinking	50	73	100	Ω
$V_{dVdTmax}$	dV/dT Max capacitor voltage(1)			5.5		V
$GAIN_{dVdT}$	dV/dT to OUT gain(1)	ΔV_{dVdT}		4.85		V/V
ILIM (CURRENT LIMIT PROGRAMMING)						
I_{ILIM}	ILIM Bias current(1)			10		µA
I_{OL}	Overload current limit(2)	R_{ILIM} = 45.3 kΩ, $V_{VIN-OUT}$ = 1 V	1.79	2.10	2.42	A
$I_{OL-R-Short}$		R_{ILIM} = 0 Ω, Shorted Resistor Current Limit (Single Point Failure Test: UL60950)(1)		0.7		A
$I_{OL-R-Open}$		R_{ILIM} = OPEN, Open Resistor Current Limit (Single Point Failure Test: UL60950)(1)		0.55		A
I_{SCL}	Short-circuit current limit(2)	R_{ILIM} = 45.3 kΩ, $V_{VIN-OUT}$ = 12 V	1.66	1.98	2.29	A
$RATIO_{FASTRIP}$	Fast-Trip comparator level w.r.t. overload current limit(1)	$I_{FASTRIP}$: I_{OL}		160%		
$V_{OpenILIM}$	ILIM Open resistor detect threshold(1)	V_{ILIM} Rising, R_{ILIM} = OPEN		3.1		V
OUT (PASS FET OUTPUT)						
$R_{DS(on)}$	FET ON resistance	T_J = 25°C	21	28	33	mΩ
		T_J = 125°C		39	46	
$I_{OUT-OFF-LKG}$	OUT Bias current in off state	$V_{EN/UVLO}$ = 0 V, V_{OUT} = 0 V (Sourcing)	–5	0	1	µA
$I_{OUT-OFF-SINK}$		$V_{EN/UVLO}$ = 0V, V_{OUT} = 300 mV (Sinking)	10	15	20	

(1) These parameters are provided for reference only and do not constitute part of TI's published device specifications for purposes of TI's product warranty.
(2) Pulsed testing techniques used during this test maintain junction temperature approximately equal to ambient temperature.

Electrical Characteristics (continued)

–40°C ≤ T_J ≤ 125°C, VIN = 12 V, $V_{EN\ /UVLO}$ = 2 V, R_{ILIM} = 45.3 kΩ, C_{dVdT} = OPEN. All voltages referenced to GND (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
BFET (BLOCKING FET GATE DRIVER)						
I_{BFET}	BFET Charging current(1)	V_{BFET} = V_{OUT}		2		µA
$V_{BFETmax}$	BFET Clamp voltage(1)			V_{VIN} + 6.4		V
$R_{BFETdisch}$	BFET Discharging resistance to GND	$V_{EN/UVLO}$ = 0 V, I_{BFET} = 100 mA	15	26	36	Ω
TSD (THERMAL SHUT DOWN)						
T_{SHDN}	TSD Threshold, rising(1)			160		°C
$T_{SHDNhyst}$	TSD Hysteresis(1)			10		°C
	Thermal fault: latched or autoretry	TPS2592ZL		LATCHED		
		TPS2592ZA		AUTO-RETRY		

8.6 Timing Requirements

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
T_{ON}	Turn-on delay(1)	EN/UVLO → H to I_{VIN} = 100 mA, 1-A resistive load at OUT		220		µs
t_{OFFdly}	Turn Off delay(2)	EN↓ to BFET↓, C_{BFET} = 0		0.4		µs
dV/dT (OUTPUT RAMP CONTROL)						
t_{dVdT}	Output ramp time	EN/UVLO → H to OUT = 11.7 V, C_{dVdT} = 0	0.7	1	1.3	ms
		EN/UVLO → H to OUT = 11.7 V, C_{dVdT} = 1 nF(2)		12		
ILIM (CURRENT LIMIT PROGRAMMING)						
$t_{FastOffDly}$	Fast-Trip comparator delay(2)	I_{OUT} > $I_{FASTRIP}$ to I_{OUT}= 0 (Switch Off)		3		µs
BFET (BLOCKING FET GATE DRIVER)						
$t_{BFET-ON}$	BFET Turn-On duration(2)	EN/UVLO → H to V_{BFET} = 12 V, C_{BFET} = 1 nF		4.2		ms
		EN/UVLO → H to VB_{FET} = 12 V, C_{BFET} = 10 nF		42		
$t_{BFET-OFF}$	BFET Turn-off duration(2)	EN/UVLO → L to $_{VBFET}$ = 1 V, C_{BFET} = 1 nF		0.4		µs
		EN/UVLO → L to V_{BFET} = 1 V, C_{BFET} = 10 nF		1.4		

(1) These parameters are provided for reference only and do not constitute part of TI's published device specifications for purposes of TI's product warranty.
(2) These parameters are provided for reference only and do not constitute part of TI's published device specifications for purposes of TI's product warranty.

8.7 Typical Characteristics

T_J = 25°C, V_{VIN} = 12 V, $V_{EN/UVLO}$ = 2 V, R_{ILIM} = 45.3 kΩ, C_{VIN} = 0.1 µF, C_{OUT} = 1 µF, C_{dVdT} = OPEN (unless stated otherwise)

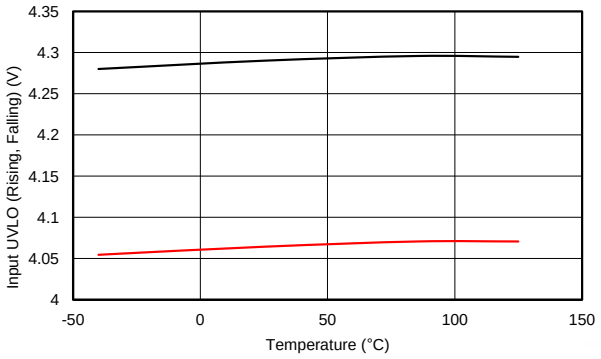


Figure 1. Input UVLO vs Temperature

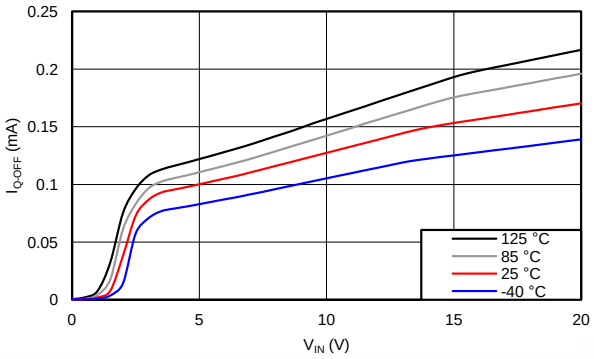
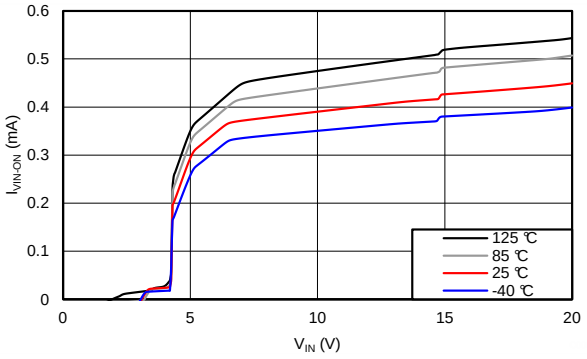


Figure 2. IQ_{OFF} vs V_{IN}



TPS2592Zx

Figure 3. I_{VIN-ON} vs V_{IN}

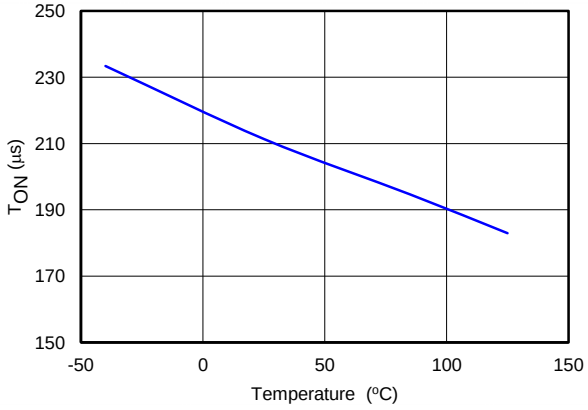


Figure 4. T_{ON} vs Temperature

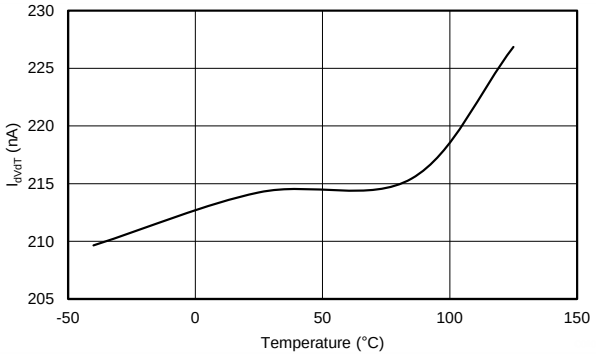
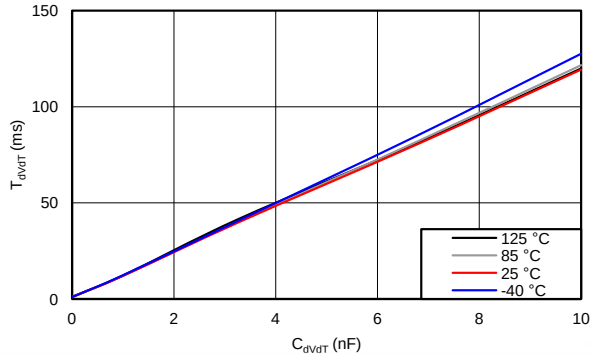


Figure 5. I_{dVdT} vs Temperature



TPS2592Zx

Figure 6. T_{dVdT} vs C_{dVdT}

Typical Characteristics (continued)

T_J = 25°C, V_{VIN} = 12 V, $V_{EN/UVLO}$ = 2 V, R_{ILIM} = 45.3 kΩ, C_{VIN} = 0.1 µF, C_{OUT} = 1 µF, C_{dVdT} = OPEN (unless stated otherwise)

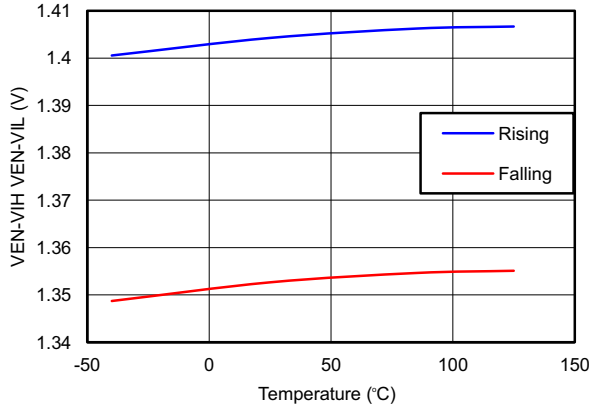


Figure 7. V_{EN_VIH}, V_{EN_VIL} vs Temperature

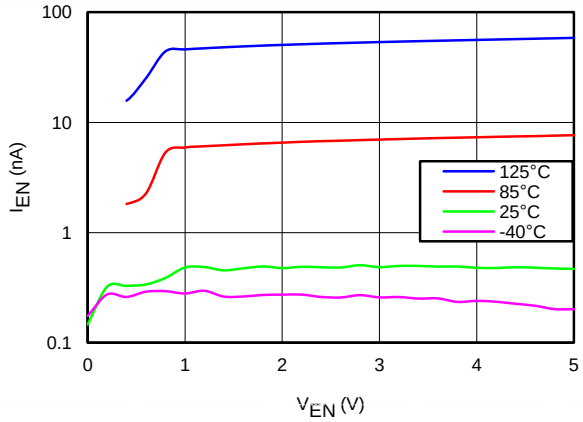
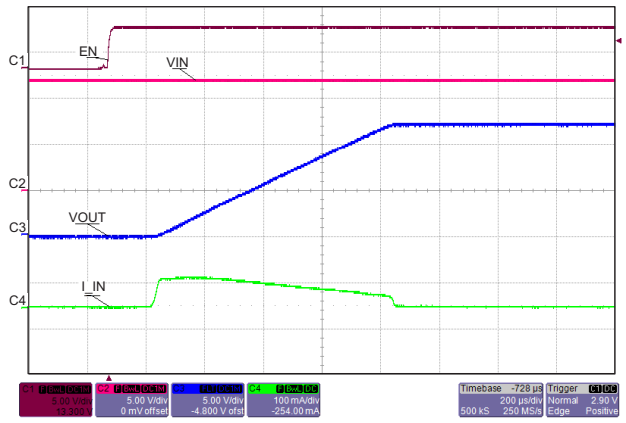
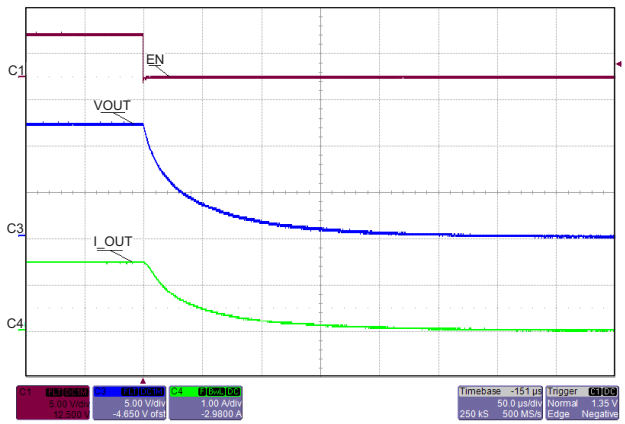


Figure 8. I_{EN} (Leakage Current) vs V_{EN}



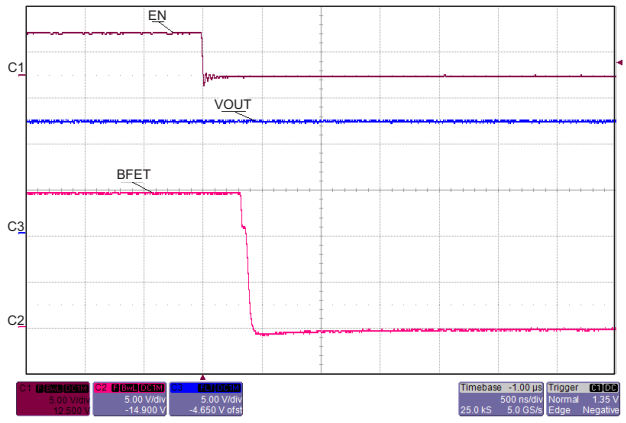
TPS2592Zx, C_{dVdT} = OPEN, C_{OUT} = 4.7 µF

Figure 9. Transient: Output Ramp:



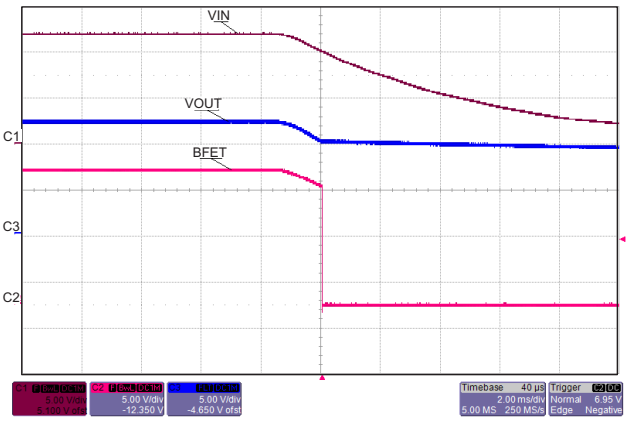
EN ↓

Figure 10. Transient: Turn Off Delay



EN↓

Figure 11. Turn Off Delay to BFET



VIN↓

Figure 12. Turn Off Delay to BFET

Typical Characteristics (continued)

T_J = 25°C, V_{VIN} = 12 V, $V_{EN/UVLO}$ = 2 V, R_{ILIM} = 45.3 kΩ, C_{VIN} = 0.1 µF, C_{OUT} = 1 µF, C_{dVdT} = OPEN (unless stated otherwise)

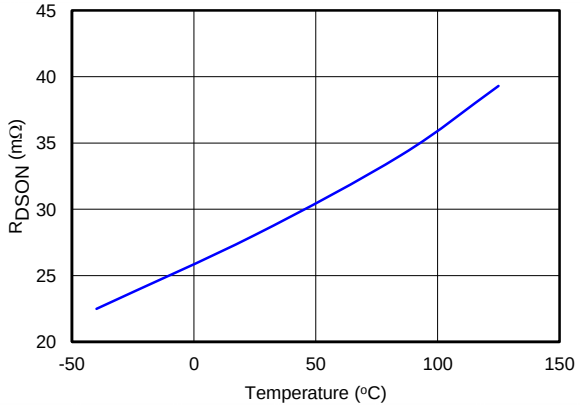
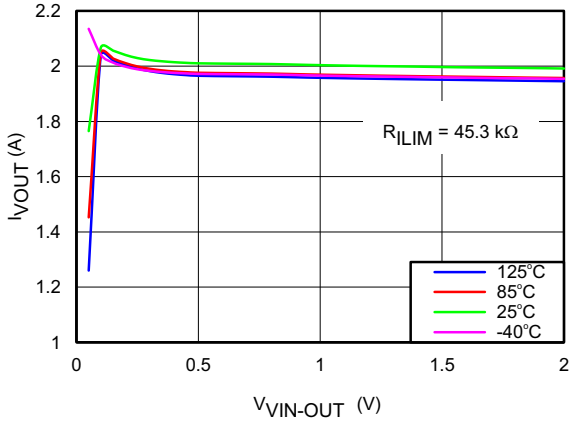
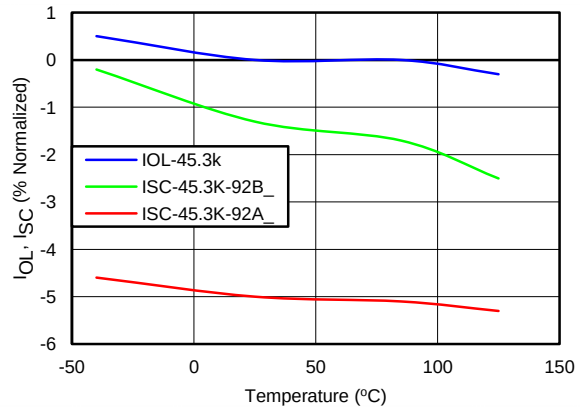


Figure 13. R_{DSON} vs Temperature



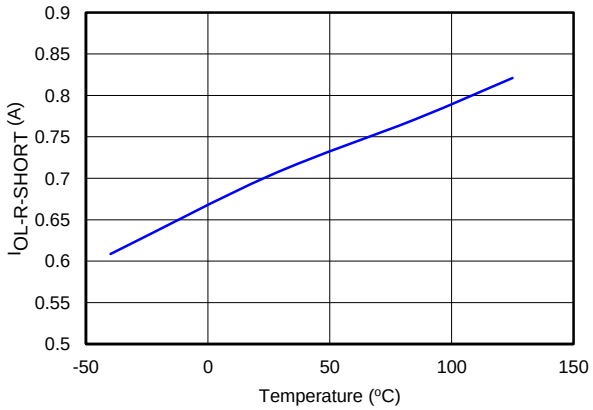
45.3 kΩ

Figure 14. I_{OUT} vs $V_{VIN-OUT}$



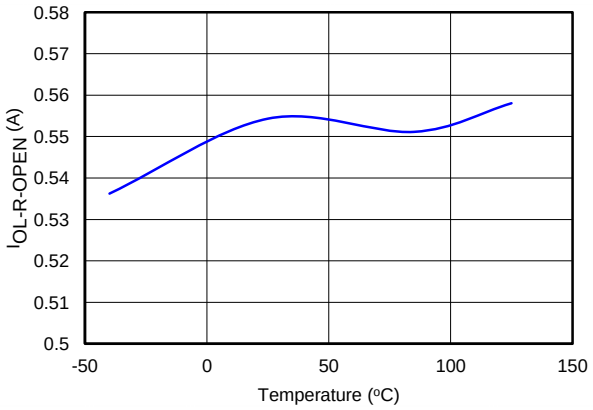
45.3 kΩ

Figure 15. I_{OL}, I_{SC} vs Temperature



R_{ILIM} = 0

Figure 16. $I_{OL-R-Short}$ vs Temperature



R_{ILIM} = OPEN

Figure 17. $I_{OL-R-Open}$ vs Temperature

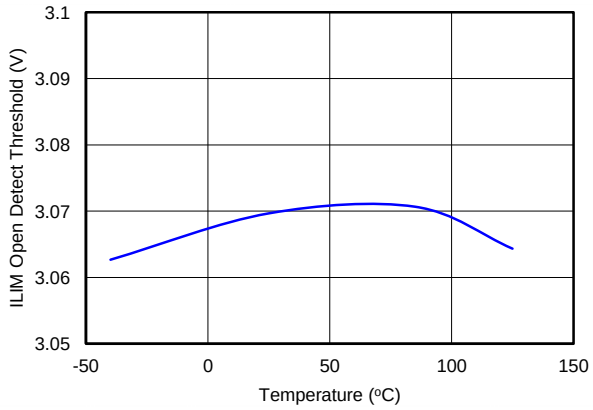


Figure 18. $V_{OpenILIM}$ vs Temperature

Typical Characteristics (continued)

T_J = 25°C, V_{VIN} = 12 V, $V_{EN/UVLO}$ = 2 V, R_{ILIM} = 45.3 kΩ, C_{VIN} = 0.1 µF, C_{OUT} = 1 µF, C_{dVdT} = OPEN (unless stated otherwise)

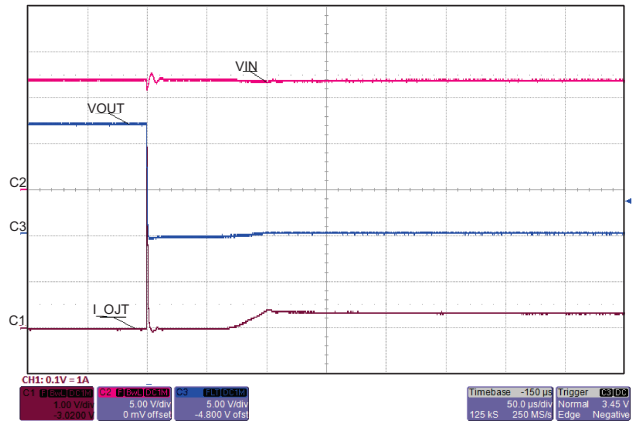


Figure 19. Transient: Output Short Circuit

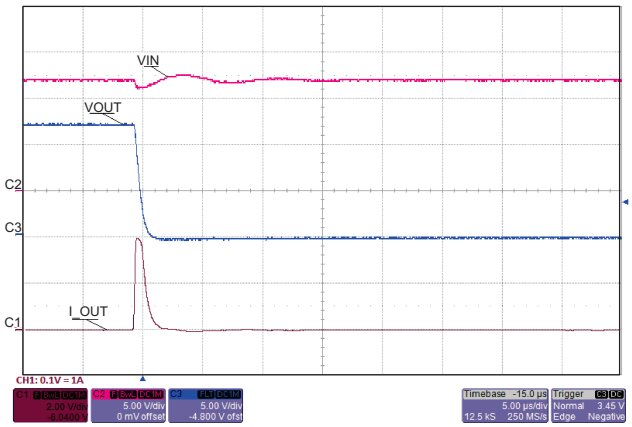
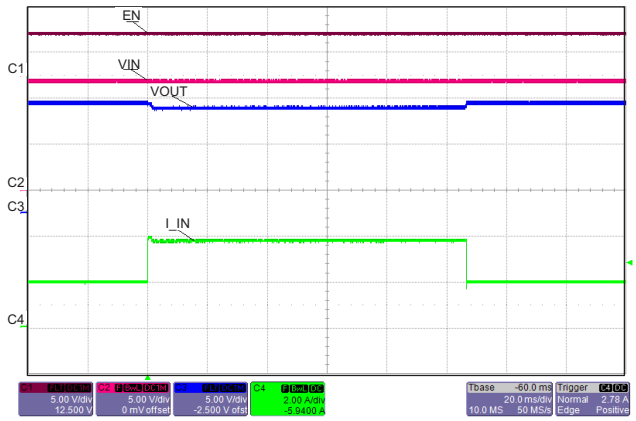
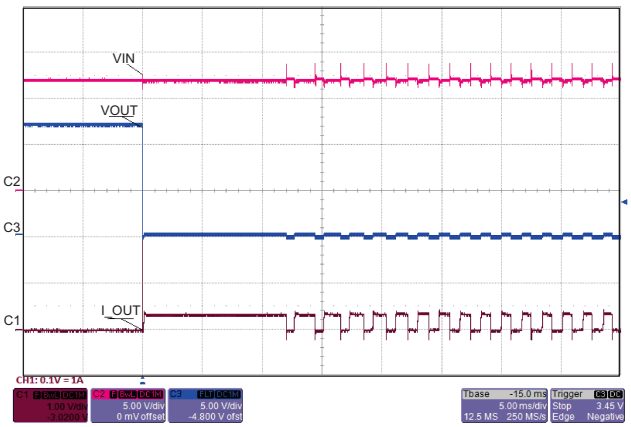


Figure 20. Short Circuit (Zoom): Fast-trip Comparator



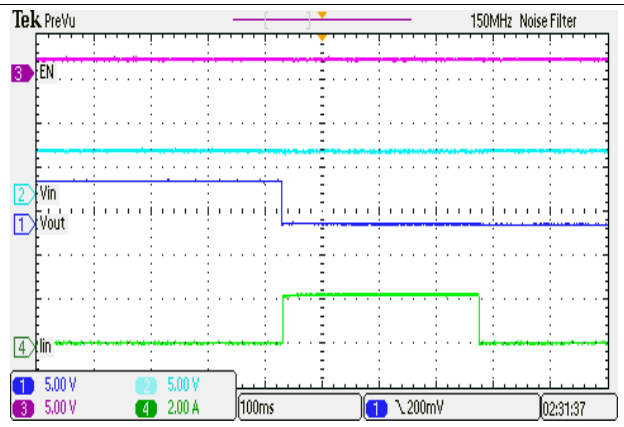
I_{LOAD} Stepped From 50% to 120%, back to 50%

Figure 21. Transient: Overload Current Limit



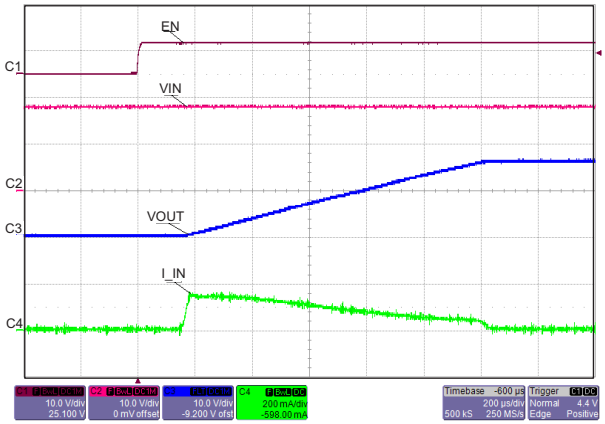
TPS2592ZA

Figure 22. Transient: Thermal Fault Auto-Retry



TPS2592ZL

Figure 23. Transient: Thermal Fault Latched



TPS2592Zx, C_{dVdT} = OPEN, C_{OUT} = 10 µF

Figure 24. Transient: Output Ramp

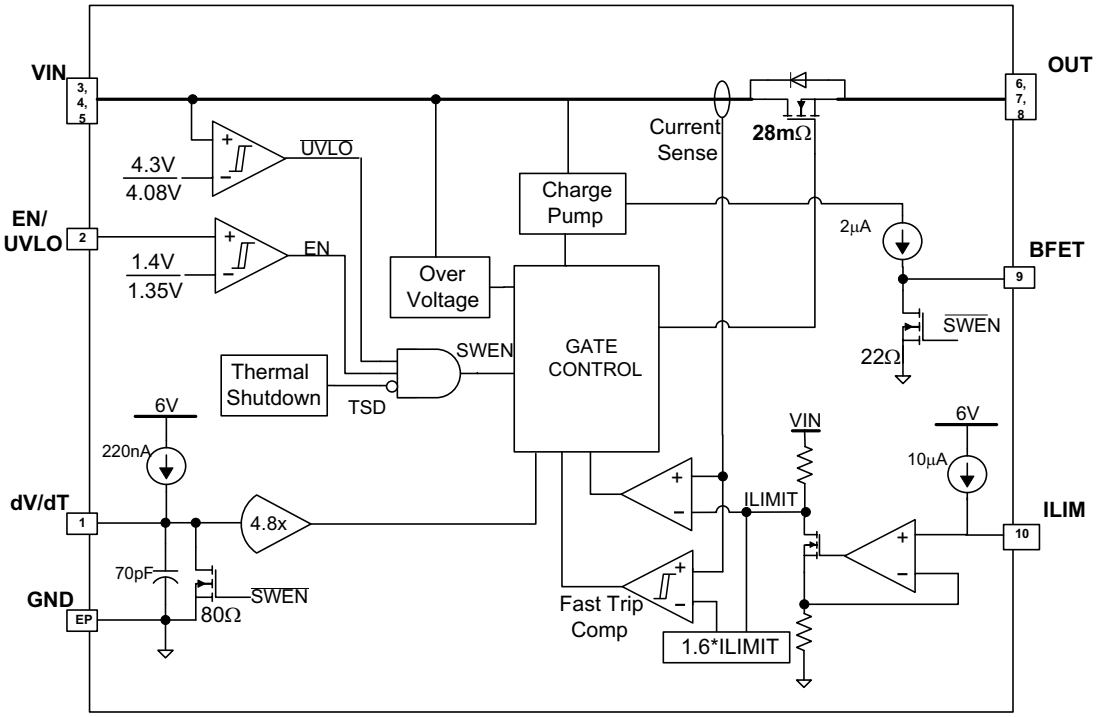
9 Detailed Description

9.1 Overview

The TPS2592xx is an e-fuse with integrated power switch that is used to manage current/voltage/start-up voltage ramp to a connected load. The device starts its operation by monitoring the VIN bus. When VIN exceeds the undervoltage-lockout threshold (V_{UVR}), the device samples the EN/UVLO pin. A high level on this pin enables the internal MOSFET. As VIN rises, the internal MOSFET of the device will start conducting and allow current to flow from VIN to OUT. When EN/UVLO is held low (below V_{ENF}), internal MOSFET is turned off. User also has the ability to modify the output voltage ramp time by connecting a capacitor between dV/dT pin and GND.

After a successful start-up sequence, the device now actively monitors its load current, ensuring that the adjustable overload current limit I_{OL} is not exceeded. The device also has built-in thermal sensor. In the event device temperature (T_J) exceeds T_{SHDN}, typically 160°C, the thermal shutdown circuitry will shut down the internal MOSFET thereby disconnecting the load from the supply. In TPS2592xL, the output will remain disconnected (MOSFET open) until power to device is recycled or EN/UVLO is toggled (pulled low and then high). The TPS2592xA device will remain off during a cooling period until device temperature falls below T_{SHDN} – 10°C, after which it will attempt to restart. This ON and OFF cycle will continue until fault is cleared.

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 GND

This is the most negative voltage in the circuit and is used as a reference for all voltage measurements unless otherwise specified.

9.3.2 VIN

Input voltage to the TPS2592Zx. A ceramic bypass capacitor close to the device from VIN to GND is recommended to alleviate bus transients. The recommended operating voltage range is 4.5 V to 18 V for TPS2592Zx. The device can continuously sustain a voltage of 20 V on VIN pin. However, above the recommended maximum bus voltage, the device will be in over-voltage protection (OVP) mode, limiting the output voltage to V_{OVC}. The power dissipation in OVP mode is P_{D_OVP} = (V_{VIN} - V_{OVC}) x I_{OUT}, which can potentially heat up the device and cause thermal shutdown.

Feature Description (continued)

9.3.3 dV/dT

Connect a capacitor from this pin to GND to control the slew rate of the output voltage at power-on. This pin can be left floating to obtain a predetermined slew rate (minimum T_{dVdT}) on the output. Equation governing slew rate at start-up is shown below:

$$\frac{dV_{OUT}}{dt} = \frac{I_{dVdT} \times GAIN_{dVdT}}{C_{dVdT} + C_{INT}} \quad (1)$$

Where:

I_{dVdT} = 220 nA (TYP)
C_{INT} = 70 pF (TYP)
$GAIN_{dVdT}$ = 4.85
$\frac{dV_{OUT}}{dT}$ = Desired output slew rate

The total ramp time (T_{dVdT}) for 0 to VIN can be calculated using the following equation:

$$T_{dVdT} = 10^6 \times V_{IN} \times (C_{dVdT} + 70\ pF) \quad (2)$$

For details on how to select an appropriate charging time/rate, refer to the applications section: *Setting Output Voltage Ramp Time (T_{dVdT})*

9.3.4 BFET

Connect this pin to an external NFET that can be used to disconnect input supply from rest of the system in the event of power failure at VIN. The BFET pin is controlled by either UVLO event or EN/UVLO (see Table 1). BFET can source charging current of 2 µA (TYP) and sink (discharge) current from the gate of the external FET via a 26-Ω internal discharge resistor to initiate fast turn-off, typically <1 µs. Due to 2 µA charging current, it is recommended to use >10 MΩ impedance when probing the BFET node.

Table 1.

EN/UVLO > V_{ENR}	VIN>V_{UVR}	BFET MODE
H	H	Charge
X	L	Discharge
L	X	Discharge

9.3.5 EN/UVLO

As an input pin, it controls both the ON/OFF state of the internal MOSFET and that of the external blocking FET. In its high state, the internal MOSFET is enabled and charging begins for the gate of external FET. A low on this pin will turn off the internal MOSFET and pull the gate of the external FET to GND via the built-in discharge resistor. High and Low levels are specified in the parametric table of the datasheet. The EN/UVLO pin is also used to clear a thermal shutdown latch in the TPS2592xL by toggling this pin (H→L).

The internal de-glitch delay on EN/UVLO falling edge is intentionally kept low (1 us typical) for quick detection of power failure. When used with a resistor divider from supply to EN/UVLO to GND, power-fail detection on EN/UVLO helps in quick turn-off of the BFET driver, thereby stopping the flow of reverse current. For applications where a higher de-glitch delay on EN/UVLO is desired, or when the supply is particularly noisy, it is recommended to use an external bypass capacitor from EN/UVLO to GND.

9.3.6 ILIM

The device continuously monitors the load current and keeps it limited to the value programmed by R_{ILIM}. After start-up event and during normal operation, current limit is set to I_{OL} (over-load current limit).

$$I_{OL} = \left(0.7 + 3 \times 10^{-5} \times R_{ILIM}\right) \quad (3)$$

When power dissipation in the internal MOSFET [$P_D = (V_{VIN} - V_{OUT}) \times I_{OUT}$] exceeds 10 W, there is a 2% – 12% thermal foldback in the current limit value so that I_{OL} drops to I_{SC}. In each of the two modes, MOSFET gate voltage is regulated to throttle short-circuit and overload current flowing to the load. Eventually, the device shuts down due to over temperature.

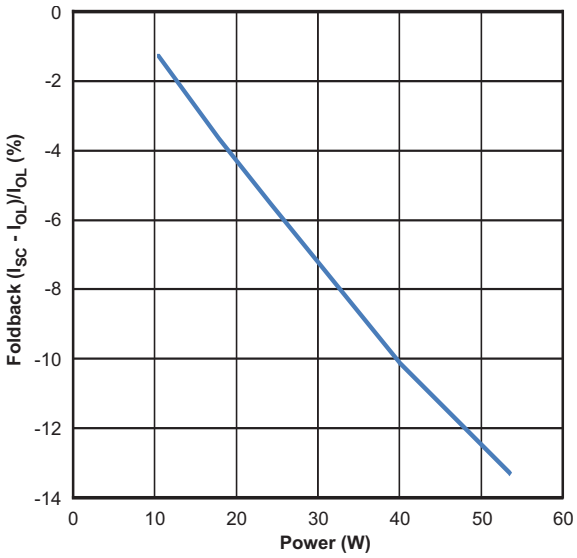


Figure 25. Thermal Foldback in Current Limit

During a transient short circuit event, the current through the device increases very rapidly. The current-limit amplifier cannot respond very quickly to this event due to its limited bandwidth. Therefore, the TPS2592 incorporates a fast-trip comparator, which shuts down the pass device very quickly when $I_{OUT} > I_{FASTRIP}$, and terminates the rapid short-circuit peak current. The trip threshold is set to 60% higher than the programmed over-load current limit ($I_{FASTRIP} = 1.6 \times I_{OL}$). After the transient short-circuit peak current has been terminated by the fast-trip comparator, the current limit amplifier smoothly regulates the output current to I_{OL} (see figure below).

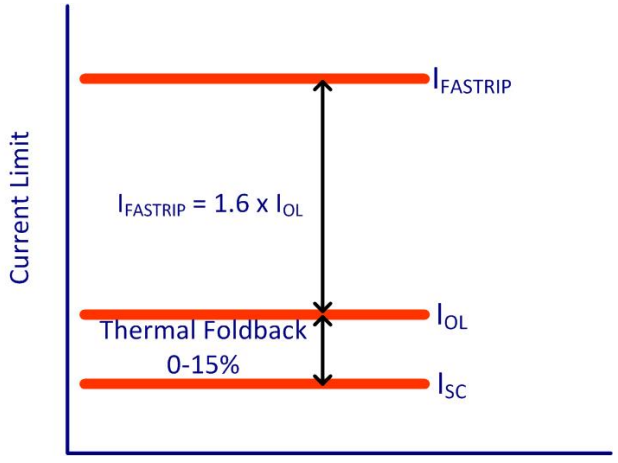


Figure 26. Fast-Trip Current

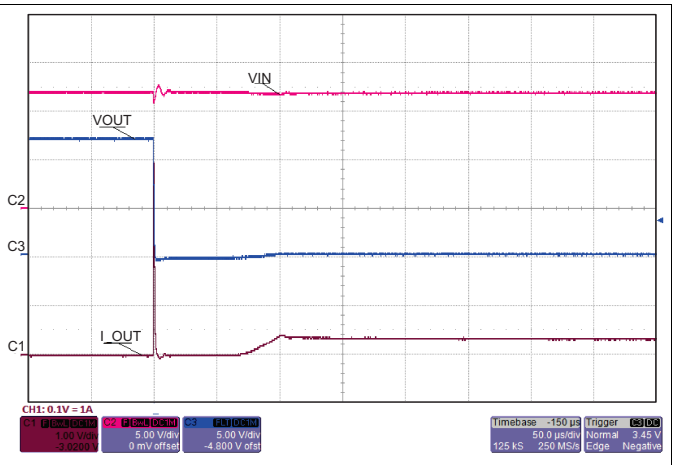


Figure 27. Fast-Trip and Current Limit Amplifier Response for Short Circuit

9.4 Device Functional Modes

The TPS2592xx is a hot-swap controller with integrated power switch that is used to manage current/voltage/start-up voltage ramp to a connected load. The device starts its operation by monitoring the VIN bus. When V_{VIN} exceeds the undervoltage-lockout threshold (V_{UVR}), the device samples the EN/UVLO pin. A high level on this pin enables the internal MOSFET and also start charging the gate of external blocking FET (if connected) via the BFET pin. As VIN rises, the internal MOSFET of the device and external FET (if connected) will start conducting and allow current to flow from VIN to OUT. When EN/UVLO is held low (that is, below V_{ENF}), the internal MOSFET is turned off and BFET pin is discharged, thereby, blocking the flow of current from VIN to OUT. User also has the ability to modify the output voltage ramp time by connecting a capacitor between dV/dT pin and GND.

Having successfully completed its start-up sequence, the device now actively monitors its load current and input voltage, ensuring that the adjustable overload current limit I_{OL} is not exceeded and input voltage spikes are safely clamped to V_{OVC} level at the output. This keeps the output device safe from harmful voltage and current transients. The device also has built-in thermal sensor. In the event device temperature (T_J) exceeds T_{SHDN} , typically 160°C, the thermal shutdown circuitry will shut down the internal MOSFET thereby disconnecting the load from the supply. In the TPS2592xL, the output will remain disconnected (MOSFET open) until power to device is recycled or EN/UVLO is toggled (pulled low and then high). The TPS2592xA device will remain off during a cooling period until device temperature falls below T_{SHDN} – 10°C, after which it will attempt to restart. This ON and OFF cycle will continue until fault is cleared.

10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

The TPA2592xx is a smart eFuse. It is typically used for Hot-Swap and Power rail protection applications. It operates from 4.5 V to 18 V with programmable current limit and undervoltage protection. The device aids in controlling the in-rush current and provides precise current limiting during overload conditions for systems such as Set-Top-Box, DTVs, Gaming Consoles, SSDs/HDDs and Smart Meters. The device also provides robust protection for multiple faults on the sub-system rail.

The following design procedure can be used to select component values for the device. Alternatively, the WEBENCH® software may be used to generate a complete design. The WEBENCH® software uses an iterative design procedure and accesses a comprehensive database of components when generating a design. Additionally, a spreadsheet design tool TPS2592 Design Calculator (SLUC571) is available on web folder. This section presents a simplified discussion of the design process.

10.2 Typical Applications

10.2.1 Simple 2.1-A eFuse Protection for Set Top Boxes

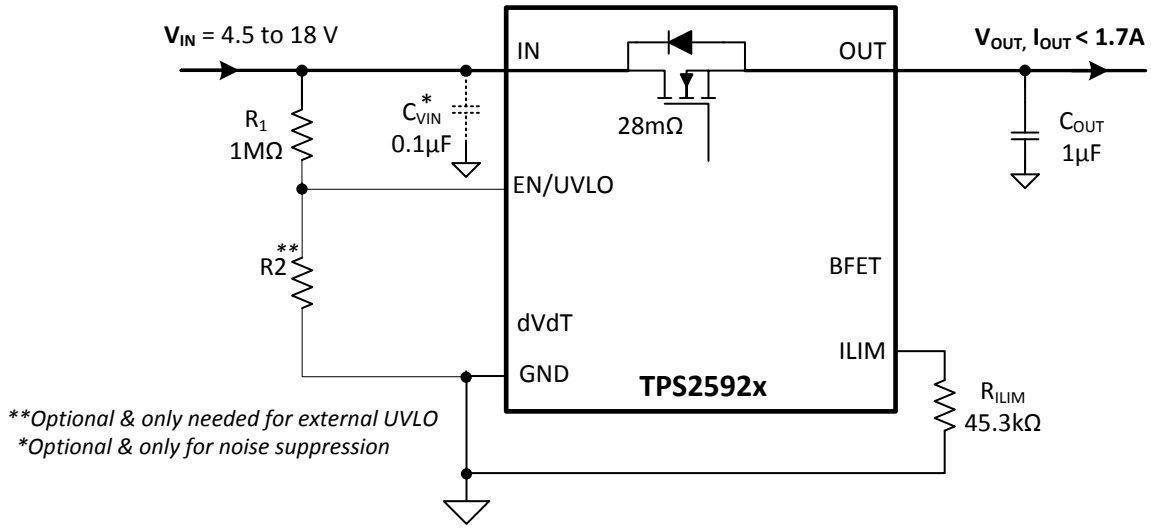


Figure 28. Typical Application Schematic: Simple e-Fuse for STBs

10.2.1.1 Design Requirements

Table 2. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range, V_{IN}	12 V
Undervoltage lockout set point, $V_{(UV)}$	Default: V_{UVR} = 4.3 V
Load at Start-Up , $R_{L(SU)}$	4 Ω
Current limit, $I_{OL} = I_{ILIM}$	2.1 A
Load capacitance , C_{OUT}	1 µF
Maximum ambient temperatures , T_A	85°C

10.2.1.2 Detailed Design Procedure

The following design procedure can be used to select component values for the TPS2592xx.

10.2.1.2.1 Step by Step Design Procedure

This design procedure below seeks to control the junction temperature of device under both static and transient conditions by proper selection of output ramp-up time and associated support components. The designer can adjust this procedure to fit the application and design criteria.

10.2.1.2.2 Programming the Current-Limit Threshold: R_{ILIM} Selection

The R_{ILIM} resistor at the ILIM pin sets the over load current limit, this can be set using Equation 4.

$$R_{ILIM} = \frac{I_{ILIM} - 0.7}{3 \times 10^{-5}} \quad (4)$$

For I_{OL} = I_{ILIM} = 2.1 A, from equation 4, R_{ILIM} = 45.3 kΩ, choose closest standard value resistor with 1% tolerance.

10.2.1.2.3 Undervoltage Lockout Set Point

The undervoltage lockout (UVLO) trip point is adjusted using the external voltage divider network of R_1 and R_2 as connected between IN, EN/UVLO and GND pins of the device. The values required for setting the undervoltage are calculated solving Equation 5.

$$V_{(UV)} = \frac{R_1 + R_2}{R_2} \times V_{ENR} \quad (5)$$

Where V_{ENR} = 1.4 V is enable voltage rising threshold.

Since R_1 and R_2 will leak the current from input supply (VIN), these resistors should be selected based on the acceptable leakage current from input power supply (VIN). The current drawnby R_1 and R_2 from the power supply {$I_{R12} = V_{IN}/(R_1 + R_2)$}.

However, leakage currents due to external active components connected to the resistor string can add error to these calculations. So, the resistor string current, I_{R12} must be chosen to be 20x greater than the leakage current expected.

For default UVLO of V_{UVR} = 4.3 V, select R_2 = OPEN, and R_1 = 1 MΩ. Since EN/UVLO pin is rated only to 7 V, it cannot be connected directly to VIN = 12 V. It has to be connected through R_1 = 1 MΩ only, so that the pull-up current for EN/UVLO pin is limited to < 20 µA.

The power failure threshold is detected on the falling edge of supply. This threshold voltage is 4% lower than the rising threshold, V_{UVR}. This is calculated using Equation 6.

$$V_{(PFAIL)} = 0.96 \times V_{UVR} \quad (6)$$

Where V_{UVR} is 4.3V, Power fail threshold set is : 4.1 V

10.2.1.2.4 Setting Output Voltage Ramp Time (T_{dVdT})

For a successful design, the junction temperature of device should be kept below the absolute-maximum rating during both dynamic (start-up) and steady state conditions. Dynamic power stresses often are an order of magnitude greater than the static stresses, so it is important to determine the right start-up time and in-rush current limit required with system capacitance to avoid thermal shutdown during start-up with and without load.

The ramp-up capacitor C_{dVdT} needed is calculated considering the two possible cases:

10.2.1.2.4.1 Case 1: Start-up without Load: Only Output Capacitance C_{OUT} Draws Current During Start-up

During start-up, as the output capacitor charges, the voltage difference as well as the power dissipated across the internal FET decreases. The average power dissipated in the device during start-up is calculated using Equation 8.

For TPS2592xx, the inrush current is determined as,

$$I_{(INRUSH)} = C_{(OUT)} \times \frac{V_{(IN)}}{T_{dVdT}} \quad (7)$$

Power dissipation during start-up is:

$$P_{D(INRUSH)} = 0.5 \times V_{(IN)} \times I_{(INRUSH)} \quad (8)$$

Equation 8 assumes that load does not draw any current until the output voltage has reached its final value.

10.2.1.2.4.2 Case 2: Start-up with Load: Output Capacitance C_{OUT} and Load Draws Current During Start-up

When load draws current during the turn-on sequence, there will be additional power dissipated. Considering a resistive load during start-up ($R_{L(SU)}$), load current ramps up proportionally with increase in output voltage during T_{dVdT} time. The average power dissipation in the internal FET during charging time due to resistive load is given by:

$$P_{D(LOAD)} = \left(\frac{1}{6}\right) \times \frac{V^2_{(IN)}}{R_{L(SU)}} \quad (9)$$

Total power dissipated in the device during startup is:

$$P_{D(STARTUP)} = P_{D(INRUSH)} + P_{D(LOAD)} \quad (10)$$

Total current during startup is given by:

$$I_{(STARTUP)} = I_{(INRUSH)} + I_L(t) \quad (11)$$

If $I_{(STARTUP)} > I_{OL}$, the device limits the current to I_{OL} and the current limited charging time is determined by:

$$T_{dVdT(Current\text{-}Limited)} = C_{OUT} \times R_{L(SU)} \times \left[\frac{I_{OL}}{I_{(INRUSH)}} - 1 + LN\left(\frac{I_{(INRUSH)}}{I_{OL} - \frac{V_{(IN)}}{R_{L(SU)}}}\right)\right] \quad (12)$$

The power dissipation, with and without load, for selected start-up time should not exceed the shutdown limits as shown in Figure 29.

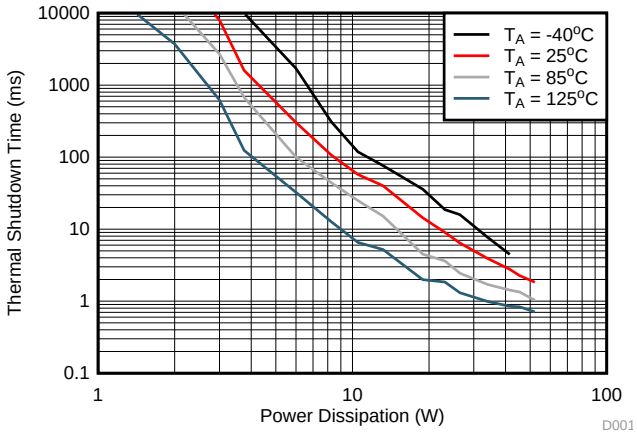


Figure 29. Thermal Shutdown Limit Plot

For the design example under discussion, select ramp-up capacitor C_{dVdT} = OPEN. Then, using Equation 2.

$$T_{dVdT} = 10^6 \times 12 \times (0 + 70\ pF) = 840\ \mu s \quad (13)$$

The inrush current drawn by the load capacitance (C_{OUT}) during ramp-up using Equation 7.

$$I_{(INRUSH)} = 1\ \mu F \times \frac{12}{840\ \mu s} = 15\ mA \quad (14)$$

The inrush Power dissipation is calculated, using Equation 8.

$$P_{D(INRUSH)} = 0.5 \times 12 \times 15\ m = 90\ mW \quad (15)$$

For 90 mW of power loss, the thermal shut down time of the device should not be less than the ramp-up time T_{dVdT} to avoid the false trip at maximum operating temperature. From thermal shutdown limit graph Figure 29 at T_A = 85°C, for 90 mW of power, the shutdown time is infinite. So it is safe to use 0.79 ms as start-up time without any load on output.

Considering the start-up with load 4 Ω, the additional power dissipation, when load is present during start up is calculated, using Equation 9.

$$P_{D(LOAD)} = \frac{12 \times 12}{6 \times 4} = 6 \text{ W} \quad (16)$$

The total device power dissipation during start up is:

$$P_{D(STARTUP)} = 6 + 90 \text{ m} = 6.09 \text{ W} \quad (17)$$

From thermal shutdown limit graph at T_A = 85°C, the thermal shutdown time for 6.09 W is more than 100 ms. So it is well within acceptable limits to use no external capacitor ($C_{dV/dT}$) with start-up load of 4 Ω.

If, due to large C_{OUT}, there is a need to decrease the power loss during start-up, it can be done with increase of C_{dVdT} capacitor.

10.2.1.3 Support Component Selection - C_{VIN}

C_{VIN} is a bypass capacitor to help control transient voltages, unit emissions, and local supply noise. Where acceptable, a value in the range of 0.001 µF to 0.1 µF is recommended for C_{VIN}.

10.2.1.4 Application Curves

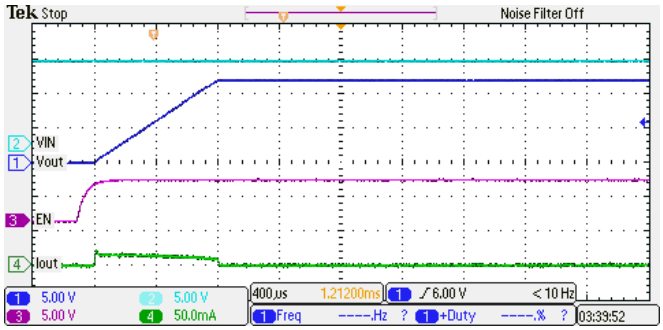


Figure 30. Output Ramp without Load on Output

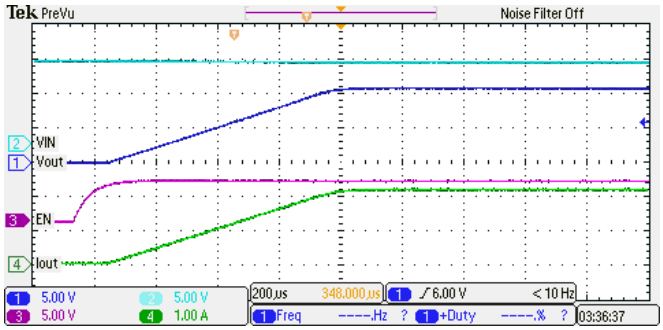


Figure 31. Output Ramp with 4-Ω Load at Start Up

10.3 Maximum Device Power Dissipation Considerations

To prevent damage to the TPS2592x, it is necessary to keep internal power dissipation (P_D) below the levels specified in below Table. The power dissipation is defined as ($P_D = (V_{IN} – V_{OUT}) \times I_{OUT}$).

		MIN	MAX	UNIT
Maximum Power Dissipation	–40°C ≤ T_A ≤ +85°C		40	W
	0°C ≤ T_A ≤ +85°C		50	

During normal operation P_D is low (typically < ½ Watt) because the FET is fully on with low ($V_{IN} – V_{OUT}$). However, during short circuit and surge protection the FET may be only partially on and ($V_{IN} – V_{OUT}$) can be high.

Example 1: Short Circuit on Output → V_{IN} = 15 V, I_{LIMIT} = 2.1 A. T_J = –40°C

- P_D = 15 V x 2.1 A = 31.5 W
- OK → (P_D = 31.5 W) < (P_{D_MAX} = 40 W)

Example 2: Short Circuit on Output → V_{IN} = 18 V, I_{LIMIT} = 2.1 A

- P_D = 18 V x 2.1 A = 37.8 W
- OK at T_J = 0°C → (P_D = 37.8 W) < (P_{D_MAX} at 0°C = 50 W)
- OK at T_J = –40°C → (P_D = 37.8 W) > (P_{D_MAX} at –40°C = 40 W)

11 Power Supply Recommendations

The device is designed for supply voltage range of 4.5 V ≤ V_{IN} ≤ 18 V. If the input supply is located more than a few inches from the device an input ceramic bypass capacitor higher than 0.1 µF is recommended. Power supply should be rated higher than the current limit set to avoid voltage droops during over current and short-circuit conditions.

11.1 Transient Protection

In case of short circuit and over load current limit, when the device interrupts current flow, input inductance generates a positive voltage spike on the input and output inductance generates a negative voltage spike on the output. The peak amplitude of voltage spikes (transients) is dependent on value of inductance in series to the input or output of the device. Such transients can exceed the *Absolute Maximum Ratings* of the device if steps are not taken to address the issue.

Typical methods for addressing transients include

- Minimizing lead length and inductance into and out of the device
- Using large PCB GND plane
- Schottky diode across the output to absorb negative spikes
- A low value ceramic capacitor ($C_{(IN)}$ = 0.001 µF to 0.1 µF) to absorb the energy and dampen the transients. The approximate value of input capacitance can be estimated with Equation 18.

$$V_{SPIKE(Absolute)} = V_{(IN)} + I_{(LOAD)} \times \sqrt{\frac{L_{(IN)}}{C_{(IN)}}} \quad (18)$$

Where:

- $V_{(IN)}$ is the nominal supply voltage
- $I_{(LOAD)}$ is the load current,
- $L_{(IN)}$ equals the effective inductance seen looking into the source
- $C_{(IN)}$ is the capacitance present at the input

Some applications may require the addition of a Transient Voltage Suppressor (TVS) to prevent transients from exceeding the *Absolute Maximum Ratings* of the device.

The circuit implementation with optional protection components (a ceramic capacitor, TVS and schottky diode) is shown in Figure 32.

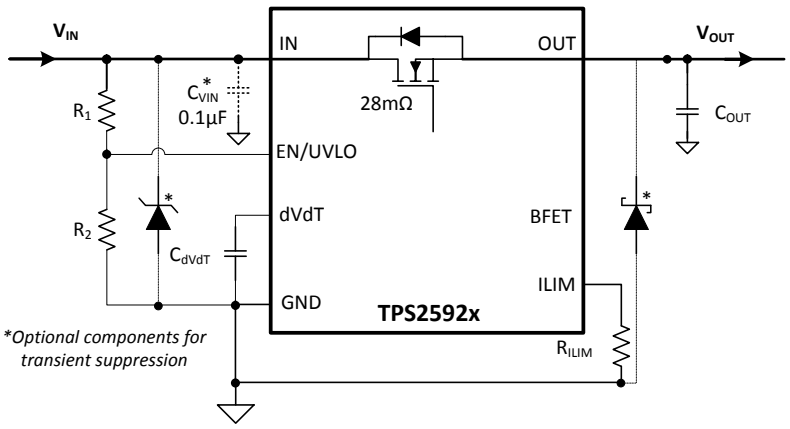


Figure 32. Circuit Implementation with Optional Protection Components

11.2 Output Short-Circuit Measurements

It is difficult to obtain repeatable and similar short-circuit testing results. Source bypassing, input leads, circuit layout and component selection, output shorting method, relative location of the short, and instrumentation all contribute to variation in results. The actual short itself exhibits a certain degree of randomness as it microscopically bounces and arcs. Care in configuration and methods must be used to obtain realistic results. Do not expect to see waveforms exactly like those in the data sheet; every setup differs.

12 Layout

12.1 Layout Guidelines

- For all applications, a 0.01-uF or greater ceramic decoupling capacitor is recommended between IN terminal and GND. For hot-plug applications, where input power path inductance is negligible, this capacitor can be eliminated/minimized.
- The optimum placement of decoupling capacitor is closest to the IN and GND terminals of the device. Care must be taken to minimize the loop area formed by the bypass-capacitor connection, the IN terminal, and the GND terminal of the IC. See Figure 33 for a PCB layout example.
- High current carrying power path connections should be as short as possible and should be sized to carry at least twice the full-load current.
- The GND terminal must be tied to the PCB ground plane at the terminal of the IC. The PCB ground should be a copper plane or island on the board.
- Locate all support components: R_{ILIM}, C_{dVdT} and resistors for EN/UVLO, close to their connection pin. Connect the other end of the component to the GND pin of the device with shortest trace length. The trace routing for the R_{ILIM} and C_{dVdT} components to the device should be as short as possible to reduce parasitic effects on the current limit and soft start timing. These traces should not have any coupling to switching signals on the board.
- Protection devices such as TVS, snubbers, capacitors, or diodes should be placed physically close to the device they are intended to protect, and routed with short traces to reduce inductance. For example, a protection Schottky diode is recommended to address negative transients due to switching of inductive loads, and it should be physically close to the OUT pins.
- Obtaining acceptable performance with alternate layout schemes is possible; however this layout has been shown to produce good results and is intended as a guideline.

12.2 Layout Example

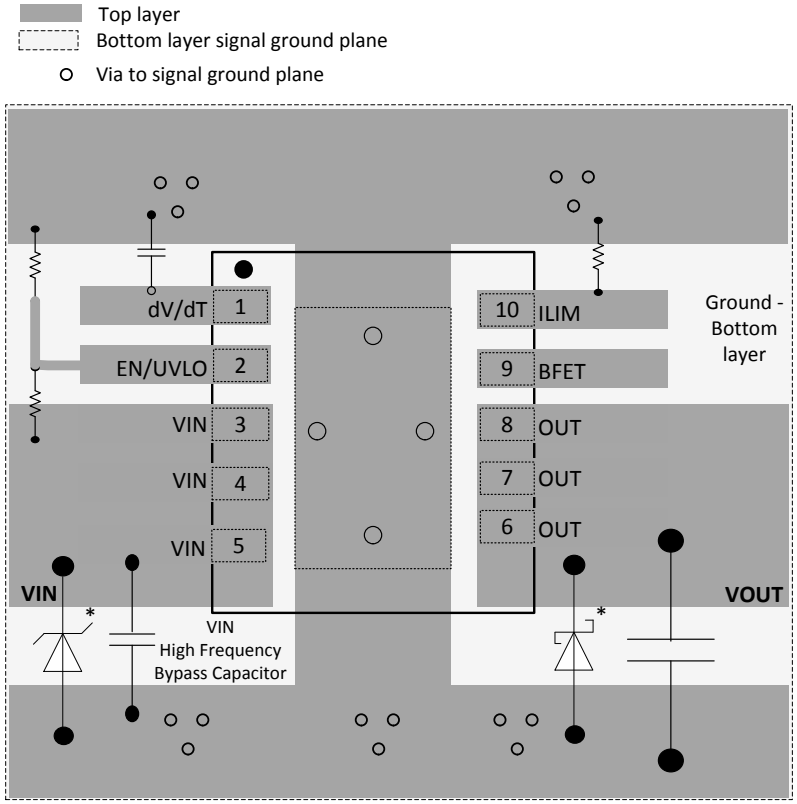


Figure 33. Layout Example

13 Device and Documentation Support

13.1 Device Support

13.1.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

13.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 3. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TPS2592ZA	Click here	Click here	Click here	Click here	Click here
TPS2592ZL	Click here	Click here	Click here	Click here	Click here

13.3 Trademarks

PowerPAD is a trademark of Texas Instruments.
WEBENCH is a registered trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

13.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS2592ZADRCR	NRND	VSON	DRC	10	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2592ZA	
TPS2592ZADRCT	NRND	VSON	DRC	10	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2592ZA	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) RoHS: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

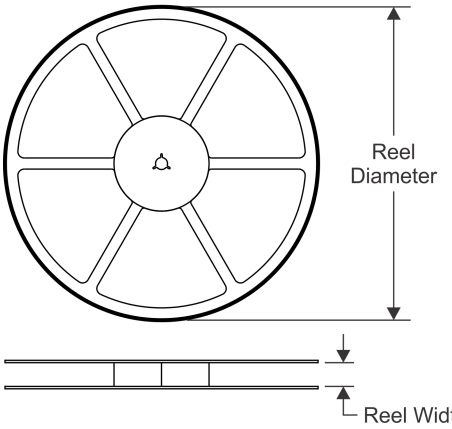
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

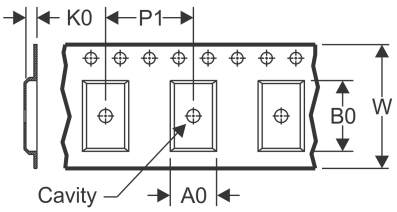
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

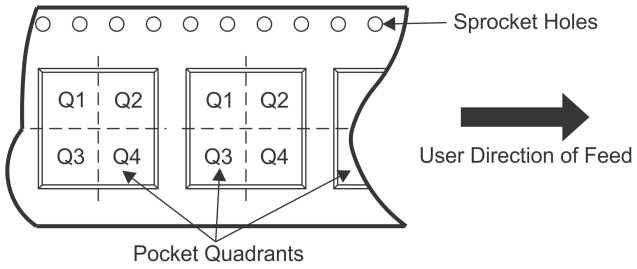


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

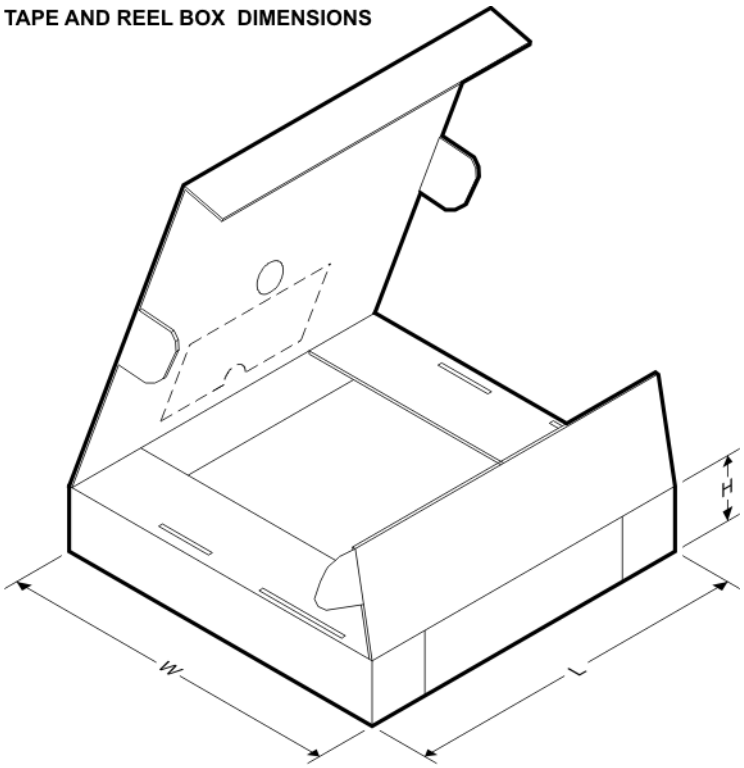
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS2592ZADRCR	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS2592ZADRCT	VSON	DRC	10	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS2592ZADRCR	VSON	DRC	10	3000	367.0	367.0	35.0
TPS2592ZADRCT	VSON	DRC	10	250	210.0	185.0	35.0

GENERIC PACKAGE VIEW

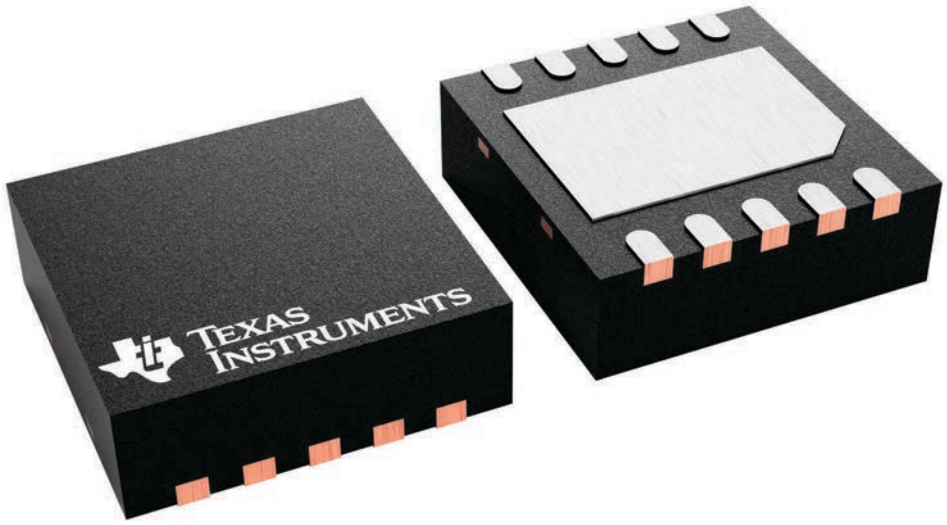
DRC 10

VSON - 1 mm max height

3 x 3, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



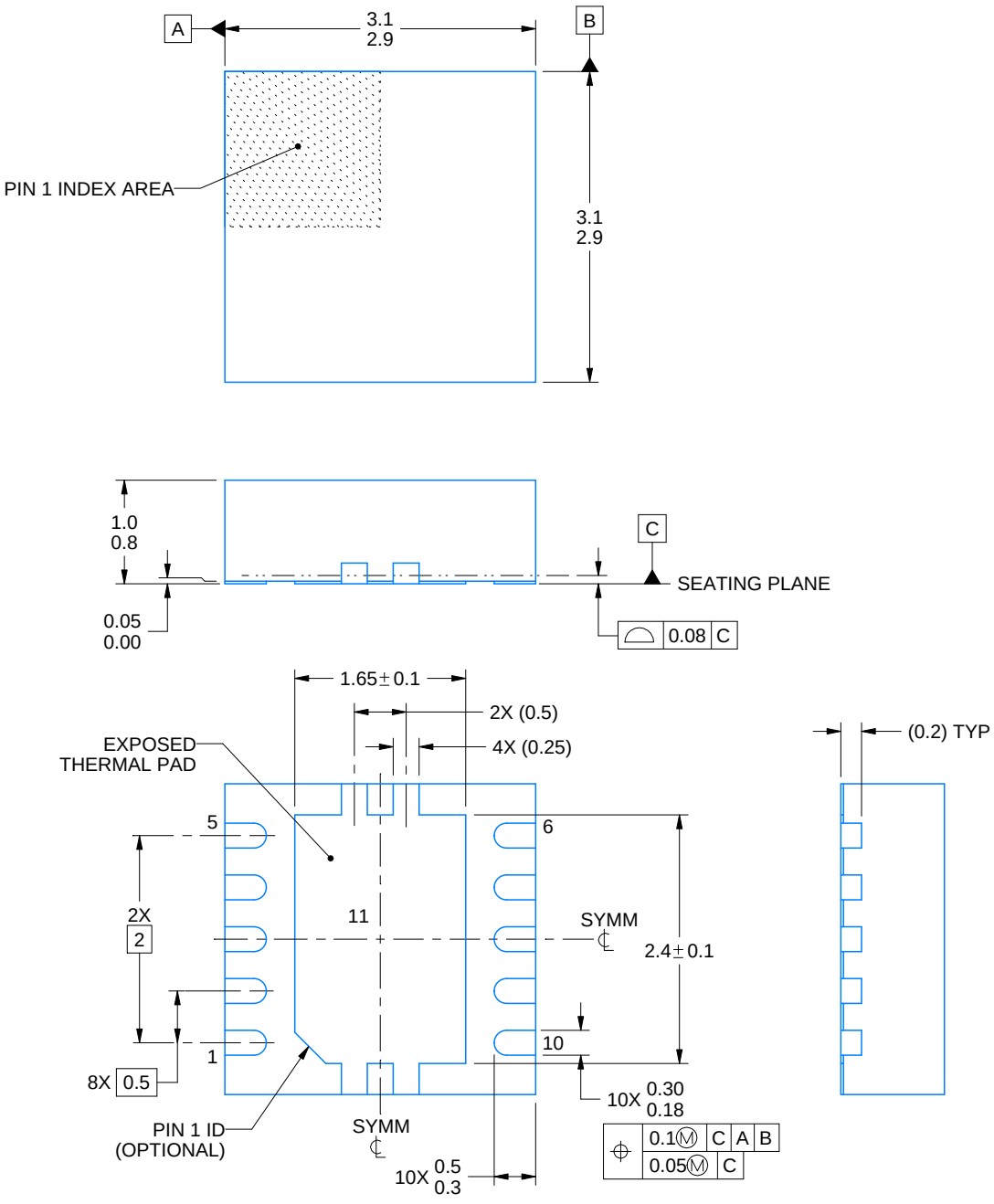
4226193/A

DRC0010J

PACKAGE OUTLINE

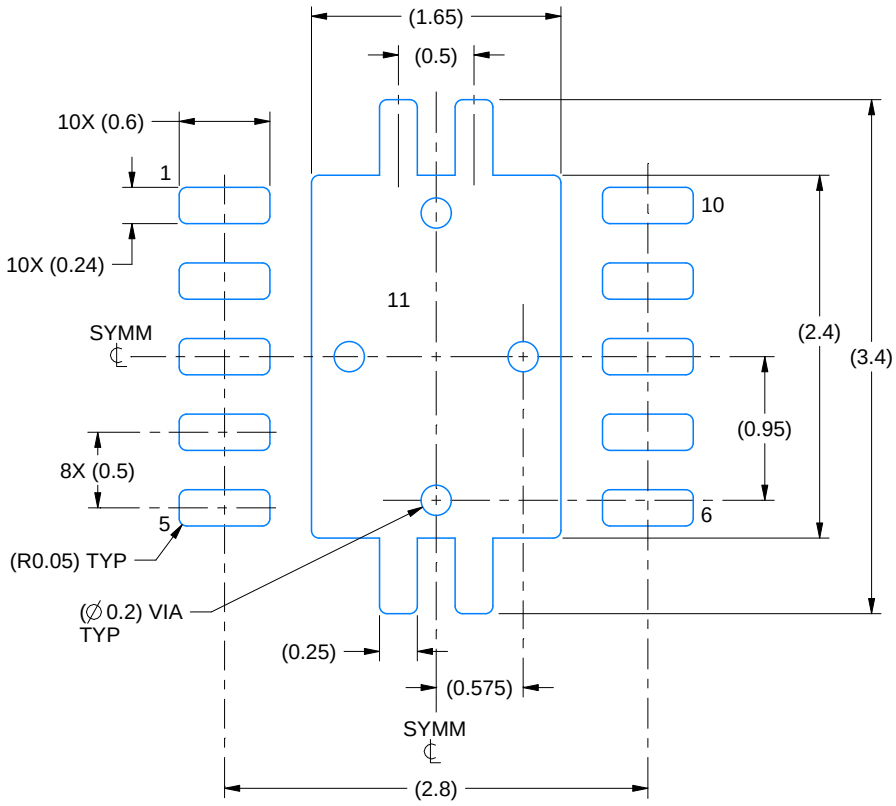
VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

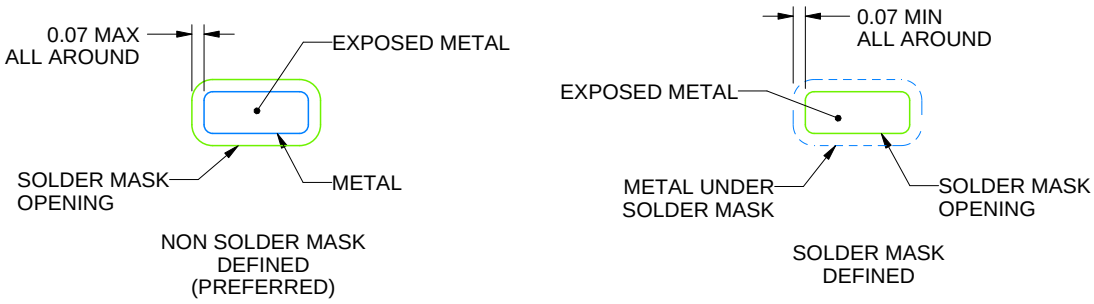


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X



SOLDER MASK DETAILS

4218878/B 07/2018

NOTES: (continued)

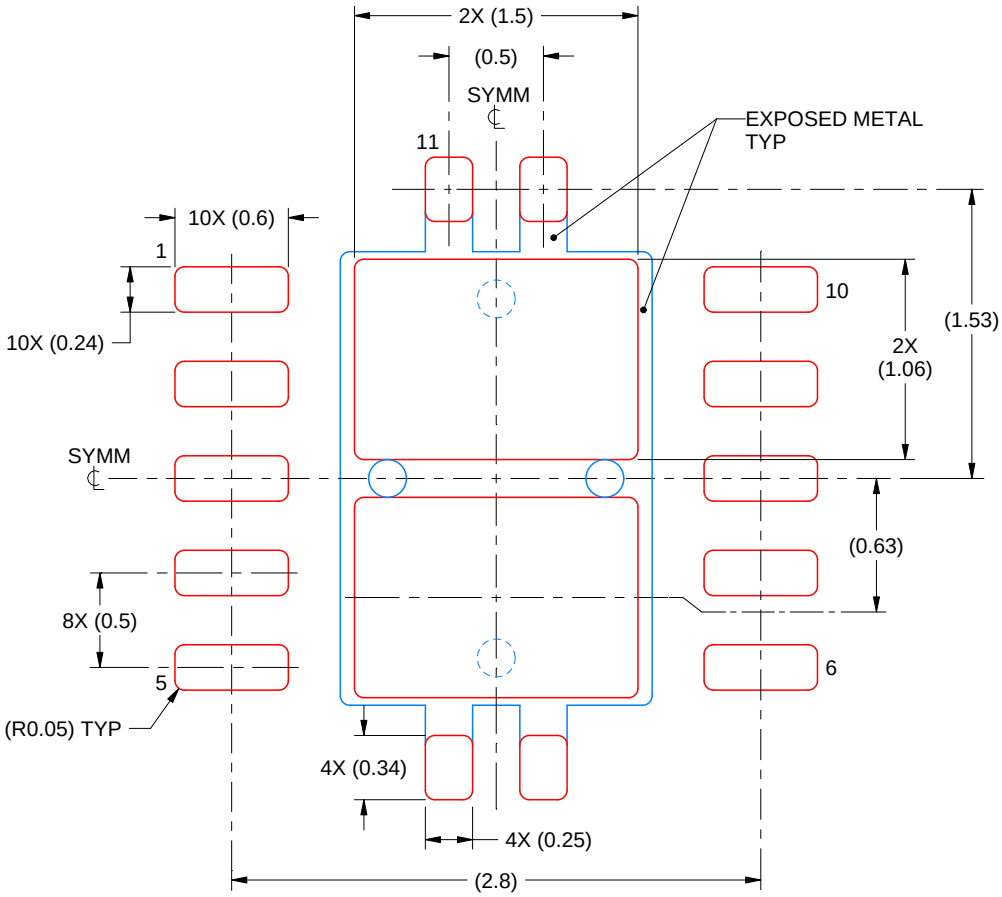
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

DRC0010J

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 11:
80% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

4218878/B 07/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale (www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265