Current-Limited, Power-Distribution Switches

Check for Samples: TPS2530

FEATURES

- **Single Power Switch**
- **Pin for Pin with Existing TI Switch Portfolio™**
- **Rated Currents of 0.5 A**
- **±25% Accurate, Fixed, Constant Current Limit**
- **Fast Over-Current Response – 2 µs**
- **Operating Range: 2.7 V to 5.5 V**
- **Deglitched Fault Reporting**
- **Reverse Current Blocking**
- **Built-in Softstart**
- **Ambient Temperature Range: –40°C to 85°C**

APPLICATIONS

- **DisplayPort**
- **USB Ports/Hubs, Laptops, Desktops**
- **Set Top Boxes**
- **Short-Circuit Protection**

DESCRIPTION

The TPS2530 power-distribution switch is intended for applications such as DisplayPort or USB Port where heavy capacitive loads and short-circuits are likely to be encountered. It offers 0.5 A fixed current-limit thresholds.

The TPS2530 limits the output current to a safe level by operating in a constant-current mode when the output load exceeds the current-limit threshold. This provides a predictable fault current under all conditions. The fast overload response time eases the burden on the main supply to provide regulated power when the output is shorted. The power-switch rise and fall times are controlled to minimize current surges during turn-on and turn-off.

TYPICAL APPLICATION

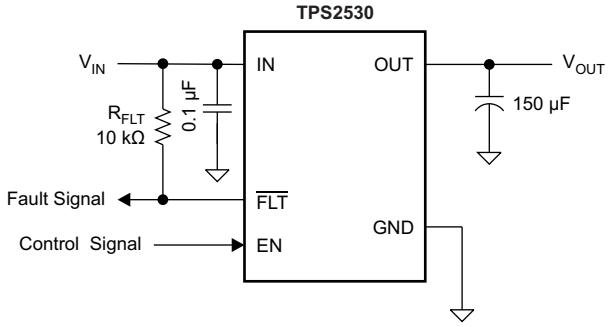


Figure 1. Typical Application

DEVICE INFORMATION(1)

MAXIMUM OPERATING CURRENT	ENABLE	BASE PART NUMBER	PACKAGED DEVICE	MARKING
0.5	High	TPS2530	SOT23-5 (DBV)	2530

(1) For the most current packaging and ordering information, see the Package Option Addendum at the end of this document, or see TI website at www.ti.com.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

		VALUE		UNIT
		MIN	MAX	
Voltage range on IN, OUT, EN, $\overline{FLT}$(2)		–0.3	6	V
Voltage range from IN to OUT		–6	6	V
Maximum junction temperature, T_J		Internally Limited		
Electrostatic Discharge	HBM	2		kV
	CDM	500		V
	IEC 6100-4-2, Contact / Air(3)	8	15	kV

(1) Voltages are with respect to GND unless otherwise noted.
(2) See the Input and Output Capacitance section.
(3) V_{OUT} was surged on a pcb with input and output bypassing per Figure 1 (except input capacitor was a 22 µF) with no device failures.

THERMAL INFORMATION

THERMAL METRIC(1)		TPS2530	UNITS
		DBV (5 PINS)	
θ_{JA}	Junction-to-ambient thermal resistance	224.9	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	95.2	
θ_{JB}	Junction-to-board thermal resistance	51.4	
ψ_{JT}	Junction-to-top characterization parameter	6.6	
ψ_{JB}	Junction-to-board characterization parameter	50.3	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	N/A	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage, IN	2.7		5.5	V
V_{EN}	Input voltage, EN	0		5.5	V
V_{IH}	High-level input voltage, EN	2			V
V_{IL}	Low-level input voltage, EN			0.7	V
I_{OUT}	Continuous output current, OUT (TPS2530)			0.5	A
T_J	Operating junction temperature	–40		125	°C
$I_{\overline{FLT}}$	Sink current into $\overline{FLT}$	0		5	mA

ELECTRICAL CHARACTERISTICS: $T_J = T_A = 25°C$ (1)

Unless otherwise noted: V_{IN} = 5 V, $V_{EN} = V_{IN}$, I_{OUT} = 0 A

PARAMETER		TEST CONDITIONS(2)		MIN	TYP	MAX	UNIT
POWER SWITCH							
$R_{DS(on)}$	Input – Output resistence	V_{IN} = 3.3 V	25°C		103	120	mΩ
			–40°C ≤ (T_J, T_A) ≤ 85°C		103	150	
		V_{IN} = 5 V	25°C		97	116	
			–40°C ≤ (T_J, T_A) ≤ 85°C		97	143	
CURRENT LIMIT							
I_{OS} (3)	Current-limit, See Figure 7	V_{IN} = 3.3 V or 5 V		0.75	1	1.25	A
SUPPLY CURRENT							
I_{SD}	Supply current, switch disabled	V_{IN} = 3.3 V or 5 V, 25°C			0.01	1	µA
		–40°C ≤ (T_J, T_A) ≤ 85°C, V_{IN} = 5.5 V				2	
I_{SE}	Supply current, switch enabled	V_{IN} = 3.3 V, 25°C			55	75	µA
		V_{IN} = 5 V, 25°C			76	96	
		–40°C ≤ (T_J, T_A) ≤ 85°C, V_{IN} = 5.5 V				118	
I_{REV}	Reverse leakage current	V_{OUT} = 5.5 V, V_{IN} = 0 V, measure I_{VOUT}			0.2	1	µA

(1) Parametrics over a wider operational range are shown in the second ELECTRICAL CHARACTERISTICS table.
(2) Pulsed testing techniques maintain junction temperature close to ambient temperature.
(3) See CURRENT LIMIT section for explanation of this parameter.

ELECTRICAL CHARACTERISTICS: –40°C ≤ T_J ≤ 125°C

Unless otherwise noted: 2.7 V ≤ V_{IN} ≤ 5.5 V, $V_{EN} = V_{IN}$, I_{OUT} = 0 A, typical values are at 5 V and 25°C.

PARAMETER		TEST CONDITIONS(1)	MIN	TYP	MAX	UNIT
POWER SWITCH						
$R_{DS(on)}$	Input – Output resistance			97	200	mΩ
ENABLE INPUT (EN)						
V_{IH}	High-level input Voltage		2			V
V_{IL}	Low-level input Voltage				0.7	
	Hysteresis (2)			0.09		
	Leakage current	V_{EN} = 0 V or 5.5 V	–1	0	1	µA
t_{ON}	Turn on time	V_{IN} = 3.3 V, C_L = 1 µF, R_L = 100 Ω, EN ↑. See Figure 2, Figure 4 and Figure 5				ms
		0.5 A	1	1.75	2.5	
t_{OFF}	Turn off time	V_{IN} = 3.3 V, C_L = 1 µF, R_L = 100 Ω, EN ↑. See Figure 2, Figure 4 and Figure 5				ms
		0.5 A	0.8	1.35	1.9	
t_R	Rise time, output	V_{IN} = 3.3 V, C_L = 1 µF, R_L = 100 Ω, See Figure 3				ms
		0.5 A	0.25	0.45	0.65	
t_F	Fall time, output	V_{IN} = 3.3 V, C_L = 1 µF, R_L = 100 Ω, See Figure 3				ms
		0.5 A	0.2	0.3	0.4	
CURRENT LIMIT						
I_{OS} (3)	Current-limit, See Figure 7		0.7	1	1.3	A
t_{IOS}	Short-circuit response time(2)	V_{IN} = 5 V (see Figure 6), One-half full load → R_{SHORT} = 50 mΩ, Measure from application to when current falls below 120% of final value		2		µs

(1) Pulsed testing techniques maintain junction temperature close to ambient temperature.
(2) These parameters are provided for reference only, and do not constitute part of TI's published device specifications for purpose of TI's product warranty.
(3) See CURRENT LIMIT section for explanation of this parameter.

ELECTRICAL CHARACTERISTICS: –40°C ≤ T_J ≤ 125°C (continued)

Unless otherwise noted: 2.7 V ≤ V_{IN} ≤ 5.5 V, V_{EN} = V_{IN}, I_{OUT} = 0 A, typical values are at 5 V and 25°C.

PARAMETER		TEST CONDITIONS(1)	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
I_{SD}	Supply current, switch disabled			0.01	10	µA
I_{SE}	Supply current, switch enabled			82	135	µA
I_{REV}	Reverse leakage current (4)	V_{OUT} = 5.5 V, V_{IN} = 0 V, Measure I_{VOUT}		0.2		µA
UNDERVOLTAGE LOCKOUT						
V_{UVLO}	Rising threshold	V_{IN}↑	2.2	2.46	2.6	V
	Hysteresis(4)	V_{IN}↓		65		mV
$\overline{FLT}$						
	Output low voltage, $\overline{FLT}$	$I_{\overline{FLT}}$ = 1 mA			0.2	V
	Off-state leakage	$V_{\overline{FLT}}$ = 5.5 V			1	µA
$t_{\overline{FLT}}$	$\overline{FLT}$ deglitch	$\overline{FLT}$ assertion and deassertion deglitch	3.5	8	12	ms
THERMAL SHUTDOWN						
T_J	Rising threshold	In current limit	135			°C
		Not in current limit	155			
	Hysteresis(4)			20		°C

(4) These parameters are provided for reference only, and do not constitute part of TI's published device specifications for purpose of TI's product warranty.

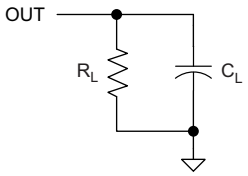


Figure 2. Output Rise / Fall Test Load

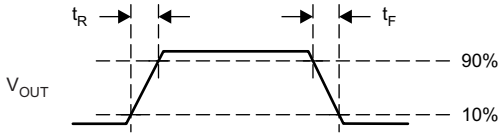


Figure 3. Power-On and Off Timing

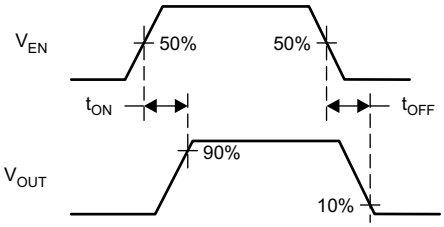


Figure 4. Enable Timing, Active High Enable

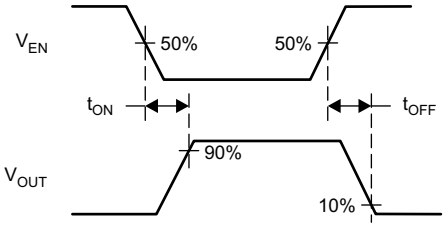


Figure 5. Enable Timing, Active Low Enable

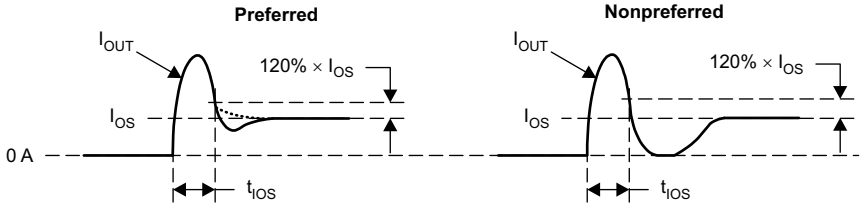


Figure 6. Output Short Circuit Parameters

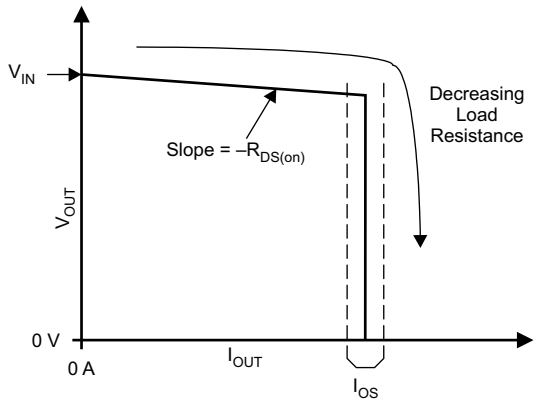
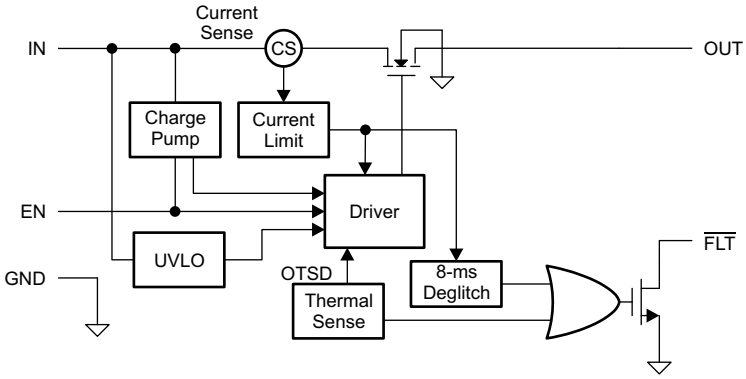


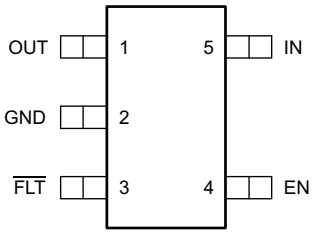
Figure 7. Output Characteristic Showing Current Limit

FUNCTIONAL BLOCK DIAGRAM



DEVICE INFORMATION

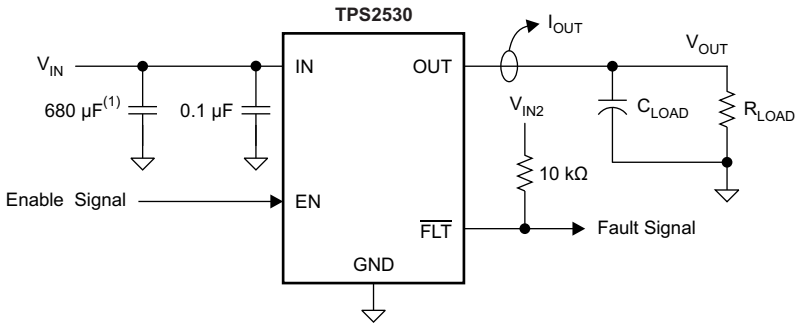
DBV Package
(Top View)



PIN FUNCTIONS

NAME	PINS	DESCRIPTION
5-PIN PACKAGE		
EN	4	Enable input, logic high turns on power switch.
GND	2	Ground connection.
IN	5	Input voltage and power-switch drain; connect a 0.1 µF or greater ceramic capacitor from IN to GND close to the IC.
$\overline{\text{FLT}}$	3	Active-low open-drain output, asserted during over-current, or over-temperature conditions.
OUT	1	Power-switch output, connect to load.

TYPICAL CHARACTERISTICS



(1) Helps with output shorting tests when external supply is used.

Figure 8. Test Circuit for System Operation in Typical Characteristics Section

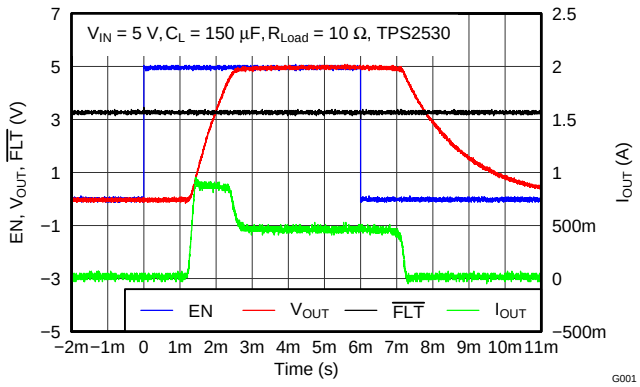


Figure 9. TPS2530 Output Rise/ Fall with 150-µF Load

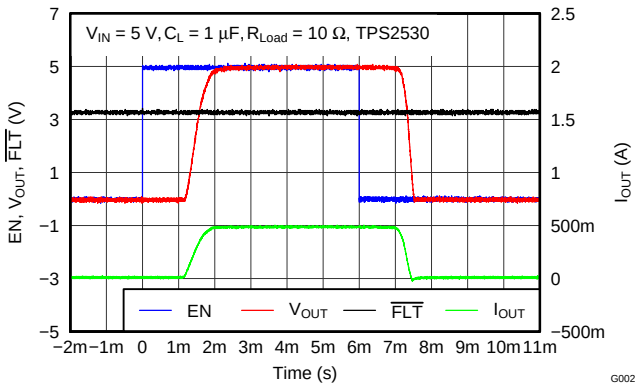


Figure 10. TPS2530 Output Rise/ Fall with 1-µF Load

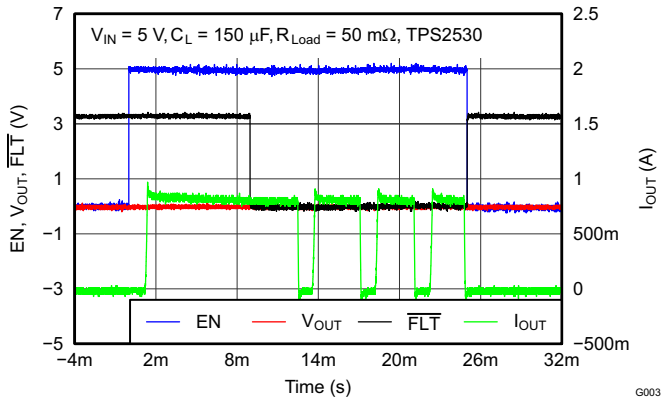


Figure 11. TPS2530 Enable and Disable Into Output Short

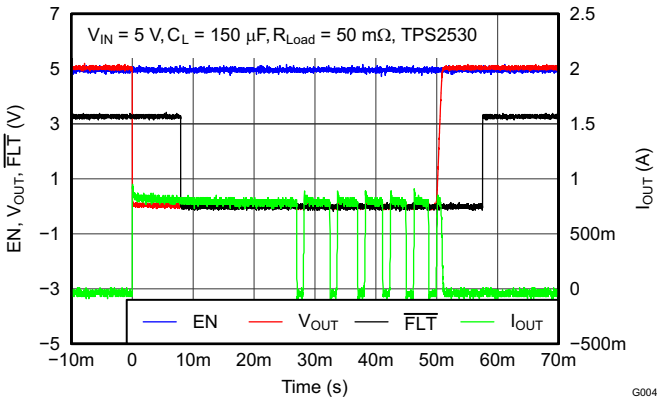


Figure 12. TPS2530 Pulsed Shorted Applied

TYPICAL CHARACTERISTICS (continued)

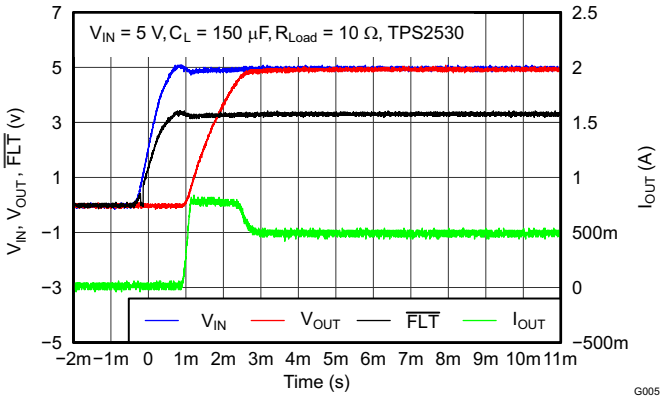


Figure 13. TPS2530 Power Up – Enabled

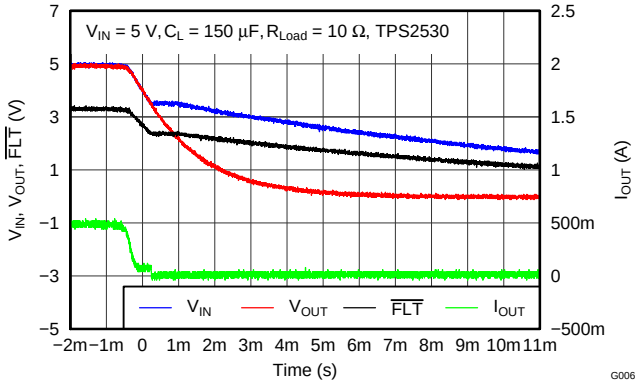


Figure 14. TPS2530 Power Down – Enabled

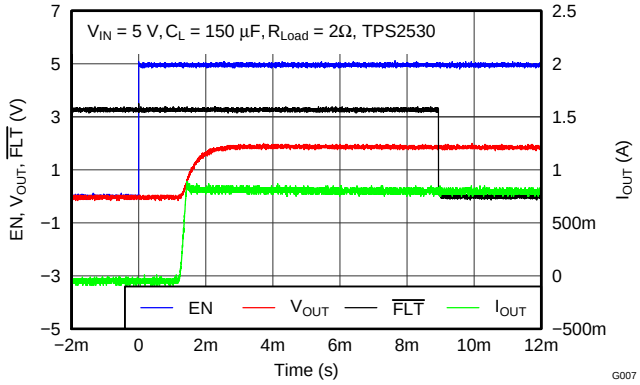


Figure 15. TPS2530 Enable with 2-Ω Load

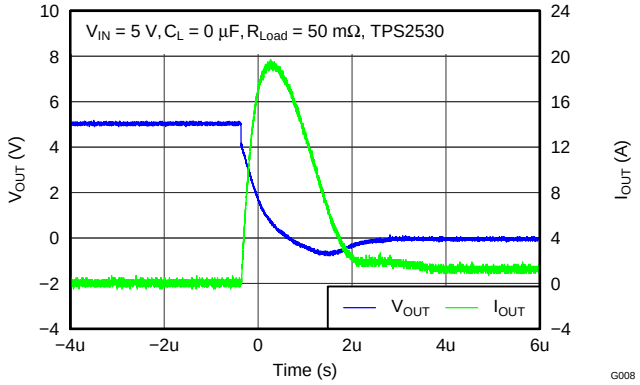


Figure 16. TPS2530 Short Applied

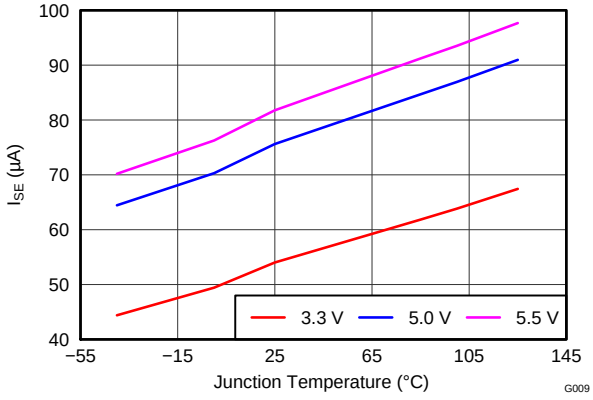


Figure 17. Supply Current (Enabled) – I_{SE} vs Temperature

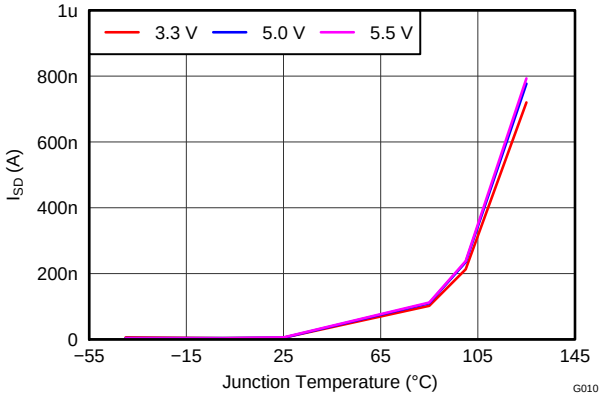


Figure 18. Supply Current (Disabled) – I_{SD} vs Temperature

TYPICAL CHARACTERISTICS (continued)

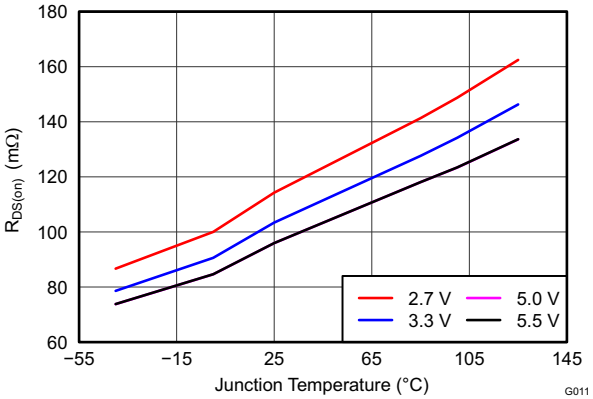


Figure 19. Input – Output Resistance – $R_{DS(on)}$ vs Temperature

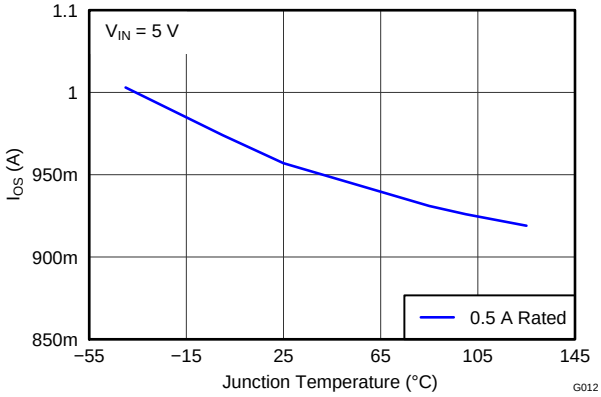


Figure 20. Current Limit – I_{OS} vs Temperature

DETAILED DESCRIPTION

TPS2530 is current-limited, power-distribution switch providing 0.5 A continuous load current in 3.3 V or 5 V circuits. The part use N-channel MOSFETs for low resistance, maintaining voltage to the load. It is designed for applications where short circuits or heavy capacitive loads are encountered. Device features include enable, reverse blocking when disabled, overcurrent protection, overtemperature protection, and deglitched fault reporting.

UVLO

The undervoltage lockout (UVLO) circuit disables the power switch until the input voltage reaches the UVLO turn on threshold. Built-in hysteresis prevents unwanted on/off cycling due to input voltage drop from large current surges. $\overline{FLT}$ is high impedance when the TPS2530 is in UVLO.

ENABLE

The logic enable input EN, controls the power switch, bias for the charge pump, driver, and other circuits. The supply current is reduced to less than 1 µA when the TPS2530 is disabled. Disabling the TPS2530 will immediately clear an active $\overline{FLT}$ indication. The enable input is compatible with both TTL and CMOS logic levels.

The turn on and turn off times (t_{ON}, t_{OFF}) are composed of a delay and a rise or fall time (t_R, t_F). The delay times are internally controlled. The rise time is controlled by both the TPS2530 and the external loading (especially capacitance). The fall time is controlled by the TPS2530 and the loading (R and C). An output load consisting of only a resistor will experience a fall time set by the TPS2530. An output load with parallel R and C elements will experience a fall time determined by the (R × C) time constant if it is longer than the TPS2530's t_F.

The enable should not be left open, and may be tied to VIN or GND depending on the device.

INTERNAL CHARGE PUMP

The device incorporate an internal charge pump and gate drive circuitry necessary to drive the N-channel MOSFET. The charge pump supplies power to the gate driver circuit and provides the necessary voltage to pull the gate of the MOSFET above the source. The driver incorporate circuitry that controls the rise and fall times of the output voltage to limit large current and voltage surges on the input supply, and provides built-in soft-start functionally. The MOSFET power switch blocks current from OUT to IN when turned off by the UVLO or disabled.

CURRENT LIMIT

The TPS2530 responds to overloads by limiting output current to the static I_{OS} levels shown in the Electrical Characteristics table. When an overload condition is present, the device maintains a constant output current, with the output voltage determined by (I_{OS} x R_{LOAD}). Two possible overload conditions can occur.

The first overload condition occurs when either: 1) input voltage is first applied, enable is true, and a short circuit is present (load which draws $I_{OUT} > I_{OS}$), or 2) input voltage is present and the TPS2530 is enabled into a short circuit. The output voltage is held near zero potential with respect to ground and the TPS2530 ramps the output current to I_{OS}. The TPS2530 limits the current to I_{OS} until the overload condition is removed or the device begins to thermal cycle.

The second condition is when an overload occurs while the device is enabled and fully turned on. The device responds to the overload condition within t_{IOS} (Figure 6 and Figure 7) when the specified overload (per the Electrical Characteristics table) is applied. The response speed and shape will vary with the overload level, input circuit, and rate of application. The current-limit response varies between settling to I_{OS}, or turnoff and controlled return to I_{OS}. Similar to the previous case, the TPS2530 limits the current to I_{OS} until the overload condition is removed or the device begins to thermal cycle.

The TPS2530 thermal cycles if an overload condition is present long enough to activate thermal limiting in any of the above cases. This is due to the relatively large power dissipation [(V_{IN} – V_{OUT}) × I_{OS}] driving the junction temperature up. The device turns off when the junction temperature exceeds 135°C (min) while in current limit. The device remains off until the junction temperature cools 20°C and then restarts.

There are two kinds of current limit profiles typically available in TI switch products similar to the TPS2530. Many older designs have an output I vs V characteristic similar to the plot labeled “Current Limit with Peaking” in Figure 21. This type of limiting can be characterized by two parameters, the current limit corner (I_{OC}), and the short circuit current (I_{OS}). I_{OC} is often specified as a maximum value. The TPS2530 does not present noticeable peaking in the current limit, corresponding to the characteristic labeled “Flat Current Limit” in Figure 21. This is why the I_{OC} parameter is not present in the Electrical Characteristics tables.

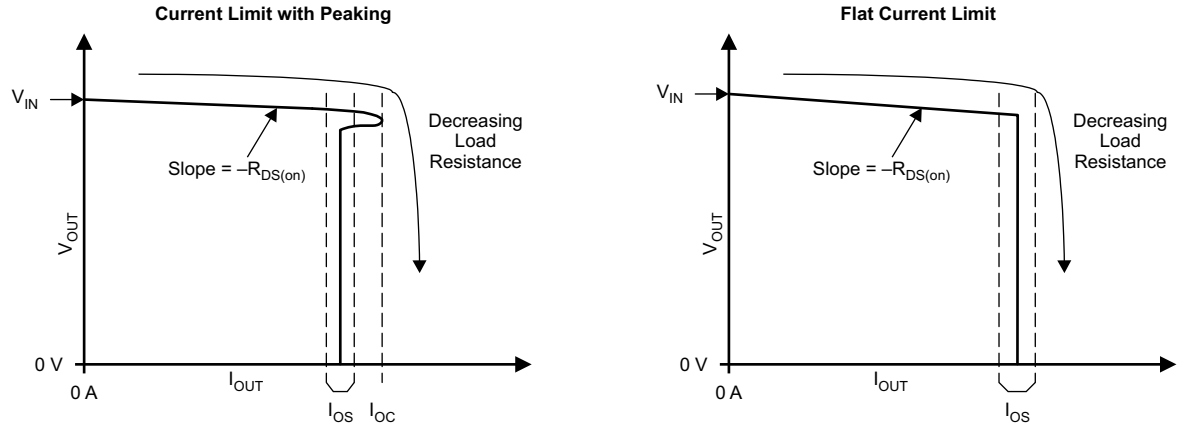


Figure 21. Current Limit Profiles

$\overline{\text{FLT}}$

The $\overline{\text{FLT}}$ open-drain output is asserted (active low) during an over-load or over-temperature condition. A 8 ms deglitch on both the rising and falling edged avoids false reporting at startup and during transients. A current limit condition shorter than the deglitch period clears the internal timer upon termination. The deglitch timer will not integrate with excessive ripple and large output capacitance may interface with operation of $\overline{\text{FLT}}$ around I_{OS} as the ripple will drive the TPS2530 in and out of current limit.

If the TPS2530 is in current limit and the over-temperature circuit goes active, $\overline{\text{FLT}}$ goes true immediately however exiting this condition is deglitched. $\overline{\text{FLT}}$ is tripped just as the knee of the constant-current limiting is entered. Disabling the TPS2530 clears and active $\overline{\text{FLT}}$ as soon as the switch turns off. $\overline{\text{FLT}}$ is high impedance when the TPS2530 is disabled or in undervoltage lockout (UVLO).

APPLICATION INFORMATION

INPUT AND OUTPUT CAPACITANCE

Input and output capacitance improves the performance of the device. The actual capacitance should be optimized for the particular application. For all applications, a 0.1 µF or greater ceramic bypass capacitor between IN and GND is recommended as close to the device as possible for local noise de-coupling.

All protection circuits such as TPS2530 will have the potential for input voltage overshoots and output voltage undershoots.

Input voltage overshoots can be caused by either of two effects. The first cause is an abrupt application of input voltage in conjunction with input power bus inductance and input capacitance when the IN terminal is high impedance (before turn on). Theoretically, the peak voltage is 2 times the applied. The second cause is due to the abrupt reduction of output short circuit current when the TPS2530 turns off and energy stored in the input inductance drives the input voltage high. Input voltage droops may also occur with large load steps and as the TPS2530 output is shorted. Applications with large input inductance (e.g. connecting the evaluation board to the bench power-supply through long cables) may require large input capacitance reduce the voltage overshoot from exceeding the absolute maximum voltage of the device. The fast current-limit speed of the TPS2530 to hard output short circuits isolate the input bus form faults. However, ceramic input capacitance in the range of 1 µF to 22 µF adjacent to the TPS2530 input aids in both speeding response time and limiting the transient seen on the input power bus. Momentary input transients to 6.5 V are permitted. In order to keep front-end power circuit work normally, it is better to increase the output cap.

Output voltage undershoot is caused by the inductance of the output power bus just after a short has occurred and the TPS2530 has abruptly reduced OUT current. Energy stored in the inductance will drive the OUT voltage down and potentially negative as it discharges. Application with large output inductance (such as from a cable) benefit from use of a high-value output capacitor to control the voltage undershoot. When implementing USB standard application, a 120 µF minimum output capacitance is required. Typically a 150 µF electrolytic capacitor is used, which is sufficient to control voltage undershoots. However, if the application does not require 120 µF of output capacitance, and there is potential to drive the output negative, a minimum of 10 µF ceramic capacitor on the output is recommended. The voltage undershoot should be controlled to less than 1.5 V for 10 µs.

POWER DISSIPATION AND JUNCTION TEMPERATURE

It is good design practice to estimate power dissipation and maximum expected junction temperature of the TPS2530. The system designer can control choices of package, proximity to other power dissipating devices, and printed circuit board (PCB) design based on these calculations. These have a direct influence on maximum junction temperature. Other factors such as airflow and maximum ambient temperature are often determined by system considerations. It is important to remember that these calculations do not include the effects of adjacent heat sources, and enhanced or restricted air flow.

Addition of extra PCB copper area around these devices is recommended to reduce the thermal impedance and maintain the junction temperature as low as practical.

The following procedure requires iteration because power loss is due to the internal MOSFET I^2 x $R_{DS(on)}$, and $R_{DS(on)}$ is a function of the junction temperature. As an initial estimate, use the $R_{DS(on)}$ at 125°C from the typical characteristics, and the preferred package thermal resistance for the preferred board construction from the thermal parameters section.

$$T_J = T_A + [(I_{OUT}^2 \times R_{DS(on)}) \times \theta_{JA}]$$

Where:

I_{OUT} = rated OUT pin current (A)
$R_{DS(on)}$ = Power switch on-resistance at an assumed T_J (Ω)
T_A = Maximum ambient temperature (°C)
T_J = Maximum junction temperature (°C)
θ_{JA} = Thermal resistance (°C/W)

If the calculated T_J is substantially different from the original assumption, look up a new value of $R_{DS(on)}$ and recalculate.

Under 85°C ambient temperature, the TPS2530 junction temperature $T_J = 85 + 0.5^2 \times 0.2 \times 224.9$ to approximately 96.5°C, so in a practical application, the $R_{DS(on)}$ is about 165 mΩ and never reach to maximum 200 mΩ as shown in the Electrical Characteristics table.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS2530DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	2530	Samples
TPS2530DBVT	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	2530	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

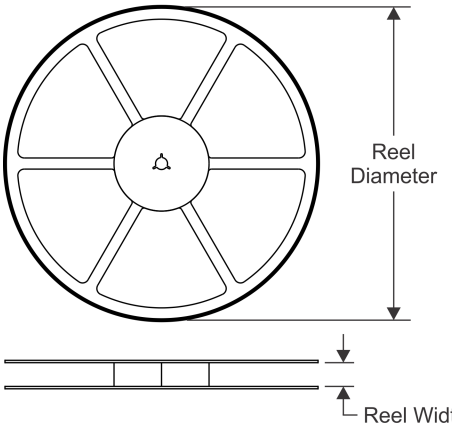
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

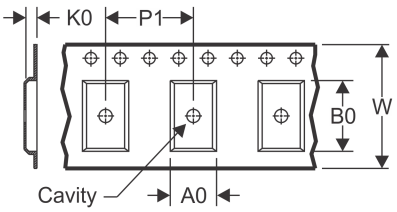
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

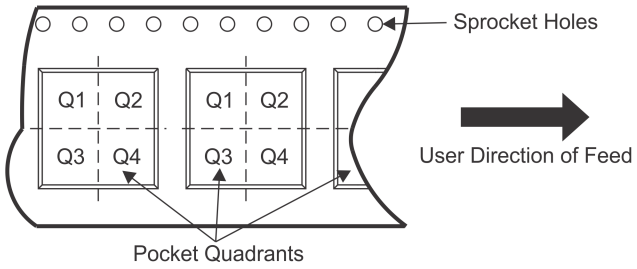


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

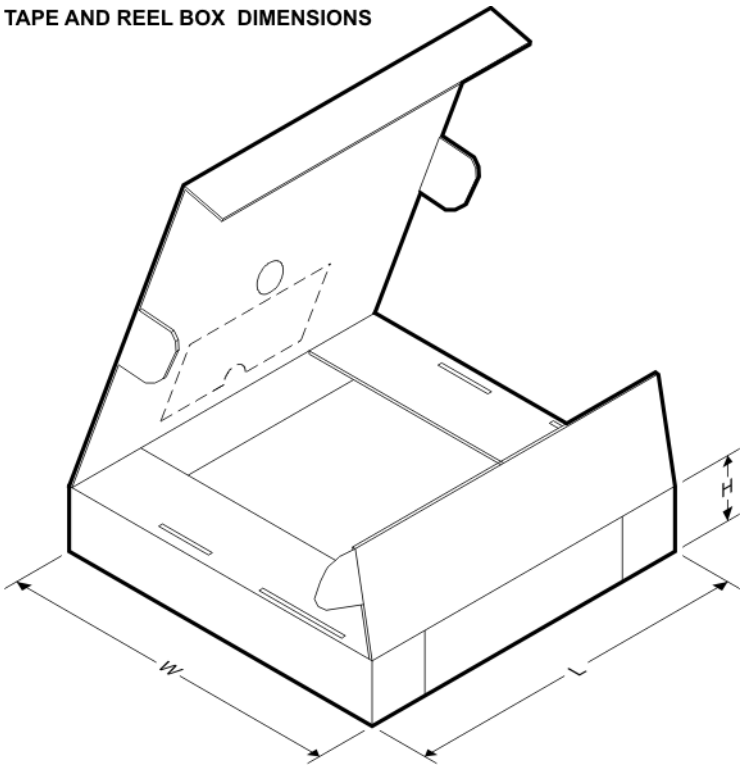
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS2530DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
TPS2530DBVT	SOT-23	DBV	5	250	178.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

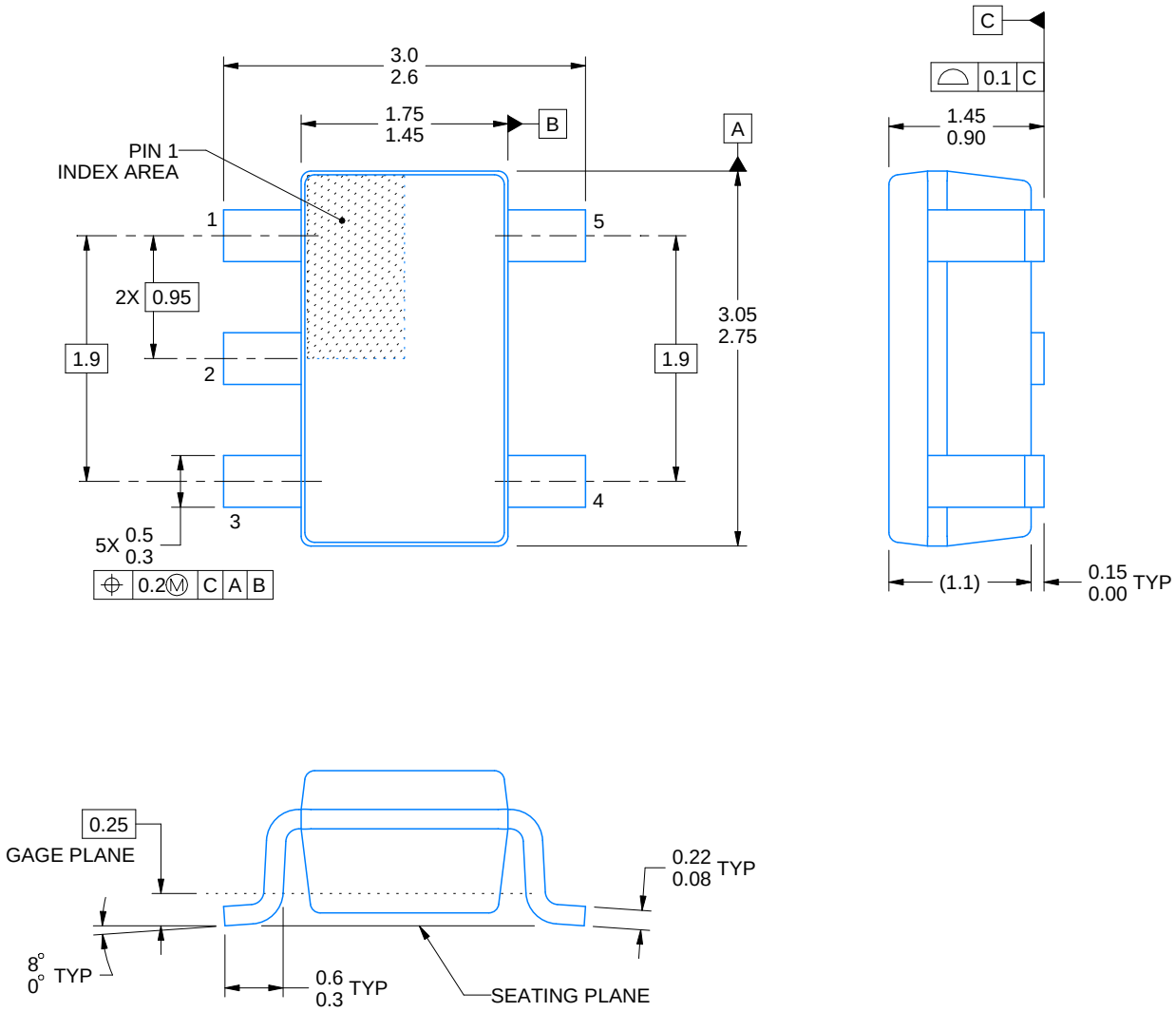
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS2530DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS2530DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

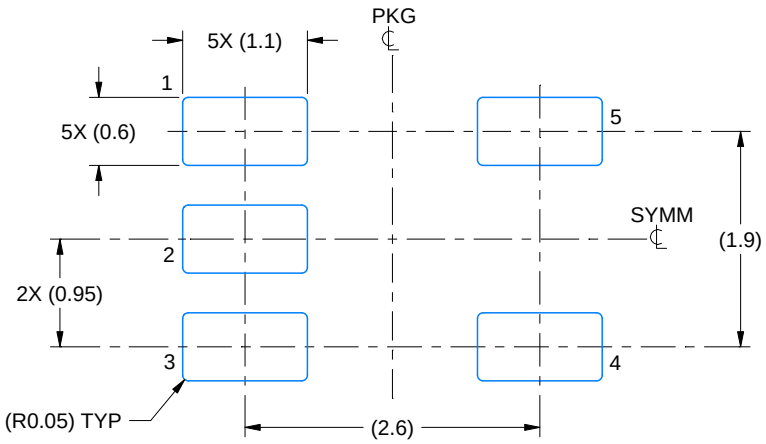
SMALL OUTLINE TRANSISTOR



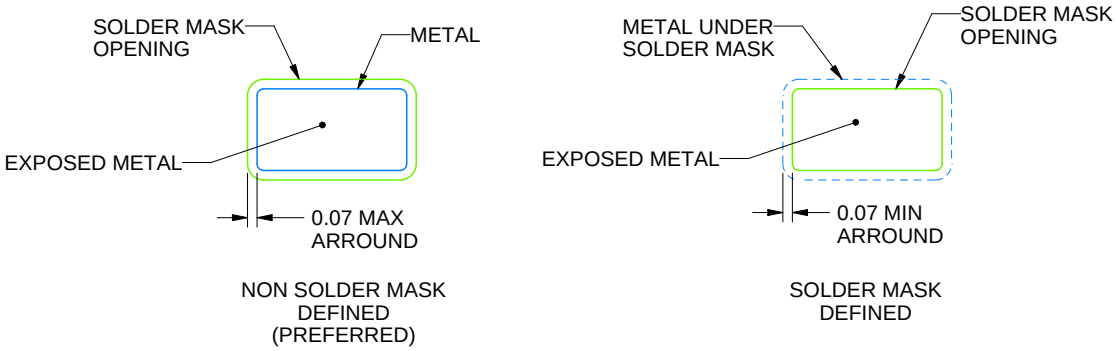
4214839/E 09/2019

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

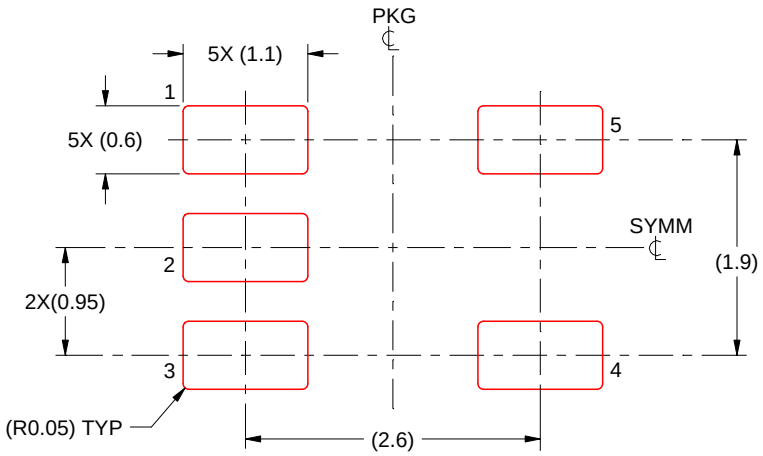


SOLDER MASK DETAILS

4214839/E 09/2019

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/E 09/2019

NOTES: (continued)

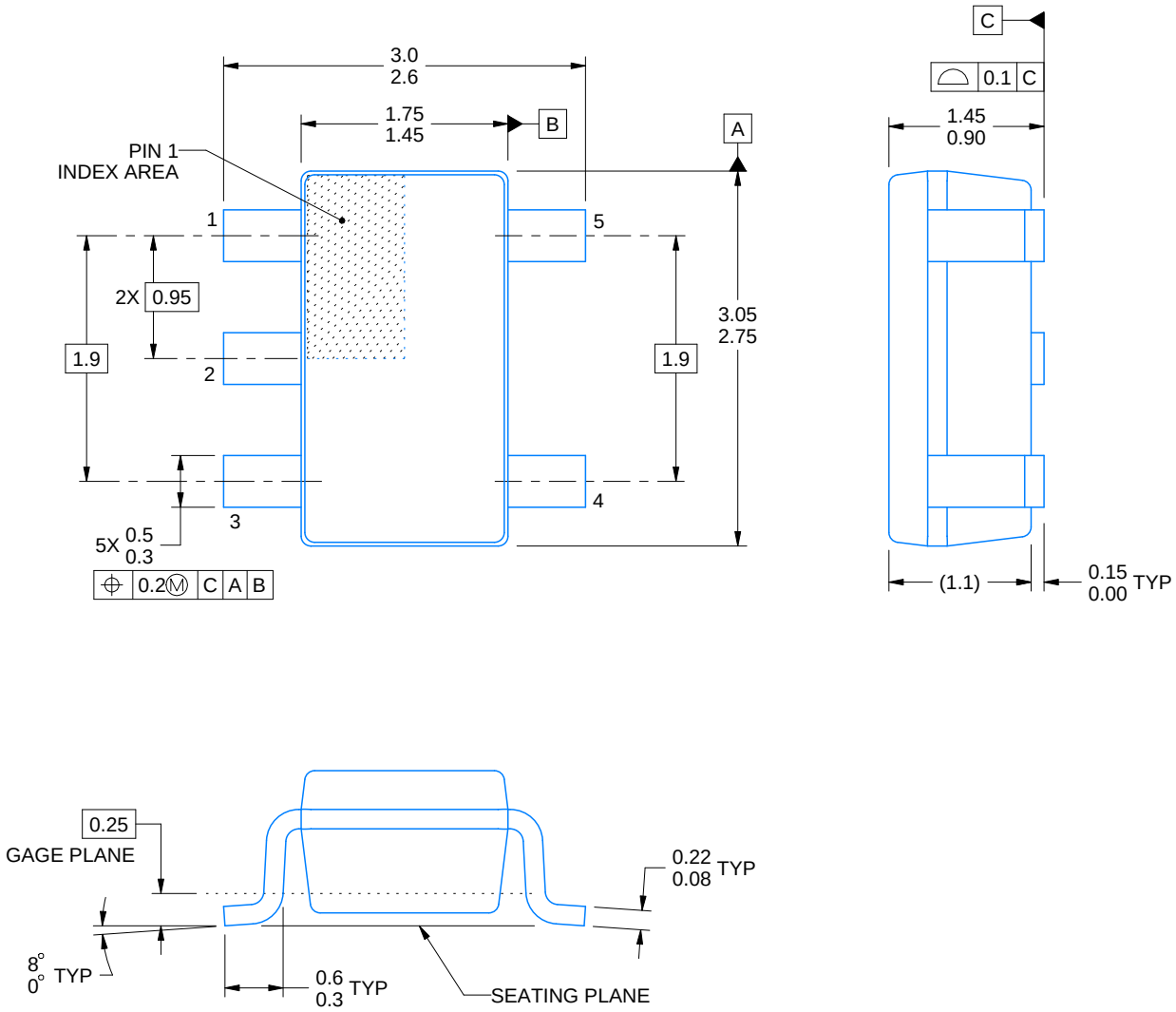
7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

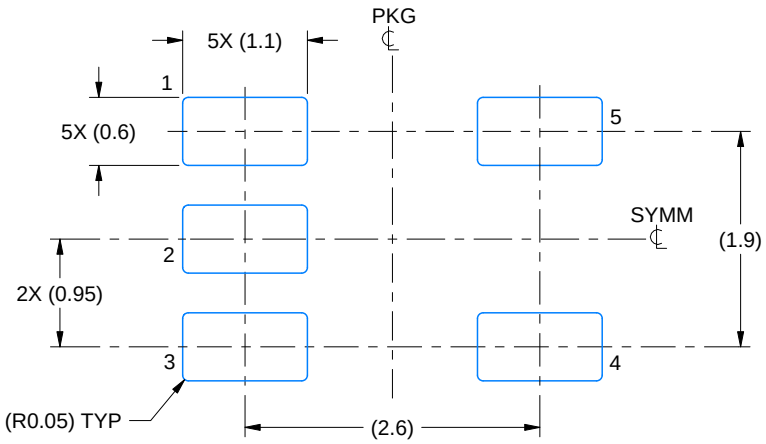
SMALL OUTLINE TRANSISTOR



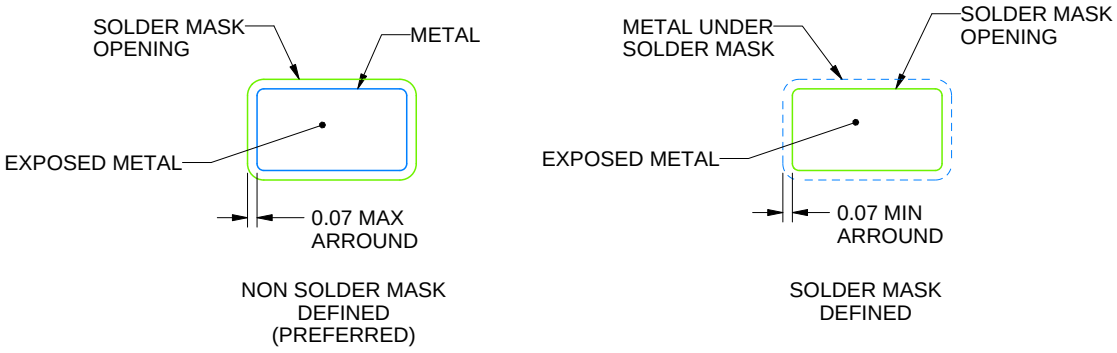
4214839/F 06/2021

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4214839/F 06/2021

NOTES: (continued)

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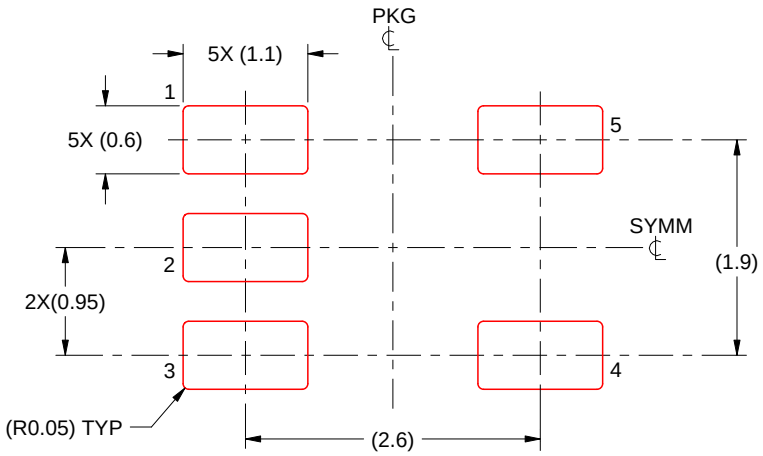

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/F 06/2021

NOTES: (continued)

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