FSC-BT901

4.2 Dual Mode Bluetooth Module Datasheet

Version 1.8

Revision History

Version	Data	Notes	
1.0	2017/06/21	Initial Version	Devin Wan
1.1	2017/07/25	Modify pin function definition and Supply voltage range; remove SPI function.	Devin Wan
1.2	2017/07/28	Modify the function description of the 7th and 15Pin	Devin Wan
1.3	2017/08/12	Increase I2S application circuit diagram	Devin Wan
1.4	2018/03/15	1, Added two new pins for program updates. No change in size of the module. 2, Modify module height of 1.7mm	Devin Wan
1.5	2018/05/05	Modify Bluetooth Version: Upgrade from BT4.0 to BT4.2	Devin Wan
1.6	2018/05/08	Updated the package dimension drawing of the module and added the application circuit diagram	Devin Wan
1.7	2020/02/25	Modify the overview description	Fish
1.8	2020/04/30	Increase power consumption parameters	Fish

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Contents

1. INTRODUCTION

Overview

The FSC-BT901 is a highly integrated Bluetooth module which BT4.2 Smart Ready device (with BR/EDR & LE support simultaneously), it features a 2.4GHz ISM RF transceiver, Bluetooth V4.2 baseband controller, flash memory, small form factor, and external antenna interface.

Built with Feasycom standard firmware by default, custo mized firmware is available too.

The FSC-BT901 is an appropriate product for designers who want to add wireless capability to their products.

Features

- Bluetooth v4.2, Class 1.5
- Low power
- UART programming and data interface (baudrate can up to 921600bps)
- I2S audio interface
- I2C/AIO/PIO/PWM control interfaces
- Postage stamp sized form factor
- Embedded Bluetooth stack profiles support: SPP/iAP, HID, GATT, ANCS etc
- USB 2.0 full-speed device/host/OTG controller
- OTA upgrade support
- MFI Support
- Support External Antenna
- RoHS compliant
- Power Consumption In Sleep Mode (VDD_3V3 at 3.3V)
  - Discoverable：1.73mA
  - BR/EDR Connection：11.12mA
  - LE Connection：2.46mA
- Power Consumption In Working Mode (VDD_3V3 at 3.3 V)
  - Discoverable：11.56mA
  - BR/EDR Connection：20.95mA
  - LE Connection：12.08mA

Application

- Audio Speaker, with TWS(Audio True Wireless) support (plus the codec)
- Analogue and USB Multimedia Dongles
- Health & Medical devices
- Measurement and monitoring systems
- Industrial sensors and controls
- Asset tracking
- Barcode and RFID scanners

Module picture as below showing

Figure 1: FSC-BT901 Picture

2. General Specification

Table 1: General Specifications

Categories	Features	Implementation
Wireless Specification	Bluetooth Version	V4.2 Dual Mode
	Frequency	2.402 - 2.480 GHz
	Transmit Power	+8.5 dBm (Maximum)
	Receive Sensitivity	-86 dBm@0.1%BER (Typical)
	Raw Data Rates (Air)	3 Mbps(Classic BT - BR/EDR)
Host Interface and Peripherals	UART Interface	TX,RX,CTS,RTS
		General Purpose I/O
		Default 115200,N,8,1
		Baudrate support from 1200 to 921600
		5, 6, 7, 8 data bit character
	GPIO	15 (maximum – configurable) lines
		O/P drive strength (4 mA)
		Pull-up resistor (33 KΩ) control
		Read pin-level
	I2C Interface	1 (configurable from GPIO total). Up to 400 kbps
	I2S Interface	Supports Master or Slave mode operation
		Supports PCM mode A, PCM mode B,
		I2S and MSB justified data format
	ADC Interface	Analog input voltage range: 0~ AVDD (AVDD=3.3V)
		Supports single 12-bit ADC conversion
		1 channels (configured from GPIO total)
		Up to 2.4 MSPS conversion
	PWM	16-bit resolution
		8-bit prescaler and clock divider
		Supports PWM interrupts
		supports input capture function
Profiles	Classic Bluetooth	SPP (Serial Port Profile) - Up to 600 Kbps
	Bluetooth Low Energy	GATT Client & Peripheral - Any Custom Services
Maximum Connections	Classic Bluetooth	7 Clients
	Bluetooth Low Energy	5 Clients
FW upgrade		Over the Air
		Via UART
		J-link
Supply Voltage	Supply	2.7-3.6V
Power Consumption		Max Peak Current(TX Power @ +8.5dBm TX): 88mA
		Standby Doze (Wait event) - 15mA (TBD)
		Deep Sleep - <1mA (TBD)
Physical	Dimensions	10mm X 11.9mm X 1.7mm; Pad Pitch 1.1mm
Environmental	Operating	-40°C to +85°C

	Storage	-40°C to +85°C
Miscellaneous	Lead Free	Lead-free and RoHS compliant
	Warranty	One Year
Humidity		10% ~ 90% non-condensing
MSL grade:		MSL 3
ESD grade:		Human Body Model: Class-2 Machine Model: Class-B

3. HARDWARE SPECIFICATION

3.1 Block Diagram and PIN Diagram

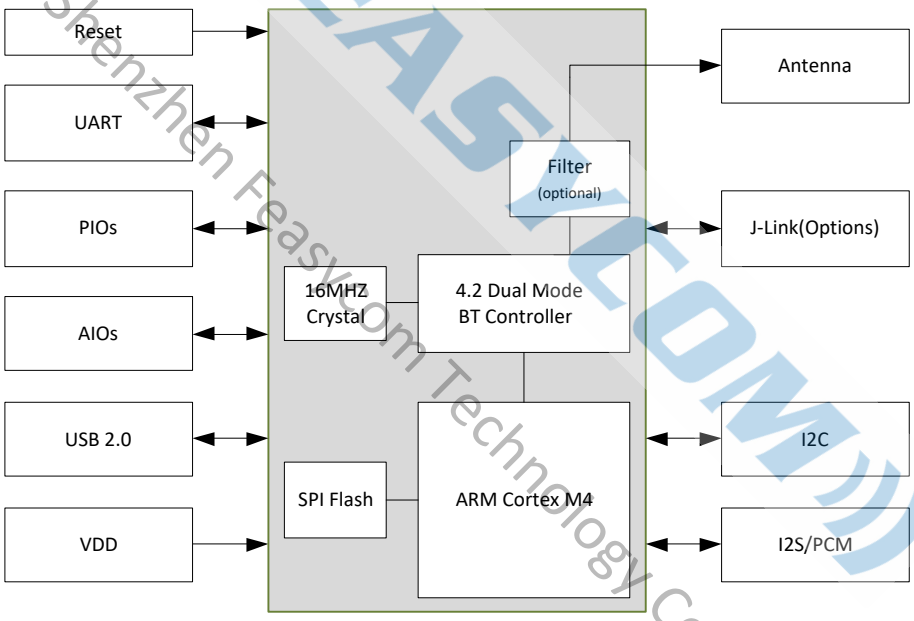


Figure 2: Block Diagram

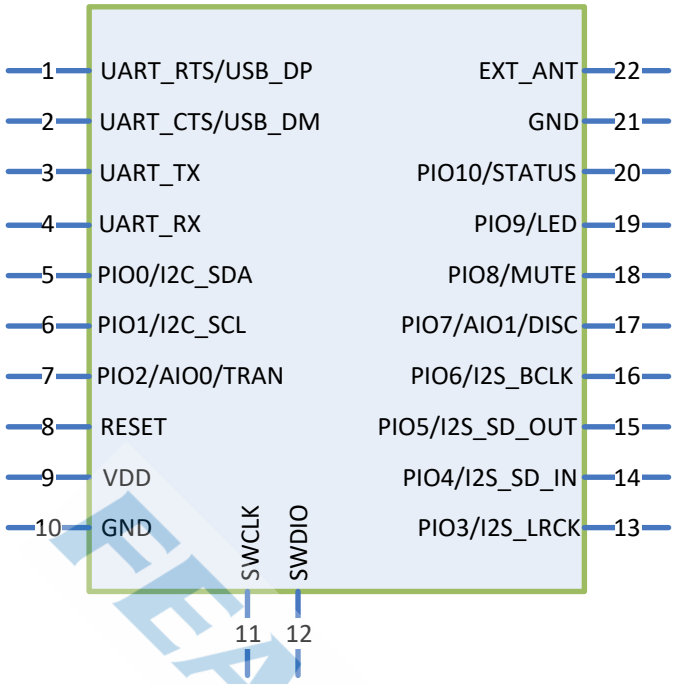


Figure 3: FSC-BT901 PIN Diagram(Top View)

3.2 PIN Definition Descriptions

Table 2: Pin definition

Pin	Pin Name	Type	Pin Descriptions	Notes
1	UART_RTS/USB_DP	O	UART Request to Send (active low)	Note 1,2
2	UART_CTS/USB_DM	I	UART Clear to Send (active low)	Note 1,2
3	UART_TX	O	UART Data output	Note 1
4	UART_RX	I	UART Data input	Note 1
5	PIO0/I2C_SDA	I/O	Programmable input/output line	Note 3
6	PIO1/I2C_SCL	I/O	Programmable input/output line	Note 3
7	PIO2/AIO0/TRAN	I/O	Programmable input/output line Alternative Function 1: Analogue programmable I/O line. Alternative Function 2: Host MCU change UART transmission mode.	Note 4
8	RESET	I	External reset input: Active LOW, with an inter an internal pull-up. Set this pin low reset to initial state.	
9	VDD_3V3	Vdd	Power supply voltage 3.3V	
10	GND	Vss	Power Ground	
11	SWCLK	I/O	Debugging through the clk line(Default)	
12	SWDIO	I/O	Debugging through the data line(Default)	
13	PIO3/I2S_LRCK	I/O	Programmable input/output line Alternative Function: I2S left right channel clock	
14	PIO4/I2S_SD_IN	I	Programmable input/output line Alternative Function: I^2S data input	

15	PIO5/I2S_SD_OUT	O	Programmable input/output line Alternative Function: I²S data out	
16	PIO6/I2S_BCLK	I/O	Programmable input/output line Alternative Function: I²S bit clock pin	
17	PIO7/AIO1/DISC	I/O	Programmable input/output line Alternative Function 1: Analogue programmable I/O line. Alternative Function 2: Host MCU disconnect bluetooth.	Note 5
18	PIO8/MUTE	I/O	Programmable input/output line Alternative Function: Mute Pin	Note 6
19	PIO9/LED	I/O	Programmable input/output line Alternative Function: LED	Note 7
20	PIO10/STATUS	I/O	Programmable input/output line Alternative Function: BT Status	Note 8
21	GND	Vss	Power Ground	
22	EXT_ANT	O	RF signal output .	Note 9

Module Pin Notes:

Note 1	For customized module, this pin can be work as I/O Interface.
Note 2	USB Specification reversion 2.0 compliant.(TBD)
Note 3	I2C Serial Clock and Data. It is essential to remember that pull-up resistors on both SCL and SDA lines are not provided in the module and MUST be provided external to the module.
Note 4	When bluetooth connection established, UART transmission mode will be determined by PIO2's level : High: Command Mode Low: Throughput Mode
Note 5	When bluetooth connection established,a rising edge of PIO7 will cause disconnection with remote device.
Note 6	Audio Mute Pin-- Mute ON: High Level; Mute OFF: Low Level.
Note 7	LED(Default)-- Power On: Light Slow Shinning ; Connected: Steady Lighting.
Note 8	BT Status(Default)-- Disconnected: Low Level; Connected: High Level.
Note 9	This PIN can connect to an external antenna to improve the Bluetooth signal coverage.

4. PHYSICAL INTERFACE

4.1 Power Supply

The transient response of the regulator is important. If the power rails of the module are supplied from an external voltage source, the transient response of any regulator used should be 20μs or less. It is essential that the power rail recovers quickly.

4.2 I2S Interfaces

The I2S can be operated in master or slave mode, in full duplex and simplex communication modes and can be configured to operate with a 16-/32-bit resolution as an input or output channel. Audio sampling frequencies from 8

kHz up to 192 kHz are supported. When either or both of the I2S interfaces is/are configured in master mode, the master clock can be output to the external DAC/CODEC at 256 times the sampling frequency.

4.3 Reset

The module may be reset from several sources: Power-on Reset (POR), Low level on the nRESET Pin (nRST), Watchdog time-out reset (WDT), Low voltage reset (LVR) or Software Reset(SYSRESETREQ, CPU Reset, CHIPRST).

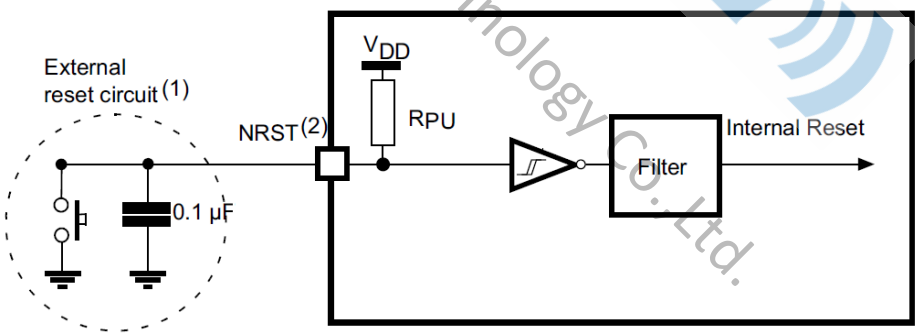
The RESET pin is an active low reset and is internally filtered using the internal low frequency clock oscillator. A reset will be performed between 1.5 and 4.0ms following RESET being active. It is recommended that RESET be applied for a period greater than 5ms.

At reset the digital I/O pins are set to inputs for bi-directional pins and outputs are tri-state. The PIOs have weak pull-ups.

Table 3: NRST pin characteristics

Parameter	Conditions	Min	Typ	Max	Unit
R_{PU} - Weak pull-up equivalent resistor(1)	VIN = VSS	30	40	50	KΩ
$V_{F(NRST)}$(2) - NRST Input filtered pulse		-	-	100	ns
$V_{NF(NRST)}$(2) - NRST Input not filtered pulse	VDD>2.7V	300	-	-	ns
T_{NRST_OUT} - Generated reset pulse duration	Internal Reset source	20	-	-	µs

1. The pull-up is designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance must be minimum (~10% order).
2. Guaranteed by design.



1. The reset network protects the device against parasitic resets.
2. The user must ensure that the level on the NRST pin can go below the VIL(NRST) max level specified in *NRST pin characteristics*. Otherwise the reset is not taken into account by the device.

Figure 4： Recommended NRST pin protection

4.4 General Purpose Analog IO

FSC-BT901 contains One 12-bit successive approximation analog-to-digital converter (ADC) with 1 single-end external input channels, performing conversions in the single-shot or scan mode. In scan mode, automatic conversion is performed on a selected group of analog inputs.

4.5 General Purpose Digital IO

There are 11 general purpose digital IOs defined in the module. All these GPIOs can be configured by software to realize various functions, such as button controls, LED drives or interrupt signals to host controller, etc. Do not connect them if not use.

The I/O type of each I/O pins can be configured by software individually as Input or Push-pull output mode. After the chip is reset, the I/O mode of all pins is input mode with no pull-up and pull-down enable. Each I/O pin has an individual pull-up and pull-down resistor which is about 40 kΩ for VDD and Vss.

4.6 RF Interface

For This Module, the default mode for antenna is external antenna.

The user can connect a 50 ohm antenna directly to the RF port.

- 2402–2480 MHz Bluetooth 4.2 Dual Mode (BT and BLE); 1 Mbps to 3 Mbps over the air data rate.
- TX output power of +8.5dBm.
- Receiver to achieve maximum sensitivity -86dBm @ 1 Mbps BLE or Classic BT, 2 Mbps, 3 Mbps).

4.7 Serial Interfaces

4.7.1 UART

FSC-BT901 provides one channels of Universal Asynchronous Receiver/Transmitters(UART)(Full-duplex asynchronous communications). The UART Controller performs a serial-to-parallel conversion on data received from the peripheral and a parallel-to-serial conversion on data transmitted from the CPU. Each UART Controller channel supports ten types of interrupts.

This is a standard UART interface for communicating with other serial devices. The UART interface provides a simple mechanism for communicating with other serial devices using the RS232 protocol.

When the module is connected to another digital device, UART_RX and UART_TX transfer data between the two devices. The remaining two signals, UART_CTS and UART_RTS, can be used to implement RS232 hardware flow control where both are active low indicators.

This module output is at 3.3V CMOS logic levels (tracks VCC). Level conversion must be added to interface with an RS-232 level compliant interface.

Some serial implementations link CTS and RTS to remove the need for handshaking. We do not recommend linking CTS and RTS except for testing and prototyping. If these pins are linked and the host sends data when the FSC-BT901 deasserts its RTS signal, there is significant risk that internal receive buffers will overflow, which could lead to an internal processor crash. This drops the connection and may require a power cycle to reset the module. We recommend that you adhere to the correct CTS/RTS handshaking protocol for proper operation.

Table 4: Possible UART Settings

Parameter		Possible Values
Baudrate	Minimum	1200 baud (≤2%Error)
	Standard	115200bps(≤1%Error)
	Maximum	921600bps(≤1%Error)
Flow control		RTS/CTS, or None
Parity		None, Odd or Even
Number of stop bits		1 /1.5/2
Bits per channel		5/6/7/8

When connecting the module to a host, please make sure to follow .

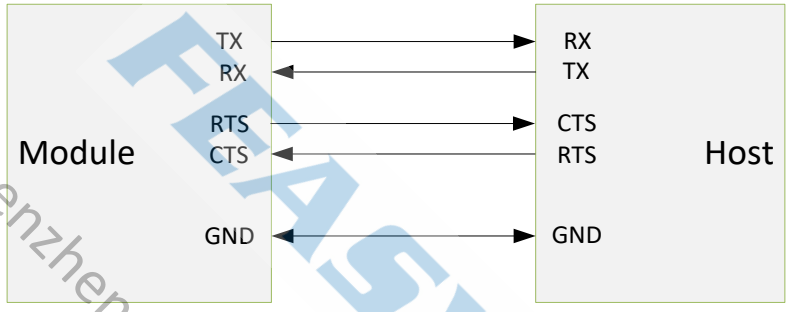


Figure 5: UART Connection

4.7.2 I2C Interface

I2C is a two-wire, bi-directional serial bus that provides a simple and efficient method of data exchange between devices. The I2C standard is a true multi-master bus including collision detection and arbitration that prevents data corruption if two or more masters attempt to control the bus simultaneously.

Data is transferred between a Master and a Slave synchronously to SCL on the SDA line on a byte-by-byte basis. Each data byte is 8-bit long. There is one SCL clock pulse for each data bit with the MSB being transmitted first. An acknowledge bit follows each transferred byte. Each bit is sampled during the high period of SCL; therefore, the SDA line may be changed only during the low period of SCL and must be held stable during the high period of SCL. A transition on the SDA line while SCL is high is interpreted as a command (START or STOP). Please refer to the following figure for more details about I2C Bus Timing.

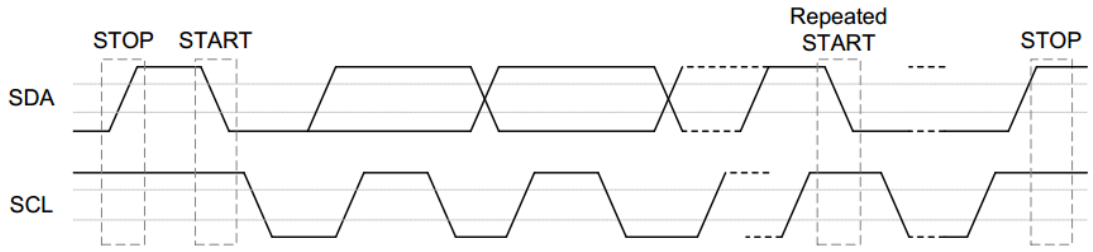


Figure 6: I2C Bus Timing

The device on-chip I2C logic provides the serial interface that meets the I2C bus standard mode specification. The I2C port handles byte transfers autonomously. The I2C H/W interfaces to the I2C bus via two pins: SDA and SCL. Pull up resistor is needed for I2C operation as these are open drain pins. When the I/O pins are used as I2C port, user must set the pins function to I2C in advance.

4.7.3 USB Device Controller

FSC-BT901 embed an USB OTG full-speed device/host/OTG peripheral with integrated transceivers.

4.8 PWM Generator and Capture Timer (PWM)

FSC-BT901 has **1** PWM generator. The PWM generator has a 16-bit PWM counter and comparator, and the PWM generator supports two standard PWM output modes: Independent output mode and Complementary output mode with 8-bit Dead-time generator. Each mode can be used as a timer and issues interrupt independently. In addition, It also has an 8-bit prescaler and clock divider with 5 divided frequencies (1, 1/2, 1/4, 1/8, 1/16) to support wide range clock frequency of PWM counter. For PWM output control unit, it supports polarity output function.

The PWM generator also supports input capture function. It supports latch PWM counter value to corresponding register when input channel has a rising transition, falling transition or both transition is happened.

5. ELECTRICAL CHARACTERISTICS

5.1 Absolute Maximum Ratings

Absolute maximum ratings for supply voltage and voltages on digital and analogue pins of the module are listed below. Exceeding these values causes permanent damage.

The average PIO pin output current is defined as the average current value flowing through any one of the corresponding pins for a 100mS period. The total average PIO pin output current is defined as the average current value flowing through all of the corresponding pins for a 100mS period. The maximum output current is defined as the value of the peak current flowing through any one of the corresponding pins.

Table 5: Absolute Maximum Rating

Parameter	Min	Max	Unit
V_{DD}-V_{SS} - DC Power Supply	-0.3	+3.6	V
V_{IN} - Input Voltage	Vss-0.3	Vdd+0.3	V
T_A - Operating Temperature	-40	+85	℃
T_{ST} - Storage Temperature	-40	+85	℃
I_{IO} - Maximum Current sunk by a I/O pin		4	mA
I_{IO} - Maximum Current sourced by a I/O pin		4	mA

5.2 Recommended Operating Conditions

Table 6: Recommended Operating Conditions

Parameter	Min	Type	Max	Unit
V_{DD}-V_{SS} - DC Power Supply	2.7	3.3	3.6	V
V_{IN} - Input Voltage	Vss-0.3	3.3	Vdd+0.3	V
T_A - Operating Temperature	-40	25	+85	°C
T_{ST} - Storage Temperature	-40	25	+85	°C
I_{IO} - Maximum Current sunk by a I/O pin	2	3	4	mA
I_{IO} - Maximum Current sourced by a I/O pin	2	3	4	mA

5.3 Input/output Terminal Characteristics

Table 7: DC Characteristics (V_{DD} - V_{SS} = 3 ~ 3.6 V, T_A = 25°C)

Parameter	Min	Type	Max	Unit
V_{DD} - Operation Voltage	3	3.3	3.6	V
V_{SS} - Power Ground	-0.3	-	-	V
V_{DD12} - Core Logic and I/O Buffer Pre-Driver Voltage	1.08	1.2	1.32	V
V_{OH} - High Level Output Voltage	2.4	-	-	V
V_{OL} - Low Level Output Voltage	-	-	0.4	V
V_{IH} - Input High Voltage	2.0	-	-	V
V_{IL} - Input Low Voltage	-	-	0.8	V
V_{TH} - Switch Threshold(Schmitt-falling-trigger)	0.87	1.05	1.2	V
V_{TH} - Switch Threshold(Schmitt-rising-trigger)	1.65	1.9	2.1	V
R_{PU} - Input Pull-up Resist(V_{IN}=V_{SS})	32	53	120	KΩ
R_{PD} - Input Pull-down Resist(V_{IN}=V_{DD})	37	49	120	KΩ
I_L - Input Leakage Current	-10	-	10	uA
I_{OZ} - Tri-State Output Leakage Current	-10	-	10	uA
I_{OL} - Low level sink current(V_{OL}=0.4V)	4	-	-	mA
I_{OH} - High level source current (V_{OH}=2.4V)	4	-	-	mA

5.4 Analog Characteristics

5.4.1 Specifications of 12-bit ADC

Table 8: ADC characteristics

Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA} - Power supply	V_{DDA} V_{REF+} < 1.2 V	1.7(1)	-	3.6	V
VREF+ - Positive reference voltage		1.7(1)	-	V_{DDA}	V
f_{ADC} - ADC clock frequency	V_{DDA} = 1.7(1) to 2.4 V	0.6	15	18	MHz
	V_{DDA} = 2.4 to 3.6 V	0.6	30	36	MHz
f_{TRIG}(2) - External trigger frequency	f_{ADC} = 30 MHz, 12-bit resolution	-	-	1764	kHz

		-	-	17	$1/f_{ADC}$
V_{AIN} - Conversion voltage range(3)		0 (V_{SSA} or V_{REF} - tied to ground)	-	V_{REF+}	V
R_{AIN}(2) - External input impedance	See **Equation 1** for details	-	-	50	KΩ
R_{ADC}(2)(4) - Sampling switch resistance		-	-	6	KΩ
C_{ADC}(2) - Internal sample and hold capacitor		-	4	7	pF
t_{lat}(2) - Injection trigger conversion latency	f_{ADC} = 30 MHz	-	-	0.100	µs
		-	-	3(5)	$1/f_{ADC}$
t_{latr}(2) - Regular trigger conversion latency	f_{ADC} = 30 MHz	-	-	0.067	µs
		-	-	2(5)	$1/f_{ADC}$
t_S(2) - Sampling time	f_{ADC} = 30 MHz	0.100	-	16	µs
		3	-	480	$1/f_{ADC}$
t_{STAB}(2) - Power-up time		-	2	3	µs
t_{CONV}(2) - Total conversion time (including sampling time)	f_{ADC} = 30 MHz 12-bit resolution	0.50	-	16.40	µs
	f_{ADC} = 30 MHz 10-bit resolution	0.43	-	16.34	µs
	f_{ADC} = 30 MHz 8-bit resolution	0.37	-	16.27	µs
	f_{ADC} = 30 MHz 6-bit resolution	0.30	-	16.20	µs
	9 to 492 (t_s for sampling +n-bit resolution for successive approximation)				$1/f_{ADC}$
f_S(2) - Sampling rate (f_{ADC} = 30 MHz, and t_S = 3 ADC cycles)	12-bit resolution Single ADC	-	-	2	M_{sps}
	12-bit resolution Interleave Dual ADC mode	-	-	3.75	M_{sps}
	12-bit resolution Interleave Triple ADC mode	-	-	6	M_{sps}
I_{VREF+}(2) - ADC V_{REF} DC current consumption in conversion mode		-	300	500	µA
I_{VDDA}(2) - ADC V_{DDA} DC current consumption in conversion mode		-	1.6	1.8	mA

1. V_{DDA} minimum value of 1.7 V is possible with the use of an external power supply supervisor
   In the circuit of this module, V_{DDA}=V_{DD}.
2. Guaranteed by characterization.
3. V_{REF+} is internally connected to V_{DDA} and V_{REF-} is internally connected to V_{SSA}.
4. R_{ADC} maximum value is given for V_{DD}=1.7 V, and minimum value for V_{DD}=3.3 V.
5. For external triggers, a delay of $1/f_{PCLK2}$ must be added to the latency specified in this Table.

Equation 1: RAIN max formula

$$R_{AIN} = \frac{(k-0,5)}{f_{ADC} \times C_{ADC} \times \ln(2^{N+2})} - R_{ADC}$$

The formula above (**Equation 1**) is used to determine the maximum external impedance allowed for an error below 1/4 of LSB. N = 12 (from 12-bit resolution) and k is the number of sampling periods defined in the ADC_SMPR1 register.

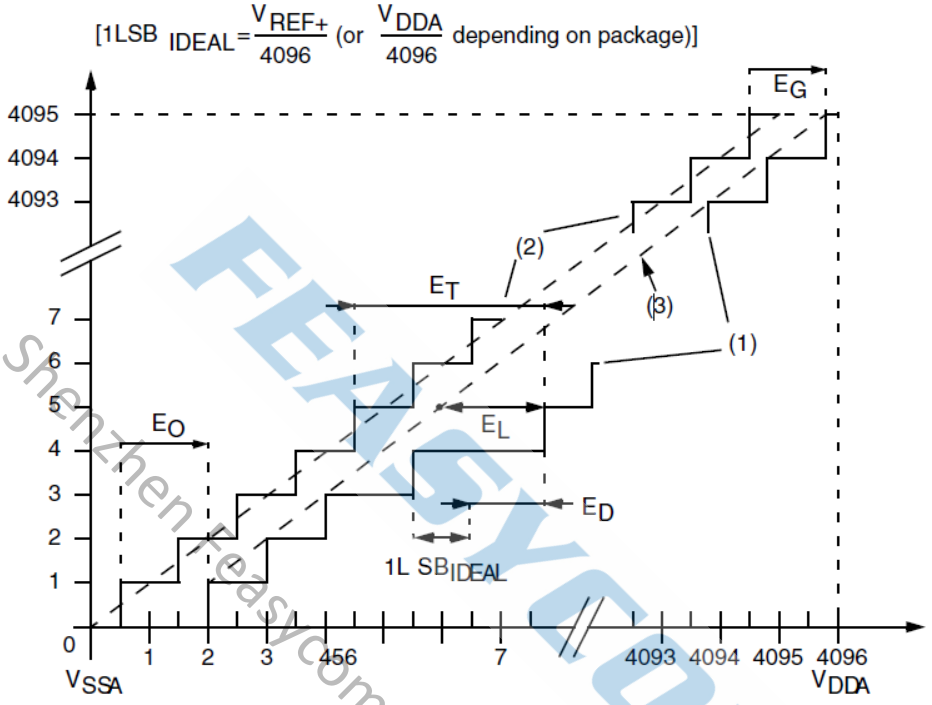


Figure 7: ADC accuracy characteristics

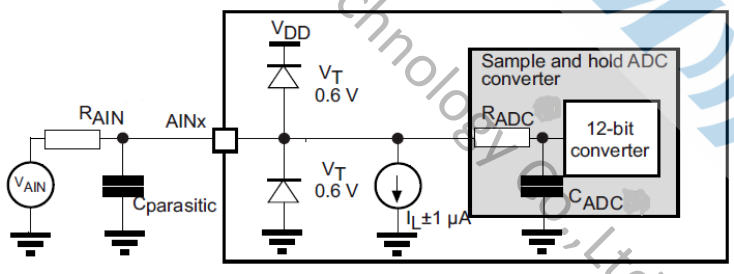


Figure 8: Typical connection diagram using the ADC

5.5 USB PHY Specifications

5.5.1 USB DC Electrical Characteristics

Table 9: USB OTG FS startup time

Parameter	Conditions	Min	Typ	Max	Unit
$t_{STARTUP}$(1) - USB OTG FS transceiver startup time				1	uS
1. Guaranteed by design.					

Table 10: USB OTG FS DC electrical characteristics

Parameter	Conditions	Min(1)	Typ	Max(1)	Unit
Input levels				1	uS
V_{DD} - USB OTG FS operating voltage		3.0(2)	-	3.6	V
V_{DI}(3) - Differential input sensitivity	I(USB_FS_DP/DM)	0.2	-	-	V
V_{CM}(3) - Differential common mode range	Includes VDI range	0.8	-	2.5	V
V_{SE}(3) - Single ended receiver threshold		1.3	-	2.0	V
Output levels					
V_{OL} - Static output level low	R_L of 1.5 kΩ to 3.6V(4)	-	-	0.3	V
V_{OH} - Static output level high	R_L of 15 kΩ to VSS(4)	2.8	-	3.6	V
R_{PD} - USB_FS_DM/DP	$V_{IN} = V_{DD}$	17	21	24	KΩ
R_{PU} - USB_FS_DM/DP	$V_{IN} = V_{SS}$	1.5	1.8	2.1	KΩ

1. All the voltages are measured from the local ground potential.
2. The USB OTG FS functionality is ensured down to 2.7 V but not the full USB full speed electrical characteristics which are degraded in the 2.7-to-3.0 V V_{DD} voltage range.
3. Guaranteed by design.
4. RL is the load connected on the USB OTG FS drivers.

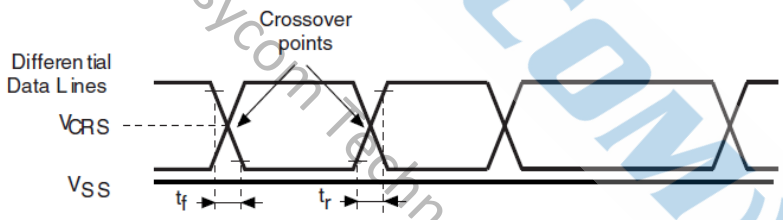


Figure 9: USB OTG FS timings: definition of data signal rise and fall time

Table 11: USB OTG FS electrical characteristics(1)

Parameter	Conditions	Min(1)	Typ	Max(1)	Unit
t_r - Rise time(2)	C_L = 50 pF	4	-	20	nS
t_f - Fall time(2)	C_L = 50 pF	4	-	20	nS
t_{rfm} - Rise/ fall time matching	t_r/t_f	90	-	110	%
V_{CRS} - Output signal crossover voltage		1.3	-	2.0	nS

1. Guaranteed by design.
2. Measured from 10% to 90% of the data signal. For more detailed informations, please refer to USB Specification - Chapter 7 (version 2.0).

5.6 I2C Dynamic Characteristics

Table 12: I2C Dynamic Characteristics

Parameter	Standard Mode[1][2]		Fast Mode[1][2]		Unit
	Min	Max	Min	Max	
t_{LOW} - SCL low period	4.7	-	1.2	-	uS
T_{HIGH} - SCL high period	4	-	0.6	-	uS
$t_{SU;STA}$ - Repeated START condition setup time	4.7	-	1.2	-	uS
$t_{HD;STA}$ - START condition hold time	4	-	0.6	-	uS
$t_{SU;STO}$ - STOP condition setup time	4	-	0.6	-	uS
t_{BUF} - Bus free time	4.7[3]	-	1.2[3]	-	uS
$t_{SU;DAT}$ - Data setup time	250	-	100	-	uS
$t_{HD;DAT}$ - Data hold time	0[4]	3.45[5]	0[4]	0.8[5]	uS
t_r - SCL/SDA rise time	-	1000	20+0.1CB	300	uS
t_f - SCL/SDA fall time	-	300	-	300	uS
C_b - Capacitive load for each bus line	-	400	-	400	pF

Note:

1. Guaranteed by design, not tested in production.
2. HCLK must be higher than 2 MHz to achieve the maximum standard mode I2C frequency. It must be higher than 8 MHz to achieve the maximum fast mode I2C frequency.
3. I2C controller must be retriggered immediately at slave mode after receiving STOP condition.
4. The device must internally provide a hold time of at least 300 ns for the SDA signal in order to bridge the undefined region of the falling edge of SCL.
5. The maximum hold time of the Start condition has only to be met if the interface does not stretch the low period of SCL signal.

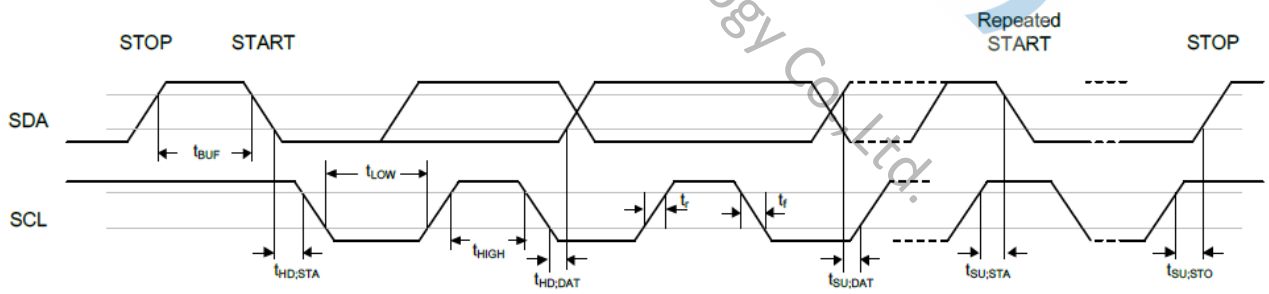
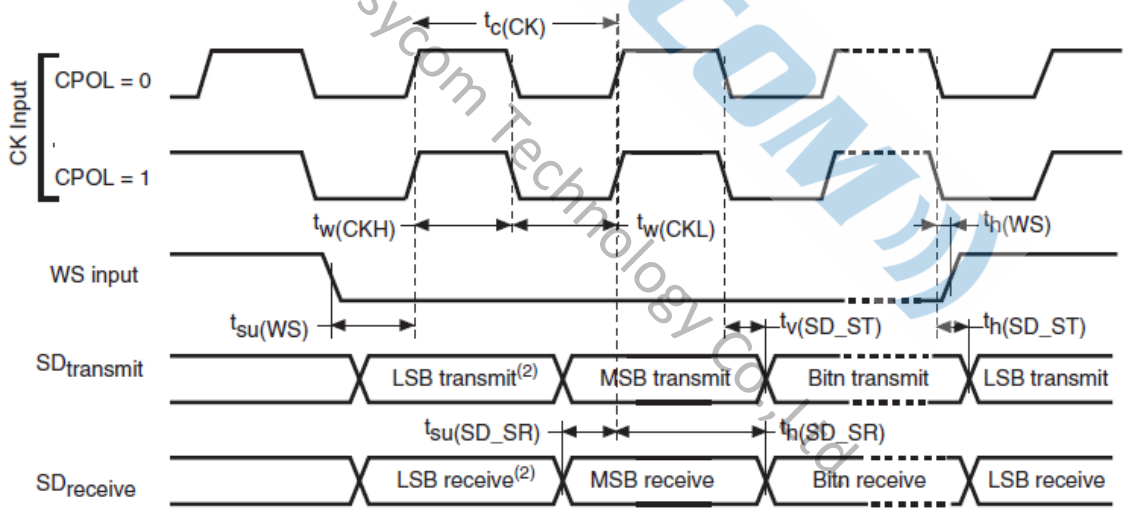


Figure 10: I2C Timing Diagram

5.7 I2S Dynamic Characteristics

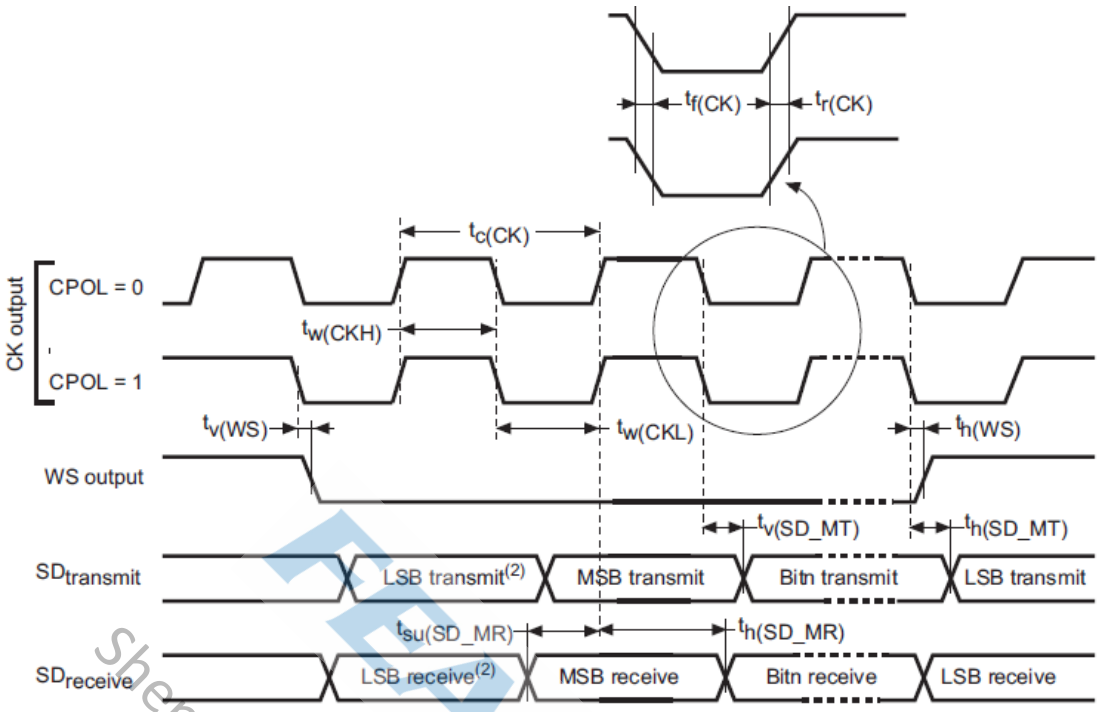
Table 13: I2S Dynamic Characteristics

Parameter	Test Conditions	Min	Max	Unit
f_{CK} - I2S clock frequency	Master data: 32 bits	-	64xFs	MHZ
	Slave data: 32 bits	-	64xFs	MHZ
D_{CK} - I2S clock frequency duty cycle	Slave receiver	30	70	%
$t_{v(WS)}$ - WS valid time	Master mode	0	6	nS
$t_{h(WS)}$ - WS hold time	Master mode	0	-	nS
$t_{su(WS)}$ - WS setup time	Slave mode	1	-	nS
$t_{h(WS)}$ - WS hold time	Slave mode	0	-	nS
$t_{su(SD\_MR)}$ - Data input setup time	Master mode	7.5	-	nS
$t_{h(SD\_SR)}$ - Data input setup time	Slave mode	2	-	nS
$t_{h(SD\_MR)}$ - Data input hold time	Master mode	0	-	nS
$t_{h(SD\_SR)}$ - Data input hold time	Slave mode	0	-	nS
$t_{v(SD\_ST)}$ - Data output valid time	Slave transmitter (after enable edge)	0	-	nS
$t_{h(SD\_ST)}$ - Data output valid time	Slave transmitter (after enable edge)	-	27	nS
$t_{v(SD\_MT)}$ - Data output valid time	Master transmitter (after enable edge)	-	20	nS
$t_{h(SD\_MT)}$ - Data output hold time	Master transmitter (after enable edge)	2.5	-	nS



1. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

Figure 11: I2S slave timing diagram (Philips protocol)(1)



1. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

Figure 12: I2S master timing diagram (Philips protocol)(1)

5.8 PWM Characteristics

Table 14: TIMx characteristics(1)(2)

Parameter	Conditions	Min	Typ	Max	Unit
$t_{res(TIM)}$ - Timer resolution time	AHB/APBx prescaler=1 or 2 or 4, $f_{TIMxCLK}$ = 84 MHz	1	-	-	$t_{TIMxCLK}$
		11.9	-	-	nS
	AHB/APBx prescaler>4, $f_{TIMxCLK}$ = 84 MHz	1	-	-	$t_{TIMxCLK}$
		11.9	-	-	nS
f_{EXT} - Timer external clock frequency	$f_{TIMxCLK}$ = 84 MHz	0	-	$f_{TIMxCLK}/2$	MHz
		0		42	MHz
Res_{TIM} - Timer resolution		-	-	16/32	bit
$t_{COUNTER}$ - 16-bit counter clock period when internal clock is selected	$f_{TIMxCLK}$ = 84 MHz	0.0119	-	780	uS
t_{MAX_COUNT} - Maximum possible count with 32-bit counter		-	-	65536 × 65536	$t_{TIMxCLK}$
	$f_{TIMxCLK}$ = 84 MHz	-	-	51.1	S

1. TIMx is used as a general term to refer to the TIM1 to TIM11 timers.
2. Guaranteed by design.
3. The maximum timer frequency on APB1 is 42 MHz and on APB2 is up to 84 MHz, by setting the TIMPRE bit in the RCC_DCKCFGR register, if APBx prescaler is 1 or 2 or 4, then TIMxCLK = HCKL, otherwise TIMxCLK >= 4x PCLKx.

5.9 Power consumptions

Table 15: Power consumptions **(TBD)**

Parameter	Test Conditions	Type	Unit
Search		~35	mA
Unconnected (Deep Sleep Idle Mode)		<1	mA
Connected Idle		~19	mA
Play with Minimum Volume	No support	-	mA
Play with Maximum Volume	No support	-	mA
Shutdown	No support		mA

6. MSL & ESD

Table 16: MSL and ESD

Parameter	Value
MSL grade:	MSL 3
ESD grade:	Human Body Model: Class-2 Machine Model: Class-B

7. RECOMMENDED TEMPERATURE REFLOW PROFILE

Prior to any reflow, it is important to ensure the modules were packaged to prevent moisture absorption. New packages contain desiccate (to absorb moisture) and a humidity indicator card to display the level maintained during storage and shipment. If directed to bake units on the card, please check the below **Table 17** and follow instructions specified by IPC/JEDEC J-STD-033.

Note: The shipping tray cannot be heated above 65°C. If baking is required at the higher temperatures displayed in the below **Table 17**, the modules must be removed from the shipping tray.

Any modules not manufactured before exceeding their floor life should be re-packaged with fresh desiccate and a new humidity indicator card. Floor life for MSL (Moisture Sensitivity Level) 3 devices is 168 hours in ambient environment 30°C/60%RH.

Table 17: Recommended baking times and temperatures

MSL	125°C Baking Temp.		90°C/≤ 5%RH Baking Temp.		40°C/ ≤ 5%RH Baking Temp.	
	Saturated @ 30°C/85%	Floor Life Limit + 72 hours @ 30°C/60%	Saturated @ 30°C/85%	Floor Life Limit + 72 hours @ 30°C/60%	Saturated @ 30°C/85%	Floor Life Limit + 72 hours @ 30°C/60%
3	9 hours	7 hours	33 hours	23 hours	13 days	9 days

Feasycom surface mount modules are designed to be easily manufactured, including reflow soldering to a PCB. Ultimately it is the responsibility of the customer to choose the appropriate solder paste and to ensure oven temperatures during reflow meet the requirements of the solder paste. Feasycom surface mount modules conform to J-STD-020D1 standards for reflow temperatures.

The soldering profile depends on various parameters necessitating a set up for each application. The data here is given only for guidance on solder reflow.

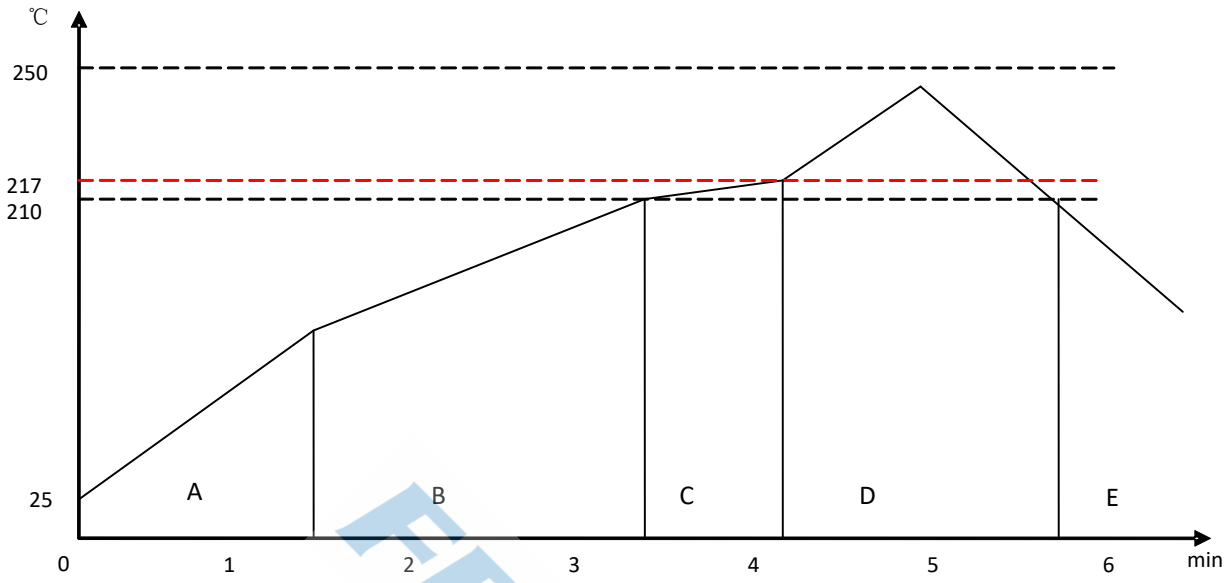


Figure 13: Typical Lead-free Re-flow

Pre-heat zone (A) — This zone raises the temperature at a controlled rate, **typically 0.5 – 2 °C/s**. The purpose of this zone is to preheat the PCB board and components to 120 ~ 150 °C. This stage is required to distribute the heat uniformly to the PCB board and completely remove solvent to reduce the heat shock to components.

Equilibrium Zone 1 (B) — In this stage the flux becomes soft and uniformly encapsulates solder particles and spread over PCB board, preventing them from being re-oxidized. Also with elevation of temperature and liquefaction of flux, each activator and rosin get activated and start eliminating oxide film formed on the surface of each solder particle and PCB board. **The temperature is recommended to be 150° to 210° for 60 to 120 second for this zone.**

Equilibrium Zone 2 (C) (optional) — In order to resolve the upright component issue, it is recommended to keep the temperature in 210 – 217 ° for about 20 to 30 second.

Reflow Zone (D) — The profile in the figure is designed for Sn/Ag3.0/Cu0.5. It can be a reference for other lead-free solder. The peak temperature should be high enough to achieve good wetting but not so high as to cause component discoloration or damage. Excessive soldering time can lead to intermetallic growth which can result in a brittle joint. The recommended peak temperature (Tp) is 230 ~ 250 °C. The soldering time should be 30 to 90 second when the temperature is above 217 °C.

Cooling Zone (E) — The cooling ate should be fast, to keep the solder grains small which will give a longer-lasting joint. **Typical cooling rate should be 4 °C.**

8. MECHANICAL DETAILS

8.1 Mechanical Details

- Dimension: 10mm(W) x 11.9mm(L) x 1.7mm(H) Tolerance: ±0.1mm
- Module size: 10mm X 11.9mm Tolerance: ±0.1mm
- Pad size: 0.9mmX0.6mm Tolerance: ±0.1mm
- Pad pitch: 1.1mm Tolerance: ±0.1mm

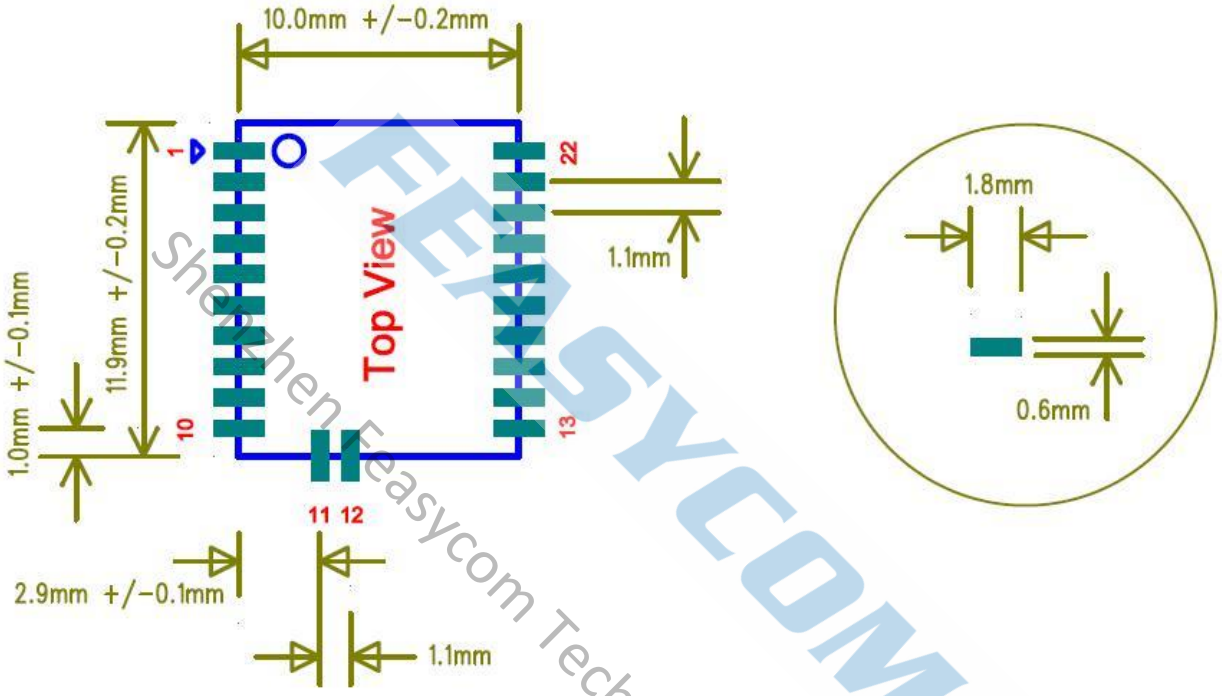


Figure 14: FSC-BT901 footprint

9. HARDWARE INTEGRATION SUGGESTIONS

9.1 Soldering Recommendations

FSC-BT901 is compatible with industrial standard reflow profile for Pb-free solders. The reflow profile used is dependent on the thermal mass of the entire populated PCB, heat transfer efficiency of the oven and particular type of solder paste used. Consult the datasheet of particular solder paste for profile configurations.

Feasycom will give following recommendations for soldering the module to ensure reliable solder joint and operation of the module after soldering. Since the profile used is process and layout dependent, the optimum profile should be studied case by case. Thus following recommendation should be taken as a starting point guide.

9.2 Layout Guidelines(Internal Antenna)

It is strongly recommended to use good layout practices to ensure proper operation of the module. Placing copper or any metal near antenna deteriorates its operation by having effect on the matching properties. Metal shield around the antenna will prevent the radiation and thus metal case should not be used with the module. Use grounding vias separated max 3 mm apart at the edge of grounding areas to prevent RF penetrating inside the PCB and causing an

unintentional resonator. Use GND vias all around the PCB edges.

The mother board should have no bare conductors or vias in this restricted area, because it is not covered by stop mask print. Also no copper (planes, traces or vias) are allowed in this area, because of mismatching the on-board antenna.

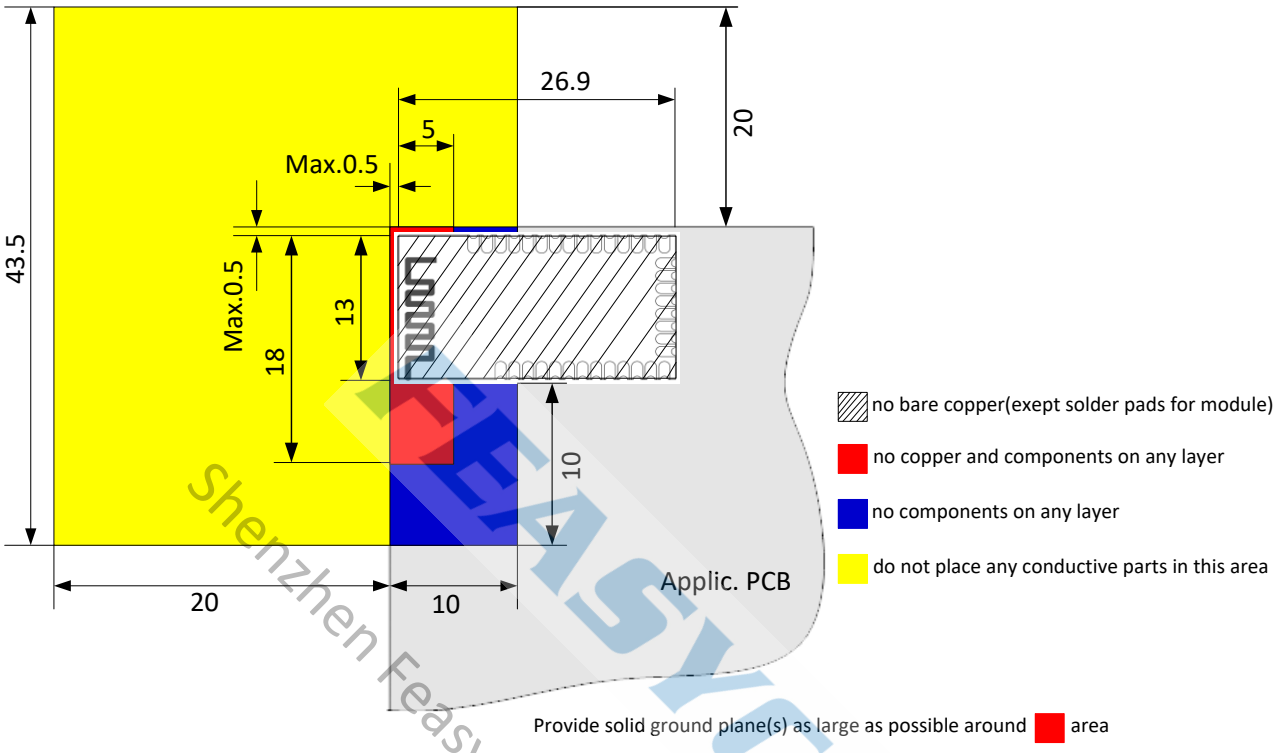


Figure 15: FSC-BT901 Restricted Area

Following recommendations helps to avoid EMC problems arising in the design. Note that each design is unique and the following list do not consider all basic design rules such as avoiding capacitive coupling between signal lines. Following list is aimed to avoid EMC problems caused by RF part of the module. Use good consideration to avoid problems arising from digital signals in the design.

Ensure that signal lines have return paths as short as possible. For example if a signal goes to an inner layer through a via, always use ground vias around it. Locate them tightly and symmetrically around the signal vias. Routing of any sensitive signals should be done in the inner layers of the PCB. Sensitive traces should have a ground area above and under the line. If this is not possible, make sure that the return path is short by other means (for example using a ground line next to the signal line).

9.3 Layout Guidelines(External Antenna)

Placement and PCB layout are critical to optimize the performances of a module without on-board antenna designs. The trace from the antenna port of the module to an external antenna should be 50Ω and must be as short as possible to avoid any interference into the transceiver of the module. The location of the external antenna and RF-IN port of the module should be kept away from any noise sources and digital traces. A matching network might be needed in between the external antenna and RF-IN port to better match the impedance to minimize the return loss.

As indicated in **Figure 16** below, RF critical circuits of the module should be clearly separated from any digital circuits on the system board. All RF circuits in the module are close to the antenna port. The module, then, should be placed in this way that module digital part towards your digital section of the system PCB.

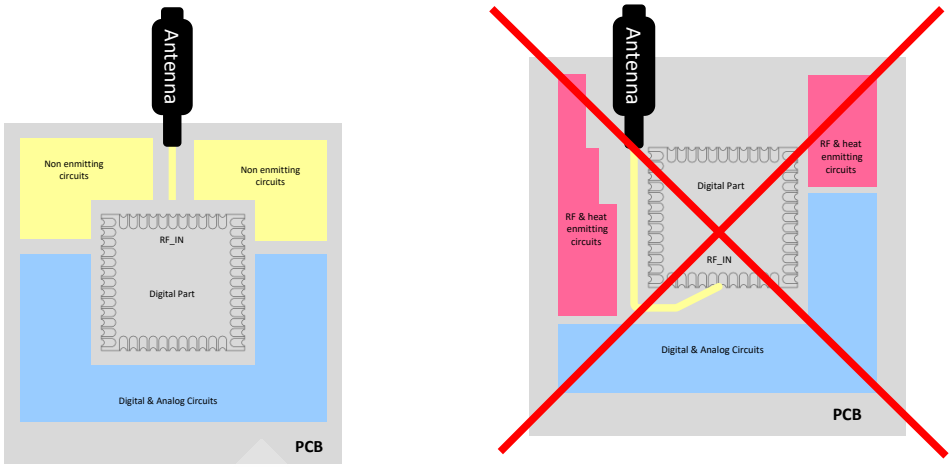


Figure 16: Placement the Module on a System Board

9.3.1 Antenna Connection and Grounding Plane Design

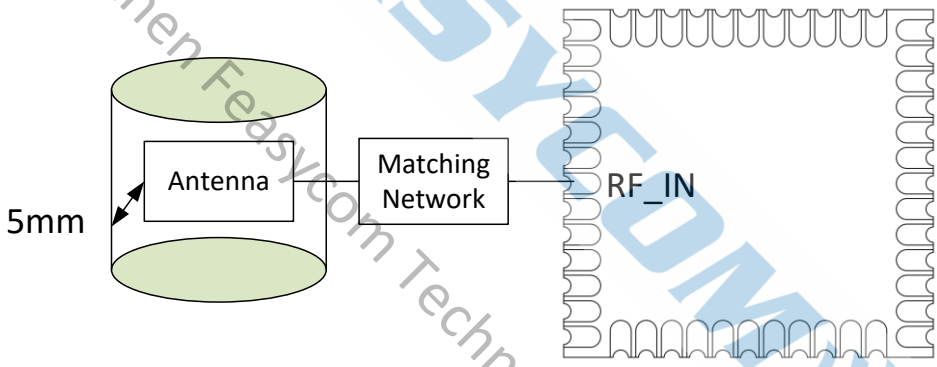


Figure 17: Leave 5mm Clearance Space from the Antenna

General design recommendations are:

- The length of the trace or connection line should be kept as short as possible.
- Distance between connection and ground area on the top layer should at least be as large as the dielectric thickness.
- Routing the RF close to digital sections of the system board should be avoided.
- To reduce signal reflections, sharp angles in the routing of the micro strip line should be avoided. Chamfers or fillets are preferred for rectangular routing; 45-degree routing is preferred over Manhattan style 90-degree routing.

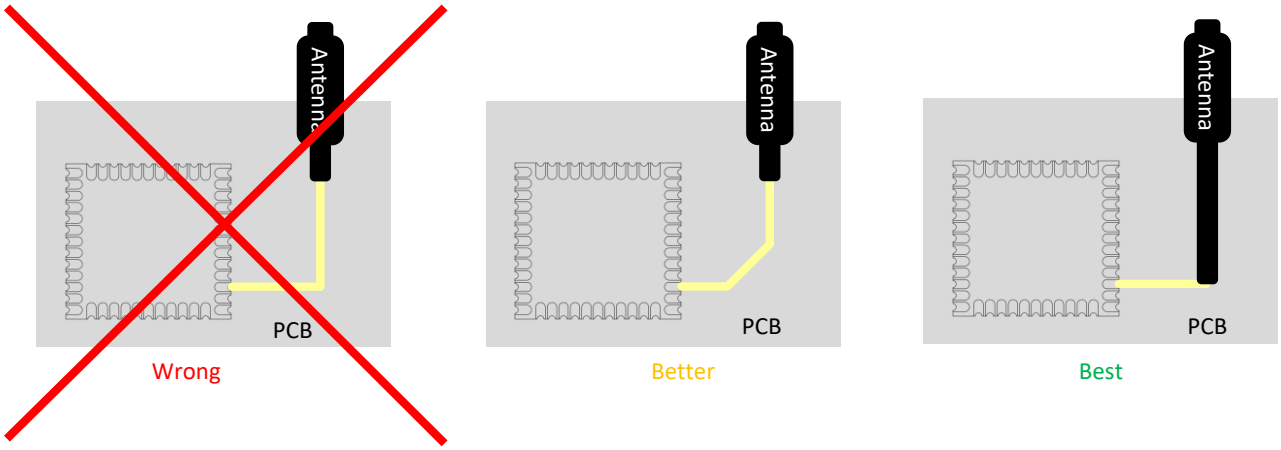


Figure 18: Recommended Trace Connects Antenna and the Module

- Routing of the RF-connection underneath the module should be avoided. The distance of the micro strip line to the ground plane on the bottom side of the receiver is very small and has huge tolerances. Therefore, the impedance of this part of the trace cannot be controlled.
- Use as many vias as possible to connect the ground planes.

10. PRODUCT PACKAGING INFORMATION

10.1 Default Packing

a, Tray vacuum

b, Tray Dimension: 180mm * 195mm

Figure 19: Tray vacuum (Image for reference only, subject to actual product)

11. APPLICATION SCHEMATIC