Data Sheet

BCM81356

16-nm 16 x 56 Gb/s PAM-4 Duplex PHY

Overview

The Broadcom® BCM81356 is a single-chip 16 × 56 Gb/s full-duplex PHY. It supports both the PAM-4 and NRZ data formats. It supports various operation modes, such as Retimer, Forward, and Reverse Gearbox modes. It also supports 10G, 25G, 40G, 50G, 100G, 200G, and 400G line-card applications.

On-chip clock synthesis is performed by a low-cost reference clock through high-frequency, low-jitter phase-locked loops (PLLs).

The BCM81356 is fabricated in advanced low-power 16-nm CMOS technology.

The BCM81356 is available in a 23 mm × 23 mm, 0.8-mm pitch, 729-ball BGA, RoHS-compliant package.

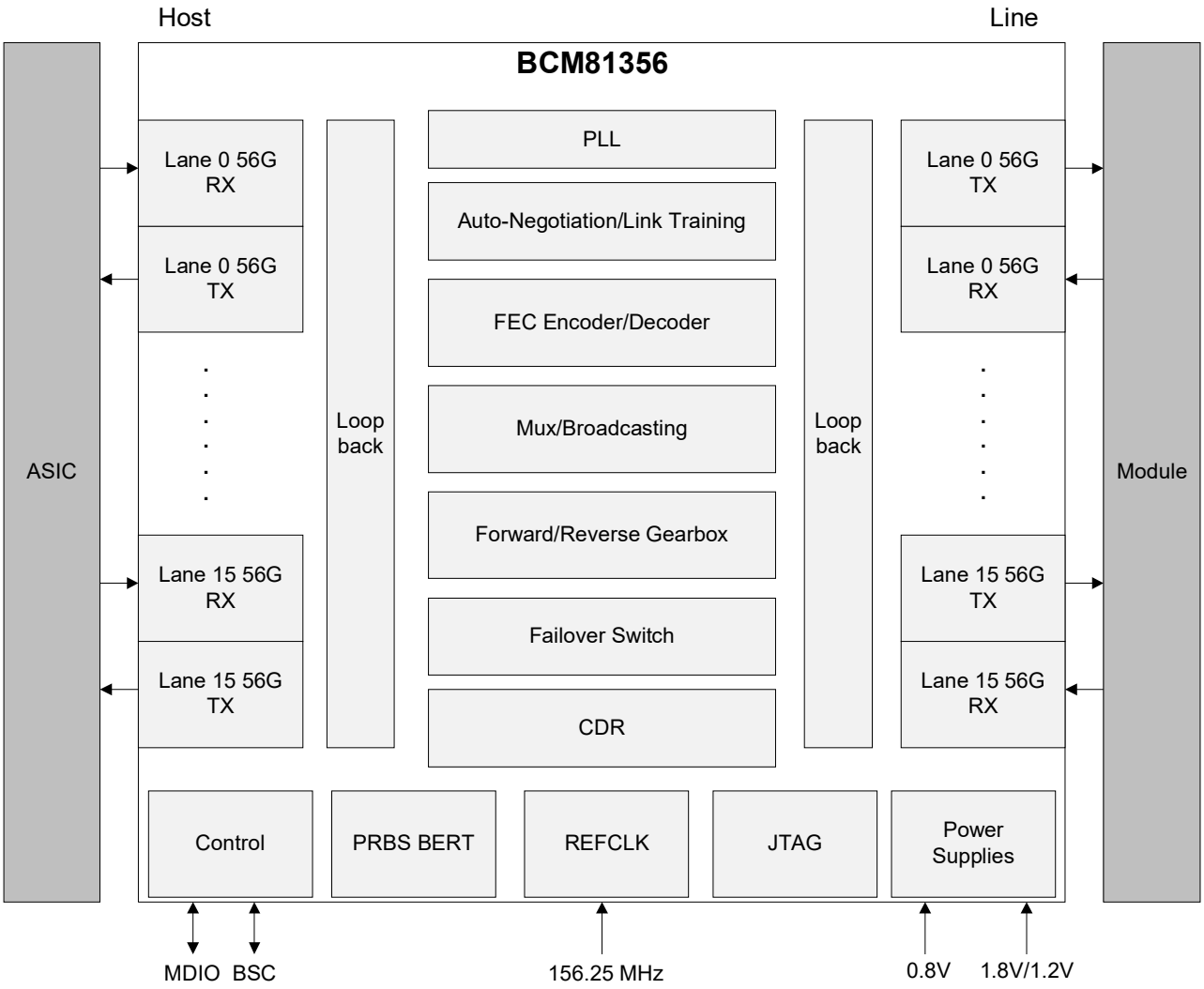
Applications

- ASIC-to-module interface 16 × 56 Gb/s front-panel and backplane applications
- High-density 10G, 25G, 40G, 50G, 100G, 200G, and 400G front-panel and backplane line-card applications

Features

- Host-side interface:
  - Long reach (LR): ~30 dB
  - High-performance analog SerDes
- Line-side interface:
  - KR: >30 dB
  - CR: >30 dB
  - Chip-to-module (C2M)
  - High-performance DSP SerDes
- Retimer, Forward, and Reverse Gearbox modes
- Flexible crossbar
- Supports forward error correction (FEC)
- Supports Mux and Broadcasting modes
- supports 400G-CR8 mode
- Integrated AC-coupling capacitors at host-side and line-side receiver
- Multiple standard and line rate support for both PAM-4 and NRZ
- Continuous auto-adaptive equalizer
- Line- and system-side loopbacks
- PRBS generator/error checker
- Eye monitoring per lane accessed through MDIO
- Dual low-cost REFCLK inputs
- Recovered clock output
- Interoperates with Broadcom ASIC and merchant switch silicon
- Low-power 16-nm CMOS design

Figure 1: BCM81356 Block Diagram



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Chapter 1: Functional Description

The PHY is made up of four cores, with each core supporting four high-speed lanes. Figure 1 shows the interface block diagram of the BCM81356.

Figure 1: BCM81356 Interface Diagram

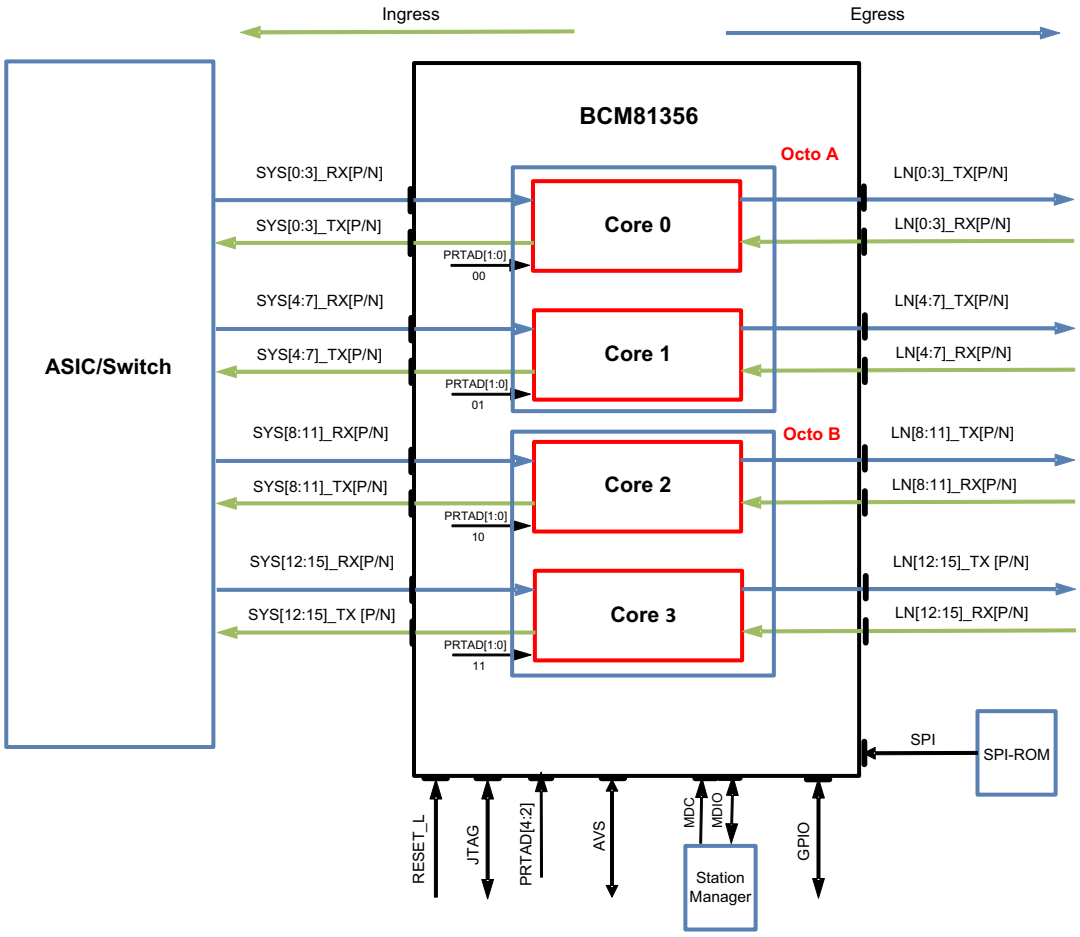
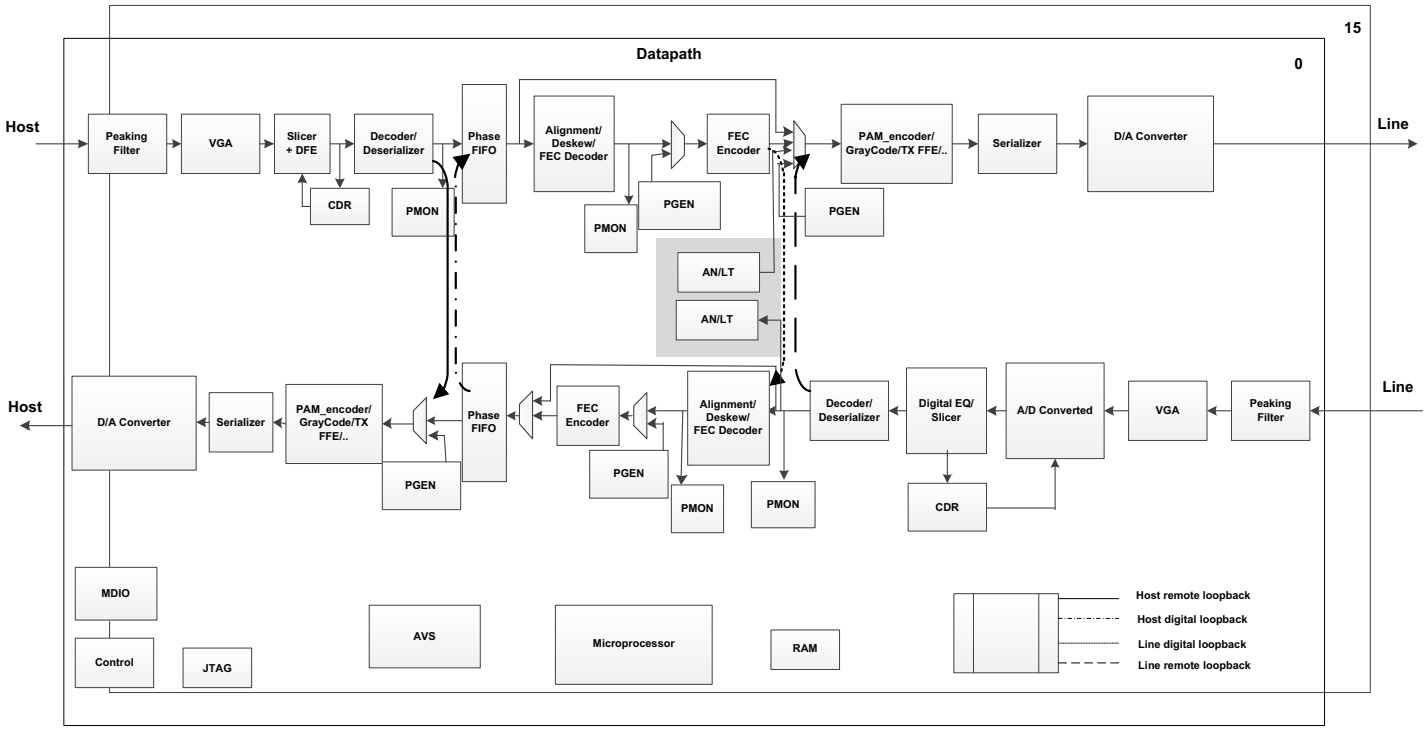


Figure 2 shows the detailed block diagram of the BCM81356.

Figure 2: BCM81356 Detailed Block Diagram



1.1 Device Functions

The BCM81356 comprises 16 channels, and each channel contains two data paths:

- Egress: host (ASIC/MAC) to line (optical module/directly attached cable [DAC]/backplane) path
- Ingress: line (optical module/DAC/backplane) to host (ASIC/MAC) path

Both line-side and host-side interface transmitter are based on a high-resolution digital-to-analog converter (DAC). The TX equalization is provided by a conventional multitap TXFIR structure.

Both line-side and host-side interfaces have pseudorandom bit sequence (PRBS) generator and checker capability. The line-side interface also supports SSPRQ, QPRBS13, and square-wave generation.

The line-side interface has link training capability compliance to the IEEE 802.3cd clause 136.

The BCM81356 has an option to have low-power digital power consumption through an adaptive voltage scaling (AVS) scheme. See Section 1.4, Adaptive Voltage Scaling.

1.2 High-Speed Line-Side Interfaces

The line-side interface receiver is a high-performance, ADC-based digital equalizer, which includes an analog peaking filter (PF) and a variable gain amplifier (VGA) in analog front end, and a high-performance analog-to-digital converter (ADC) with digital equalizer of feed-forward equalizer (FFE) and a clock and data recovery (CDR) circuitry. There are integrated AC-coupling capacitors on the line-side receiver. The line-side interface is compliant to the CEI-28G/56G-LR specifications, and can support backplane channels with 30 dB insertion loss (in Nyquist frequency).

1.2.1 Peaking Filter and VGA

The analog PF realized by a programmable continuous-time linear equalizer (CTLE) provides the first-order equalization by boosting the high-frequency content to compensate the intersymbol interference (ISI) on the incoming data. The peak of the peaking filter can be adjusted by registers for different backplane channel characteristics. After analog PF, the signal is further enhanced through a variable gain amplifier (VGA) and the gain is automatically controlled by means of a gain control loop for best ADC performance.

1.2.2 Analog-to-Digital Converter (ADC)/Equalizer/Timing Recovery

A high-performance ADC is implemented after the PF and VGA stages. The incoming data samples at baud rate, and the digitalized samples are subsequently post-processed by the digital equalizer (EQ) prior to slicing.

The digital equalizer has a multitap baud-rate FFE, which equalizes the sampled signal. The equalizer is continuously adapted to the incoming signal variation with the least mean squared (LMS) algorithm.

The timing recovery block recovers both the phase and frequency of the incoming data stream. Further, it determines the optimal sampling phase for obtaining the best-recovered signal after equalization. Data is determined at slicer with optimal timing by fully adapted timing recovery block.

All RX EQ and analog parameters are automatically configured and adapted for best CDR and EQ operation using a combination of hardware and firmware running in a microcontroller.

1.3 High-Speed Host-Side Interfaces

The host-side interface receiver is an analog equalizer including a PF, a VGA, and a multitap decision-feedback equalizer (DFE) with a CDR circuit synchronizing the receiver with the incoming data stream. There is an integrated on-die AC-coupling capacitor on the host receiver. See Section 3.1, Functional Ball Descriptions, for common-mode and maximum peaking voltage restriction.

1.3.1 Peaking Filter and VGA

The host-side analog front end implements a similar analog block of PF and VGA as the line side.

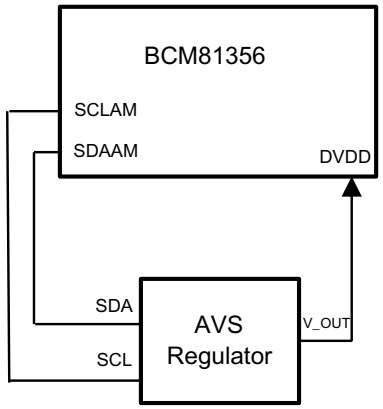
1.3.2 Decision Feedback Equalizer (DFE)/Timing Recovery

A multitap DFE is implemented after the PF and VGA stage, where it continuously adapts to the incoming signal with the least mean squared (LMS) algorithm, together with a CDR block, recover both the phase and frequency of the incoming data stream and determine the optimal sampling phase for obtaining the best-recovered signal after equalization.

1.4 Adaptive Voltage Scaling

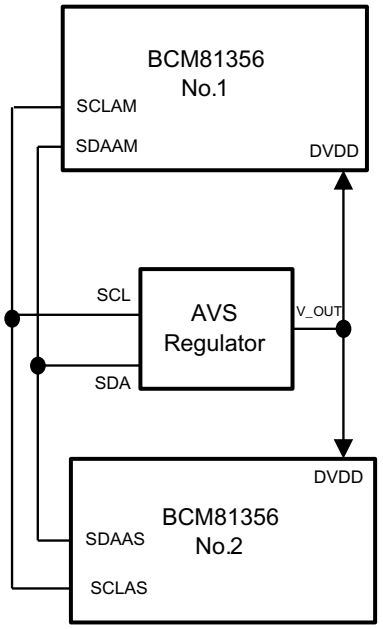
The BCM81356 implements Broadcom Serial Control (BSC) interface to achieve lower digital power consumption through adaptive voltage scaling (AVS). The BSC master interface is compatible with the I^2C standard. The hardware configuration (as shown in Figure 3) is realized by connecting an AVS voltage regulator, with a secondary I^2C-compatible port, to the BCM81356 BSC master pins (SCLAM, SDAAM), and the output of the AVS regulator connecting to the BCM81356 DVDD power rail. The AVS process is controlled automatically by the firmware, where the AVS algorithm is part of firmware and, when enabled, the firmware controls the AVS regulator's output voltage to adapt to the lowest DVDD voltage possible at the chip live operating condition, while still ensuring proper chip operation. Clearly, the lowest digital power consumption is achieved by maintaining lowest DVDD voltage possible at the live chip operating condition.

Figure 3: AVS Configuration (One Regulator for One Retimer)



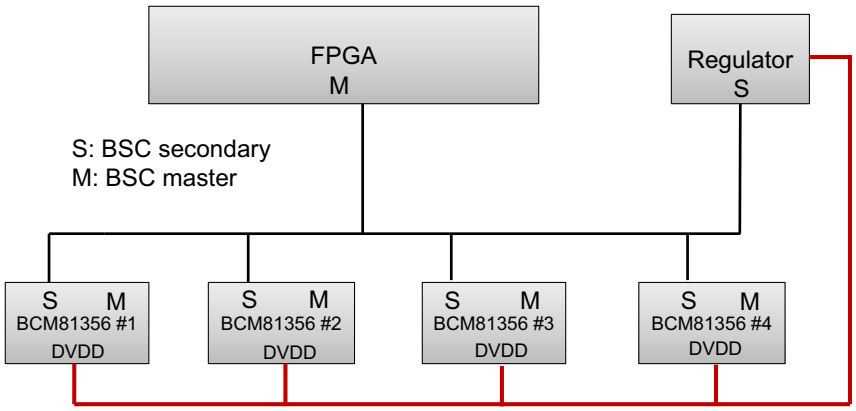
Two BCM81356 devices can share one AVS regulator as shown in Figure 5. The BCM81356 no. 1 is the master package that controls both the AVS regulator and the BCM81356 no. 2, where the BCM81356 no. 2 secondary AVS BSC port should be connected to the AVS master BSC ports of the BCM81356 no. 1.

Figure 4: AVS Configuration (One Regulator for Two Retimers)



An example configuration of multiple BCM81356 devices sharing one AVS regulator is shown in Figure 5. All the BCM81356 devices are secondary devices. The external FPGA is the master that collects voltage information from the secondary devices and controls the regulator accordingly. Additional control algorithms are provided.

Figure 5: AVS Configuration (One Regulator for Multiple Packages)



1.5 Loss of Signal and Signal Detection

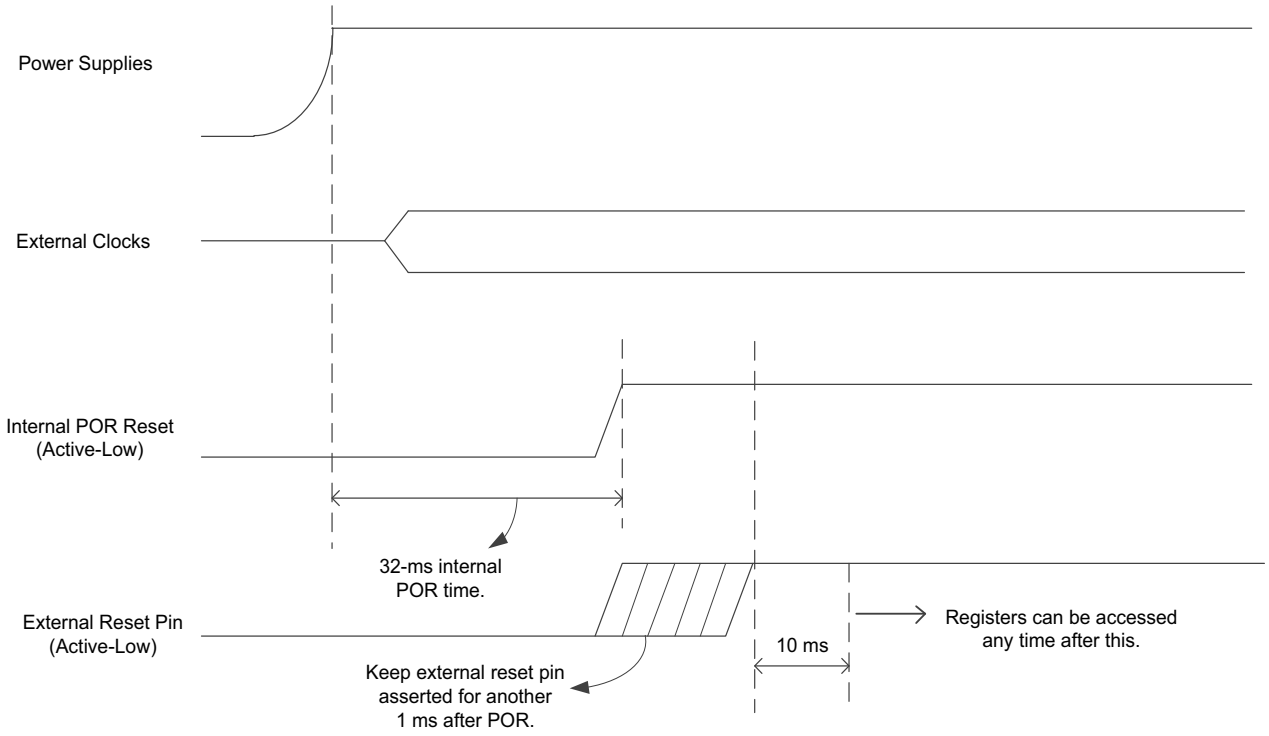
The BCM81356 contains a loss-of-signal (LOS) detect circuit that monitors the energy of the receiving signal. A peak detector looks for a minimum amplitude swing. The LOS status is observable in the RX status register.

1.6 Reset Timing

The RESET_L is a global hardware reset pin that is used to clear the entire chip, including all registers and data path. The RESET_L pin has an internal pull-up resistor to DVDD18. The reset timing diagram is shown in Figure 6.

The RESET_L pins must be held low for at least 1 ms after reference clock presence and internal POR release. The management interface requires 10 ms after the application of the reset to be in the ready state.

Figure 6: Reset Timing Diagram



1.7 Microcode Loading

The microcode (or firmware) must be loaded into the microcontroller RAM for PHY operation. The microcode download is possible using one of the following methods:

- Downloading the microcode from the external SPI-ROM.
- Downloading the microcode directly over the management interface (MDIO).

It is also possible to program the external SPI-ROM over the MDIO with updated microcode.

External 24-bit addressing, no less than 256-KB SPI-EEPROM or SPI-Flash, can be used to store the microcode. The microcode is automatically downloaded through the SCK, SS_N, MOSI, and MISO pins into the PHY microcontroller RAM after the PHY comes out of reset.

NOTE: Only a limited number of SPI-EEPROM or SPI-Flash memories are validated for the BCM81356. Consult your Broadcom FAE or AE for details.

Chapter 2: Modes and Rates

The BCM81356 includes two logical groups, Octo A and Octo B.

2.1 Retimer, Gearbox, and Reverse Gearbox Modes

Table 1 describes the Retimer, Gearbox, and Reverse Gearbox modes for Octo A and Octo B, respectively.

Table 1: Retimer (Octo A and B) Non-MUX Mode

Device Mode	Operation Mode	Logical Function	Traffic Type from Host ASIC	Host-Side SerDes Mode Per Port	FEC Inside Device on Host Side Per Port	FEC Inside Device on Line Side Per Port	Line-Side SerDes Mode Per Port	Octo A			Octo B		
								Logical Port Number	Host-Side SerDes Lane Mapping	Line-side SerDes Lane Mapping	Logical Port Number	Host-Side SerDes Lane Mapping	Line-Side SerDes Lane Mapping
1A	2 ports of 400GbE	PAM-4 retimer	CL-119 FEC (RS-544)	8 × 53G PAM-4 400GAUI-8	No	No	8 × 53G PAM-4 400GAUI-8 (optics) 400G-CR8 (copper) with AN/LT	Port 0	H0 to H7	L0 to L7	Port 1	H8 to H15	L8 to L15
1D	1 port of 400GbE	Forward gearbox	CL-119 FEC (RS-544)	16 × 26G NRZ 400GAUI-16	No	No	8x53G PAM-4 400GAUI-8 (optics) 400G-CR8 (copper) with AN/LT	Port 0	H0 to H7	L0 to L3	Port 0	H8 to H15	L8 to L11
2A	2 ports of 200GbE	NRZ retimer	CL-119 FEC (RS-544)	8 × 26G NRZ 200GAUI-8	No	No	8 × 26G NRZ 200GAUI-8 (optics)	Port 0	H0 to H7	L0 to L7	Port 1	H8 to H15	L8 to L15
2B	4 ports of 200GbE	PAM-4 retimer with or without FEC termination and generation	CL-119 FEC (RS-544)	4 × 53G PAM-4 200GAUI-4	No or CL-119 FEC (RS-544)	No or CL-119 FEC (RS-544)	4 × 53G PAM-4 200GAUI-4 (optics) 200G-CR4 (copper) with AN/LT	Port 0	H0 to H3	L0 to L3	Port 2	H8 to H11	L8 to L11
								Port 1	H4 to H7	L4 to L7	Port 3	H12 to H15	L12 to L15

Table 1: Retimer (Octo A and B) Non-MUX Mode (Continued)

Device Mode	Operation Mode	Logical Function	Traffic Type from Host ASIC	Host-Side SerDes Mode Per Port	FEC Inside Device on Host Side Per Port	FEC Inside Device on Line Side Per Port	Line-Side SerDes Mode Per Port	Octo A			Octo B		
								Logical Port Number	Host-Side SerDes Lane Mapping	Line-side SerDes Lane Mapping	Logical Port Number	Host-Side SerDes Lane Mapping	Line-Side SerDes Lane Mapping
2C	2 ports of 200GbE	Forward gearbox	CL-119 FEC (RS-544)	8 × 26G NRZ 200GAUI-8	No	No	4 × 53G PAM-4 200GAUI-4 (optics) 200G-CR4 (copper) with AN/LT	Port 0	H0 to H7	L0 to L3	Port 1	H8 to H15	L8 to L11
3A	4 ports of 100GbE	PAM-4 retimer with or without FEC termination and generation	CL-91 FEC (RS-544)	2 × 53G PAM-4 100GAUI-2	No or CL-91 FEC (RS-544 over 2 lanes)	No or CL-91 FEC (RS-544 over 2 lanes)	2 × 53G PAM-4 100GAUI-2 (optics) 100G-CR2 (copper) with AN/LT	Port 0	H0 to H1	L0 to L1	Port 4	H8 to H9	L8 to L9
								Port 1	H2 to H3	L2 to L3	Port 5	H10 to H11	L10 to L11
								Port 2	H4 to H5	L4 to L5	Port 6	H12 to H13	L12 to L13
								Port 3	H6 to H7	L6 to L7	Port 7	H14 to H15	L14 to L15
3B	4 ports of 100GbE	NRZ retimer	CL-91 FEC (RS-528) CL-82 PCS (no FEC)	4 × 25G NRZ CAUI-4 and 100GAUI-4	No	No	4 × 25G NRZ CAUI-4 and 100GAUI-4 (optics) 100G-CR4 (copper) with AN/LT	Port 0	H0 to H3	L0 to L3	Port 2	H8 to H11	L8 to L11
								Port 1	H4 to H7	L4 to L7	Port 3	H12 to H15	L12 to L15
3C	4 ports of 100GbE	Reverse gearbox (M1)	CL-91 FEC (RS-544)	2 × 53G PAM-4 100G-GAUI-2	CL-91 FEC (RS-544 over 2 lanes)	CL-91 FEC (RS-528 over 4 lanes) or CL-82 PCS (no FEC over 4 lanes)	4 × 25G NRZ CAUI-4 and 100GAUI-4 (optics) 100G-CR4 (copper) with AN/LT	Port 0	H0 to H1	L0 to L3	Port 2	H8 to H9	L8 to L11
								Port 1	H4 to H5	L4 to L7	Port 3	H12 to H13	L12 to L15
		Reverse gearbox (M2)	CL-91 FEC (RS-544)	2 × 53G PAM-4 100G-GAUI-2	CL-91 FEC (RS-544 over 2 lanes)	CL-91 FEC (RS-528 over 4 lanes) or CL-82 PCS (no FEC over 4 lanes)	4 × 25G NRZ CAUI-4 and 100GAUI-4 (optics) 100G-CR4 (copper) with AN/LT	Port 0	H0 to H1	L0 to L3	Port 2	H8 to H9	L8 to L11
								Port 1	H2 to H3	L4 to L7	Port 3	H10 to H11	L12 to L15

Table 1: Retimer (Octo A and B) Non-MUX Mode (Continued)

Device Mode	Operation Mode	Logical Function	Traffic Type from Host ASIC	Host-Side SerDes Mode Per Port	FEC Inside Device on Host Side Per Port	FEC Inside Device on Line Side Per Port	Line-Side SerDes Mode Per Port	Octo A			Octo B		
								Logical Port Number	Host-Side SerDes Lane Mapping	Line-side SerDes Lane Mapping	Logical Port Number	Host-Side SerDes Lane Mapping	Line-Side SerDes Lane Mapping
3C1	4 ports of 100GbE	Bit mux reverse gearbox (M1)	CL-91 FEC (RS-544)	2 × 53G PAM-4 100G-GAUI-2	No	No	4 × 26G NRZ CAUI-4 and 100GAUI-4 (optics) 100G-CR4 (copper) with AN/LT	Port 0	H0 to H1	L0 to L3	Port 2	H8 to H9	L8 to L11
								Port 1	H4 to H5	L4 to L7	Port 3	H12 to H13	L12 to L15
		Bit mux reverse gearbox (M2)	CL-91 FEC (RS-544)	2 × 53G PAM-4 100G-GAUI-2	No	No	4 × 26G NRZ CAUI-4 and 100GAUI-4 (optics) 100G-CR4 (copper) with AN/LT	Port 0	H0 to H1	L0 to L3	Port 2	H8 to H9	L8 to L11
								Port 1	H2 to H3	L4 to L7	Port 3	H10 to H11	L12 to L15
3D	4 ports of 100GbE	Forward gearbox (M2)	CL-91 FEC (RS-528) CL-82 PCS (no FEC)	4 × 25G NRZ CAUI-4 and 100GAUI-4	CL-91 FEC (RS-528 over 4 lanes) or CL-82 PCS (no FEC over 4 lanes)	CL-91 FEC (RS-544 over 2 lanes)	2 × 53G PAM-4 100GAUI-2 (optics) 100G-CR2 (copper) with AN/LT	Port 0	H0 to H3	L0 to L1	Port 2	H8 to H11	L8 to L9
								Port 1	H4 to H7	L2 to L3	Port 3	H12 to H15	L10 to L11
3D1	4 ports of 100GbE	Bit mux forward gearbox (M2)	CL-91 FEC (RS-544)	4 × 26G NRZ CAUI-4 and 100GAUI-4	No	No	2 × 53G PAM-4 100GAUI-2 (optics) 100G-CR2 (copper) with AN/LT	Port 0	H0 to H3	L0 to L1	Port 2	H8 to H11	L8 to L9
								Port 1	H4 to H7	L2 to L3	Port 3	H12 to H15	L10 to L11
4A	16 ports of 50GbE	PAM-4 Retimer with or without FEC termination and generation	CL-134 FEC (RS-544)	1 × 53G PAM-4 50GAUI-1	No or CL-134 FEC (RS-544 over 1 lane)	No or CL-134 FEC (RS-544 over 1 lane)	1 × 53G PAM-4 50GAUI-1 (optics) 50G-CR (copper) with AN/LT	Ports 0 to 7	H0 to H7	L0 to L7	Ports 8 to 15	H8 to H15	L8 to L15

Table 1: Retimer (Octo A and B) Non-MUX Mode (Continued)

Device Mode	Operation Mode	Logical Function	Traffic Type from Host ASIC	Host-Side SerDes Mode Per Port	FEC Inside Device on Host Side Per Port	FEC Inside Device on Line Side Per Port	Line-Side SerDes Mode Per Port	Octo A			Octo B		
								Logical Port Number	Host-Side SerDes Lane Mapping	Line-side SerDes Lane Mapping	Logical Port Number	Host-Side SerDes Lane Mapping	Line-Side SerDes Lane Mapping
4B	8 ports of 50GbE/ Consortium	NRZ Retimer	Cons FEC (RS-528) Cons PCS (no FEC) CL-74 FEC (FC-FEC)	2 × 25G NRZ LAUI-2	No	No	2 × 25G NRZ LAUI-2 (optics) 50G-CR2 (copper) with AN/LT	Port 0	H0 to H1	L0 to L1	Port 4	H8 to H9	L8 to L9
								Port 1	H2 to H3	L2 to L3	Port 5	H10 to H11	L10 to L11
								Port 2	H4 to H5	L4 to L5	Port 6	H12 to H13	L12 to L13
								Port 3	H6 to H7	L6 to L7	Port 7	H14 to H15	L14 to L15
4C	8 ports of 50GbE/ Consortium	Reverse gearbox (M1)	CL-134 FEC (RS-544)	1 × 53G PAM-4 50GAUI-1	CL-134 FEC (RS-544 over 1 lane)	Consortium FEC (RS-528 over 2 lanes) or Consortium PCS (no FEC over 2 lanes) or CL-74 FEC (FC-FEC over 2 lanes)	2 × 25G NRZ LAUI-2 (optics) 50G-CR2 (copper) with AN/LT	Port 0	H0	L0 to L1	Port 4	H8	L8 to L9
								Port 1	H2	L2 to L3	Port 5	H10	L10 to L11
								Port 2	H4	L4 to L5	Port 6	H12	L12 to L13
								Port 3	H6	L6 to L7	Port 7	H14	L14 to L15
		Reverse gearbox (M2)	CL-134 FEC (RS-544)	1 × 53G PAM-4 50GAUI-1	CL-134 FEC (RS-544 over 1 lane)	Consortium FEC (RS-528 over 2 lanes) or Consortium PCS (no FEC over 2 lanes) or CL-74 FEC (FC-FEC over 2 lanes)	2 × 25G NRZ LAUI-2 (optics) 50G-CR2 (copper) with AN/LT	Port 0	H0	L0 to L1	Port 4	H8	L8 to L9
								Port 1	H1	L2 to L3	Port 5	H9	L10 to L11
								Port 2	H2	L4 to L5	Port 6	H10	L12 to L13
								Port 3	H3	L6 to L7	Port 7	H11	L14 to L15

Table 1: Retimer (Octo A and B) Non-MUX Mode (Continued)

Device Mode	Operation Mode	Logical Function	Traffic Type from Host ASIC	Host-Side SerDes Mode Per Port	FEC Inside Device on Host Side Per Port	FEC Inside Device on Line Side Per Port	Line-Side SerDes Mode Per Port	Octo A			Octo B		
								Logical Port Number	Host-Side SerDes Lane Mapping	Line-side SerDes Lane Mapping	Logical Port Number	Host-Side SerDes Lane Mapping	Line-Side SerDes Lane Mapping
4C1	8 ports of 50GbE	Reverse gearbox (M1)	CL-134 FEC (RS-544)	1 × 53G PAM-4 50GAUI-1	No	No	2 × 26G NRZ LAUI-2 (optics) 50G-CR2 (copper) with AN/LT	Port 0	H0	L0 to L1	Port 4	H8	L8 to L9
								Port 1	H2	L2 to L3	Port 5	H10	L10 to L11
								Port 2	H4	L4 to L5	Port 6	H12	L12 to L13
								Port 3	H6	L6 to L7	Port 7	H14	L14 to L15
		Reverse gearbox (M2)	CL-134 FEC (RS-544)	1 × 53G PAM-4 50GAUI-1	No	No	2 × 26G NRZ LAUI-2 (optics) 50G-CR2 (copper) with AN/LT	Port 0	H0	L0 to L1	Port 4	H8	L8 to L9
								Port 1	H1	L2 to L3	Port 5	H9	L10 to L11
								Port 2	H2	L4 to L5	Port 6	H10	L12 to L13
								Port 3	H3	L6 to L7	Port 7	H11	L14 to L15
4D	8 ports of 50GbE/ Consortium	Forward gearbox (M2)	Consortium FEC (RS-528) or Consortium PCS (no FEC) or CL-74 FEC (FC-FEC)	2 × 25G NRZ LAUI-2	Consortium FEC (RS-528 over 2 lanes) or Consortium PCS (no FEC over 2 lanes) or CL-74 FEC (FC-FEC over 2 lanes)	CL-134 FEC (RS-544 over 1 lane)	1 × 53G PAM-4 50GAUI-1 (optics) 50G-CR (copper) with AN/LT	Port 0	H0 to H1	L0	Port 4	H8 to H9	L8
								Port 1	H2 to H3	L1	Port 5	H10 to H11	L9
								Port 2	H4 to H5	L2	Port 6	H12 to H13	L10
								Port 3	H6 to H7	L3	Port 7	H14 to H15	L11
4D1	8 ports of 50GbE/ Consortium	Bit mux forward gearbox (M2)	—	2 × 26G NRZ LAUI-2	No	No	1 × 53G PAM-4 50GAUI-1 (optics) 50G-CR (copper) with AN/LT	Port 0	H0 to H1	L0	Port 4	H8 to H9	L8
								Port 1	H2 to H3	L1	Port 5	H10 to H11	L9
								Port 2	H4 to H5	L2	Port 6	H12 to H13	L10
								Port 3	H6 to H7	L3	Port 7	H14 to H15	L11
5A	4 ports of 40GbE	NRZ retimer	CL-82 PCS (no FEC)	4 × 10G NRZ XLPPI-4	No	No	4 × 10G NRZ XLPPI-4 (optics) 40G-CR4 (copper) with AN/LT	Port 1	H0 to H3	L0 to L3	Port 2	H8 to H11	L8 to L11
								Port 2	H4 to H7	L4 to L7	Port 3	H12 to H15	L12 to L15

Table 1: Retimer (Octo A and B) Non-MUX Mode (Continued)

Device Mode	Operation Mode	Logical Function	Traffic Type from Host ASIC	Host-Side SerDes Mode Per Port	FEC Inside Device on Host Side Per Port	FEC Inside Device on Line Side Per Port	Line-Side SerDes Mode Per Port	Octo A			Octo B		
								Logical Port Number	Host-Side SerDes Lane Mapping	Line-side SerDes Lane Mapping	Logical Port Number	Host-Side SerDes Lane Mapping	Line-Side SerDes Lane Mapping
5B	4 ports of 40GbE	Reverse gearbox (M1)	CL-82 PCS (no FEC)	2 × 20G NRZ XLPPI-2	No	No	4 × 10G NRZ XLPPI-4 (optics) 40G-CR4 (copper) with AN/LT	Port 3	H0 to H1	L0 to L3	Port 2	H8 to H9	L8 to L11
								Port 1	H4 to H5	L4 to L7	Port 3	H12 to H13	L12 to L15
		Reverse gearbox (M2)	CL-82 PCS (no FEC)	2 × 20G NRZ XLPPI-2	No	No	4 × 10G NRZ XLPPI-4 (optics) 40G-CR4 (copper) with AN/LT	Port 0	H0 to H1	L0 to L3	Port 2	H8 to H9	L8 to L11
								Port 1	H2 to H3	L4 to L7	Port 3	H10 to H11	L12 to L15
6	16 ports of 25GbE	NRZ retimer	CL-49 PCS (no FEC) CL-74 FEC (FC-FEC) CL-108 FEC (RS-528)	1 × 25G NRZ 25GAUI	No	No	1 × 25G NRZ 25GAUI (optics) 25G-CR (copper) with AN/LT	Port 0 to 7	H0 to H7	L0 to L7	Port 8 to 15	H8 to H15	L8 to L15
7	16 ports of 10GbE	NRZ retimer	CL-49 PCS (no FEC)	1 × 10G NRZ SFI	No	No	1 × 10G NRZ SFI (optics) SFI (copper)	Port 0 to 7	H0 to H7	L0 to L7	Port 8 to 15	H8 to H15	L8 to L15
8	16 ports of 1GbE	NRZ retimer	CL-36 PCS (no FEC)	1 × 1G NRZ	No	No	1 × 1G NRZ	Port 0 to 7	H0 to H7	L0 to L7	Port 8 to 15	H8 to H15	L8 to L15

2.2 Hitless Mux/Broadcasting Modes

Table 2 shows the Hitless Mux/Broadcasting operating modes for Octo A and Octo B, respectively.

Table 2: Retimer (Octo A and B) Mux Modes

Device Mode	Operation Mode	Logical Function	Traffic Type Per Port	Host-Side SerDes Mode Per Port	FEC on Host Side Per Port	FEC on Line Side Per Port	Line-Side SerDes Mode Per Port	Octo A			Octo B			Notes
								Logical Port Number	Host-Side SerDes Lane Mapping	Line-Side SerDes Lane Mapping	Logical Port Number	Host-Side SerDes Lane Mapping	Line-Side SerDes Lane Mapping	
2	2 port of 200GbE	Mux (egress)/ broadcast (ingress)	CL-119 FEC (RS-544 over 4 lanes)	4 × 53G + 4 × 53G PAM-4	CL-119 FEC (RS-544 over 4 lanes) Decode only	CL-119 FEC (RS-544 over 4 lanes) Encode only	4 × 53G PAM-4 200GAUI-4 (optics) 200G-CR4 (copper) with AN/LT	Port 0	H0 to H3 + H4 to H7	L0 to L3	Port 1	H8 to H11 + H12 to H15	L8 to L11	FEC termination and reduced PCS for auto-switching logic. AN/LT is supported on the line side. Host side and line side support same traffic type per port. Ingress is repeater and broadcasting. Egress has FEC termination and regeneration.
3A	4 ports of 100GbE	Mux (egress)/ broadcast (ingress)	CL-91 FEC (RS-544 over 2 lanes)	2 × 53G + 2 × 53G PAM-4	CL-91 FEC (RS-544 over 2 lanes) Decode only	CL-91 FEC (RS-544 over 2 lanes) Encode only	2 × 53G PAM-4 100GAUI-2 (optics) 100G-CR2 (copper) with AN/LT	Port 0	H0 to H1 + H4 to H5	L0 to L1	Port 2	H8 to H9 + H12 to H13	L8 to L9	FEC termination and reduced PCS for auto-switching logic. AN/LT is supported on the line side. Host side and line side support same traffic type per port. Ingress is repeater and broadcasting Egress has FEC termination and regeneration.
								Port 1	H2 to H3 + H6 to H7	L2 to L3	Port 3	H10 to H11 + H14 to H15	L10 to L11	
3B	2 ports of 100GbE	Mux (egress)/ broadcast (ingress)	CL-91 FEC (RS-528 over 4 lanes) or no FEC (PCS over 4 × PHY lanes)	4 × 25G + 4 × 25G NRZ	CL-91 FEC (RS-528 over 4 lanes) or no FEC (PCS over 4 × PHY lanes) or PCS/FEC Decoder only	CL-91 FEC (RS-528 over 4 lanes) or no FEC (PCS over 4 × PHY lanes) or PCS/FEC Encoder only	4 × 25G NRZ CAUI-4 and 100GAUI-4 (optics) 100G-CR4 (copper) with AN/LT	Port 0	H0 to H3 + H4 to H7	L0 to L3	Port 1	H8 to H11 + H12 to H15	L8 to L11	FEC termination and reduced PCS for auto-switching logic. AN/LT is supported on the line side. Host side and line side support same traffic type per port. Egress can support PCS traffic pass-through or FEC termination and regeneration. Ingress is repeater and broadcasting.
3C	4 ports of 100GbE	Reverse gearbox + mux (egress)/ broadcast (ingress)	CL-91 FEC (RS-544 over 2 lanes)	2 × 53G + 2 × 53G PAM-4	CL-91 FEC (RS-544 over 2 lanes) Both encoder and decoder	No FEC (PCS over 4 × PHY lanes) or CL-91 FEC (RS-528 over 4 lanes) or both encoder and decoder	4 × 25G NRZ CAUI-4 and 100GAUI-4 (optics) 100G-CR4 (copper) with AN/LT	Port 0	H0 to H1 + H4 to H5	L0 to L3	Port 2	H8 to H9 + H12 to H13	L8 to L11	Termination of FEC on the host side and PCS/PMA/ FEC encoding on the line side. Auto-switching before PCS/PMA or FEC encoding on the line side. AN/LT is supported on the line side.
								Port 1	H2 to H3 + H6 to H7	L4 to L7	Port 3	H10 to H11 + H14 to H15	L12 to L15	
4A	8 ports of 50GbE	Mux (egress)/ broadcast (ingress)	CL-134 FEC (RS-544 over 1 lane)	1 × 53G + 1 × 53G PAM-4	CL-134 FEC (RS-544 over 1 lane) Decoder only	CL-134 FEC (RS-544 over 1 lane) Encoder only	1 × 53G PAM-4 50GAUI-1 (optics) 50G-CR (copper) with AN/LT	Port 0	H0 + H4	L0	Port 4	H8 + H12	L8	FEC termination and reduced PCS for auto-switching logic. AN/LT is supported on the line side. Host side and line side support same traffic type per port. Ingress is repeater and broadcasting. Egress has FEC termination and regeneration.
								Port 1	H1 + H5	L1	Port 5	H9 + H13	L9	
								Port 2	H2 + H6	L2	Port 6	H10 + H14	L10	
								Port 3	H3 + H7	L3	Port 7	H11 + H15	L11	

Table 2: Retimer (Octo A and B) Mux Modes (Continued)

Device Mode	Operation Mode	Logical Function	Traffic Type Per Port	Host-Side SerDes Mode Per Port	FEC on Host Side Per Port	FEC on Line Side Per Port	Line-Side SerDes Mode Per Port	Octo A			Octo B			Notes
								Logical Port Number	Host-Side SerDes Lane Mapping	Line-Side SerDes Lane Mapping	Logical Port Number	Host-Side SerDes Lane Mapping	Line-Side SerDes Lane Mapping	
4B	4 ports of 50GbE/ Consortium	Mux (egress)/ broadcast (ingress) Consortium mode	No FEC (PCS over 2 × PHY lanes) or FC-FEC (FC-FEC over 2 × PHY lanes) or CL-91 FEC (RS-528 over 2 lanes)	2 × 25G + 2 × 25G NRZ	No FEC (PCS over 2 × PHY lanes) or FC-FEC (FC-FEC over 2 × PHY lanes) or CL-91 FEC (RS-528 over 2 lanes) Decoder only	No FEC (PCS over 2 × PHY lanes) or FC-FEC (FC-FEC over 2 × PHY lanes) or CL-91 FEC (RS-528 over 2 lanes) or encoder only	2 × 25G NRZ LAUI-2 (optics) 50G-CR2 (copper) with AN/LT	Port 0	H0 to H1 + H4 to H5	L0 to L1	Port 2	H8 to H9 + H12 to H14	L8 to L9	FEC termination and (or only) reduced PCS for auto-switching logic. Same traffic protocol both sides. AN/LT required on the line side. Host side and line side support same traffic type per port. Ingress is repeater and broadcasting. Egress has FEC/PCS termination and regeneration.
								Port 1	H2 to H3 + H6 to H7	L2 to L3	Port 3	H10 to H11 + H14 to H15	L10 to L11	
4C	8 ports of 50GbE/ Consortium	Reverse gearbox + mux (egress)/ broadcast (ingress) Consortium mode	CL-134 FEC (RS-544 over 1 lane)	1 × 53G + 1 × 53G PAM-4	CL-134 FEC (RS-544 over 1 lane) Decoder and encoder	No FEC (PCS over 2 × PHY lanes) or FC-FEC (PCS over FC-FEC over 2 × PHY lanes) or CL-91 FEC (RS-528 over 2 lanes) or decoder and encoder	2 × 25G NRZ LAUI-2 (optics) 50G-CR2 (copper) with AN/LT	Port 0	H0 + H4	L0 to L1	Port 4	H8 + H12	L8 to L9	Termination of FEC on the host side and PCS/PMA/ FEC encoding on the line side. Auto-switching before PCS/PMA or FEC encoding on the line side. AN/LT required on the line side.
								Port 1	H1 + H5	L2 to L3	Port 5	H9 + H13	L10 to L11	
								Port 2	H2 + H6	L4 to L5	Port 6	H10 + H14	L12 to L13	
								Port 3	H3 + H7	L6 to L7	Port 7	H11 + H15	L14 to L15	
5A	2 port of 40GbE	Mux (egress)/ broadcast (ingress)	CL-82 PCS over 4 lanes	4 × 10G + 4 × 10G NRZ	CL-82 PCS over 4 lanes Decoder only	CL-82 PCS over 4 lanes Encoder only	4 × 10G NRZ XLPPI-4 (optics) 40G-CR4 (copper) with AN/LT	Port 0	H0 to H3 + H4 to H7	L0 to L3	Port 1	H8 to H11 + H12 to H15	L8 to L11	Only reduced PCS (no decoding) for auto-switching logic. AN/LT is supported on the line side. Host side and line side would support same traffic type per port. Ingress is repeater and broadcasting. Egress has FEC/PCS termination and regeneration.
5B	4 ports of 40GbE	Reverse gearbox + mux (egress)/ broadcast (ingress)	CL-82 PCS over 2 lanes	2 × 20G + 2 × 20G NRZ	CL-82 PCS over 2 lanes Decoder only	CL-82 PCS over 2 lanes Encoder only	4 × 10G NRZ XLPPI-4 (optics) 40G-CR4 (copper) with AN/LT	Port 0	H0 to H1 + H4 to H5	L0 to L3	Port 2	H8 to H9 + H12 to H13	L8 to L11	Only reduced PCS (no decoding) for auto-switching logic. Bit muxing for reverse gearbox. AN/LT is supported on the line side. Host side and line side would support same traffic type per port. Ingress is repeater and broadcasting. Egress has FEC/PCS termination and regeneration.
								Port 1	H2 to H3 + H6 to H7	L4 to L7	Port 3	H10 to H11 + H14 to H15	L12 to L15	

Table 2: Retimer (Octo A and B) Mux Modes (Continued)

Device Mode	Operation Mode	Logical Function	Traffic Type Per Port	Host-Side SerDes Mode Per Port	FEC on Host Side Per Port	FEC on Line Side Per Port	Line-Side SerDes Mode Per Port	Octo A			Octo B			Notes
								Logical Port Number	Host-Side SerDes Lane Mapping	Line-Side SerDes Lane Mapping	Logical Port Number	Host-Side SerDes Lane Mapping	Line-Side SerDes Lane Mapping	
6	8 ports of 25GbE	Mux (egress)/ broadcast (ingress) IEEE And Consortium	CL-49 PCS (no FEC over 1 lane) or CL-74 FEC (FC-FEC over 1 lane) or CL-108 FEC (RS-528 over 1 lane)	1 × 25G + 1 × 25G NRZ	CL-49 PCS (no FEC over 1 lane) or CL-74 FEC (FC-FEC over 1 lane) or CL-108 FEC (RS-528 over 1 lane) or decoder only	CL-49 PCS (no FEC over 1 lane) or CL-74 FEC (FC-FEC over 1 lane) or CL-108 FEC (RS-528 over 1 lane) or encoder only	1 × 25G NRZ 25GAUI (optics) 25G-CR (copper) with AN/LT	Port 0	H0 + H4	L0	Port 4	H8 + H12	L8	FEC termination and (or only) reduced PCS for auto-switching logic. AN/LT is supported on the line side. Host side and line side support same traffic type per port. Ingress is repeater and broadcasting. Egress has FEC/PCS termination and regeneration.
								Port 1	H1 + H5	L1	Port 5	H9 + H13	L9	AN/LT required on the line side.
								Port 2	H2 + H6	L2	Port 6	H10 + H14	L10	AN/LT required on the line side.
								Port 3	H3 + H7	L3	Port 7	H11 + H15	L11	AN/LT required on the line side.
7	8 ports of 10GbE	Mux (egress)/ broadcast (ingress)	CL-49 PCS over 1 lane	1 × 10G + 1 × 10G NRZ	CL-49 PCS over 1 lane	CL-49 PCS over 1-lane	1 × 10G NRZ SFI (optics) SFI (copper)	Port 0	H0 + H4	L0	Port 4	H8 + H12	L8	Only reduced PCS (no decoding) for auto-switching logic. Host side and line side support same traffic type per port. Ingress is repeater and broadcasting. Egress has FEC/PCS termination and regeneration.
								Port 1	H1 + H5	L1	Port 5	H9 + H13	L9	
								Port 2	H2 + H6	L2	Port 6	H10 + H14	L10	
								Port 3	H3 + H7	L3	Port 7	H11 + H15	L11	

2.3 Mixed Mode

For the BCM81356, lane 0 and lane 1 as a pair share the same PLL. Lane 0 and lane 1 can have different OSR settings (1, 2, or 4). That is, when lane 0 is working to 25G, lane 1 can be working to 25G, 12.5G, or 6.25G with an OSR setting of 1, 2, or 4, respectively. Lane 0 egress and ingress data paths share the same OSR setting, so lane 0 egress and ingress should be running at the same data rate, the same as lane 1.

This also applies to other pairs: lane 2/lane 3, lane 4/lane 5, lane 6/lane 7, lane 8/lane 9, lane 10/ lane 11, lane 12/lane 13, and lane 14/lane 15.

The user can set the BCM81356 to mixed modes as described in Table 1 and Table 2 with attention to the following:

- No lane mapping conflict on both the line side and system side.
- No violation on the PLL sharing between the lane pair. For example, the user cannot set lane 0/lane 1 and lane 2 to mode 6 (25.78125G NRZ) in Table 1 while lane 3, lane 4/lane 5, and lane 6/lane 7 is set to mode 7 (10.3125G NRZ) because lane 2 and lane 3 share the same PLL.

2.4 Supported Bit Rates

Table 3 shows the bit rates supported by the BCM81356 SerDes lane as well as the corresponding supported standard.

Table 3: Supported Bit Rates

Bit Rate (Gb/s)	Reference
1.25	IEEE 802.3ab
4.25	FC-PI-6 4FC
8.5	FC-PI-6 16FC
9.95328	10G Base-W (IEEE 802.3ba)
10.3125	IEEE 802.3ba
10.52581	ITU-T G.709 OTUCn (no FEC)
10.709	ITU-T OTU2
10.755	ITU-T OTL3.4
11.049	ITU-T OTU1e
11.0957	ITU-T OTU-2e
11.181	ITU-T OTU4
14.025	FC-PI-6 16FC
20.625	Custom
25.78125	IEEE 802.3bm
27.95	ITU-T OTL4.4
28.05	FC-PI-6 32FC
53.125 PAM-4	IEEE 802.3bs, IEEE 802.3cd
56.1 PAM-4	FC-PI-7 64FC

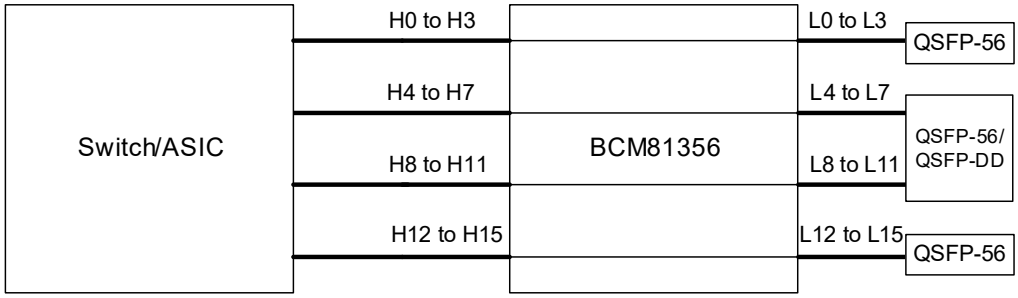
2.5 Lane Swap

The BCM81356 supports flexible lane swap, which enables reconfigurable system schemes. Auto-negotiation and link training are supported across Octo for standard Ethernet traffic.

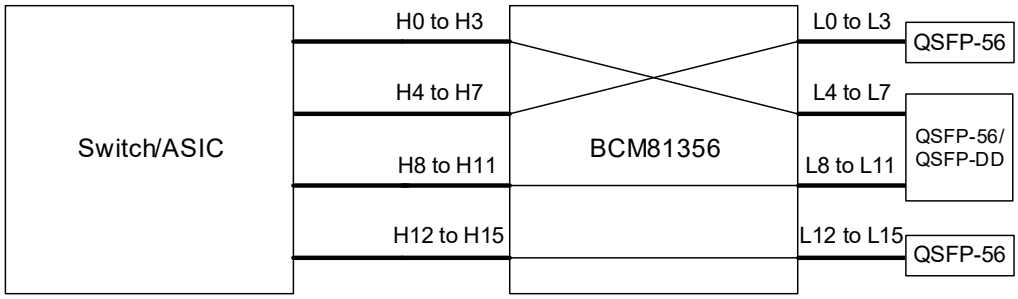
2.5.1 800G Applications

Figure 7 shows lane swap for 800G applications.

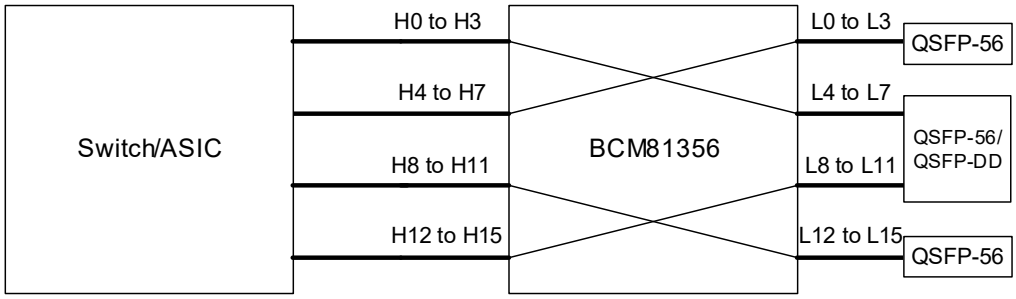
Figure 7: Lane Swap for 800G Applications



Straight pass-through: QSFP-DD + 2 QSFP-56 or 3 QSFP-56



Half cross-connection: QSFP-DD + 2 QSFP-56 or 3 QSFP-56

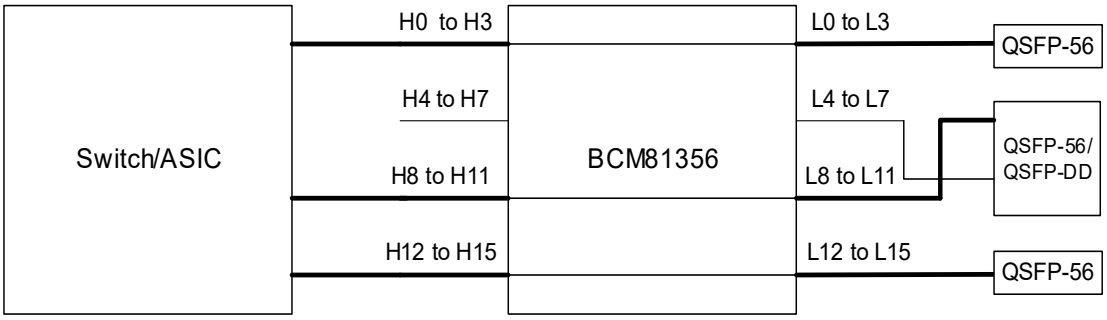


Full cross-connection: QSFP-DD + 2 QSFP-56 or 3 QSFP-56

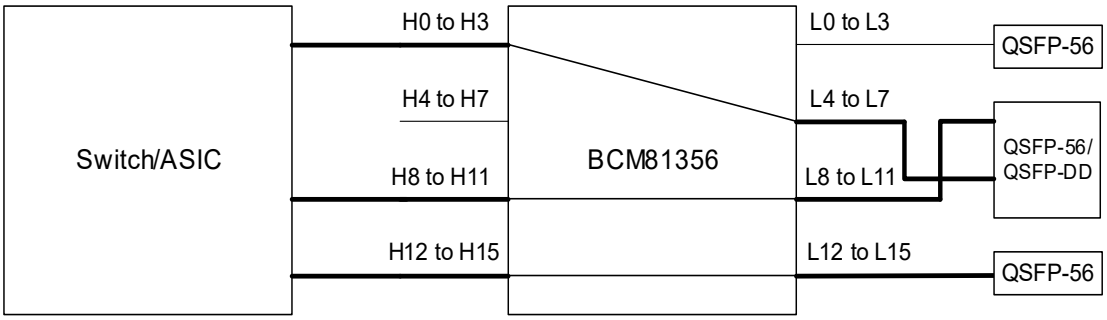
2.5.2 600G Applications

Figure 8 shows lane swap for 600G applications.

Figure 8: Lane Swap for 600G Applications



Straight pass-through: 3 QSFP-56

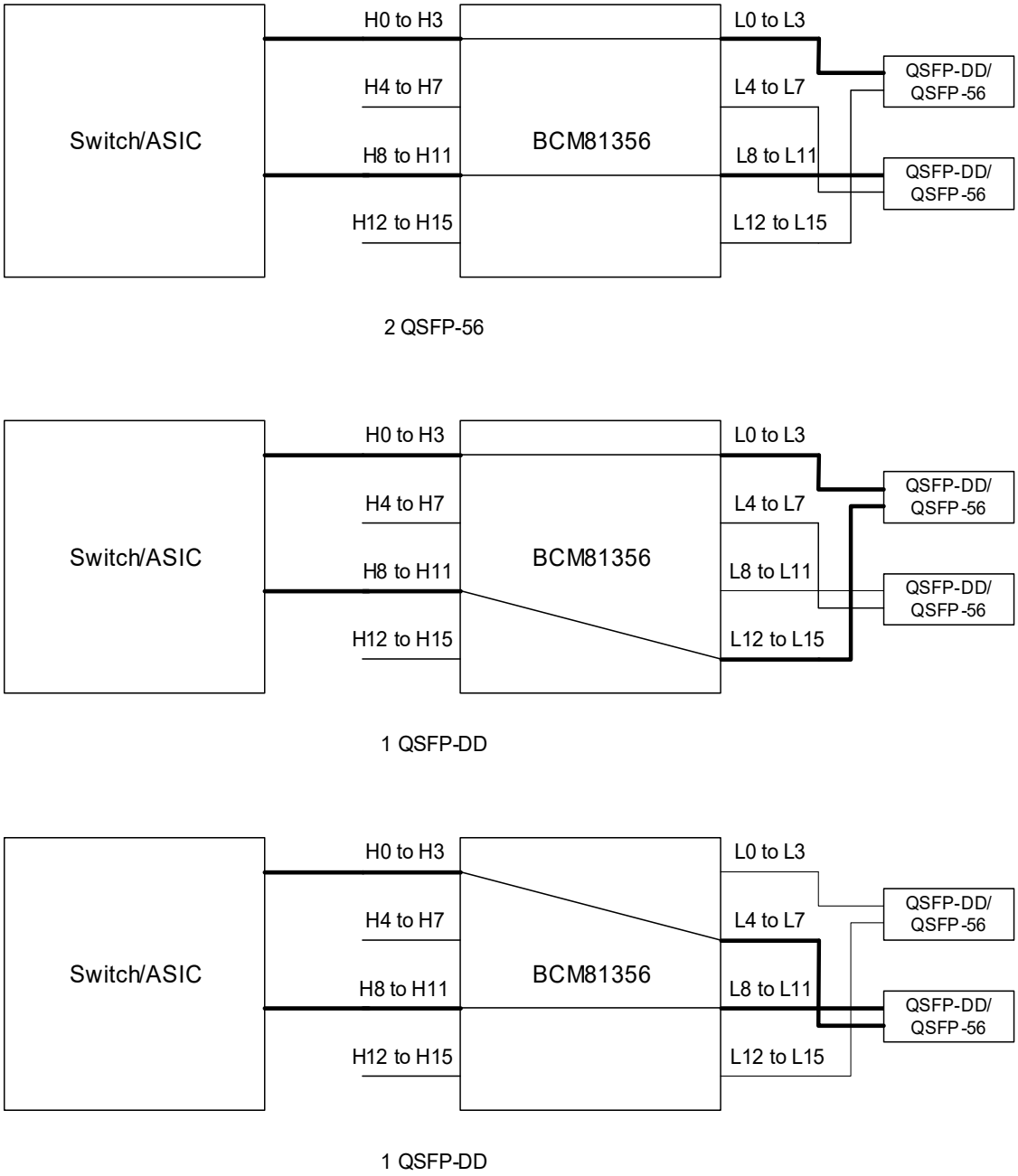


Cross-connection : QSFP-DD + QSFP-56

2.5.3 400G Applications

Figure 9 shows lane swap for 400G applications.

Figure 9: Lane Swap for 400G Applications



Chapter 3: Ball Assignments and Descriptions

The following sections provide the BCM81356 ball functional descriptions and ballout locations.

3.1 Functional Ball Descriptions

Table 4: Line-Side High-Speed Receiver Serial Electrical Interface

Ball No.	Ball Name	Ball Type	Level	Description
V2	LN0_RXP	I	Internally biased and terminated with 100Ω Internally AC-coupled	Line port 0 ingress serial data input.
V1	LN0_RXN			
Y2	LN1_RXP	I	Internally biased and terminated with 100Ω Internally AC-coupled	Line port 1 ingress serial data input.
Y1	LN1_RXN			
AC4	LN2_RXP	I	Internally biased and terminated with 100Ω Internally AC-coupled	Line port 2 ingress serial data input.
AD4	LN2_RXN			
AC6	LN3_RXP	I	Internally biased and terminated with 100Ω Internally AC-coupled	Line port 3 ingress serial data input.
AD6	LN3_RXN			
AC8	LN4_RXP	I	Internally biased and terminated with 100Ω Internally AC-coupled	Line port 4 ingress serial data input.
AD8	LN4_RXN			
AC10	LN5_RXP	I	Internally biased and terminated with 100Ω Internally AC-coupled	Line port 5 ingress serial data input.
AD10	LN5_RXN			
AC12	LN6_RXP	I	Internally biased and terminated with 100Ω Internally AC-coupled	Line port 6 ingress serial data input.
AD12	LN6_RXN			
AC14	LN7_RXP	I	Internally biased and terminated with 100Ω Internally AC-coupled	Line port 7 ingress serial data input.
AD14	LN7_RXN			
AC16	LN8_RXP	I	Internally biased and terminated with 100Ω Internally AC-coupled	Line port 8 ingress serial data input.
AD16	LN8_RXN			
AC18	LN9_RXP	I	Internally biased and terminated with 100Ω Internally AC-coupled	Line port 9 ingress serial data input.
AD18	LN9_RXN			
AC20	LN10_RXP	I	Internally biased and terminated with 100Ω Internally AC-coupled	Line port 10 ingress serial data input.
AD20	LN10_RXN			
AC22	LN11_RXP	I	Internally biased and terminated with 100Ω Internally AC-coupled	Line port 11 ingress serial data input.
AD22	LN11_RXN			
AC24	LN12_RXP	I	Internally biased and terminated with 100Ω Internally AC-coupled	Line port 12 ingress serial data input.
AD24	LN12_RXN			

Table 4: Line-Side High-Speed Receiver Serial Electrical Interface (Continued)

Ball No.	Ball Name	Ball Type	Level	Description
AB26	LN13_RXP	I	Internally biased and terminated with 100Ω Internally AC-coupled	Line port 13 ingress serial data input.
AB27	LN13_RXN			
Y26	LN14_RXP	I	Internally biased and terminated with 100Ω Internally AC-coupled	Line port 14 ingress serial data input.
Y27	LN14_RXN			
V26	LN15_RXP	I	Internally biased and terminated with 100Ω Internally AC-coupled	Line port 15 ingress serial data input.
V27	LN15_RXN			

Table 5: System-Side High-Speed Receiver Serial Electrical Interface

Ball No.	Ball Name	Ball Type	Level	Description
AB2	LN0_TXP	O	Internally biased and terminated with 95Ω External AC-coupling required.	Line port 0 egress serial data output.
AB1	LN0_TXN			
AD2	LN1_TXP	O	Internally biased and terminated with 95Ω External AC-coupling required.	Line port 1 egress serial data output.
AD1	LN1_TXN			
AF2	LN2_TXP	O	Internally biased and terminated with 95Ω External AC-coupling required.	Line port 2 egress serial data output.
AG2	LN2_TXN			
AF4	LN3_TXP	O	Internally biased and terminated with 95Ω External AC-coupling required	Line port 3 egress serial data output.
AG4	LN3_TXN			
AF6	LN4_TXP	O	Internally biased and terminated with 95Ω External AC-coupling required	Line port 4 egress serial data output.
AG6	LN4_TXN			
AF8	LN5_TXP	O	Internally biased and terminated with 95Ω External AC-coupling required	Line port 5 egress serial data output.
AG8	LN5_TXN			
AF10	LN6_TXP	O	Internally biased and terminated with 95Ω External AC-coupling required	Line port 6 egress serial data output.
AG10	LN6_TXN			
AF12	LN7_TXP	O	Internally biased and terminated with 95Ω External AC-coupling required	Line port 7 egress serial data output.
AG12	LN7_TXN			
AF14	LN8_TXP	O	Internally biased and terminated with 95Ω External AC-coupling required	Line port 8 egress serial data output.
AG14	LN8_TXN			
AF16	LN9_TXP	O	Internally biased and terminated with 95Ω External AC-coupling required	Line port 9 egress serial data output.
AG16	LN9_TXN			
AF18	LN10_TXP	O	Internally biased and terminated with 95Ω External AC-coupling required	Line port 10 egress serial data output.
AG18	LN10_TXN			

Table 5: System-Side High-Speed Receiver Serial Electrical Interface (Continued)

Ball No.	Ball Name	Ball Type	Level	Description
AF20	LN11_TXP	O	Internally biased and terminated with 95Ω External AC-coupling required	Line port 11 egress serial data output.
AG20	LN11_TXN			
AF22	LN12_TXP	O	Internally biased and terminated with 95Ω External AC-coupling required	Line port 12 egress serial data output.
AG22	LN12_TXN			
AF24	LN13_TXP	O	Internally biased and terminated with 95Ω External AC-coupling required	Line port 13 egress serial data output.
AG24	LN13_TXN			
AF26	LN14_TXP	O	Internally biased and terminated with 95Ω External AC-coupling required	Line port 14 egress serial data output.
AG26	LN14_TXN			
AD26	LN15_TXP	O	Internally biased and terminated with 95Ω External AC-coupling required	Line port 15 egress serial data output.
AD27	LN15_TXN			

Table 6: System-Side High-Speed Receiver Serial Electrical Interface

Ball	Ball Name	Ball Type	Level	Description
K2	SYS0_RXP	I	Internally biased and terminated with 90Ω. Internally AC-coupled	Host-side port 0 egress serial data input.
K1	SYS0_RXN			
H2	SYS1_RXP	I	Internally biased and terminated with 90Ω. Internally AC-coupled	Host-side port 1 egress serial data input.
H1	SYS1_RXN			
E4	SYS2_RXP	I	Internally biased and terminated with 90Ω. Internally AC-coupled	Host-side port 2 egress serial data input.
D4	SYS2_RXN			
E6	SYS3_RXP	I	Internally biased and terminated with 90Ω. Internally AC-coupled	Host-side port 3 egress serial data input.
D6	SYS3_RXN			
E8	SYS4_RXP	I	Internally biased and terminated with 90Ω Internally AC-coupled	Host-side port 4 egress serial data input.
D8	SYS4_RXN			
E10	SYS5_RXP	I	Internally biased and terminated with 90Ω Internally AC-coupled	Host-side port 5 egress serial data input.
D10	SYS5_RXN			
E12	SYS6_RXP	I	Internally biased and terminated with 90Ω Internally AC-coupled	Host-side port 6 egress serial data input.
D12	SYS6_RXN			
E14	SYS7_RXP	I	Internally biased and terminated with 90Ω Internally AC-coupled	Host-side port 7 egress serial data input.
D14	SYS7_RXN			
E16	SYS8_RXP	I	Internally biased and terminated with 90Ω Internally AC-coupled	Host-side port 8 egress serial data output.
D16	SYS8_RXN			
E18	SYS9_RXP	I	Internally biased and terminated with 90Ω Internally AC-coupled	Host-side port 9 egress serial data input.
D18	SYS9_RXN			

Table 6: System-Side High-Speed Receiver Serial Electrical Interface (Continued)

Ball	Ball Name	Ball Type	Level	Description
E20	SYS10_RXP	I	Internally biased and terminated with 90Ω Internally AC-coupled	Host-side port 10 egress serial data input.
D20	SYS10_RXN			
E22	SYS11_RXP	I	Internally biased and terminated with 90Ω Internally AC-coupled	Host-side port 11 egress serial data input.
D22	SYS11_RXN			
E24	SYS12_RXP	I	Internally biased and terminated with 90Ω Internally AC-coupled	Host-side port 12 egress serial data input.
D24	SYS12_RXN			
F26	SYS13_RXP	I	Internally biased and terminated with 90Ω Internally AC-coupled	Host-side port 13 egress serial data input.
F27	SYS13_RXN			
H26	SYS14_RXP	I	Internally biased and terminated with 90Ω Internally AC-coupled	Host-side port 14 egress serial data input.
H27	SYS14_RXN			
K26	SYS15_RXP	I	Internally biased and terminated with 90Ω Internally AC-coupled	Host-side port 15 egress serial data input.
K27	SYS15_RXN			
NOTE: The V_{IH} of the incoming signal to SYSxx_RXP/N should be no greater than SYS_AVDDRX.				

Table 7: System-Side High-Speed Transmitter Serial Electrical Interface

Ball No.	Ball Name	Ball Type	Level	Description
F2	SYS0_TXP	O	Internally biased and terminated with 90Ω External AC-coupling required	Host-side port 0 ingress serial data output.
F1	SYS0_TXN			
D2	SYS1_TXP	O	Internally biased and terminated with 90Ω External AC-coupling required	Host-side port 1 ingress serial data output.
D1	SYS1_TXN			
B2	SYS2_TXP	O	Internally biased and terminated with 90Ω External AC-coupling required	Host-side port 2 ingress serial data output.
A2	SYS2_TXN			
B4	SYS3_TXP	O	Internally biased and terminated with 90Ω External AC-coupling required	Host-side port 3 ingress serial data output.
A4	SYS3_TXN			
B6	SYS4_TXP	O	Internally biased and terminated with 90Ω External AC-coupling required	Host-side port 4 ingress serial data output.
A6	SYS4_TXN			
B8	SYS5_TXP	O	Internally biased and terminated with 90Ω. External AC-coupling required	Host-side port 5 ingress serial data output.
A8	SYS5_TXN			
B10	SYS6_TXP	O	Internally biased and terminated with 90Ω External AC-coupling required	Host-side port 6 ingress serial data output.
A10	SYS6_TXN			
B12	SYS7_TXP	O	Internally biased and terminated with 90Ω. External AC-coupling required	Host-side port 7 ingress serial data output.
A12	SYS7_TXN			

Table 7: System-Side High-Speed Transmitter Serial Electrical Interface (Continued)

Ball No.	Ball Name	Ball Type	Level	Description
B14	SYS8_TXP	O	Internally biased and terminated with 90Ω External AC-coupling required	Host-side port 8 ingress serial data output.
A14	SYS8_TXN			
B16	SYS9_TXP	O	Internally biased and terminated with 90Ω External AC-coupling required	Host-side port 9 ingress serial data output.
A16	SYS9_TXN			
B18	SYS10_TXP	O	Internally biased and terminated with 90Ω External AC-coupling required	Host-side port 10 ingress serial data output.
A18	SYS10_TXN			
B20	SYS11_TXP	O	Internally biased and terminated with 90Ω External AC-coupling required	Host-side port 11 ingress serial data output.
A20	SYS11_TXN			
B22	SYS12_TXP	O	Internally biased and terminated with 90Ω External AC-coupling required	Host-side port 12 ingress serial data output.
A22	SYS12_TXN			
B24	SYS13_TXP	O	Internally biased and terminated with 90Ω External AC-coupling required	Host-side port 13 ingress serial data output.
A24	SYS13_TXN			
B26	SYS14_TXP	O	Internally biased and terminated with 90Ω External AC-coupling required	Host-side port 14 ingress serial data output.
A26	SYS14_TXN			
D26	SYS15_TXP	O	Internally biased and terminated with 90Ω External AC-coupling required	Host-side port 15 ingress serial data output.
D27	SYS15_TXN			

Table 8: Reference Clock

Ball No.	Ball Name	Ball Type	Level	Description
T2	REFCLK_0P	I	Internally biased and differentially terminated with 100Ω External AC-coupling required	Reference clock input for channels 0 to 7. Frequency is 156.25 MHz for Ethernet applications.
T1	REFCLK_0N			
T27	REFCLK_1P	I	Internally biased and differentially terminated with 100Ω External AC-coupling required	Reference clock input for channels 8 to 15. Frequency is 156.25 MHz for Ethernet applications.
T26	REFCLK_1N			
G15	REFDIV_SEL1	I	DVDDIO internal pull-down	Reference clock divider select. If REF_SEL1 = 0 and REF_SEL0 = 0, reference clock frequency range = 100 to 174.7 MHz. Other settings are invalid.
G13	REFDIV_SEL0			

Table 9: Recovered Clock

Ball No.	Ball Name	Ball Type	Level	Description
P2	RCLK_DIFF_P	O	Internally biased and differentially terminated with 100Ω. External AC-coupling required	Differential recovered clock output. Clock can be used for Synchronous Ethernet.
P1	RCLK_DIFF_N			
M25	RCLK0	O	DVDDIO CMOS output	Single-ended recovered clock output. Clock can be used for Synchronous Ethernet.
M27	RCLK1	O	DVDDIO CMOS output	Single-ended recovered clock output. Clock can be used for Synchronous Ethernet.

Table 10: Reset

Ball No.	Ball Name	Ball Type	Level	Description
M3	RESET_L	I	DVDDIO Schmitt trigger Internal pull-up	PHY reset input. Active-low. A minimum low period of 1 ms is required.

Table 11: MDIO Secondary

Ball No.	Ball Name	Ball Type	Level	Description
P4	MDC	I	DVDD_MDIO Schmitt trigger	Management data clock. When DVDD_MDIO = 1.8V, the MDIO/MDC can operate at 2.5V and 3.3V signaling using an external pull-up to higher supply. When DVDD_MDIO = 1.2V, only 1.2V signaling is supported.
M5	MDIO	IOD	DVDD_MDIO open-drain	Management data input/output for MDIO secondary device. A pull-up resistor is required on this pin. When DVDD_MDIO = 1.8V, the MDIO/MDC can operate at 2.5V and 3.3V signaling using an external pull-up to higher supply. When DVDD_MDIO = 1.2V, only 1.2V signaling is supported.
U24	PHY_ADDR4	I	DVDD_MDIO internal pull-down	PHY address 4:2. MSB of MDIO PHY address [4:0]. Bits 1:0 are hardwired internally.
U13	PHY_ADDR3			
J5	PHY_ADDR2			

Table 12: AVS Two-Wire Interfaces

Ball No.	Ball Name	Ball Type	Level	Description
L15	SCLAS	I	DVDDIO open-drain External pull-up required	BSC secondary serial clock input.
L13	SDAAS	IOD	DVDDIO open-drain External pull-up required	BSC secondary serial data input/output. Open-drain output.
M13	SCLAM	OD	DVDDIO open-drain External pull-up required	BSC master serial clock output.

Table 12: AVS Two-Wire Interfaces (Continued)

Ball No.	Ball Name	Ball Type	Level	Description
M4	SDAAM	IOD	DVDDIO open-drain External pull-up required	BSC master serial data input/output.

Table 13: SPI Master

Ball No.	Ball Name	Ball Type	Level	Description
K5	SCK	O	DVDDIO Internal pull-down	SPI serial clock output to SPI ROM secondary device.
K4	SS_N	O	DVDDIO Internal pull-up	SPI chip select output to SPI ROM secondary device.
M14	MISO	I	DVDDIO Internal pull-down	SPI master data input from SPI ROM secondary output.
R24	MOSI	O	DVDDIO Internal pull-down	SPI master data output to SPI ROM secondary input.
H13	SERBOOT	I	DVDDIO Internal pull-up	Set high to load firmware from external SPI-ROM.

Table 14: Interrupt

Ball No.	Ball Name	Ball Type	Level	Description
R4	INTR_N_0	OD	DVDDIO	Open-drain output for channel 0 through 7 interrupts. Requires an external pull-up resistor. 3.3V tolerant.
L14	INTR_N_1	OD	DVDDIO	Open-drain output for channel 8 through 15 interrupts. Requires an external pull-up resistor. 3.3V tolerant.

Table 15: GPIO

Ball No.	Ball Name	Ball Type	Level	Description
M12	GPIO5_0	I/O	DVDDIO internal pull-down	General-purpose I/O for lanes 0 to 7.
M11	GPIO4_0	I/O	DVDDIO internal pull-down	General-purpose I/O for lanes 0 to 7.
M10	GPIO3_0	I/O	DVDDIO internal pull-down	General-purpose I/O for lanes 0 to 7.
M9	GPIO2_0	I/O	DVDDIO internal pull-down	General-purpose I/O for lanes 0 to 7.
M8	GPIO1_0	I/O	DVDDIO internal pull-down	General-purpose I/O for lanes 0 to 7.
M7	GPIO0_0	I/O	DVDDIO internal pull-down	General-purpose I/O for lanes 0 to 7.
M22	GPIO5_1	I/O	DVDDIO internal pull-down	General-purpose I/O for lanes 8 to 15.
M21	GPIO4_1	I/O	DVDDIO internal pull-down	General-purpose I/O for lanes 8 to 15.
M20	GPIO3_1	I/O	DVDDIO internal pull-down	General-purpose I/O for lanes 8 to 15.
M19	GPIO2_1	I/O	DVDDIO internal pull-down	General-purpose I/O for lanes 8 to 15.
M18	GPIO1_1	I/O	DVDDIO internal pull-down	General-purpose I/O for lanes 8 to 15.
M17	GPIO0_1	I/O	DVDDIO internal pull-down	General-purpose I/O for lanes 8 to 15.

Table 16: JTAG

Ball No.	Ball Name	Ball Type	Level	Description
M24	TRSTB	I	DVDDIO Schmitt trigger Internal pull-down	JTAG test reset input. Active-low. Resets the JTAG controller. Signal must be pulled low during normal operation.
M16	TCK	I	DVDDIO Schmitt trigger Internal pull-down	JTAG test clock input.
K23	TMS	I	DVDDIO internal pull-up	JTAG test mode select input.
K24	TDI	I	DVDDIO internal pull-up	JTAG serial test data input.
M15	TDO	O	DVDDIO tristate	JTAG serial test data output.

Table 17: Power Supplies and Common Pins

Ball No.	Ball Name	Ball Type	Level	Description
K7, V4	AVDDPLL_01	PWR	0.8V	PLL power supply.
K8, V6	AVDDPLL_23	PWR	0.8V	PLL power supply.
K10, V9	AVDDPLL_45	PWR	0.8V	PLL power supply.
K11, V11	AVDDPLL_67	PWR	0.8V	PLL power supply.
K17, V15	AVDDPLL_89	PWR	0.8V	PLL power supply.
K18, V17	AVDDPLL_AB	PWR	0.8V	PLL power supply.
K20, V20	AVDDPLL_CD	PWR	0.8V	PLL power supply.
K21, V22	AVDDPLL_EF	PWR	0.8V	PLL power supply.
K9, K19, V8, V19	AVDDPLL1P8	PWR	1.8V	1.8V PLL power supply.
V13, V24, Y7, Y8, Y13, Y18, Y19, Y24	LN_AVDDTX	PWR	0.8V	Line-side transmit power supply.
AA7, AA8, AA13, AA18, AA19, AA24, W13, W24	LN_AVDDTXDRV	PWR	0.8V to 1.0V	Line-side analog driver TX power. **NOTE:** The voltage can be 0.8V to 1.0V. The differential voltage of the analog transmitter is 0.8V peak-to-peak with a 0.8V driver. If only 0.8V peak-to-peak is required on the line side, LN_AVDDTXDRV can be tied to LN_AVDDTX.
AA4, AA5, AA10, AA11, AA15, AA16, AA21, AA22, Y4, Y5, Y10, Y11, Y15, Y16, Y21, Y22	LN_AVDDRX	PWR	0.8V	Line-side receive power supply.
H9, H19	SYS_AVDDTX	PWR	0.8V	Host-side transmit power supply.
G9, G19	SYS_AVDDTXDRV	PWR	0.8V to 1.0V	Host-side analog driver TX power. **NOTE:** The voltage can be 0.8V to 1.0V. The differential voltage of the analog transmitter is 0.8V peak-to-peak with a 0.8V driver. If only 0.8V peak-to-peak is required on the host side, SYS_AVDDTXDRV can be tied to SYS_AVDDTX.
G7, G11, G17, G21, H7, H11, H17, H21	SYS_AVDDRX	PWR	0.8V	Host-side receive power supply.
P6, P7, P8, P9, P10, P11, P12, P13, P15, P16, P17, P18, P19, P20, P21, P22, P23, R5, R6, R7, R8, R9, R10, R11, R12, R15, R16, R17, R18, R19, R20, R21, R22	DVDD	PWR	0.72/ 0.8V	DVDD supply. DVDD can be set to 0.72V to reduce digital power consumption.
P14	DVDDM	PWR	0.8V	Digital memory supply. Can be combined with other supplies.

Table 17: Power Supplies and Common Pins (Continued)

Ball No.	Ball Name	Ball Type	Level	Description
R14	DVDD_MDIO	PWR	1.8V/ 1.2V	MDIO interface supply.
R13, R23	DVDDIO	PWR	1.8V	Digital I/O supply.
A1, A3, A5, A7, A9, A11, A13, A15, A17, A19, A21, A23, A25, A27, AA1, AA2, AA3, AA6, AA9, AA12, AA14, AA17, AA20, AA23, AA25, AA26, AA27, AB3, AB4, AB5, AB6, AB7, AB8, AB9, AB10, AB11, AB12, AB13, AB14, AB15, AB16, AB17, AB18, AB19, AB20, AB21, AB22, AB23, AB24, AB25, AC1, AC2, AC3, AC5, AC7, AC9, AC11, AC13, AC15, AC17, AC19, AC21, AC23, AC25, AC26, AC27, AD3, AD5, AD7, AD9, AD11, AD13, AD15, AD17, AD19, AD21, AD23, AD25, AE1, AE2, AE3, AE4, AE5, AE6, AE7, AE8, AE9, AE10, AE11, AE12, AE13, AE14, AE15, AE16, AE17, AE18, AE19, AE20, AE21, AE22, AE23, AE24, AE25, AE26, AE27, AF1, AF3, AF5, AF7, AF9, AF11, AF13, AF15, AF17, AF19, AF21, AF23, AF25, AF27, AG1, AG3, AG5, AG7, AG9, AG11, AG13, AG15, AG17, AG19, AG21, AG23, AG25, AG27, B1, B3, B5, B7, B9, B11, B13, B15, B17, B19, B21, B23, B25, B27, C1, C2, C3, C4, C5, C6, C7, C8, C9, C10, C11, C12, C13, C14, C15, C16, C17, C18, C19, C20, C21, C22, C23, C24, C25, C26, C27, D3, D5, D7, D9, D11, D13, D15, D17, D19, D21, D23, D25, E1, E2, E3, E5, E7, E9, E11, E13, E15, E17, E19, E21, E23, E25, E26, E27, F3, F4, F5, F6, F7, F8, F9, F10, F11, F12, F13, F14, F15, F16, F17, F18, F19, F20, F21, F22, F23, F24, F25, G1, G2, G3, G6, G8, G10, G12, G16, G18, G20, G22, G25, G26, G27, H3, H4, H5, H6, H8, H10, H12, H16, H18, H20, H22, H23, H24, H25, J1, J2, J3, J6, J7, J8, J9, J10, J11, J12, J16, J17, J18, J19, J20, J21, J22, J25, J26, J27, K3, K6, K12, K16, K22, K25, L1, L2, L3, L6, L7, L8, L9, L10, L11, L12, L16, L17, L18, L19, L20, L21, L22, L25, L26, L27, M26, N1, N2, N3, N6, N7, N8, N9, N10, N11, N12, N13, N14, N15, N16, N17, N18, N19, N20, N21, N22, N23, N25, N26, N27, P3, P25, R1, R2, R3, R25, R26, R27, T3, T5, T6, T7, T8, T9, T10, T11, T12, T13, T14, T15, T16, T17, T18, T19, T20, T21, T22, T23, T25, U1, U2, U3, U4, U5, U6, U7, U8, U9, U10, U11, U12, U14, U15, U16, U17, U18, U19, U20, U21, U22, U23, U25, U26, U27, V3, V5, V7, V10, V12, V14, V16, V18, V21, V23, V25, W1, W2, W3, W4, W5, W6, W7, W8, W9, W10, W11, W12, W14, W15, W16, W17, W18, W19, W20, W21, W22, W23, W25, W26, W27, Y3, Y6, Y9, Y12, Y14, Y17, Y20, Y23, Y25	VSS	GND	0V	—

Table 17: Power Supplies and Common Pins (Continued)

Ball No.	Ball Name	Ball Type	Level	Description
G4, G5, G14, G23, G24, H14, H15, J4, J13, J14, J15, J23, J24, K13, K14, K15, L4, L5, L23, L24, M1, M2, M6, M23, N4, N5, N24, P5, P24, P26, P27, T4, T24	NC	—	—	Not connected.

3.2 Ballout Location Diagram

Figure 10: Ballout Locations (Top View)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	
A	VSS	SYS2_TXN	VSS	SYS3_TXN	VSS	SYS4_TXN	VSS	SYS5_TXN	VSS	SYS6_TXN	VSS	SYS7_TXN	VSS	SYS8_TXN	VSS	SYS9_TXN	VSS	SYS10_TXN	VSS	SYS11_TXN	VSS	SYS12_TXN	VSS	SYS13_TXN	VSS	SYS14_TXN	VSS	A
B	VSS	SYS2_TXP	VSS	SYS3_TXP	VSS	SYS4_TXP	VSS	SYS5_TXP	VSS	SYS6_TXP	VSS	SYS7_TXP	VSS	SYS8_TXP	VSS	SYS9_TXP	VSS	SYS10_TXP	VSS	SYS11_TXP	VSS	SYS12_TXP	VSS	SYS13_TXP	VSS	SYS14_TXP	VSS	B
C	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	C
D	SYS1_TXN	SYS1_TXP	VSS	SYS2_RXN	VSS	SYS3_RXN	VSS	SYS4_RXN	VSS	SYS5_RXN	VSS	SYS6_RXN	VSS	SYS7_RXN	VSS	SYS8_RXN	VSS	SYS9_RXN	VSS	SYS10_RXN	VSS	SYS11_RXN	VSS	SYS12_RXN	VSS	SYS15_TXP	SYS15_TXN	D
E	VSS	VSS	VSS	SYS2_RXP	VSS	SYS3_RXP	VSS	SYS4_RXP	VSS	SYS5_RXP	VSS	SYS6_RXP	VSS	SYS7_RXP	VSS	SYS8_RXP	VSS	SYS9_RXP	VSS	SYS10_RXP	VSS	SYS11_RXP	VSS	SYS12_RXP	VSS	VSS	VSS	E
F	SYS0_TXN	SYS0_TXP	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	SYS13_RXP	SYS13_RXN	F
G	VSS	VSS	VSS	NC	NC	VSS	SYS_AVDDRX	VSS	SYS_AVDDTXDRV	VSS	SYS_AVDDRX	VSS	REFDIV_SEL0	NC	REFDIV_SEL1	VSS	SYS_AVDDRX	VSS	SYS_AVDDTXDRV	VSS	SYS_AVDDRX	VSS	NC	NC	VSS	VSS	VSS	G
H	SYS1_RXN	SYS1_RXP	VSS	VSS	VSS	VSS	SYS_AVDDRX	VSS	SYS_AVDDTX	VSS	SYS_AVDDRX	VSS	SER BOOT	NC	NC	VSS	SYS_AVDDRX	VSS	SYS_AVDDTX	VSS	SYS_AVDDRX	VSS	VSS	VSS	VSS	SYS14_RXP	SYS14_RXN	H
J	VSS	VSS	VSS	NC	PHY_ADDR2	VSS	VSS	VSS	VSS	VSS	VSS	VSS	NC	NC	NC	VSS	VSS	VSS	VSS	VSS	VSS	VSS	NC	NC	VSS	VSS	VSS	J
K	SYS0_RXN	SYS0_RXP	VSS	SS_N	SCK	VSS	AVDD PLL_01	AVDDPLL_23	AVDDPLL1P8	AVDDPLL_45	AVDDPLL_67	VSS	NC	NC	NC	VSS	AVDD PLL_89	AVDD PLL_AB	AVDDPLL1P8	AVDDPLL_CD	AVDDPLL_EF	VSS	TMS	TDI	VSS	SYS15_RXP	SYS15_RXN	K
L	VSS	VSS	VSS	NC	NC	VSS	VSS	VSS	VSS	VSS	VSS	VSS	SDAAS	INTR_N_1	SCLAS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	NC	NC	VSS	VSS	VSS	L
M	NC	NC	RESET_L	SDAAM	MDIO	NC	GPIO0_0	GPIO1_0	GPIO2_0	GPIO3_0	GPIO4_0	GPIO5_0	SCLAM	MISO	TDO	TCK	GPIO0_1	GPIO1_1	GPIO2_1	GPIO3_1	GPIO4_1	GPIO5_1	NC	TRSTB	RCLK0	VSS	RCLK1	M
N	VSS	VSS	VSS	NC	NC	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	NC	VSS	VSS	VSS	N
P	RCLK_DIFF_N	RCLK_DIFF_P	VSS	MDC	NC	DVDD	DVDD	DVDD	DVDD	DVDD	DVDD	DVDD	DVDD	DVDDM	DVDD	DVDD	DVDD	DVDD	DVDD	DVDD	DVDD	DVDD	DVDD	NC	VSS	NC	NC	P
R	VSS	VSS	VSS	INTR_N_0	DVDD	DVDD	DVDD	DVDD	DVDD	DVDD	DVDD	DVDD	DVDDIO	DVDD_MDIO	DVDD	DVDD	DVDD	DVDD	DVDD	DVDD	DVDD	DVDD	DVDDIO	MOSI	VSS	VSS	VSS	R
T	REFCLK_0N	REFCLK_0P	VSS	NC	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	NC	VSS	REFCLK_1N	REFCLK_1P	T
U	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	PHY_ADDR3	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	PHY_ADDR4	VSS	VSS	VSS	U
V	LN0_RXN	LN0_RXP	VSS	AVDD PLL_01	VSS	AVDD PLL_23	VSS	AVDD PLL1P8	AVDDPLL_45	VSS	AVDD PLL_67	VSS	LN_AVDDTX	VSS	AVDD PLL_89	VSS	AVDD PLL_AB	VSS	AVDDPLL1P8	AVDDPLL_CD	VSS	AVDD PLL_EF	VSS	LN_AVDDTX	VSS	LN15_RXP	LN15_RXN	V
W	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	LN_AVDDTXDRV	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	LN_AVDDTXDRV	VSS	VSS	VSS	W
Y	LN1_RXN	LN1_RXP	VSS	LN_AVDDRX	LN_AVDDRX	VSS	LN_AVDDTX	LN_AVDDTX	VSS	LN_AVDDRX	LN_AVDDRX	VSS	LN_AVDDTX	VSS	LN_AVDDRX	LN_AVDDRX	VSS	LN_AVDDTX	LN_AVDDTX	VSS	LN_AVDDRX	LN_AVDDRX	VSS	LN_AVDDTX	VSS	LN14_RXP	LN14_RXN	Y
AA	VSS	VSS	VSS	LN_AVDDRX	LN_AVDDRX	VSS	LN_AVDDTXDRV	LN_AVDDTXDRV	VSS	LN_AVDDRX	LN_AVDDRX	VSS	LN_AVDDTXDRV	VSS	LN_AVDDRX	LN_AVDDRX	VSS	LN_AVDDTXDRV	LN_AVDDTXDRV	VSS	LN_AVDDRX	LN_AVDDRX	VSS	LN_AVDDTXDRV	VSS	VSS	VSS	AA
AB	LN0_TXN	LN0_TXP	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	LN13_RXP	LN13_RXN	AB
AC	VSS	VSS	VSS	LN2_RXP	VSS	LN3_RXP	VSS	LN4_RXP	VSS	LN5_RXP	VSS	LN6_RXP	VSS	LN7_RXP	VSS	LN8_RXP	VSS	LN9_RXP	VSS	LN10_RXP	VSS	LN11_RXP	VSS	LN12_RXP	VSS	VSS	VSS	AC
AD	LN1_TXN	LN1_TXP	VSS	LN2_RXN	VSS	LN3_RXN	VSS	LN4_RXN	VSS	LN5_RXN	VSS	LN6_RXN	VSS	LN7_RXN	VSS	LN8_RXN	VSS	LN9_RXN	VSS	LN10_RXN	VSS	LN11_RXN	VSS	LN12_RXN	VSS	LN15_TXP	LN15_TXN	AD
AE	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	AE
AF	VSS	LN2_TXP	VSS	LN3_TXP	VSS	LN4_TXP	VSS	LN5_TXP	VSS	LN6_TXP	VSS	LN7_TXP	VSS	LN8_TXP	VSS	LN9_TXP	VSS	LN10_TXP	VSS	LN11_TXP	VSS	LN12_TXP	VSS	LN13_TXP	VSS	LN14_TXP	VSS	AF
AG	VSS	LN2_TXN	VSS	LN3_TXN	VSS	LN4_TXN	VSS	LN5_TXN	VSS	LN6_TXN	VSS	LN7_TXN	VSS	LN8_TXN	VSS	LN9_TXN	VSS	LN10_TXN	VSS	LN11_TXN	VSS	LN12_TXN	VSS	LN13_TXN	VSS	LN14_TXN	VSS	AG
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	

Chapter 4: Management Interfaces

This section provides details on the BCM81356 management interfaces.

4.1 MDIO Access

The BCM81356 can operate in MDIO with indirect MDIO access as shown in Table 18.

For a write transfer, follow this procedure:

1. Program the indirect control register IND_CTRL for the desired data type and address mode.
2. Write two indirect address registers, IND_ADDRL and IND_ADDRH, for a 32-bit address.
3. Write one or two indirect data registers, IND_DATAL and IND_DATAH. In the case of a word transfer, program IND_DATAL first then IND_DATAH; otherwise, write only to IND_DATAL.

For a read transfer, follow this procedure:

1. Program the indirect control register IND_CTRL for the desired data type and address mode.
2. Write two indirect address registers, IND_ADDRL and IND_ADDRH, for a 32-bit address.
3. Read from one or two indirect data registers, IND_DATAL and IND_DATAH. In the case of a word transfer, read IND_DATAL first then IND_DATAH; otherwise, read only IND_DATAL.

Table 18: MDIO Indirect Address Descriptions

Name	MDIO Address	APB Offset Address	Bit	Access	Description
IND_ADDRL	0x0000	—	15:0	R/W	Indirect access address low [15:0]. Address must be aligned with the data types.
IND_ADDRH	0x0001	—	15:0	R/W	Indirect access address high [31:16].
IND_DATAL	0x0002	—	15:0	R/W	Indirect access data low [15:0]: ■ Write this register to start DMA byte data for IND_DATAL[7:0] write transfer when IND_CTRL[5:4]=00. ■ Write this register to start DMA half-word data for IND_DATAL[15:0] write transfer when IND_CTRL[5:4]=01. ■ Read this register to start DMA data read transfer. When IND_CTRL[5:4]=00, IND_DATAL[7:0] is valid. When IND_CTRL[5:4]=01/10, IND_DATAL[15:0] is valid.
IND_DATAH	0x0003	—	15:0	R/W	Indirect access data high [31:16]: ■ Write this register to start DMA byte data for both IND_DATAL[15:0] and IND_DATAH[15:0] write transfer when IND_CTRL[5:4]=10. ■ Read this register to get higher 16-bit read data when IND_CTRL[5:4]==10.

Table 18: MDIO Indirect Address Descriptions (Continued)

Name	MDIO Address	APB Offset Address	Bit	Access	Description
IND_CTRL	0x0004	—	6:0	R/W	Indirect access control: Bits 3 through 0: Reserved Bits 5 through 4: Indirect access data type/size ■ 00: Byte (8 bit) ■ 01: Half-word (16 bit) ■ 11: Reserved Bit 6: Indirect address auto post increment: ■ 0: Fixed address ■ 1: Address post auto increment by the size of IND_CTRL[5:4] on writes, by word on reads
MDIO_STAT	0x0005	0x000	1:0	R/W	MDIO status: Bit 0: DMA transfer error Bit 1: MDIO read data late error

4.2 MDIO (Secondary) Interface

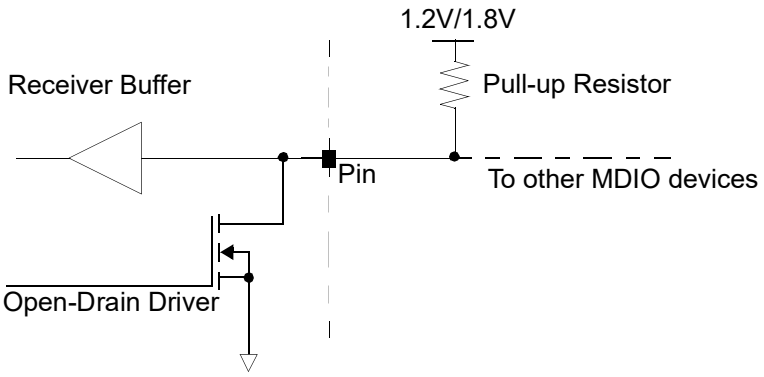
The PHY supports IEEE 802.3 Clause 45 Station Management Interface. Clause 22 is not supported. The PHY acts as an MDIO manageable secondary device (MMD) and responds to the host when it receives frames with a matching PRTAD and DEVAD.

When an MDIO write/read operation is executed, the PHY compares the PRTAD field with its own PHY address. The operation is executed only when the PRTAD matches the PHY port address.

The MDIO is a two-wire interface standard, using the MDIO signal for serial data and the MDC for the serial clock. A 16-bit shift register receives data from the MDIO pin on the rising edge of the MDC clock. The frame format begins with a preamble for clock synchronization followed by the start-of-frame sequence. The read or write opcode, PRTAD, and DEVAD fields follow next. Only one device type is supported for DEVAD: 11111. Depending on the read/write opcode, data is either received or transmitted by the PHY. Once the 16-bit data field is transferred, the MDIO signal is returned to a high-impedance state (idle).

Figure 11 shows the MDIO interface.

Figure 11: MDIO Interface



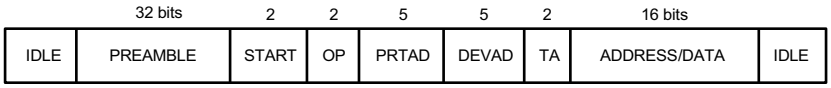
4.3 MDIO Frame Format

The MDIO frame format begins with a preamble and then is followed by the start-of-frame sequence. The read or write opcode, PRTAD, and DEVAD fields follow next. Depending on the read/write opcode, data is either received or transmitted by the PHY. After the 16-bit data field is transferred, the MDIO signal is returned to a high-impedance state (idle).

Figure 12 shows the MDIO frame format. This format is used for both read and write operations.

- Preamble = 32-bit 1s (optional)
- START = Start of frame indicated by 00 pattern
- OP = Opcode (access type)
  - 00: Address
  - 01: Write
  - 11: Read
  - 10: Postread increment address
- TA = Turnaround
  - Z0: Read
  - 10: Write
- PRTAD = Physical address
- DEVAD = Device address
  - 11111: Only option for the BCM81356
- Address/data = 16-bit address or data

Figure 12: MDIO Frame Format



NOTE: The BCM81356 operates with indirect MDIO access 32-bit address/data. See Section 4.1, MDIO Access, indirect addressing details.

Any read or write operation to a PHY register requires the transmission of at least two MDIO frames from the host. The first frame tells the PHY the address of the target register (with opcode = 00), and the second frame performs the actual read or write operation (with opcode = 11 for read and opcode = 01 for write).

Chapter 5: Register Summary

The tables below describe the chip-level registers of the BCM81356.

Table 19: CHIP ID REG LSB (0x5200_cb20)

Bits	Name	Type	Default	Description
31:16	Reserved	RSVD	0x0	Reserved bits must be written with 0. A read returns an unknown value.
15:0	chip_id_lower_word	RO	0x1356	Chip ID[15:0].

Table 20: CHIP ID REG MSB (0x5200_cb24)

Bits	Name	Type	Default	Description
31:4	Reserved	RSVD	0x0	Reserved bits must be written with 0. A read returns an unknown value.
3:0	chip_id_high_nibble	RO	0x0008	Chip ID[19:16].

Table 21: REV ID REG (0x5200_cb28)

Bits	Name	Type	Default	Description
31:8	Reserved	RSVD	0x0	Reserved bits must be written with 0. A read returns an unknown value.
7:0	rev_id	RO	0xb0	Revision ID.

Chapter 6: Electrical and Timing Characteristics

The tables and figures below show the BCM81356 electrical and timing characteristics.

Table 22: Power Consumption

Parameter	Condition	Min.	Typ.	Max.	Unit
Power consumption (retimer with AVS)	Default	—	11.86[a]	—	W

a. Power consumption with AVS.

Table 23: Absolute Maximum Ratings

Parameter	Min.	Typ.	Max.	Unit
Storage temperature	–45	—	+150	°C
Supply voltage on VDDIO and AVDDPLL1P8	–0.3	—	2.1	V
Supply voltage on VDD_MDIO	–0.3V	—	2.1	V
Supply voltage on AVDD_TX, AVDD_RX, AVDD_PLL, and DVDD	–0.3	—	1	V
Voltage on any CML, CMOS, or LVPECL input pin with respect to VSS	–0.3	—	VDD + 0.3	V

CAUTION! Permanent damage may result if the device is stressed beyond the absolute maximum ratings. The device specifications are guaranteed only under the recommended operating conditions.

Table 24: Recommended Operating Conditions

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Ambient temperature under bias	Ta	—	0	25	70	°C
Operating junction temperature	Tj	—	0	—	110	°C
Supply voltage on AVDDPLL_xx, LN_AVDDTX, LN_AVDDRX, SYS_AVDDTX, SYS_AVDDRX, and DVDDM	—	—	0.776	0.8	0.824	V
Supply voltage on DVDD	DVDD	—	0.685	0.72/0.8	0.824	V
Supply voltage on DVDD_MDIO	DVDD_MDIO	—	—	1.2/1.8	—	V
Supply voltage on DVDDIO and AVDDPLL1P8	—	—	1.71	1.8	1.85	V
Supply voltage on LV_AVDDTXDRV and SYS_AVDDTXDRV	—	—	0.776	0.8	1.0	V
Ground voltage (VSS)	VSS	—	—	0	—	V
Reference clock frequency (typical)	—	—	—	156.25	—	MHz
Reference clock frequency tolerance asynchronous	—	—	–100	—	+100	ppm
Reference clock input voltage swing differential	Differential VPPD	—	600	800	1200	mV
Reference clock duty cycle	—	—	40	—	60	%
Reference clock rise and fall times	—	20% to 80% of amplitude	—	500	600	ps
Reference clock jitter (phase jitter)	—	12 kHz to 20 MHz	—	—	0.25	psRMS

Figure 13: Clock Input Receiver

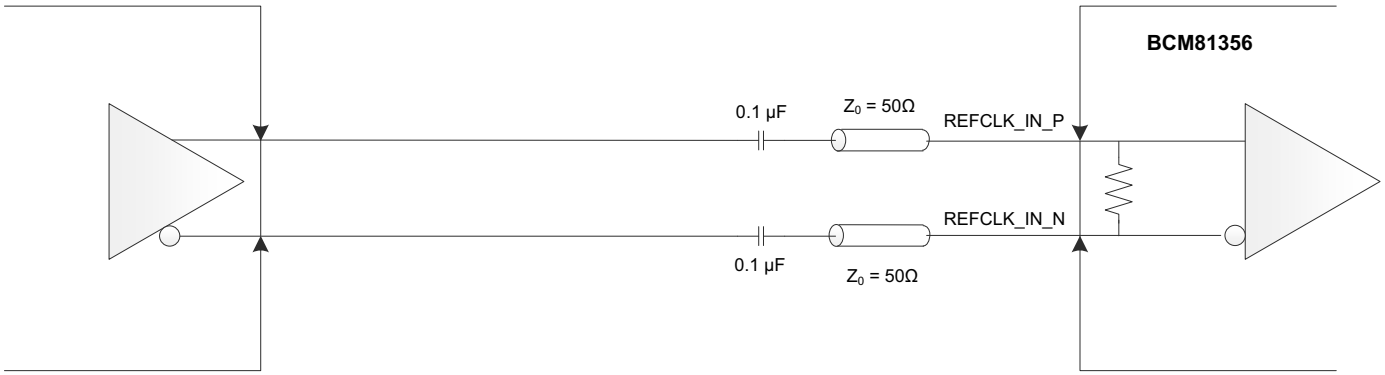


Table 25: Recovered Clock

Parameter	Min.	Typ.	Max.	Unit
Differential p-to-p output voltage	—	500	—	mV
Frequency (selectable, data rate/divider ratio)	—	—	—	MHz
Jitter	—	1	—	psRMS

Table 26: 1.8V CMOS DC Characteristics

Parameter	Condition	Specification			Unit
		Min.	Typ.	Max.	
CMOS output low voltage V_{OL}	—	—	—	0.4	V
CMOS output high voltage V_{OH}	8 mA*	1.4	—	—	V
CMOS input low voltage V_{IL}	—	—	—	0.63	V
CMOS input high voltage V_{IH}	—	1.17	—	—	V
Input low current I_{IL}	—	—	—	–5	µA
Input high current I_{IH}	—	—	—	5	µA

NOTE:

- Digital I/O power supply = 1.8V.
- * Drive strength: 16 mA for MDIO and 12 mA for INT0. Open-drain driver output high voltage depends on external pull-up voltage level.
- The specifications of the BSC interface (SCALAM and SDAAM) are I^2C compliant.

Table 27: MDC and MDIO AC Characteristics

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
MDIO output propagation delay after rising edge of MDC	t_{C2D}	—	—	—	25	ns
MDIO output from driven to high impedance after rising edge of MDC	t_{D2Z}	—	—	—	20	ns
MDC frequency	$MDC_{frequency}$	—	—	9	—	MHz
MDC duty cycle	t_{CKH}/t_{CK}	—	30	—	70	%
MDIO input setup time to rising edge of MDC	t_{DIS}	—	5	—	—	ns
MDIO input hold time after rising edge of MDC	t_{DIH}	—	5	—	—	ns

Figure 14: MDC and MDIO Timing Waveforms

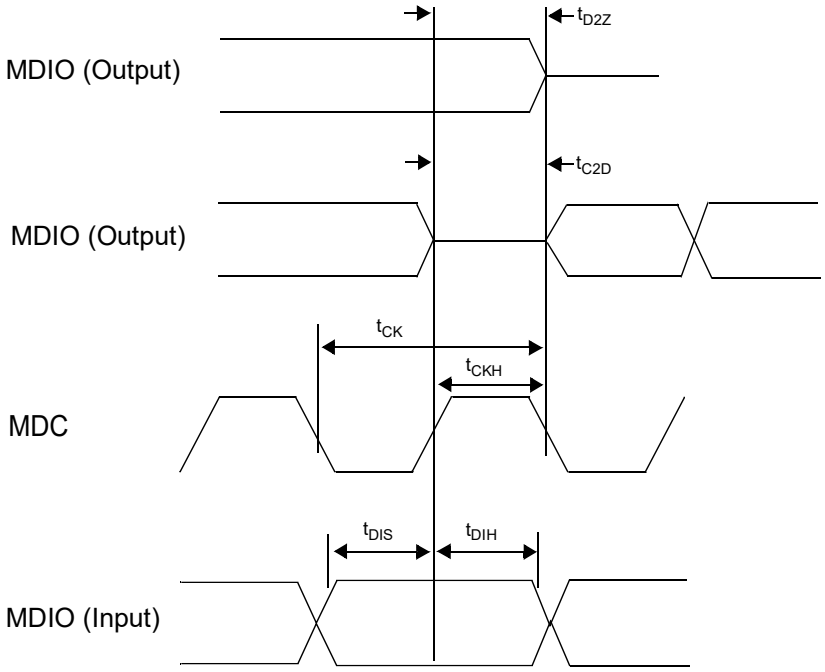


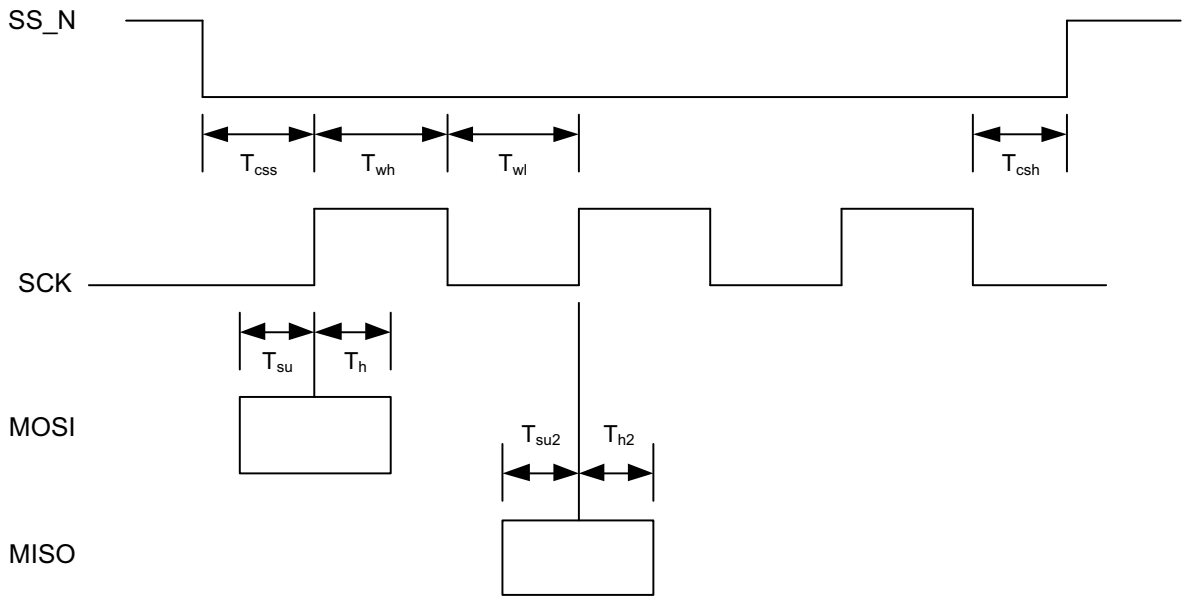
Table 28: SPI Interface AC Characteristics, Connecting to SPI-EEPROM

Parameter	Symbol	Min.	Typ.	Unit
Operating frequency	F_{sck}	2.44	3.9	MHz
SPI CS setup time	T_{css}	200	—	ns
SPI CS hold time	T_{ch}	200	—	ns
SPI CK high-pulse width	T_{wh}	—	200	ns
SPI CK low-pulse width	T_{wl}	—	200	ns
Data output setup time	T_{su}	80	—	ns
Data output hold time	T_{h}	80	—	ns
Input data setup time	T_{su2}	—	15	ns
Input data hold time	T_{h2}	—	15	ns

Table 29: SPI Interface AC Characteristics, Connecting to SPI-Flash

Parameter	Symbol	Min.	Typ.	Unit
Operating frequency	F_{sck}	—	9.77	MHz
SPI CS setup time	T_{css}	50	—	ns
SPI CS hold time	T_{ch}	50	—	ns
SPI CK high-pulse width	T_{wh}	—	60	ns
SPI CK low-pulse width	T_{wl}	—	60	ns
Data output setup time	T_{su}	20	—	ns
Data output hold time	T_{h}	20	—	ns
Input data setup time	T_{su2}	—	15	ns
Input data hold time	T_{h2}	—	15	ns

Figure 15: SPI Interface Timing Waveforms



Chapter 7: Reference Clock PCB Design Guidelines

Follow these reference clock PCB design guidelines for the BCM81356:

- Always use a designated 100Ω differential transmission line (no split) from the reference clock source to the BCM81356 package reference clock input with minimal P and N skew (preferably under 10 mils) using the best design practice.
- Route the reference clock on external layers to avoid a via stub. Route on the top or bottom layers.
- Minimize routing layer changes to reduce the number of vias in the signal path. Less than two routing layer changes are recommended.
- Install DC blocking capacitors closer to the source of the crystal oscillator than to the BCM81356 input.
- Long routing (>10 in.) is acceptable provided:
  - Signal amplitude meets the Broadcom reference clock specifications at the input of the package after being attenuated by long routing traces.
  - No more impedance discontinuity than discussed here to create the reflection point.

Chapter 8: Recovered Clocks

Table 30 lists the recovered clock pins.

Table 30: Recovered Clock Pins

Ball Number	Ball Name
P2	RCLK_DIFF_P
P1	RCLK_DIFF_N
M25	RCLK0
M27	RCLK1

Pins P2 and P1 are the differential recovered clock output pins. Pins M25 and M27 are individual single-ended recovered clock output pins.

The differential recovered clock can be used for the higher-speed recovered clock output (which is 50 MHz and above), whereas the single-ended recovered clocks are for the lower-speed recovered clock outputs (which are below 50 MHz). The three recovered clock outputs are independent and can be sourced separately from the CDR recovered clock of any lane on either the line side or host side.

Under loss-of-signal or loss-of-lock conditions, the recovered clocks are squelched.

The recovered clock frequency can be calculated by the following formula:

recovered clock frequency = lane baud rate × OSR / divider ratio

The baud rate of the lane chosen as the recovered clock source is half of the lane data rate with PAM-4 signaling or equal to the lane data rate with NRZ signaling. The OSR refers to the oversampling ratio, which is set by the BCM81356 firmware according to the lane data-rate setting. The user does not need to set or change the OSR setting manually.

Table 31 lists the OSR for various lane data rates.

Table 31: Lane Data Rate OSR

Lane Data Rate (Gb/s)	OSR
53.125	1
25.78125	1
26.5625	1
20.625	1
10.3125	2
1.25	16.5

Table 32 lists the divider ratios for the single-ended and differential recovered clock outputs.

Table 32: Divider Ratios

Divider Ratio	Recovered Clocks	
	Single-Ended Outputs	Differential Output
32	N/A	Yes
64	N/A	Yes
128	N/A	Yes
256	N/A	Yes
512	Yes	Yes
1024	Yes	Yes
2048	Yes	Yes
4096	Yes	Yes

NOTE: The differential recovered clock outputs require external AC-coupling capacitors. Both the single-ended and the differential recovered clock outputs need external clock cleanup circuitry for synchronous Ethernet applications.

Chapter 9: Decoupling Recommendations

Table 33 and Figure 16 show the decoupling groups and decoupling circuit.

Table 33: Decoupling Groups

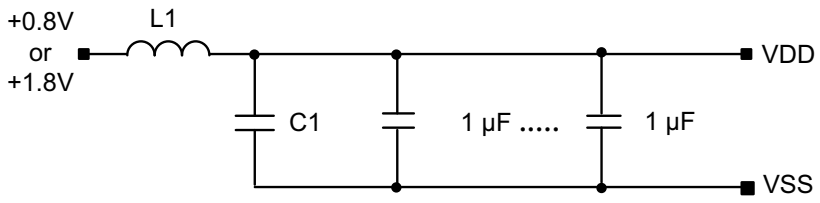
Pin Group	Filter Values		Filter Bandwidth 3-dB Cutoff (kHz)	Maximum Ripple (mVpp)
	Inductor L1 (µH)	Capacitor C1 (µF)		
AVDDPLL	4.7	33	15	3
AVDDTX	1	10	50	3
AVDDRX	1	10	50	3
AVDDTXDRV	4.7	33	15	3
DVDD	—	3 × 330	50	10
DVDDM	Ferrite bead	2.2	50	10
DVDDIO	Ferrite bead	2.2	50	20
DVDD_MDIO	Ferrite bead	2.2	50	20

For the pin group column in Table 33:

- AVDDPLL refers to AVDDPLL_01, AVDDPLL_23, AVDDPLL_45, AVDDPLL_67, AVDDPLL_89, AVDDPLL_AB, AVDDPLL_CD, AVDDPLL_EF, and AVDDPLL1P8
- AVDDTX refers to LN_AVDDTX and SYS_AVDDTX
- AVDDRX refers to LN_AVDDRX and SYS_AVDDRX
- AVDDTXDRV refers to LN_AVDDTXDRV and SYS_AVDDTXDRV

Each group of supply pins must have its own independent decoupling circuits. All decoupling circuits must use the same discrete components as shown in Figure 16. Each power rail must use multiple 1-µF capacitors placed close to the pins (use about one per power pin). Inductors with sufficient DC resistance must be chosen to keep DC loss at an acceptable level, given the supply tolerance of the various supply domains.

Figure 16: Decoupling Circuit



Chapter 10: Power-Sequencing Requirements

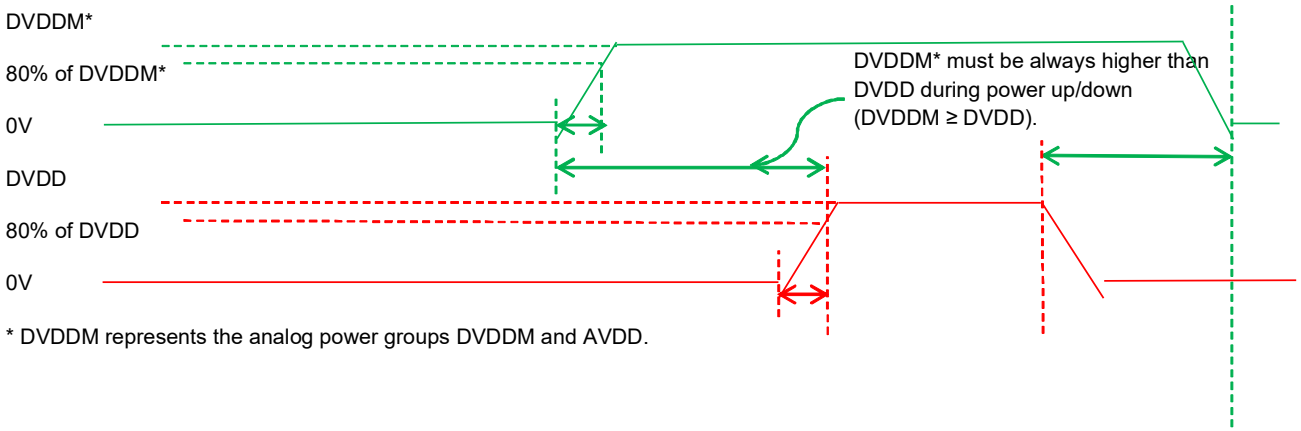
These are the power-sequencing requirements for all power rails.

1. The ramp-up and ramp-down times of all power rails must be less than 40 ms. The ramp-up time is defined as the time from 0V to 80% of each power rail's valid voltage level.
2. Between the digital power rails DVDD and DVDDM, the DVDDM must be higher than the DVDD during power-up/down (DVDDM ≥ DVDD). In a steady state, if the DVDDM is higher than DVDD, then keep DVDDM ≤ DVDD + 350 mV. If the DVDD is higher than the DVDDM, then keep DVDD ≤ DVDDM + 250 mV. Figure 17 shows the DVDDM and DVDD power-sequence timing diagram.
3. Analog AVDD (0.8V) and digital DVDDM can share the same power source.
4. Digital DVDD1P8 and analog AVDDPLL1P8 should be powered up last. When powered down, digital DVDD1P8 and analog AVDDPLL1P8 should be powered down first.

In summary, the power sequence of these power rails in power-up and power-down phases are as follows:

- When powered up: DVDDM/AVDD, DVDD, DVDD1P8
- When powered down: DVDD1P8, DVDD, DVDDM/AVDD

Figure 17: Power-Sequence Timing Diagram



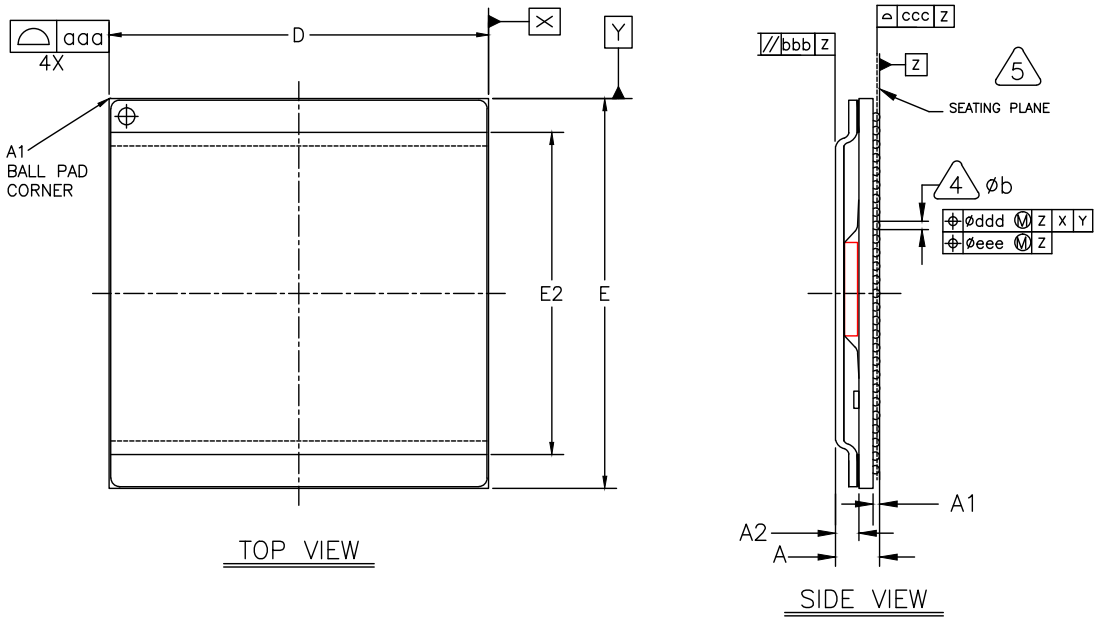
Chapter 11: Mechanical, Thermal, and ESD Information

The package, thermal, and ESD information is provided in these sections.

11.1 Package Outline Drawing

Figure 18 shows the BCM81356 package outline drawing.

Figure 18: 23 mm × 23 mm Package Outline



DIMENSIONAL REFERENCES (mm)			
REF.	MIN	NOM	MAX
A	2.45	2.67	2.89
A1	0.27	0.40	0.53
A2	---	1.41	---
D	22.85	23.00	23.15
D1		20.80 BSC	
D2		---	
E	22.85	23.00	23.15
E1		20.80 BSC	
E2		19.00 REF	
b	0.45	0.50	0.55
e		0.80 BSC	
f	–	1.10	–
aaa	–	–	0.15
bbb	–	–	0.35
ccc	–	–	0.20
ddd	–	–	0.20
eee	–	–	0.08

Filename: MOD81356 Rev.001

6. PCB LAND PATTERN RECOMMENDATION: LAND PATTERN KEY D REFER TO BROADCOM PACKAGING APPLICATION NOTE "PRINTED CIRCUIT BOARD LAND PATTERN RECOMMENDATIONS FOR BALL GRID ARRAY PACKAGES."

5 PRIMARY DATUM Z AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.

4 DIMENSION IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM Z.

3. THE BASIC SOLDER BALL GRID PITCH IS 0.80mm.

2. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M–1994.

1. THIS PACKAGE MEETS JEDEC REGISTERED AND STANDARD OUTLINES.

NOTES: UNLESS OTHERWISE SPECIFIED

11.2 Thermal Characteristics

The following tables show the package thermal resistances.

Table 34: Thermal Resistance (Package Only)

Device	θ_{JA}, °C/W	Airflow, m/s
BCM81356	15.67	0
θ_{JB} = 2.77°C/W	13.41	1
θ_{JC} = 0.96°C/W	12.31	2

Table 35: Thermal Resistance (Package with 40 × mm 40 × mm × 30 mm Heat Sink)

Device	θ_{JA}, °C/W	Airflow, m/s
BCM81356	5.91	0
θ_{JB} = 2.77°C/W	3.04	1
θ_{JC} = 0.96°C/W	2.64	2

11.3 Electrostatic Discharge Handling Precautions

Devices that comply with Broadcom design guidelines tolerate nominal electrostatic discharge (ESD) levels without damage. These high-speed, state-of-the-art devices undergo ESD susceptibility testing of input and output cells as part of a product qualification process before production.

Additionally, Broadcom employs personnel fully trained in proper ESD handling procedures. Devices are handled in static-controlled rooms with special workstations. All packaged devices are shipped in aluminum sealed bags inside boxes with Faraday cages designed to eliminate the risk of ESD damage.

CAUTION! Extreme caution must be exercised to prevent ESD damage. Proper use of wrist and heel grounding straps to discharge static electricity is required when handling these devices. Always store the unused material in its anti-static packaging.

Table 36: ESD Rating by Ball Type

Ball Type	ESD Rating	Units
Any ball to any ball JEDEC JESD-A114-B (human body model)	1000	V

Chapter 12: Ordering Information

The BCM81356 part ordering details are provided in this section.

Table 37: Ordering Information

Part Number	Description	Temperature Range
BCM81356B0KFSBG	B0 silicon, 23 mm × 23 mm, 0.8-mm ball pitch, 729-ball BGA, RoHS-compliant	0°C to 70°C
BCM81356B0IFSBG	B0 silicon, 23 mm × 23 mm, 0.8-mm ball pitch, 729-ball BGA, RoHS-compliant	–20°C to 85°C