



# FSUSB73

## 3:1 High-Speed USB Multiplexer and Hub Routing Switch

### Features

Switch Type	3:1 MUX + Isolation Switch
USB	USB 2.0 High-Speed & Full-Speed Compliant
R <sub>ON</sub>	6.5Ω
C <sub>ON</sub>	6pF
ESD (IEC61000-4-2)	15kV (Air), 8kV (Contact)
V <sub>CC</sub>	2.5 to 4.4V
I <sub>CCSLP</sub>	<1μA
I <sub>CCACT</sub>	9μA
Package	16-Lead UMLP 1.8 x 2.6 x 0.55mm, 0.40mm Pitch
Ordering Information	FSUSB73UMX (UMLP)

### Description

The FSUSB73 is a bi-directional, low-power, high-speed USB 2.0 3:1 MUX plus one isolation switch. It is optimized for switching three high-speed (480Mbps) or full / low-speed USB / UART sources to one USB 2.0 connector. In addition, the FSUSB73 has an integrated routing USB switch to allow communication between a USB hub and another processor without re-enumeration.

### Related Resources

- For samples and questions, please contact: [Analog.Switch@fairchildsemi.com](mailto:Analog.Switch@fairchildsemi.com).
- FSUSB73 Demonstration Board
- FSUSB73 Evaluation Board

### Applications

- MP3 Portable Media Players
- Cellular Phones, Smartphones
- Netbook, Mobile Internet Device (MID)
- Enables USB Hub Switching

### Typical Application

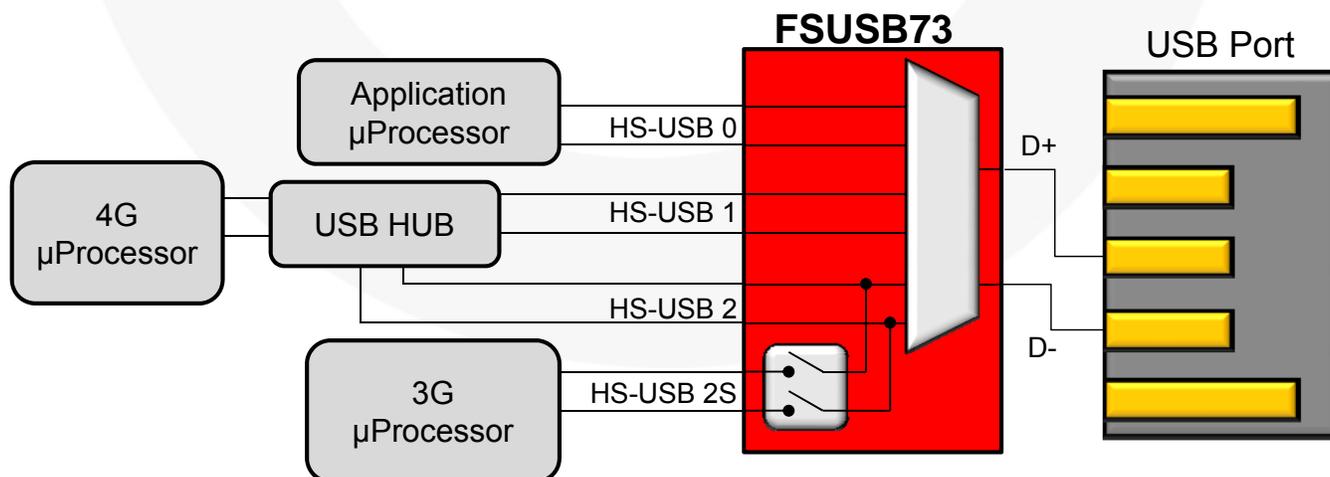


Figure 1. Mobile Phone Example

## Pin Configuration

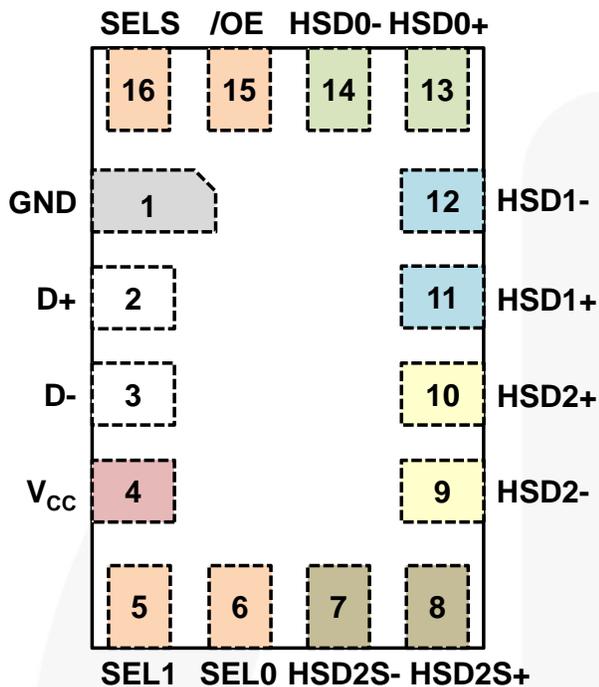


Figure 2. Pin Assignments (Top View)

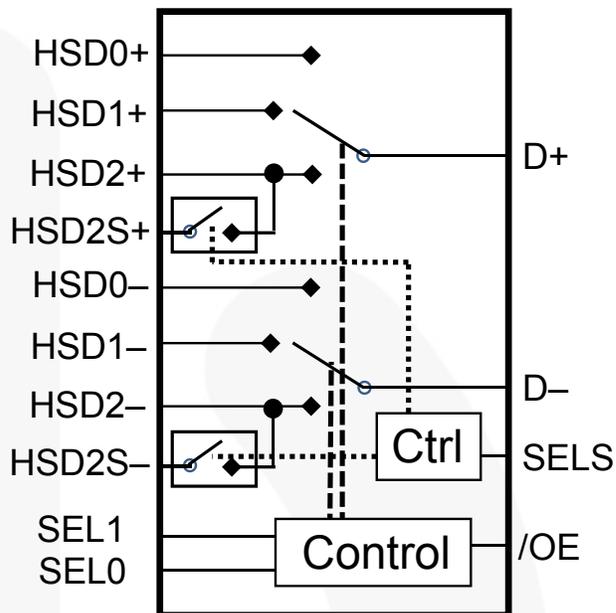


Figure 3. Analog Symbol

## Pin Descriptions

Pin #	Name	Type	Description
1	GND	Ground	Ground
2	D+	I/O	D+ Common Port (HS or FS USB)
3	D-	I/O	D- Common Port (HS or FS USB)
4	V <sub>CC</sub>	Power Supply	Supply Voltage
5	SEL1	Input	Path Selection Control Input (see Truth Tables)
6	SEL0	Input	Path Selection Control Input (see Truth Tables)
7	HSD2S-	I/O	HSD2- from Isolation Switch (HS or FS USB)
8	HSD2S+	I/O	HSD2+ from Isolation Switch (HS or FS USB)
9	HSD2-	I/O	D- from Third Source Path (HS or FS USB)
10	HSD2+	I/O	D+ from Third Source Path (HS or FS USB)
11	HSD1+	I/O	D+ from Second Source Path (HS or FS USB)
12	HSD1-	I/O	D- from Second Source Path (HS or FS USB)
13	HSD0+	I/O	D+ from First Source Path (HS or FS USB)
14	HSD0-	I/O	D- from First Source Path (HS or FS USB)
15	/OE	Input	Enable Control Input (see Truth Tables)
16	SELS	Input	Path Selection Control Input (see Truth Table)

## Truth Tables

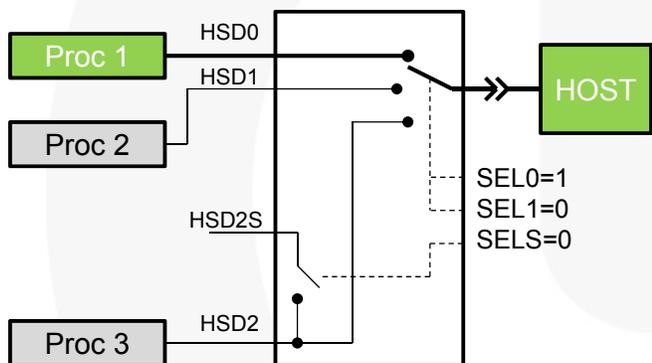
**Table 1. 3:1 USB Switch Control**

/OE	SEL1	SEL0	Function
1	X	X	All Switch Paths Open
0	0	1	D+ = HSD0+, D- = HSD0-
0	1	0	D+ = HSD1+, D- = HSD1-
0	1	1	D+ = HSD2+, D- = HSD2-
0	0	0	All Switch Paths Open

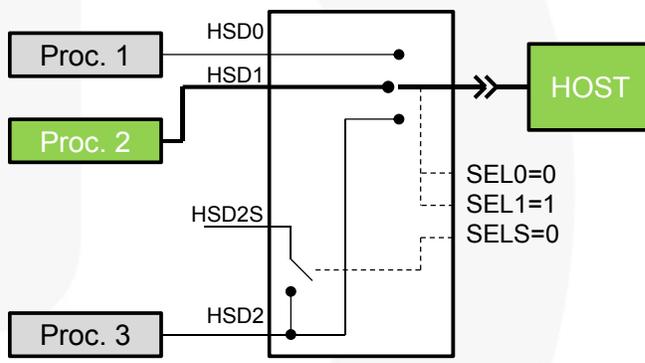
**Table 2. Isolation Switch Control**

SELS	Function
0	HSD2S+ = Open, HSD2S- = Open
1	HSD2S+ = HSD2+, HSD2S- = HSD2-

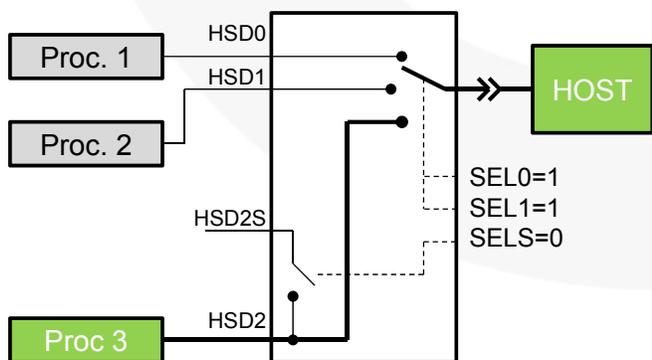
## Functionality



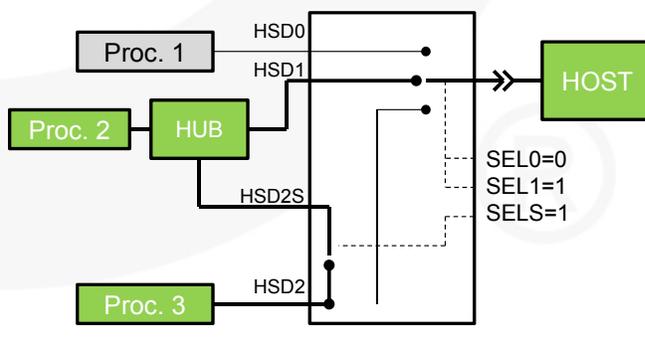
**Figure 4. Typical USB Application 1**



**Figure 5. Typical USB Application 2**



**Figure 6. Typical USB Application 3**



**Figure 7. Loopback USB Application**

## Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Min.	Max.	Unit	
V <sub>CC</sub>	Supply Voltage	-0.50	5.25	V	
V <sub>CNTRL</sub>	DC Input Voltage (SEL1, SEL0, /OE, SELS) <sup>(1)</sup>	-0.5	V <sub>CC</sub>	V	
V <sub>SW</sub>	DC Switch I/O Voltage <sup>(1)</sup>	-0.50	5.25	V	
I <sub>IK</sub>	DC Input Diode Current	-50		mA	
T <sub>STG</sub>	Storage Temperature	-65	+150	°C	
MSL	Moisture Sensitivity Level (JEDEC J-STD-020A)		1	Level	
ESD	IEC61000-4-2 System on USB Connector Pins D+ & D-	Air Gap	15		kV
		Contact	8		
	Human Body Model, JEDEC: JESD22-A114	D+, D- to GND	6		
		Power to GND	12		
		All Other Pins	2		

**Note:**

- The input and output negative ratings may be exceeded if the input and output diode current ratings are observed.

## Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Min.	Max.	Unit
V <sub>CC</sub>	Supply Voltage	2.5	4.4	V
V <sub>CNTRL</sub>	Control Input Voltage (SEL1, SEL0, /OE, and SELS) <sup>(2)</sup>	0	V <sub>CC</sub>	V
V <sub>SW</sub>	Switch I/O Voltage	-0.5	4.4	V
T <sub>A</sub>	Operating Temperature	-40	+85	°C

**Note:**

- The control input must be held HIGH or LOW; it must not float.

## DC Electrical Characteristics

All typical values are for  $V_{CC}=3.3V$  at  $T_A=25^{\circ}C$  unless otherwise specified.

Symbol	Parameter	Conditions	$V_{CC}$ (V)	$T_A=-40^{\circ}C$ to $+85^{\circ}C$			Unit
				Min.	Typ.	Max.	
$R_{ON}$	HS Switch On Resistance <sup>(3)</sup>	$V_{SW}=0.4V$ , $I_{ON}=-8mA$ , Figure 8	3.3		6.5	9.0	$\Omega$
$\Delta R_{ON}$	HS Delta $R_{ON}$ <sup>(4,3)</sup>	$V_{SW}=0.4V$ , $I_{ON}=-8mA$	3.3		0.5		$\Omega$
$I_{IN}$	Control Input Leakage	All Combinations of /OE, SELS, SEL1, SEL0 in Truth Tables (Table 1, Table 2) ( $1=V_{CC}$ , $0=0V$ )	4.4	-1		1	$\mu A$
$I_{OZ}$	Off State Leakage	$0 \leq D_n$ , HSD0n, HSD1n, HSD2n, HSD3n, HSD2Sn $\leq 4.4V$	4.4	-1		1	$\mu A$
$I_{OFF}$	Power-Off Leakage Current (All I/O Ports)	$V_{SW}=0V$ to $4.4V$ , $V_{CC}=0V$ , Figure 9	0	-1		1	$\mu A$
$I_{CCSLP}$	Sleep Mode Supply Current	All Disabled Conditions in Truth Tables (Table 1, Table 2)	4.4			1	$\mu A$
$I_{CCACT}$	Active Mode Supply Current	All Active Modes in Truth Tables (Table 1, Table 2)	4.4		9	18	$\mu A$
$I_{CCT}$	Increase in $I_{CC}$ Current per Control Input and $V_{CC}$	$V_{CTRL}=1.8V$	4.4		3.3	4.0	$\mu A$
		$V_{CTRL}=1.2V$	4.4		4.9	6.0	$\mu A$
$V_{IK}$	Clamp Diode Voltage	$I_{IN}=-18mA$	2.5			-1.2	V
$V_{IH}$	Control Input Voltage HIGH	SEL1, SEL0, /OE, SELS	2.5 to 4.4	1.0			V
$V_{IL}$	Control Input Voltage LOW	SEL1, SEL0, /OE, SELS	2.5 to 4.4			0.35	V

### Notes:

- Measured by the voltage drop between HSDn and Dn pins at the indicated current through the switch. On resistance is determined by the lower of the voltage on the two (HSDn or Dn ports).
- Guaranteed by characterization.

## AC Electrical Characteristics

All typical values are for  $V_{CC}=3.3V$  at  $T_A=25^{\circ}C$  unless otherwise specified.

Symbol	Parameter	Conditions	$V_{CC}$ (V)	$T_A=-40^{\circ}C$ to $+85^{\circ}C$			Unit
				Min.	Typ.	Max.	
$t_{ON}$	Turn-On Time when Switching from One USB Path (or Disabled i.e. /OE=1) to Another USB Path	$R_L=50\Omega$ , $C_L=35pF$ , $V_{SW}=0.8V$ , Figure 10, Figure 11	2.5 to 4.4	126		400	$\mu s$
$t_{OFF}$	Turn-Off Time, Turning Off Any of the USB Paths	$R_L=50\Omega$ , $C_L=35pF$ , $V_{SW}=0.8V$ , Figure 10, Figure 11	2.5 to 4.4			80	ns
$t_{PD}$	Propagation Delay <sup>(5)</sup>	$C_L=5pF$ , $R_L=50\Omega$ , Figure 10, Figure 12	3.3		0.25		ns
$t_{RF}$	Slow Turn on/off Switch Paths <sup>(5)</sup>	$C_L=5pF$ , Dn at 0V or 3.6V, 40.5 $\Omega$ in Series with Switch 10% to 90%	3.3		4.5		ns
$t_{BBM}$	Break-Before-Make Time <sup>(5)</sup>	$R_L=50\Omega$ , $C_L=35pF$ , $V_{SW1}=V_{SW2}=0.8V$ , Figure 14	2.5 to 4.4	126		400	$\mu s$
$O_{IRR}$	Off Isolation <sup>(5)</sup>	$R_L=50\Omega$ , $f=240MHz$ , Figure 16	2.5 to 4.4		-40		dB
Xtalk	Channel-to-Channel Crosstalk <sup>(5)</sup>	$R_L=50\Omega$ , $f=240MHz$ , Figure 17	2.5 to 4.4		-40		dB
$t_{SK(P)}$	Pulse Skew <sup>(5)</sup>	$V_{SW}=0.2V_{diffPP}$ , Figure 13, $C_L=5pF$	2.5 to 4.4		25		ps
$t_{SK(I)}$	Skew Between Differential Signals within a Pair <sup>(5)</sup>	$V_{SW}=0.2V_{diffPP}$ , Figure 13, $C_L=5pF$	2.5 to 4.4		25		ps

### Note:

5. Guaranteed by characterization.

## Capacitance Characteristics

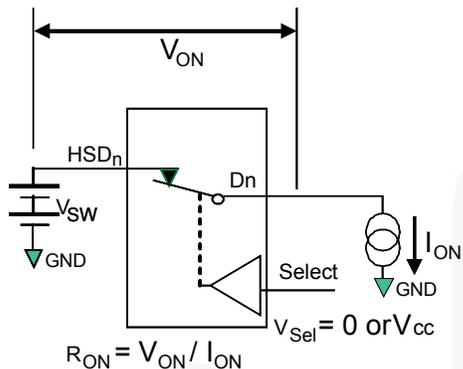
All typical values are for  $V_{CC}=3.3V$  at  $T_A=25^{\circ}C$  unless otherwise specified.

Symbol	Parameter	Conditions	$V_{CC}$ (V)	$T_A=-40^{\circ}C$ to $+85^{\circ}C$	Unit
				Typ.	
$C_{IN}$	Input Capacitance <sup>(6)</sup>		0	3.0	pF
$C_{ONa}$	D+/D- On Capacitance <sup>(6)</sup>	HSD0 or HSD1 path, $f=1MHz$ , Figure 19	3.3	7.2	pF
$C_{ONb}$	D+/D- On Capacitance <sup>(6)</sup>	HSD2 path, $f=1MHz$ , Figure 19	3.3	7.7	pF
$C_{ONc}$	D+/D- On Capacitance <sup>(6)</sup>	HSD2S to HSD2S path, $f=1MHz$ , Figure 19	3.3	5.4	pF
$C_{OFF}$	HSD0n, HSD1n, HSD2Sn, HSD3n Off Capacitance <sup>(6)</sup>	If $V_{CC}=3.3V$ , then /OE=3.3V, $f=1MHz$ , Figure 18	0 or 3.3	2.2	pF

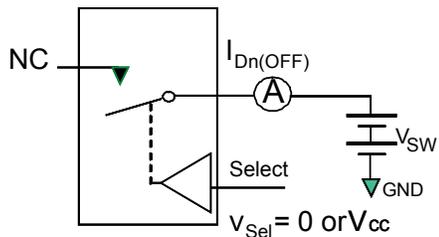
### Note:

6. Guaranteed by characterization

### Test Diagrams

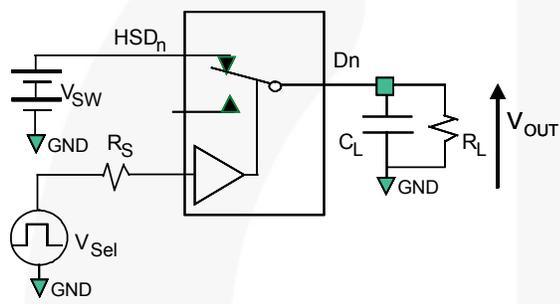


**Figure 8. On Resistance**



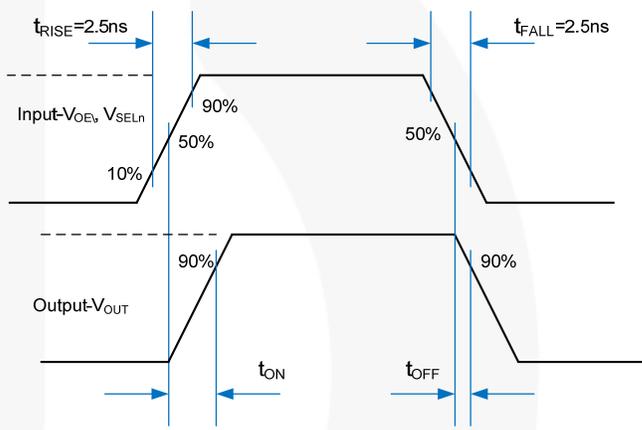
\*\*Each switch port is tested separately

**Figure 9. Off Leakage**

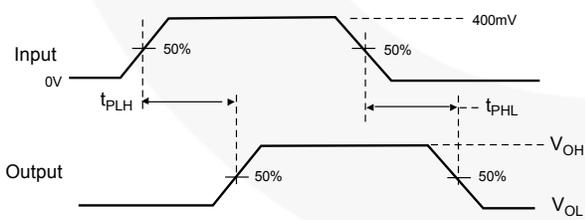


$R_L$ ,  $R_S$ , and  $C_L$  are functions of the application environment (see AC Tables for specific values)  
 $C_L$  includes test fixture and stray capacitance.

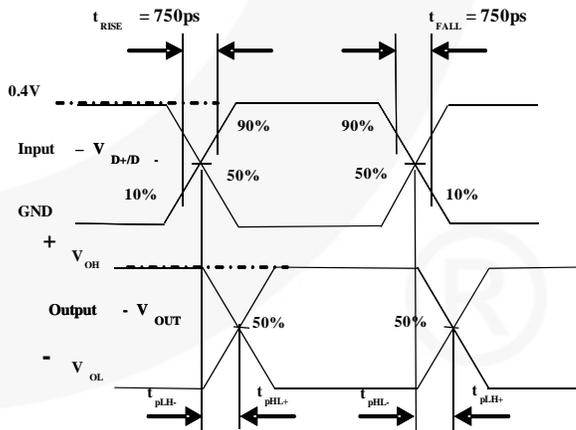
**Figure 10. AC Test Circuit Load**



**Figure 11. Turn-On / Turn-Off Waveforms**

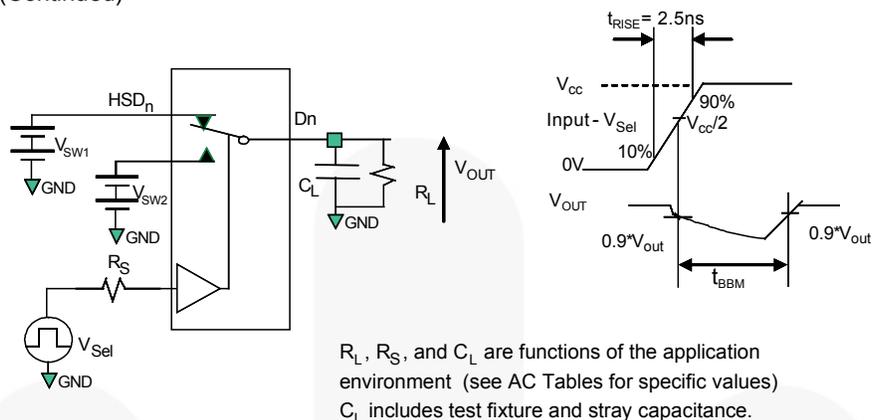


**Figure 12. Propagation Delay ( $t_{rtf} = 500ps$ )**

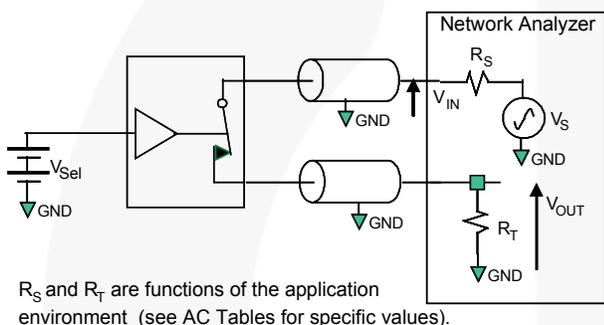


**Figure 13. Skew Test Waveforms**  
 $t_{SK(P)} = |t_{pLH-} - t_{pLH+}|$  OR  $|t_{pLH+} - t_{pLH-}|$   
 $t_{SK(I)} = |t_{pLH-} - t_{pLH+}|$  OR  $|t_{pLH+} - t_{pLH-}|$

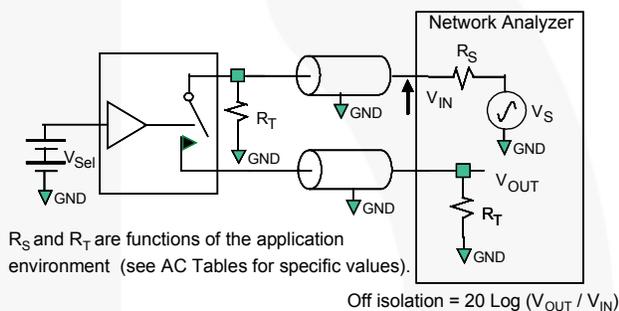
**Test Diagrams (Continued)**



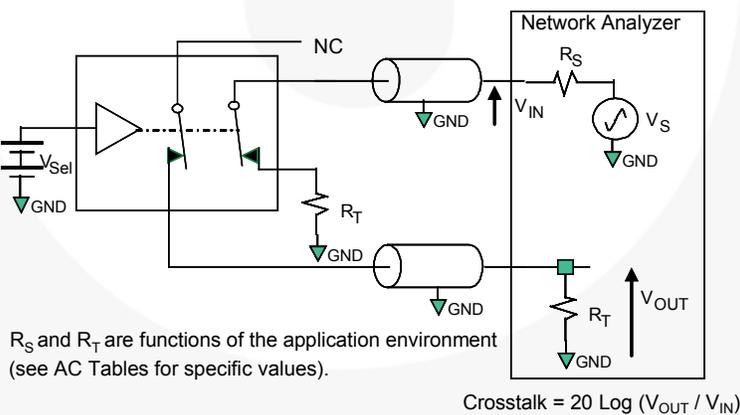
**Figure 14. Break-Before-Make Interval Timing**



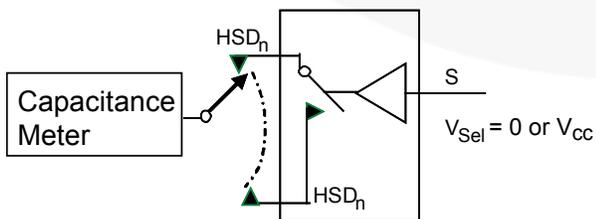
**Figure 15. Bandwidth**



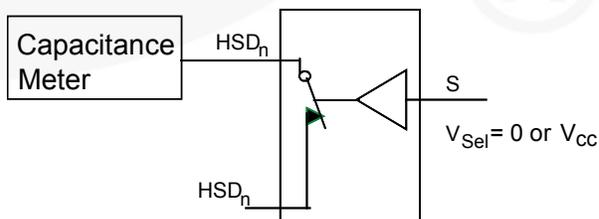
**Figure 16. Channel-Off Isolation**



**Figure 17. Non-Adjacent Channel-to-Channel Crosstalk**

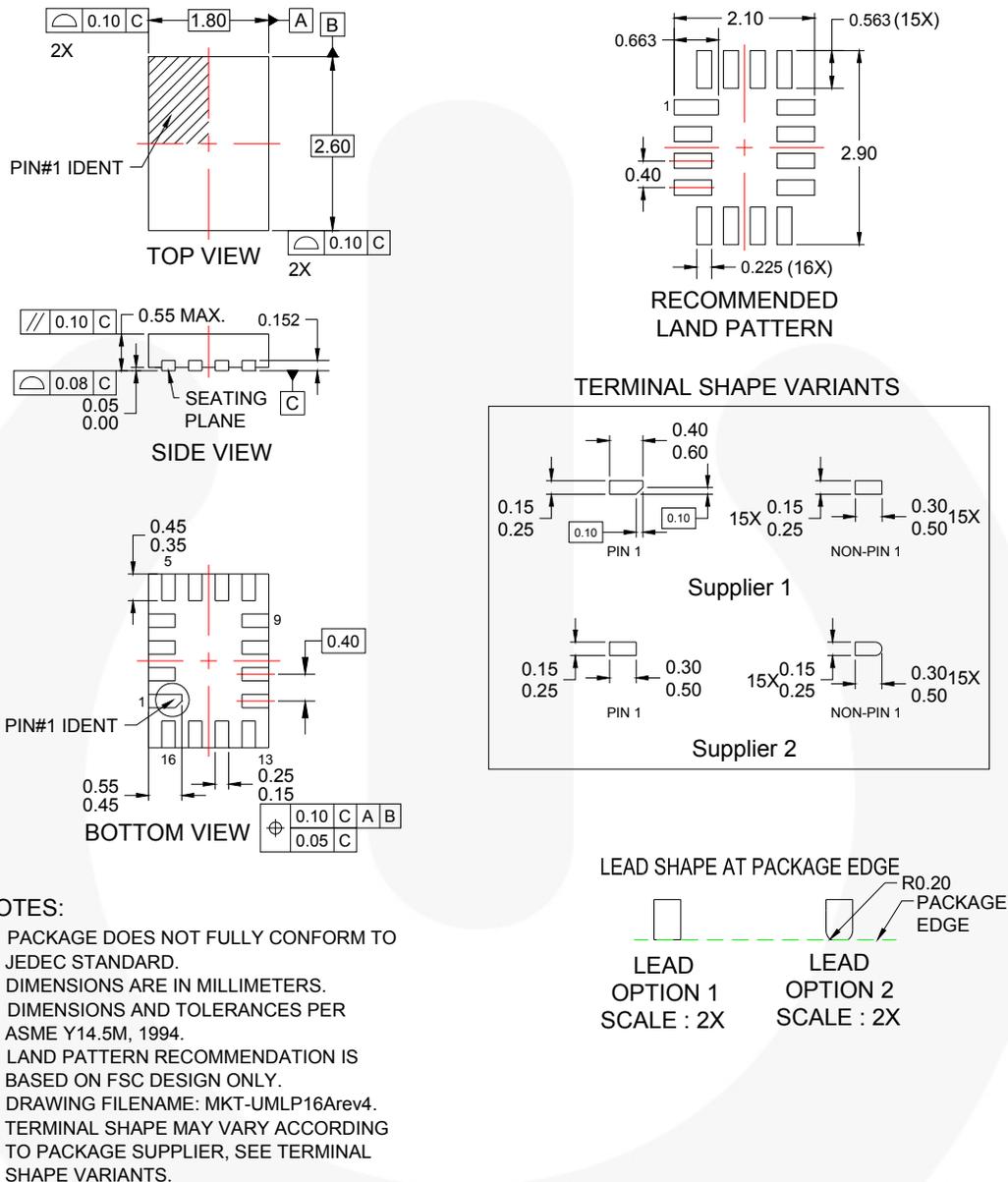


**Figure 18. Channel Off Capacitance**



**Figure 19. Channel On Capacitance**

### Physical Dimensions



**Figure 20. 16-Pin Ultrathin Molded Leadless Package (UMLP)**

Order Number	Operating Temperature Range	Package Description	Packing Method
FSUSB73UMX	-40 to 85°C	16-Terminal Ultrathin Molded Leadless Package (UMLP)	Tape & Reel

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