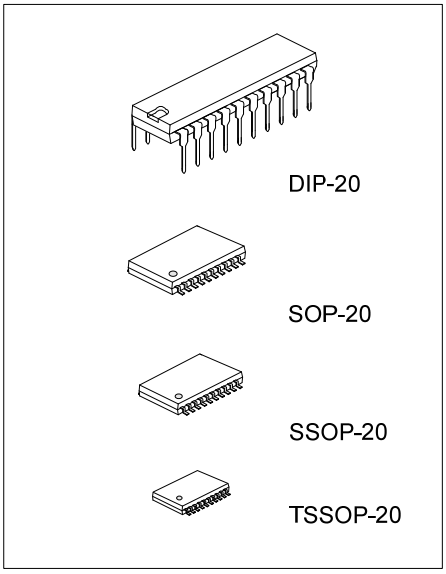
U74HC273

CMOS IC

OCTAL D-TYPE FLIP-FLOPS WITH CLEAR



■ DESCRIPTION

The **U74HC273** devices are positive-edge-triggered D-type flip-flops with a direct active low clear (CLR) input.

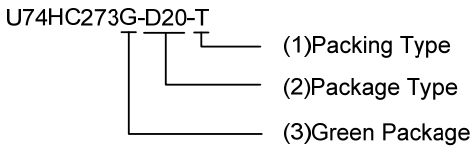
Information at the data (D) inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock (CLK) pulse. Clock triggering occurs at a particular voltage level and is not related directly to the transition time of the positive-going pulse. When CLK is at either the high or low level, the D input has no effect at the output.

■ FEATURES

* Wide Operating Voltage Range of 2 V to 6 V
* Low Power Consumption, 80-μA Maximum ICC
*Typical t_{PD} = 12 ns
* ±4mA Output Drive at 5 V
* Low Input Current of 1 μA Maximum
* Contain Eight Flip-Flops With Single-Rail Outputs
* Direct Clear Input
* Individual Data Input to Each Flip-Flop

■ ORDERING INFORMATION

Ordering Number		Package	Packing
Lead Free	Halogen Free		
U74HC273L-D20-T	U74HC273G-D20-T	DIP-20	Tube
U74HC273L-P20-R	U74HC273G-P20-R	TSSOP-20	Tape Reel
U74HC273L-R20-R	U74HC273G-R20-R	SSOP-20	Tape Reel
U74HC273L-S20-R	U74HC273G-S20-R	SOP-20	Tape Reel

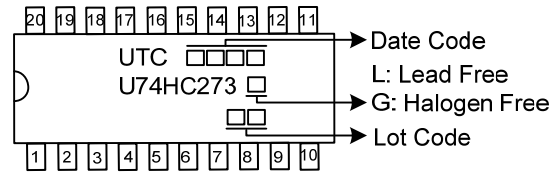
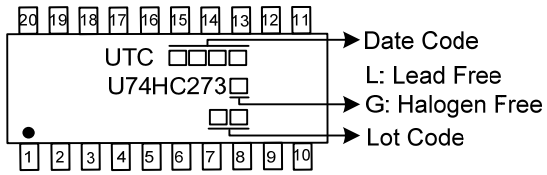


(1) T: Tube, R: Tape Reel

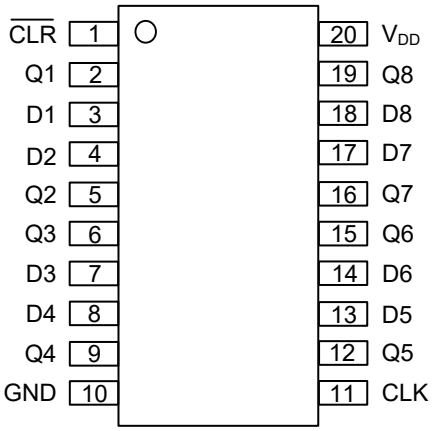
(2) D20: DIP-20, P20: TSSOP-20, R20: SSOP-20, S20: SOP-20

(3) G: Halogen Free and Lead Free, L: Lead Free

■ MARKING

DIP-20	SOP-20 / SSOP-20 / TSSOP-20
	

■ PIN CONFIGURATION

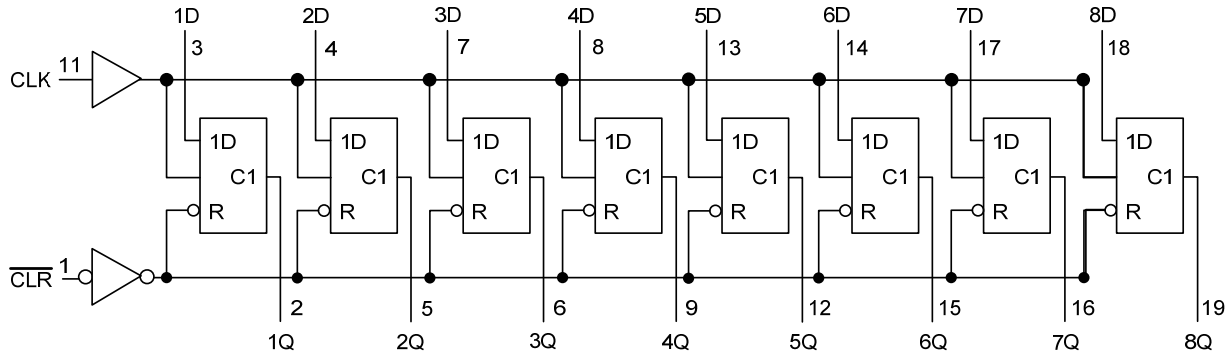


■ FUNCTION TABLE

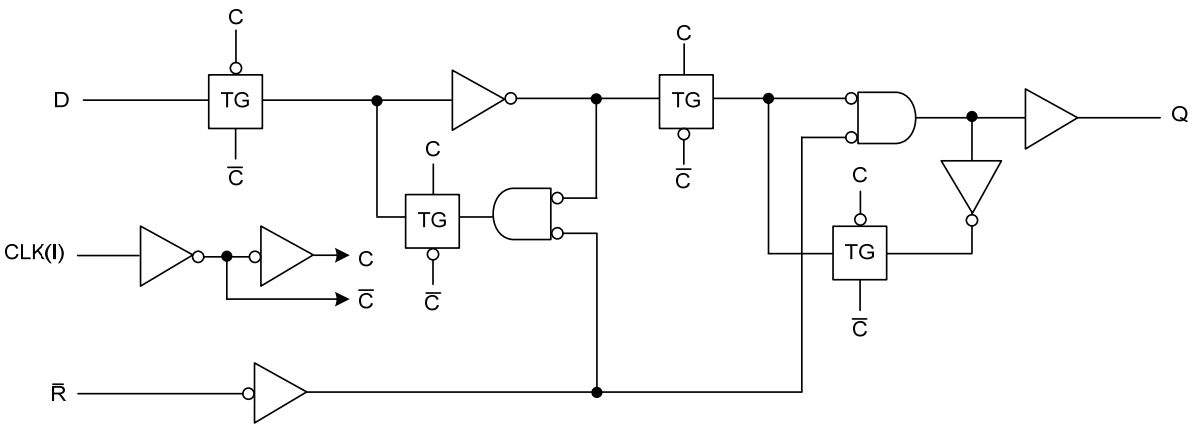
INPUTS			OUTPUT
$\overline{CLR}$	CLK	D	Q
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	Q_0

H = High voltage level；L = Low voltage level；X = Don't care

■ FUNCTIONAL BLOCK DIAGRAM



■ LOGIC DIAGRAM, EACH FLIP-FLOP (POSITIVE LOGIC)



■ ABSOLUTE MAXIMUM RATING (T_A=25°C, unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	RATINGS	UNIT
Supply Voltage	V_{CC}		-0.5 ~ 7	V
Continuous Output Current	I_{OUT}	V_{OUT}=0 ~ V_{CC}	±25	mA
Input Clamp Current	I_{IK}	V_{IN}<0 or V_{IN}>V_{CC}	±20	mA
Output Clamp Current	I_{OK}	V_{IN}<0 or V_{OUT}>V_{CC}	±20	mA
Storage Temperature Range	T_{STG}		-65 ~ +150	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ RECOMMENDED OPERATING COMDITIONS

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage	V_{CC}		2	5	6	V
High-Level Input Voltage	V_{IH}	V_{CC}=2V	1.5			V
		V_{CC}=4.5V	3.15			V
		V_{CC}=6V	4.2			V
Low-Level Input Voltage	V_{IL}	V_{CC}=2V			0.5	V
		V_{CC}=4.5V			1.35	V
		V_{CC}=6V			1.8	V
Input Voltage	V_{IN}		0		V_{CC}	V
Output Voltage	V_{OUT}		0		V_{CC}	V
Input Transition Rise or Fall Rate	$\Delta t/\Delta v$	V_{CC}=2V			1000	ns/V
		V_{CC}=4.5V			500	ns/V
		V_{CC}=6V			400	ns/V
Operating Temperature	T_A		-40		+125	°C

■ ELECTRICAL CHARACTERISTICS (Unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	T_A=25°C			T_A=-40~+125°C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
High-Level Output Voltage	V_{OH}	V_{CC}=2V, I_{OH}=-20μA	1.9	1.998		1.9			V
		V_{CC}=4.5V, I_{OH}=-20μA	4.4	4.499		4.4			V
		V_{CC}=6V, I_{OH}=-20μA	5.9	5.999		5.9			V
		V_{CC}=4.5V, I_{OH}=-4mA	3.98	4.3		3.7			V
		V_{CC}=6V, I_{OH}=-5.2mA	5.48	5.8		5.2			V
Low-Level Output Voltage	V_{OL}	V_{CC}=2V, I_{OL}=20μA		0.002	0.1			0.1	V
		V_{CC}=4.5V, I_{OL}=20μA		0.001	0.1			0.1	V
		V_{CC}=6V, I_{OL}=20μA		0.001	0.1			0.1	V
		V_{CC}=4.5V, I_{OL}=4mA		0.17	0.26			0.4	V
		V_{CC}=6V, I_{OL}=5.2mA		0.15	0.26			0.4	V
Input Leakage Current	$I_{I(LEAK)}$	V_{CC}=6V, V_I=V_{CC} or 0		±0.1	±100			±100	μA
Quiescent Supply Current	I_{CC}	V_{CC}=6V, V_I=V_{CC} or 0, I_{OUT}=0			8			160	μA

■ SWITCHING CHARACTERISTICS (C_L=50pF, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	T_A=25°C			T_A=-40~+125°C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Maximum clock pulse frequency	f_{MAX}	V_{CC}=2.0V	5	11		4			MHz
		V_{CC}=4.5V	27	50		20			MHz
		V_{CC}=6.0V	32	60		24			MHz
Propagation delay from input ($\overline{CLR}$) to output (Any)	t_{PHL}	V_{CC}=2.0V		55	160			225	ns
		V_{CC}=4.5V		15	32			45	ns
		V_{CC}=6.0V		12	27			38	ns
Propagation delay from input (CLK) to output (Any)	t_{PD}	V_{CC}=2.0V		56	160			225	ns
		V_{CC}=4.5V		15	32			45	ns
		V_{CC}=6.0V		13	27			38	ns
Propagation delay to output (Any)	t_t	V_{CC}=2.0V		38	75			110	ns
		V_{CC}=4.5V		8	15			22	ns
		V_{CC}=6.0V		6	13			19	ns

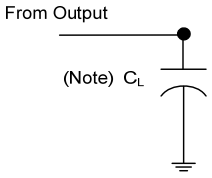
■ TIMING REQUIREMENTS (Input: t_R, t_F≤2.5ns; PRR≤1MHz)

PARAMETER		SYMBOL	Conditions	T_A=25°C			T_A=-40~+125°C			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
Clock frequency		f_{CLOCK}	V_{CC}= 2V			5			4	MHZ
			V_{CC}=4.5V			27			20	MHZ
			V_{CC}=6V			32			24	MHZ
Pulse duration	CLK high or low	t_W	V_{CC}= 2V		80		120			ns
			V_{CC}=4.5V		16		24			ns
			V_{CC}=6V		14		20			ns
	$\overline{CLR}$ low		V_{CC}= 2V		80		120			ns
			V_{CC}=4.5V		16		24			ns
			V_{CC}=6V		14		20			ns
Setup time before CLK↑	Data	t_{SU}	V_{CC}= 2V		100		120			ns
			V_{CC}=4.5V		20		24			ns
			V_{CC}=6V		17		20			ns
	$\overline{CLR}$ inactive		V_{CC}= 2V		100		120			ns
			V_{CC}=4.5V		20		24			ns
			V_{CC}=6V		17		20			ns
Hold time ,data after CLK↑		t_H	V_{CC}= 2V		0		-6			ns
			V_{CC}=4.5V		0		-2			ns
			V_{CC}=6V		0		-2			ns

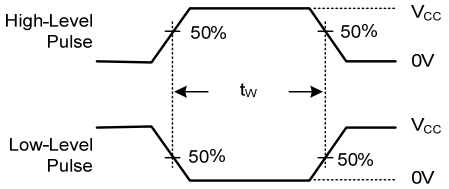
■ OPERATING CHARACTERISTICS (T_A=25°C , unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input Capacitance	C_I	V_{CC}=2V~6V		3	10	pF
Power Dissipation Capacitance per flip-flop	C_{PD}	No load.		35		pF

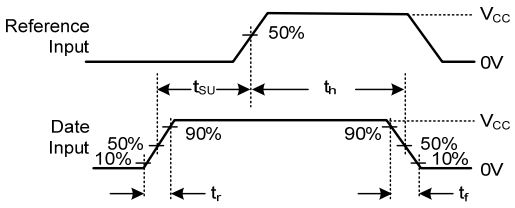
■ TEST CIRCUIT AND WAVEFORMS



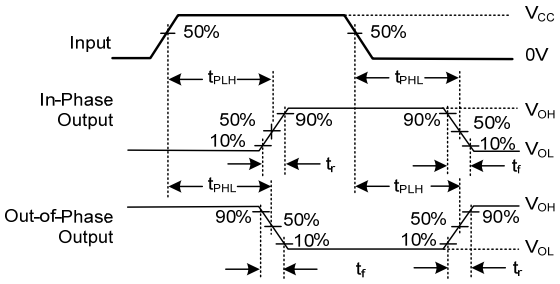
Load Circuit



Voltage Waveforms Pulse Durations



Voltage Waveforms Setup and Hold Times



Voltage Waveforms Propagation Delay and Output Transition Times

Notes: 1. C_L includes probe and jig capacitance.
2. All input pulses are supplied by generators having the following characteristics: PRR ≤1MHz, Z_O = 50Ω, t_r = 6 ns, t_f = 6 ns.
3. For clock inputs, fmax is measured when the input duty cycle is 50%.
4. The outputs are measured one at a time with one input transition per measurement.