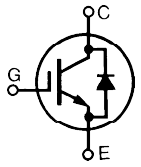
IXYS

High Voltage, High Gain BIMOSFET™

IXBF55N300

V_{CES} = 3000V
I_{C110} = 34A
$V_{CE(sat)} \leq$ 3.2V

Monolithic Bipolar MOS Transistor

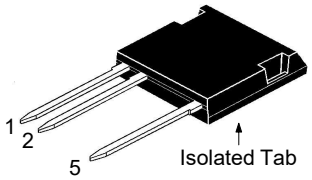


(Electrically Isolated Tab)

Symbol	Test Conditions	Maximum Ratings	
V_{CES}	T_C = 25°C to 150°C	3000	V
V_{CGR}	T_J = 25°C to 150°C, R_{GE} = 1MΩ	3000	V
V_{GES}	Continuous	± 25	V
V_{GEM}	Transient	± 35	V
I_{C25}	T_C = 25°C	86	A
I_{C110}	T_C = 110°C	34	A
I_{CM}	T_C = 25°C, 1ms	600	A
SSOA (RBSOA)	V_{GE} = 15V, T_{VJ} = 125°C, R_G = 2Ω Clamped Inductive Load	I_{CM} = 110 1500	A V
T_{SC} **(SCSOA)**	V_{GE} = 15V, T_J = 125°C, R_G = 10Ω, V_{CE} = 1250V, Non-Repetitive	10	µs
P_C	T_C = 25°C	357	W
T_J		-55 ... +150	°C
T_{JM}		150	°C
T_{stg}		-55 ... +150	°C
T_L	Maximum Lead Temperature for Soldering 1.6 mm (0.062 in.) from Case for 10s	300	°C
F_C	Mounting Force	20..120 / 4.5..27	N/lb
V_{ISOL}	50/60Hz, 1 Minute	4000	V~
Weight		5	g

Symbol	Test Conditions (T_J = 25°C Unless Otherwise Specified)	Characteristic Values Min.	Typ.	Max.	
BV_{CES}	I_C = 1mA, V_{GE} = 0V	3000			V
$V_{GE(th)}$	I_C = 4mA, V_{CE} = V_{GE}	3.0		5.0	V
I_{CES}	V_{CE} = V_{CES}, V_{GE} = 0V			50	µA
	Note 2, T_J = 125°C			3	mA
I_{GES}	V_{CE} = 0V, V_{GE} = ± 25V			±200	nA
$V_{CE(sat)}$	I_C = 55A, V_{GE} = 15V, Note 1		2.7	3.2	V
	T_J = 125°C		3.3		V

ISOPLUS i4-Pak™



1 = Gate 5 = Collector
2 = Emitter

Features

- Silicon Chip on Direct-Copper Bond (DCB) Substrate
- Isolated Mounting Surface
- 4000V~ Electrical Isolation
- High Blocking Voltage
- High Peak Current Capability
- Low Saturation Voltage

Advantages

- Low Gate Drive Requirement
- High Power Density

Applications

- Switch-Mode and Resonant-Mode Power Supplies
- Uninterruptible Power Supplies (UPS)
- Laser Generators
- Capacitor Discharge Circuits
- AC Switches

Symbol	Test Conditions (T_J = 25°C Unless Otherwise Specified)	Characteristic Values Min.	Typ.	Max.
g_{fs}	I_C = 55A, V_{CE} = 10V, Note 1	32	50	S
C_{ies}	V_{CE} = 25V, V_{GE} = 0V, f = 1MHz		7300	pF
C_{oes}			275	pF
C_{res}			83	pF
Q_g	I_C = 55A, V_{GE} = 15V, V_{CE} = 1000V		335	nC
Q_{ge}			47	nC
Q_{gc}			130	nC
$t_{d(on)}$	**Resistive Switching Times, T_J = 25°C**		54	ns
t_r	I_C = 110A, V_{GE} = 15V		307	ns
$t_{d(off)}$	V_{CE} = 1250V, R_G = 2Ω		230	ns
t_f			268	ns
$t_{d(on)}$	**Resistive Switching Times, T_J = 125°C**		52	ns
t_r	I_C = 110A, V_{GE} = 15V		585	ns
$t_{d(off)}$	V_{CE} = 1250V, R_G = 2Ω		215	ns
t_f			260	ns
R_{thJC}				0.35 °C/W
R_{thCS}			0.15	°C/W

Reverse Diode

Symbol	Test Conditions (T_J = 25°C Unless Otherwise Specified)	Characteristic Values Min.	Typ.	Max	
V_F	I_F = 55A, V_{GE} = 0V, Note 1			2.5	V
t_{rr}	I_F = 28A, V_{GE} = 0V, $-di_F/dt$ = 100A/μs		1.9		μs
I_{RM}	V_R = 100V, V_{GE} = 0V		54		A

Notes:

1. Pulse test, t < 300μs, duty cycle, d < 2%.
2. Device must be heatsunk for high-temperature leakage current measurements to avoid thermal runaway.

Additional provisions for lead-to-lead isolation are required at V_{CE} > 1250V.

Fig. 1. Output Characteristics @ T_J = 25ºC

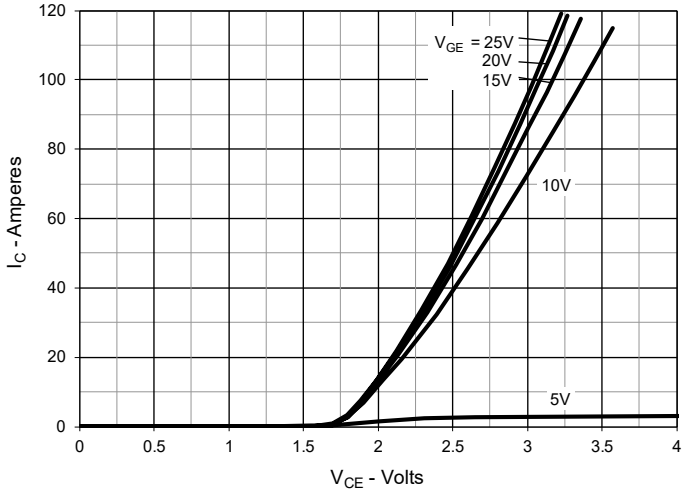


Fig. 2. Extended Output Characteristics @ T_J = 25ºC

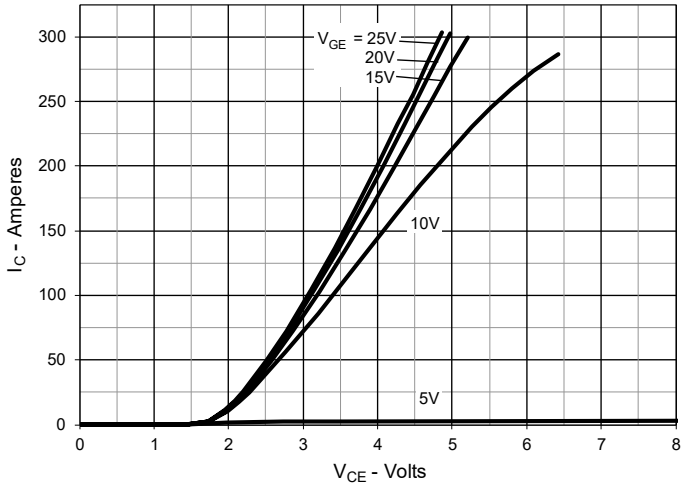


Fig. 3. Output Characteristics @ T_J = 125ºC

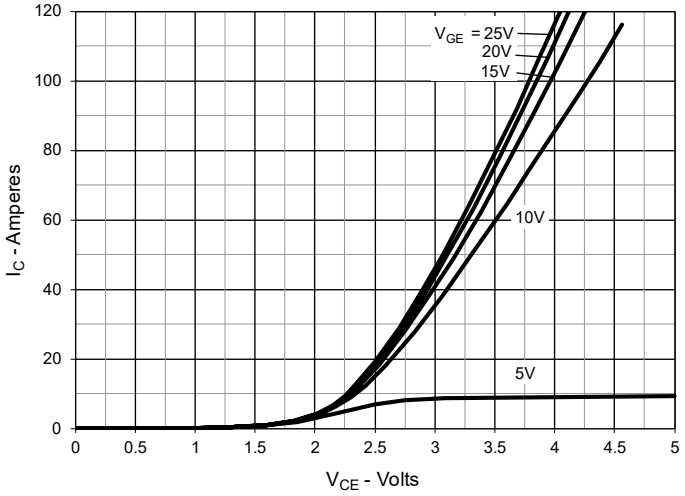


Fig. 4. Dependence of $V_{CE(sat)}$ on Junction Temperature

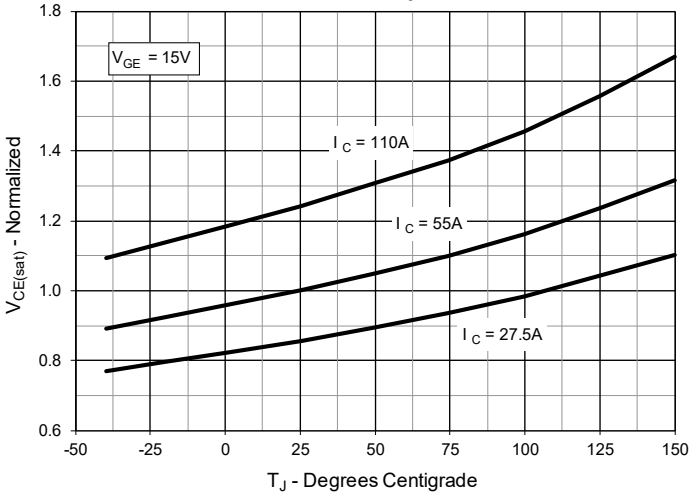


Fig. 5. Collector-to-Emitter Voltage vs. Gate-to-Emitter Voltage

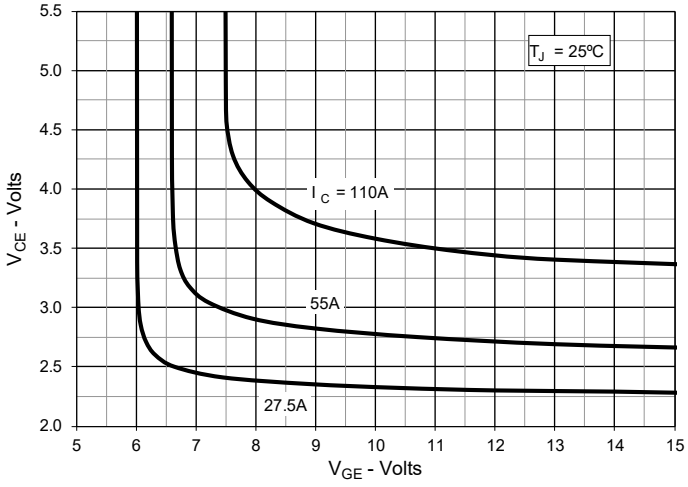


Fig. 6. Input Admittance

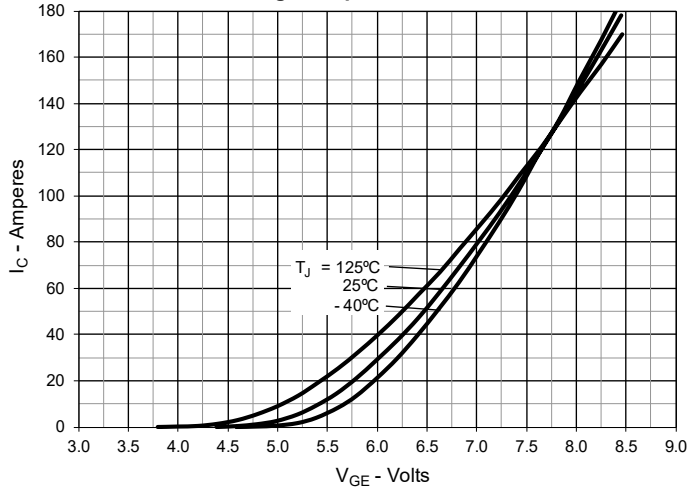


Fig. 7. Transconductance

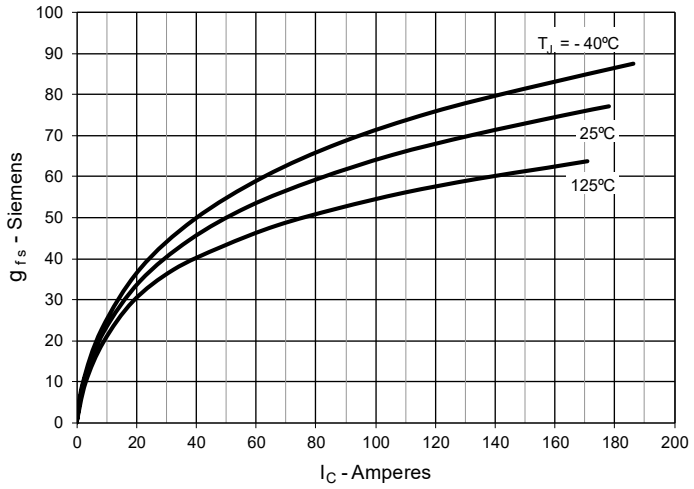


Fig. 8. Forward Voltage Drop of Intrinsic Diode

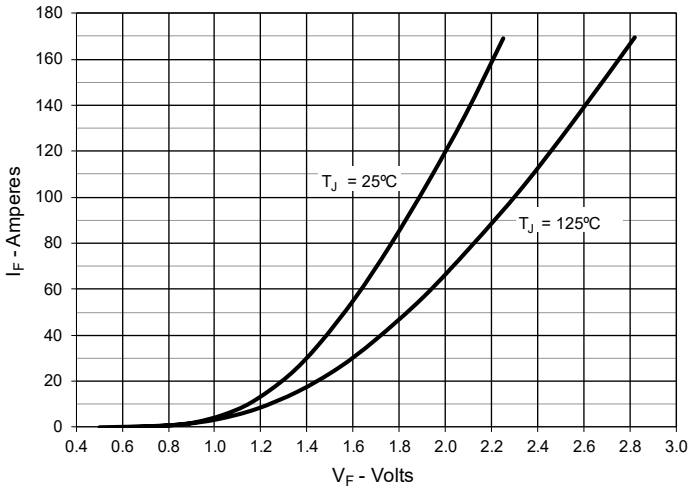


Fig. 9. Gate Charge

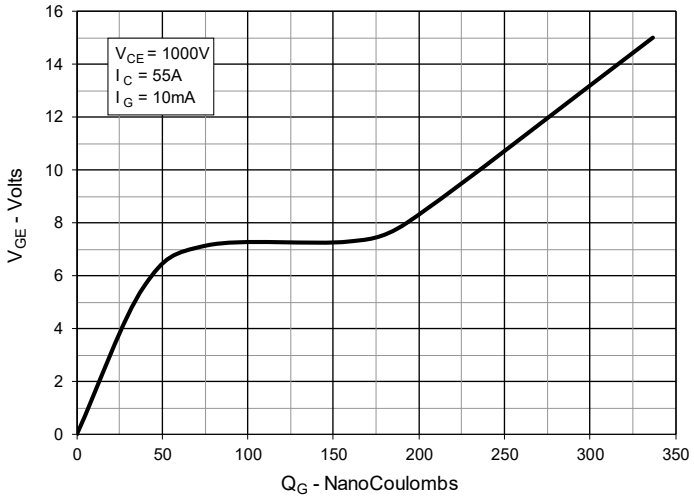


Fig. 10. Capacitance

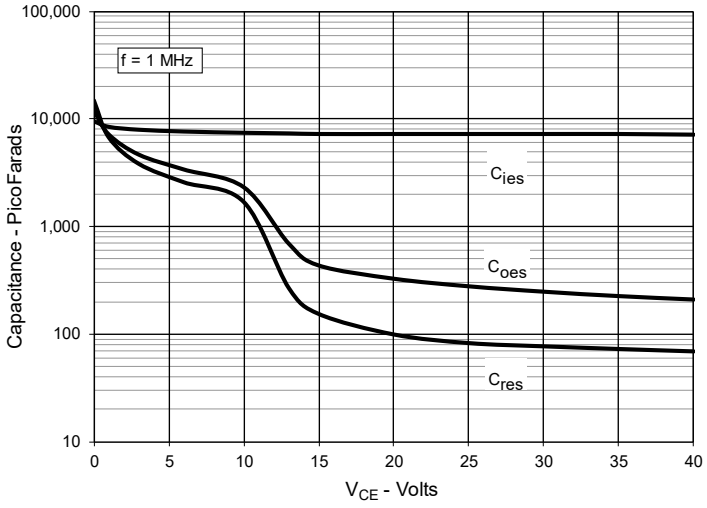


Fig. 11. Reverse-Bias Safe Operating Area

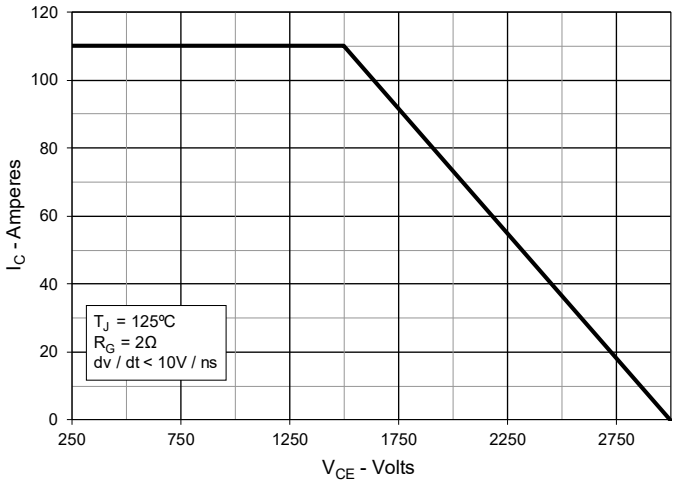


Fig. 12. Maximum Transient Thermal Impedance

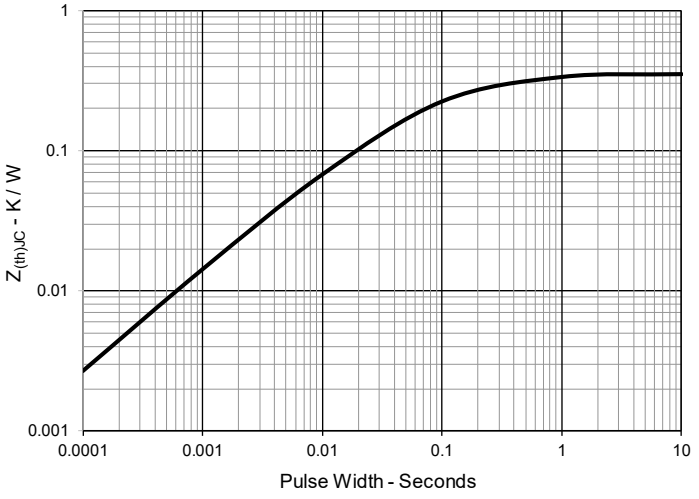


Fig. 13. Resistive Turn-on Rise Time vs. Junction Temperature

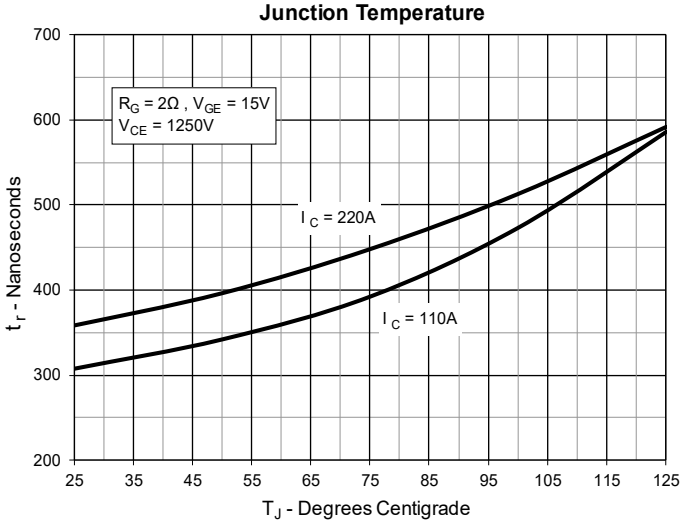


Fig. 14. Resistive Turn-on Rise Time vs. Collector Current

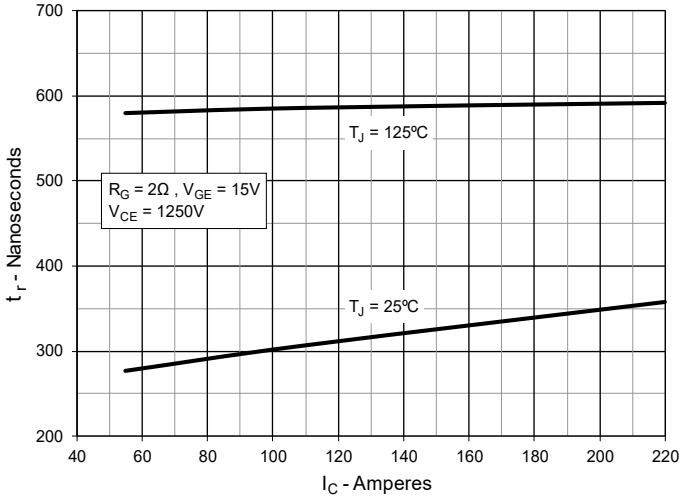


Fig. 15. Resistive Turn-on Switching Times vs. Gate Resistance

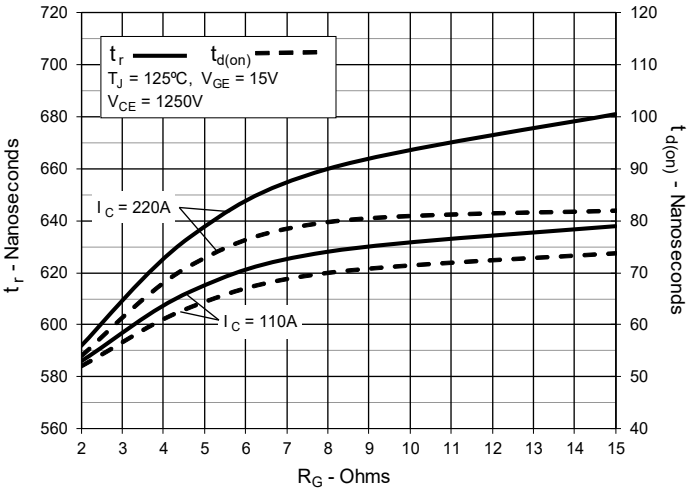


Fig. 16. Resistive Turn-off Switching Times vs. Junction Temperature

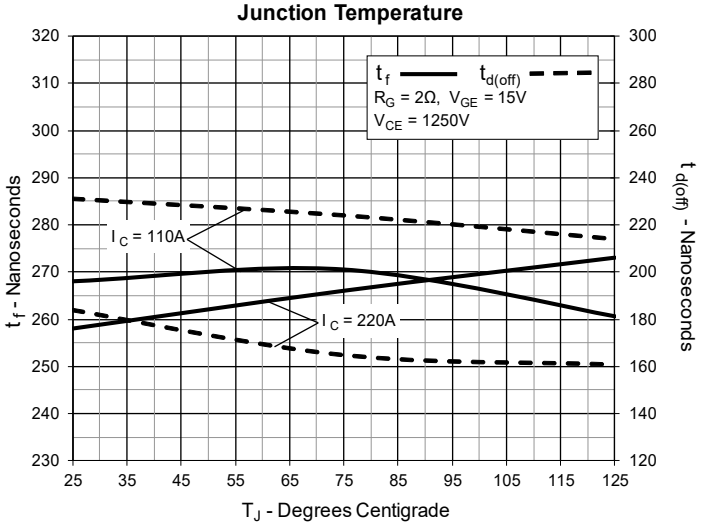


Fig. 17. Resistive Turn-off Switching Times vs. Collector Current

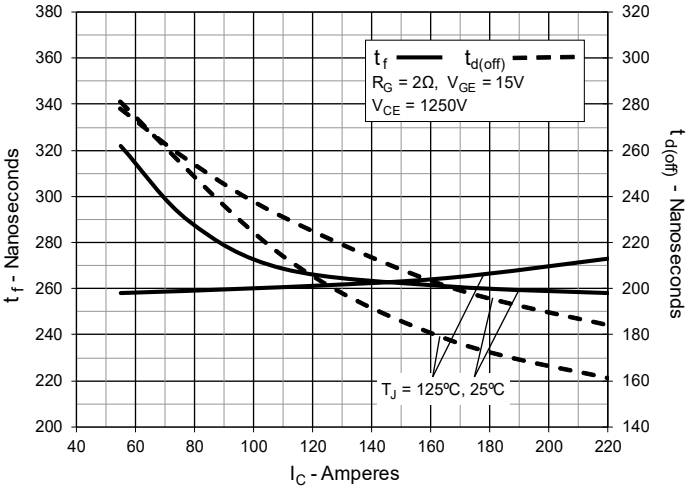


Fig. 18. Resistive Turn-off Switching Times vs. Gate Resistance

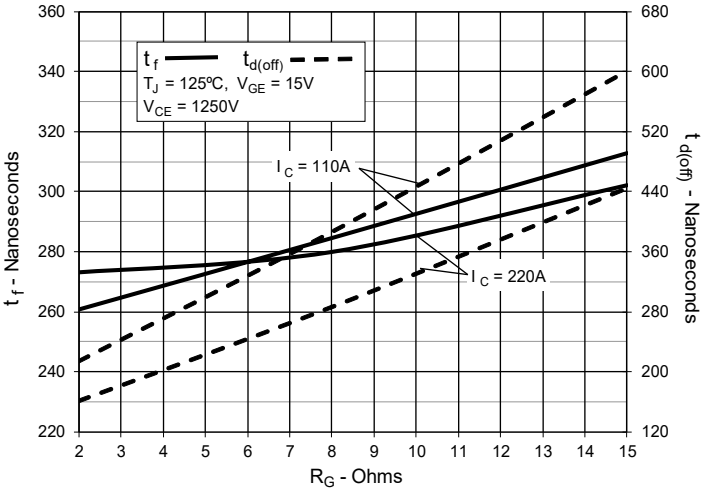


Fig. 19. Forward-Bias Safe Operating Area @ T_C = 25ºC

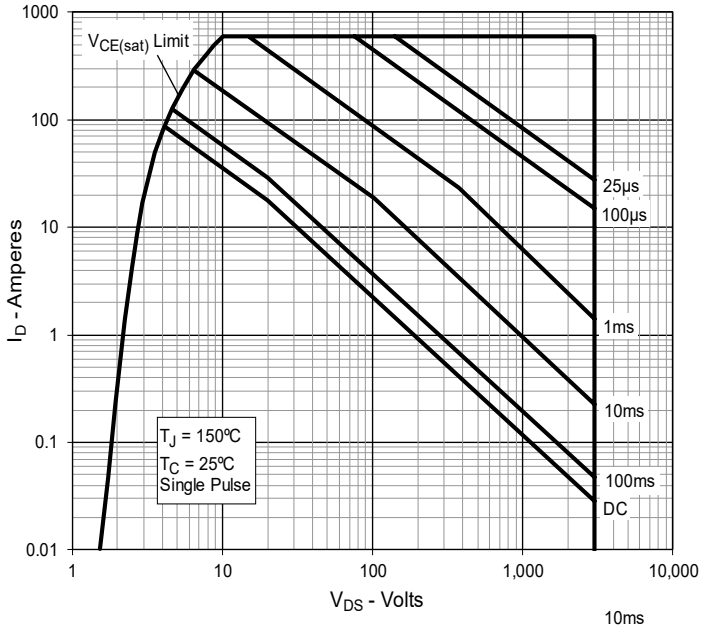
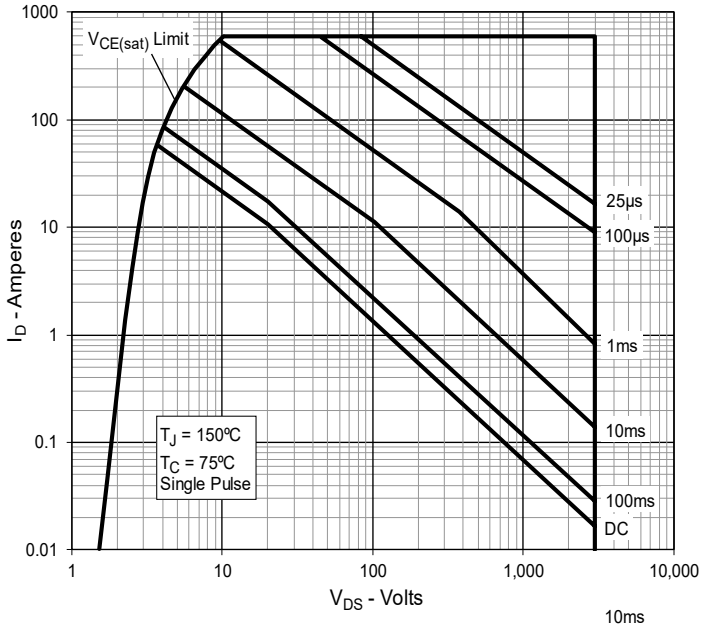
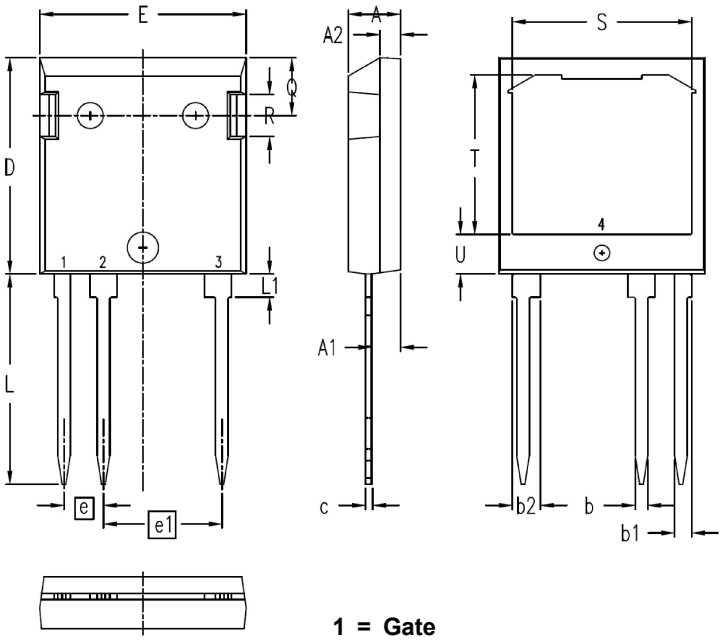


Fig. 20. Forward-Bias Safe Operating Area @ T_C = 75ºC



ISOPLUS i4-Pak Outline



1 = Gate
2 = Emitter
3,4 = Colector

SYM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.193	.201	4.90	5.10
A1	.106	.114	2.70	2.90
A2	.075	.083	1.90	2.10
b	.047	.055	1.20	1.40
b1	.061	.069	1.55	1.75
b2	.087	.094	2.20	2.40
c	.020	.029	0.51	0.74
D	.819	.846	20.80	21.50
E	.768	.799	19.50	20.30
e	.150 BSC		3.81 BSC	
e1	.450 BSC		11.43 BSC	
L	.780	.838	19.80	21.30
L1	.083	.094	2.10	2.40
Q	.213	.236	5.40	6.00
R	.157	.169	4.00	4.30
S	.673	.685	17.10	17.40
T	.602	.614	15.30	15.60
U	.142	.154	3.60	3.90

IXYS
A Littelfuse Technology