

### FEATURES

- Wideband integrated bidirectional bridge**
  - Raw directivity >10 dB up to 17 GHz typical
  - Low insertion loss <2.5 dB typical
  - Return Loss >12 dB typical
- Phase synchronization across multiple devices (ports)**
- SPI-configurable LO interface**
  - 10 MHz to 20 GHz direct LO drive
  - LO frequency doubler and quadrupler
  - Low frequency divider
- IF frequency offset mixer with input divider ratio 1, 2, or 4**
- High dynamic range, wideband IF signal paths**
  - SPI-programmable IF bandwidth from 1 MHz to 100 MHz
  - Individually SPI-programmable amplifiers, 6 dB step size
  - Externally adjustable output common mode level
- 5-bit SPI readable temperature sensor**
- Active supply current (using direct LO drive) 110 mA at 5.0 V**
- Low power shutdown mode**
- 3 mm × 4 mm, 26-lead LFCSP**

### APPLICATIONS

- Broadband, multi-port vector network analyzers
- S-parameter magnitude and phase measurement
- In-line RF power measurement
- Automated test equipment
- Reflectometers
- Materials analysis

### GENERAL DESCRIPTION

The ADL5960 is a wideband vector network analyzer front-end consisting of a resistive bidirectional bridge, down-conversion mixers, programmable IF amplifiers and filters, and a highly flexible local oscillator (LO) interface. The bridge provides >10 dB of directivity up to 17 GHz, and the primary transmission line of the bridge, from RFIN to RFOUT, is wideband impedance matched to 50 Ω and has a flat frequency response with <2.5 dB typical insertion loss.

The ADL5960 supports several different LO interface configurations that simplify the clocking design of a VNA solution as well as the interfacing of the device to an analog-to-digital converter (ADC). The frequency divider and multipliers in the LO interface enable measurement sweeps beyond the operating frequency range of the source driving the (LOP and LOM) pins. This enables operation over the full 20 GHz bandwidth of the ADL5960 using a 6 GHz synthesizer as the LO source. The IF frequency offset mixer, driven through the (OFFP and

### FUNCTIONAL BLOCK DIAGRAM

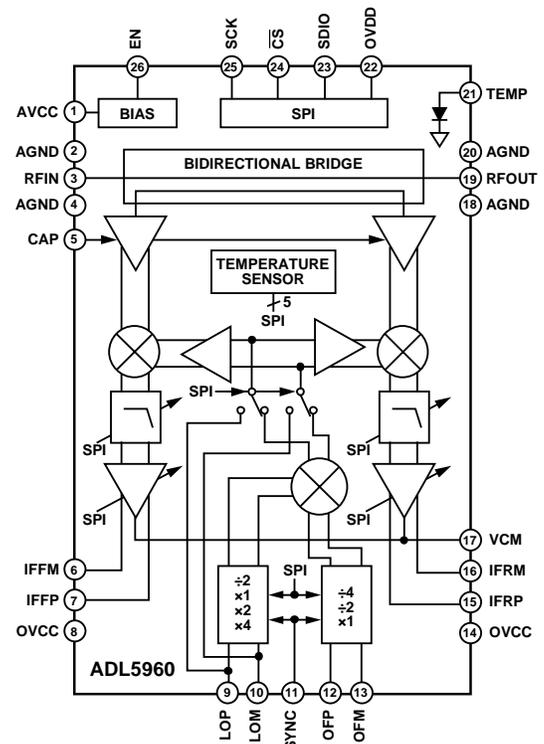


Figure 1.

OFM) interface, enables further simplification by allowing the (swept) RF and LO signals to be driven by the same frequency source. The frequency of the IF output signals is then determined by the low-frequency source driving the (OFFP and OFM) interface. Driving this interface at the ADC sample frequency with the divide by 4 enabled, automatically centers the IF output signal in the first Nyquist zone.

The IF filters with programmable bandwidth and IF amplifiers with individually programmable gain enable simultaneous dynamic range optimization of the IF signals at the incident channel (IFFP and IFFM) and reverse channel (IFRP and IFRM) IF interfaces. The IF amplifiers have an adjustable output common-mode level and sufficient drive capability to interface directly with a wide range of ADCs.

All configurations and functions in the ADL5960 are fully programmable through a 3-wire serial peripheral interface (SPI) using the ADI-SPI interface standard. The ADL5960 is offered in a small footprint 26-lead, 3 mm × 4 mm LFCSP.

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## SPECIFICATIONS

AVCC = OVCC = 5.0 V, EN = OVDD = 3.3 V, VCM = 2.5 V, TC = 25°C, 50 Ω source and load impedance, continuous wave (CW) input at RFIN, characteristic impedance ( $Z_0$ ) = 50 Ω, RF power ( $P_{RF}$ ) = 0 dBm, LO drive single-ended, power ( $P_{LO}$ ) = 0 dBm, RF frequency ( $f_{RF}$ ) = 1 GHz, and  $f_{LO} = f_{RF} + 2.5\text{MHz}$ , unless otherwise noted. BYPASS = 1. Test circuit shown in Figure 20.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
BIDIRECTIONAL BRIDGE	RFIN to RFOUT	0.01		20	GHz
Frequency Range			<2.5		dB
Insertion Loss			>12		dB
Return Loss					dB
DOWN CONVERSION MIXERS	RFIN to (IFFP, IFFM), RFOUT to (IFRP, IFRM)		0.01 to 20		GHz
RF Frequency Range			TBD		GHz
LO Frequency Range	Direct LO drive (default)				GHz
OF Offset Input Frequency Range					GHz
IF Frequency Range			0.1 to 100		MHz
INPUT THIRD ORDER INTERCEPT (IP3)	RFIN to RFOUT				dBm
$f_{RF} = 10\text{ MHz}$			TBD		dBm
$f_{RF} = 1\text{ GHz}$			71		dBm
$f_{RF} = 10\text{ GHz}$			TBD		dBm
$f_{RF} = 15\text{ GHz}$			TBD		dBm
$f_{RF} = 18\text{ GHz}$			TBD		dBm
$f_{RF} = 20\text{ GHz}$			TBD		dBm
DIRECTIVITY <sup>1</sup>					dB
$f_{RF} = 10\text{ MHz}$			27		dB
$f_{RF} = 1\text{ GHz}$			27		dB
$f_{RF} = 10\text{ GHz}$			18		dB
$f_{RF} = 15\text{ GHz}$			9		dB
$f_{RF} = 18\text{ GHz}$			6		dB
$f_{RF} = 20\text{ GHz}$			5		dB
MAXIMUM CONVERSION GAIN <sup>2</sup>	RFIN to (IFFP, IFFM), RFOUT to (IFRP, IFRM), FGAIN, RGAIN = 0x6B				dB
$f_{RF} = 10\text{ MHz}$			TBD		dB
$f_{RF} = 1\text{ GHz}$			43		dB
$f_{RF} = 10\text{ GHz}$			43		dB
$f_{RF} = 15\text{ GHz}$			43		dB
$f_{RF} = 18\text{ GHz}$			42		dB
$f_{RF} = 20\text{ GHz}$			40.8		dB
MINIMUM CONVERSION GAIN <sup>2</sup>	RFIN to (IFFP, IFFM), RFOUT to (IFRP, IFRM), FGAIN or RGAIN = 0x00				dB
$f_{RF} = 10\text{ MHz}$			TBD		dB
$f_{RF} = 1\text{ GHz}$			-14		dB
$f_{RF} = 10\text{ GHz}$			-14		dB
$f_{RF} = 15\text{ GHz}$			-14		dB
$f_{RF} = 18\text{ GHz}$			-14.5		dB
$f_{RF} = 20\text{ GHz}$			-16		dB

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
IF GAIN STEP			6.0		dB
OUTPUT P1dB	RFIN to (IFFP, IFFM), RFOUT to (IFRP, IFRM) f <sub>RF</sub> = 10 MHz f <sub>RF</sub> = 1 GHz f <sub>RF</sub> = 10 GHz f <sub>RF</sub> = 15 GHz f <sub>RF</sub> = 18 GHz f <sub>RF</sub> = 20 GHz		TBD 17 17 17 17 17		dBm dBm dBm dBm dBm dBm
NOISE FIGURE	RFIN to (IFFP, IFFM), RFOUT to (IFRP, IFRM) f <sub>RF</sub> = 10 MHz f <sub>RF</sub> = 1 GHz f <sub>RF</sub> = 10 GHz f <sub>RF</sub> = 15 GHz f <sub>RF</sub> = 18 GHz f <sub>RF</sub> = 20 GHz		TBD 50 TBD 54 TBD 56		dB dB dB dB dB dB
LO INTERFACE (LOP AND LOM)					
Frequency Range		0.01		20	GHz
Return Loss	Z <sub>0</sub> = 100 Ω		>10		dB
Input Power		-6	0	6	dBm
OFFSET LO INTERFACE (OFP AND OFM)					
Frequency Range		0.1		100	MHz
Impedance	Differential, 10 MHz		8.5  3		kΩ  pF
Voltage Swing	Differential	0.125	0.5	2.0	V p-p
IF OUTPUT INTERFACE (IFFP, IFFM, IFRP, AND IFRM)					
Output Frequency Range		0.1		100	MHz
Maximum Peak-to-Peak Voltage	Differential		8		V p-p
Short-Circuit Output Current	Differential		200		mA
VCM INTERFACE					
Output Voltage Range		1.0		4.0	V
Input Impedance			TBD  TBD		kΩ  pF
POWER SUPPLY					
Supply Voltage (AVCC AND OVCC)		4.75	5.0	5.25	V
SPI Supply Interface (OVDD)		1.2	3.3	3.6	V
Active Supply Current (AVCC + OVCC)	Register 0x20 = 0x0B	TBD	220	TBD	mA
	Register 0x20 = 0x1D	TBD	117	TBD	mA
Shutdown Supply Current	EN = 0 V		20		μA

<sup>1</sup> Directivity (dB) = coupling (dB) – isolation (dB).

<sup>2</sup> The conversion gain is the difference in the voltage at the IF outputs with no termination and the voltage at the RF input with a 50 Ω termination.

**TIMING SPECIFICATIONS**

Table 2.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
SPI Timing		See Figure 35				
Setup Time Between Data and Rising Edge of SCLK	$t_{DS}$		2			ns
Hold Time Between Data and Rising Edge of SCLK	$t_{DH}$		2			ns
Clock Period	$t_{CLK}$		20			ns
Setup Time Between $\overline{CS}$ and SCLK	$t_S$		5			ns
Hold Time Between $\overline{CS}$ and SCLK	$t_H$		5			ns
Minimum Period that SCLK Should Be in a Logic High State	$t_{HI}$		10			ns
Minimum Period that SCLK Should Be in a Logic Low State	$t_{LO}$		10			ns
Maximum Time Delay Between $\overline{CS}$ Deactivation and SDIO Bus Return to High Impedance	$t_Z$				20	ns
Maximum Time Delay Between Falling Edge of SCLK and Output Data Valid for a Read Operation	$t_{ACCESS}$				15	ns

## ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Supply Voltage (AVCC and OVCC)	5.5 V
RFIN and RFOUT Input AC Power	
Average <sup>1</sup>	30 dBm
Peak <sup>1</sup>	35 dBm
DC Voltage	
RFIN and RFOUT to AGND <sup>1</sup>	-5 V to +10 V
OVDD	-0.3 V to +3.8 V
SCK, $\overline{\text{CS}}$ , and SDIO	-0.3 V to OVDD + 0.3 V
IFFP, IFFM, IFRP, and IFRM <sup>2</sup>	-0.3 V to OVCC + 0.3 V
Any Other Pin <sup>3</sup>	-0.3 V to AVCC + 0.3 V
DC Current RFIN to/from RFOUT	100 mA
Temperature	
Maximum Junction (T <sub>j</sub> )	150°C
Case Operating Range (T <sub>c</sub> )	-40°C to +105°C
Storage Range	-65°C to +150°C

<sup>1</sup> Not production tested. Guaranteed by design and correlation to production tested parameters.

<sup>2</sup> The voltage on these pins should not exceed 5.5 V, OVCC + 0.3 V or be less than -0.3 V.

<sup>3</sup> The voltage on these pins should not exceed 5.5 V, AVCC + 0.3 V or be less than -0.3 V.

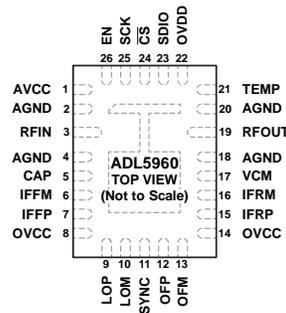
Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

### ESD CAUTION



**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

## PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



**NOTES**  
 1. EXPOSED PAD. THE EXPOSED PAD (EPAD) ON THE UNDERSIDE OF THE DEVICE IS ALSO INTERNALLY CONNECTED TO GROUND AND REQUIRES GOOD THERMAL AND ELECTRICAL CONNECTION TO THE GROUND OF THE PRINTED CIRCUIT BOARD (PCB). CONNECT ALL GROUND PINS TO A LOW IMPEDANCE GROUND PLANE TOGETHER WITH THE EPAD.

22886-012

Figure 2. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	AVCC	Analog Positive Power Supply Pin. Bypass AVCC with 1 nF and a 4.7 μF capacitors placed as close as possible to AVCC.
2, 4, 18, 20	AGND	Analog Ground Pins. All ground pins are internally connected. Use Pin 2 and Pin 4 as the RF return ground for the RFIN transmission line (Pin 3). Use Pin 18 and Pin 20 as the RF return ground for the RFOUT transmission line (Pin 19).
3, 19	RFIN, RFOUT	RF Input/Output of the Primary Transmission Line. RFIN and RFOUT have a 50 Ω load characteristic impedance and can dc-couple to a source and load. When using open and short terminations, do not exceed the maximum power dissipation ratings.
5	CAP	Bypass Capacitor. A 4.7 nF capacitor is recommended for 10 MHz operation.
6, 7, 15, 16	IFFM, IFFP, IFRP, IFRM	Differential IF Outputs. Pin 6 and Pin 7 are coupled to the forward power transfer (from RFIN to RFOUT). Pin 15 and Pin 16 are coupled to the reverse power transfer (from RFOUT to RFIN).
8, 14	OVCC	IF Amplifier Positive Power Supply Pin. Bypass OVCC with a 1 nF and a 4.7 μF capacitor on each pin before connecting to AVCC. Place the capacitors as close as possible to OVCC.
9, 10	LOP, LOM	Down Conversion Mixer LO Input, internally terminated with 100Ω differential. A differential or single-ended signal source can drive the LOP and LOM pins. Register 0x20 configures the LO interface.
11	SYNC	Synchronization Input. This CMOS input pin stops the dividers in the LO and IF input interfaces when driven high and initiates synchronization when driven back low. If the SYNC pin is floating, an internal 415 kΩ pull-down resistor disables the SYNC function.
12, 13	OFP, OFM	IF Offset Reference Frequency Inputs. The OFP and OFM pins set the center frequency at the IF outputs when bitfield IFMODE in register 0x20 equals 0x0, 0x1, or 0x2. Setting IFMODE to 0x3 disables this input.
17	VCM	IF Output Common-Mode Voltage Control. The VCM pin sets the output common-mode voltage at IFFM, IFFP, IFRP, and IFRM. Floats to OVCC/2 if left open.
21	TEMP	Temperature Sensing Diode. The TEMP pin connects to the anode of an on-chip junction diode. It can be used to measure the die temperature by measuring the voltage at this pin, while forcing a known current into the pin.
22	OVDD	SPI Positive Power Supply Pin. Connecting this pin to the (SPI) power supply of the SPI master avoids the need of voltage level translators in the SPI bus connections.
23	SDIO	SPI Data Input/Output. If the SDIO pin is floating, an internal 415 kΩ pull-down resistor ties the pin to a low impedance ground plane.
24	$\overline{CS}$	SPI Chip Select (Active Low). If the $\overline{CS}$ pin is floating, an internal 415 kΩ pull-up resistor ties the pin to OVDD.
25	SCK	SPI Clock Input. If the SCK pin is floating, an internal 415 kΩ pull-down resistor ties the pin to a low impedance ground plane.
26	EN	Chip Enable. A logic high at the EN pin enables the chip. A logic low at the EN pin shuts down the ADL5960. If the EN pin is floating, an internal 415 kΩ pull-down resistor disables the ADL5960.
	EPAD	Exposed Pad. The exposed pad (EPAD) on the underside of the device is also internally connected to AGND and requires good thermal and electrical connection to the ground of the printed circuit board (PCB). Connect all ground pins to a low impedance ground plane together with the EPAD.

TYPICAL PERFORMANCE CHARACTERISTICS

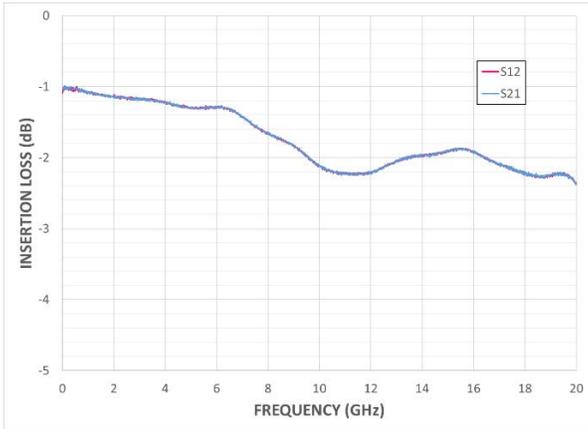


Figure 3. Bridge Insertion Loss

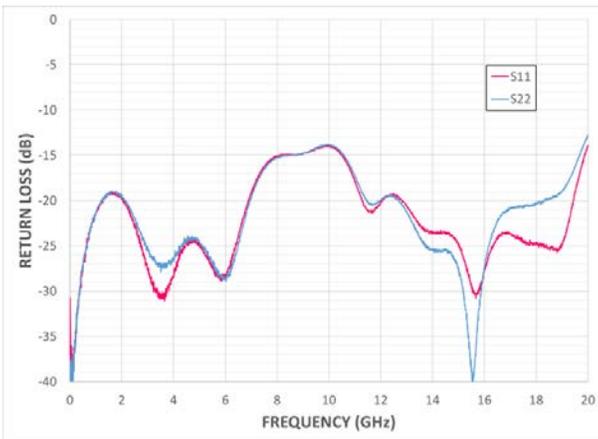


Figure 4. Bridge Return Loss

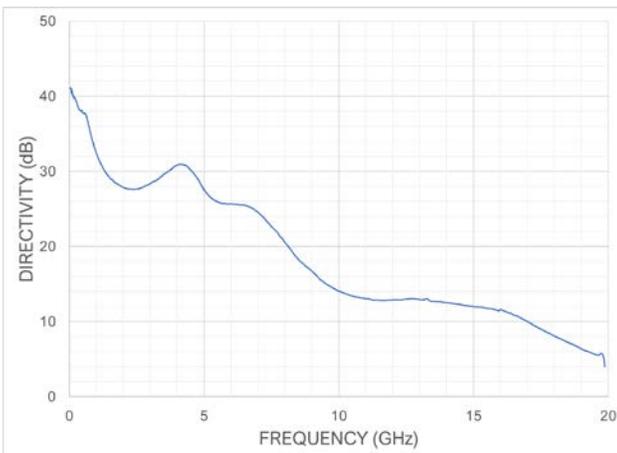


Figure 5. Bridge Raw Directivity

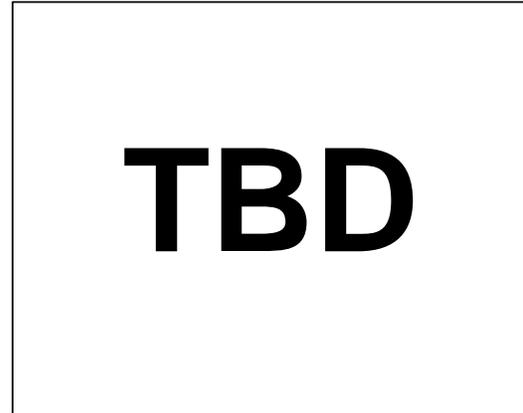


Figure 6. S11 Measurement Over Temperature of a 50 Ω Load after Calibration at Room Temperature

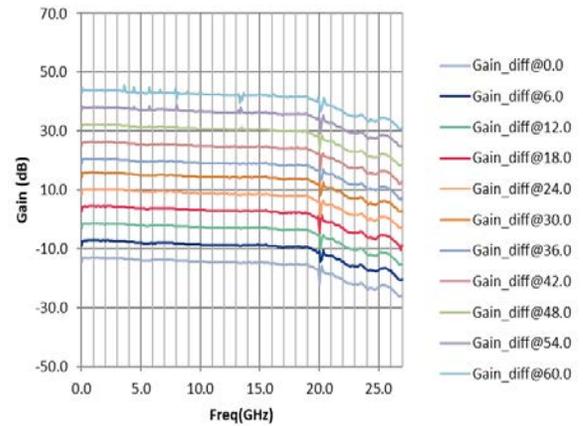


Figure 7. Differential Output Gain vs. RF Frequency

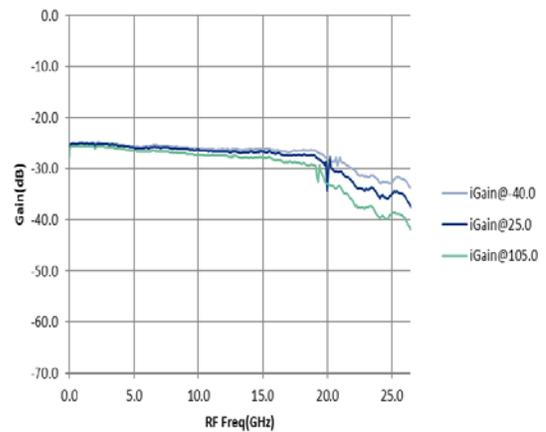


Figure 8. Gain vs. RF Frequency Over Temperature

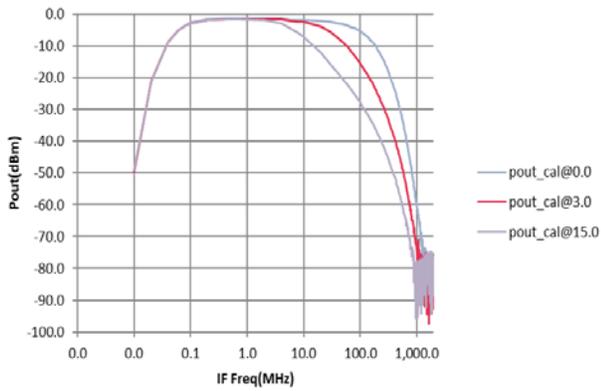


Figure 9. Normalized CIF1 Filter Response, CIF2 = 0

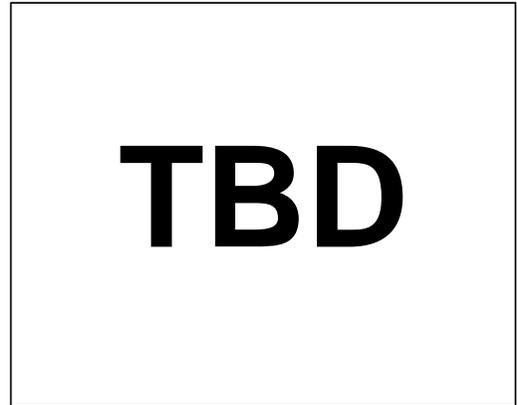


Figure 12. OIP2 vs. RF Frequency

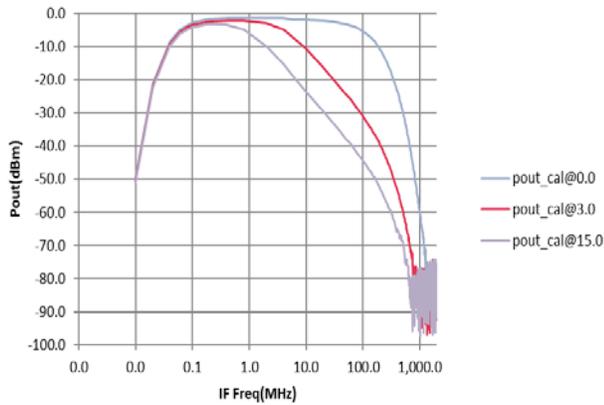


Figure 10. Normalized CIF2 Filter Response, CIF1 = 0

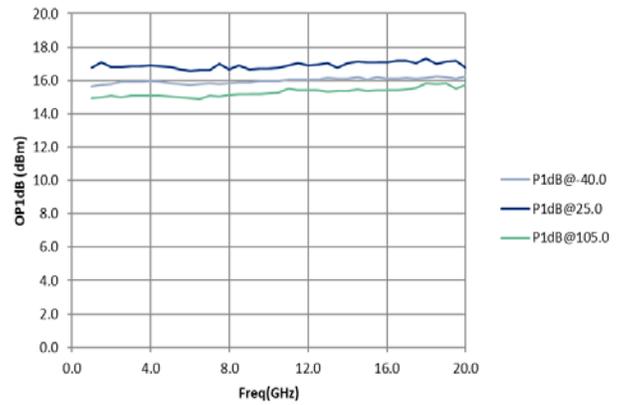


Figure 13. Output P1dB vs. RF Frequency

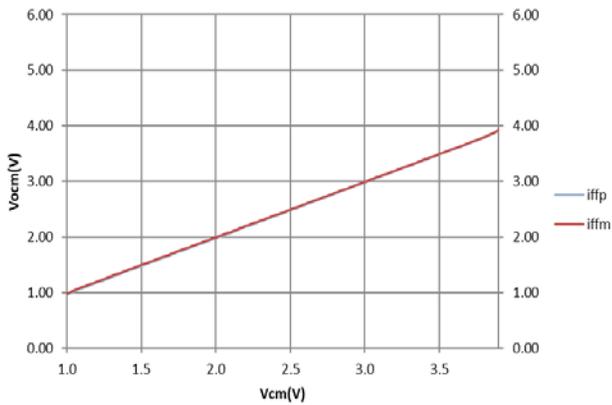


Figure 11.  $V_{OCM}$  vs. Input  $V_{CM}$

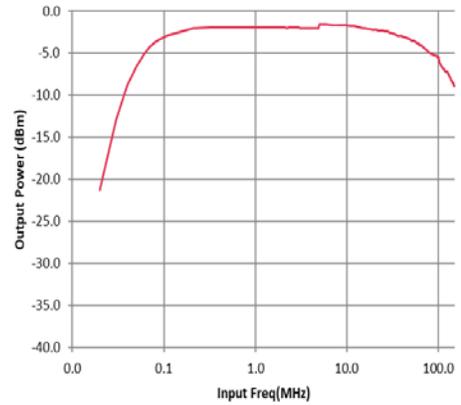


Figure 14. Offset Mixer Input Frequency vs. Output Power  $\times 1$  Mode

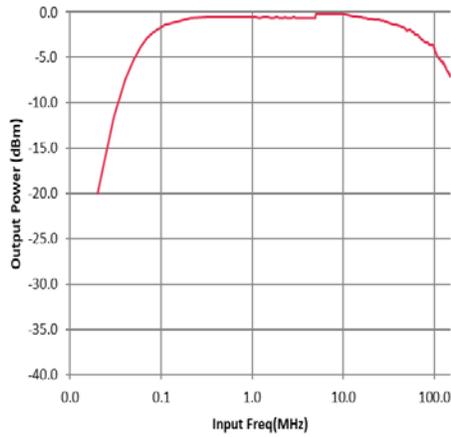


Figure 15. Offset Mixer Input Frequency vs. Output Power Divide/2 Mode

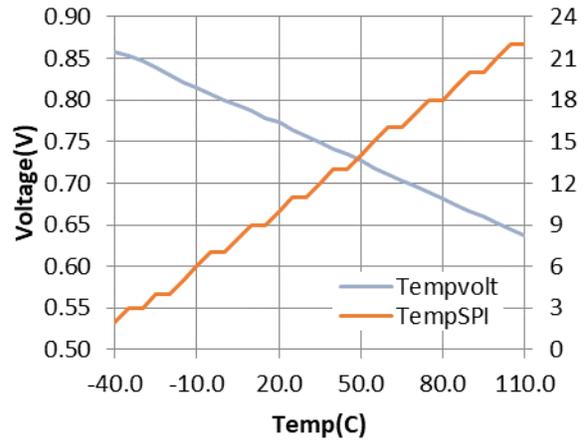


Figure 18. Temperature Voltage and Digital Reading vs. Temperature

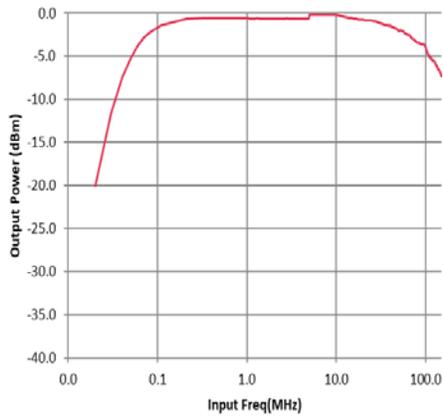


Figure 16. Offset Mixer Input Frequency vs. Output Power Divide/4 Mode

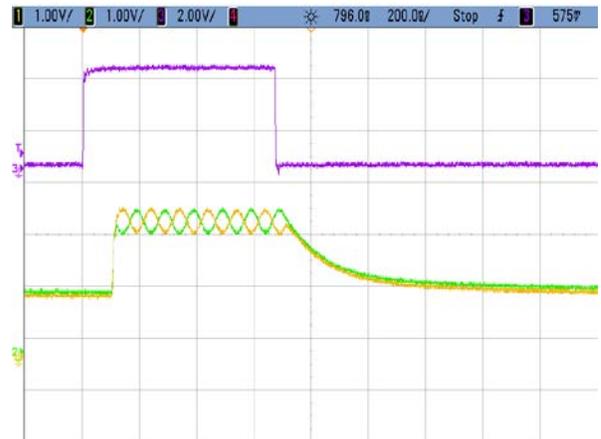


Figure 19. EN Pulse Timing,  $f_{IN} = 1 \text{ GHz}$ ,  $10 \text{ dBm}$ ,  $f_{OUT} = 10 \text{ MHz}$ , Ch3: EN, Ch2/1: IF Out

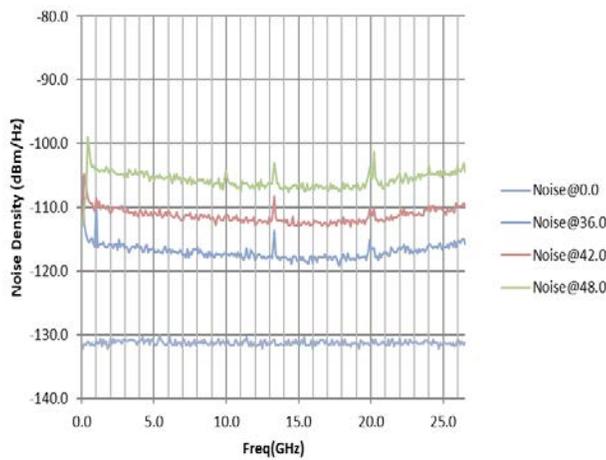


Figure 17. Output Spectral Noise Density vs. RF Frequency for Various Gain Settings

TEST CIRCUITS

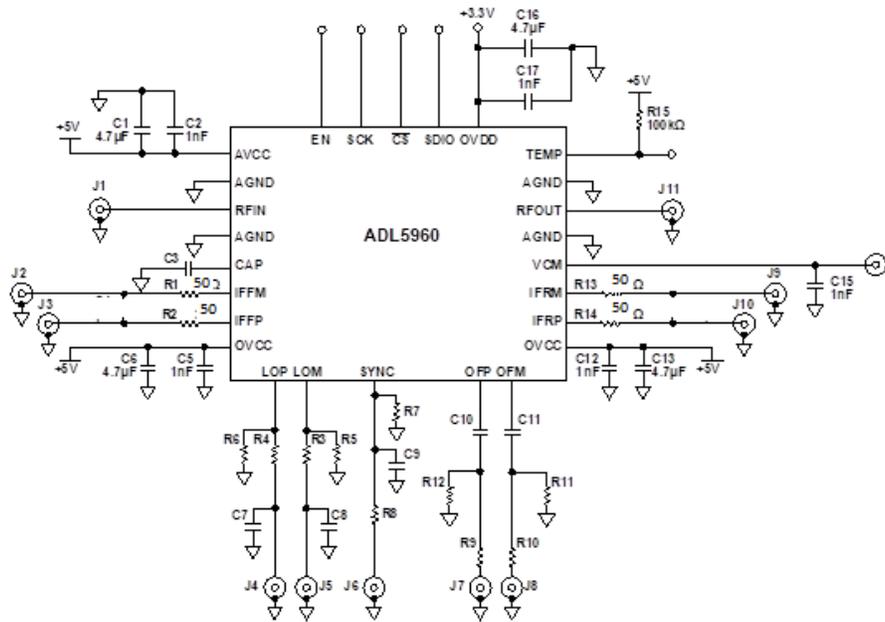


Figure 20. Test Circuit

## THEORY OF OPERATION

The ADL5960 is designed to enable a broadband multiport network analyzer solution in a small footprint.

It is built around an integrated broadband bi-directional resistive bridge, coupled to broadband dual down-conversion mixers. The differential IF outputs of the mixers are passed through lowpass filters with SPI-programmable bandwidth and IF amplifiers with individually SPI programmable gain.

The LO interface to the mixers supports multiple SPI-programmable configurations, designed to simplify the frequency plan in a vector network analyzer application. The LO interface contains frequency multipliers and dividers, that enable a wider frequency range of operation than supported by the LO signal source itself. A second input to the LO interface, the offset interface (OFP and OFM), enables a zero-offset operating mode, with greatly simplified frequency plan. In this mode, only a single swept high-frequency signal source is needed, driving both the RF and LO interfaces of the ADL5960, that is, the RF and LO are swept with zero frequency offset. The signal supplied to the offset interface (OFP and OFM) controls the frequency of the IF output signal, as it mixes with the LO signal supplied to the (LOP and LOM) interface that drives the down-conversion mixers.

Multiple ADL5960 devices can be phase-synchronized and operated simultaneously, which enables the construction of small footprint multi-port network analyzers.

### BASIC ONE PORT VECTOR NETWORK ANALYZER

A one port network analyzer, or reflectometer, can be used to measure the magnitude and phase of the reflection coefficient versus frequency of an unknown load.

Figure 21 depicts the basic configuration of a one port analyzer using the ADL5960.

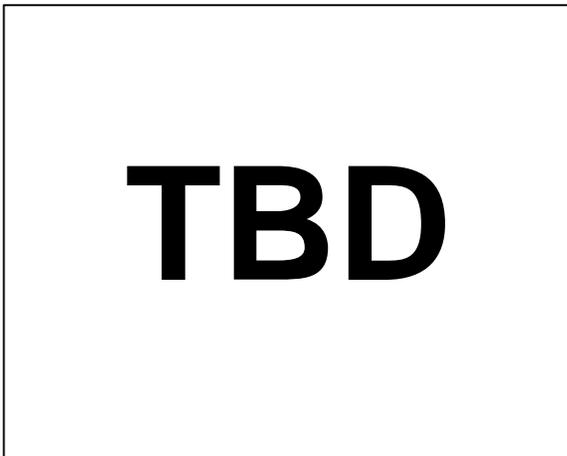


Figure 21. Basic 1 Port Reflectometer with ADL5960

The RFIN interface of the ADL5960 connects to the RF signal sources (typically CW), while the RFOUT interface connects to the unknown load, the device under test (DUT). Because the ADL5960 is completely symmetric, the RF source could also have been connected to RFOUT and the load to RFIN. The RF source injects an (incident) RF signal into the directional bridge of the ADL5960, travelling from the source to the load. At the load, part of this incident (power) wave is reflected and travels back to the source, while the other part is absorbed by the load. The reflection coefficient to be measured (both magnitude and phase) equals the ratio of the reflected power to the incident power at the load.

The directional bridge on the ADL5960 supplies a fraction of the incident signal to the down-conversion mixer in the incident channel, and a fraction of the reflected signal to the input of the reverse channel. Both these signals are down-converted, filtered, amplified and made available at the differential (IFFP and IFFM) and (IFRP and IFRM) interfaces respectively.

After analog-to-digital conversion, the low frequency output signals of the ADL5960, representing the incident and reflected waves, are digitally quadrature down-converted to extract the in-phase and quadrature components, and their ratio is calculated to obtain the reflection coefficient.

### FREQUENCY PLANNING—LO CONFIGURATIONS

The bypass mode selected by setting Bit 4 in Register 0x20, is the most basic (and highest performance) mode of operation of the ADL5960. In this mode, the LO signal supplied to the (LOP and LOM) directly drives the down-conversion mixers, bypassing the frequency multipliers, dividers, and offset mixer. To maintain a fixed IF output frequency, the LO signal must maintain a fixed frequency offset to the RF signal across the entire frequency sweep:

$$f_{LO} = f_{RF} \pm f_{IF}$$

The plus sign corresponds to high-side injection, and the minus sign corresponds to low-side injection. High-side injection often results in slightly better dynamic range, as more of the mixing products land at higher frequencies than the desired IF signal and can be suppressed by low-pass filtering.

The ADL5960 supports IF frequencies up to 100 MHz. However, for a high dynamic range (analog-to-digital conversion), an IF frequency of a few MHz is often preferable, which, on the other hand, creates challenges for the signal sources, requiring an accurate, small frequency offset of a few MHz up to 20 GHz signal frequencies.

The LO interface of the ADL5960 contains a frequency divider and frequency multipliers that enable frequency sweeps beyond the frequency range supported by the LO source connected to the (LOP and LOM) interface, typically a frequency synthesizer. When Bit 4 in Register 0x20 is cleared (disabling bypass mode),

Bits[1:0] can be used to program the LO multiplication factor  $M$  to  $2^{-1}$  (divide-by-two),  $2^0 = 1$ ,  $2^1$  and  $2^2 = 4$ . To land the desired output signal at an IF frequency  $f_{IF}$ , the frequency supplied to the LO interface should meet the following condition:

$$f_{LO} = (f_{RF} \pm f_{IF})/M$$

Note from Table 1 that the divide-by-two mode can only be used for LO input frequencies up to TBD GHz, while the doubler and quadrupler modes only operate above TBD GHz and TBD GHz respectively. The LO interface also contains high frequency filters that suppress the harmonics and subharmonics in the multiplier outputs. The center frequency of these filters can be programmed through Register 0x21 and Register 0x22.

The offset LO mixer enables the use of the zero-offset frequency sweep mode of the ADL5960. The IF output frequency is then controlled by the signal applied to the (OFP and OFM) interface. To enable the offset mixer, clear Bit 4 in Register 0x20 and program Bits[3:2]. The offset frequency input interface contains a programmable divider with ratios  $R$  equal to 1, 2, and 4. With the offset mixer enabled, the IF output signal frequency equals:

$$f_{IF} = f_{RF} - Mf_{LO} + f_{OF}/R$$

By setting  $f_{LO} = f_{RF}/M$  the IF frequency is completely determined by the offset frequency  $f_{OF}$ . The setting  $R = 4$  is particularly useful; it lands the IF output signal in the middle of the first Nyquist zone when the offset input is driven by the clock of the ADC that monitors the ADL5960 IF outputs.

### IF SIGNAL PATH CONFIGURATION

The IF output signal of the mixers is passed through lowpass filters to remove unwanted mixing products and noise. The bandwidth of these filters is SPI-programmable through Register 0x25. The same settings apply to both ADL5960 IF channels.

Following the lowpass filters, both IF channels contain IF amplifiers with individually SPI-programmable gain. Because the magnitude of the incident and reflected signal can be vastly different, and change over frequency, independent programming of the incident and reverse channel gain settings

enables optimal interfacing of both channels to the ADC input range.

### MULTIPOINT VECTOR NETWORK ANALYZER

The ADL5960 can also be used to create network analyzers consisting of multiple ports, as depicted in Figure 22.

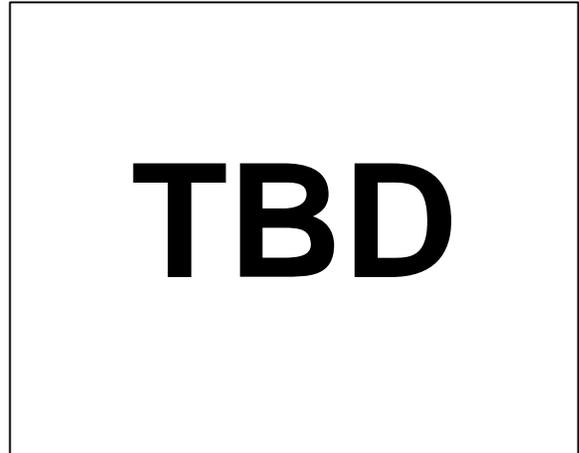


Figure 22. Multiport Network Analyzer Using ADL5960 Devices

Each port connects to one ADL5960 device, and RF switches route the RF signal to one ADL5960 at a time. Phase synchronization between the ADL5960 devices is achieved through the LO and offset frequency signals. For good accuracy, it is preferable to match the propagation delays from the LO source to each of the ADL5960 devices. Residual delay differences can be address through calibration procedures for the VNA system. Routing of the signal lines to the offset interface is less critical, as these operate at much lower frequencies.

The SYNC interface is used to force the LO and offset dividers in all ADL5960 devices to the same known initial state, such that no phase ambiguities exist between the devices. A single pulse applied to this input after power-on is sufficient to synchronize all devices.

For the best accuracy, simultaneous sampling of all ADL5960 IF channels is recommended.

## CIRCUIT DESCRIPTION

### POWER SUPPLY INTERFACES

The AVCC, OVCC, and OVDD pins have independent supply clamps and should be ramped slower than 100  $\mu$ s to avoid triggering the clamps.

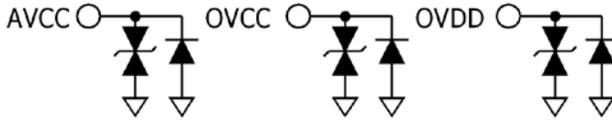


Figure 23. Power Supply Interfaces

### RFIN AND RFOUT INTERFACE

The RFIN and RFOUT pins are connected by a 6  $\Omega$  resistive directional bridge. Currents up to 100 mA can be safely passed through for biasing applications such as an RF amplifier. Voltages in the range of -5 V to +10 V are safe to apply to these pins.

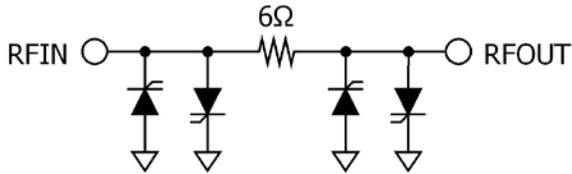


Figure 24. RFIN and RFOUT Interface

### IFFM, IFFP, IFRM, AND IFRP INTERFACES

The differential IF output amplifiers are capable of driving 100  $\Omega$  differential loads up to 8 V p-p. In the event of an output short circuit to ground or AVCC, an internal clamp limits the current to less than roughly 200 mA for each of the single-ended outputs (IFFM, IFFP, IFRP, and IFRM).

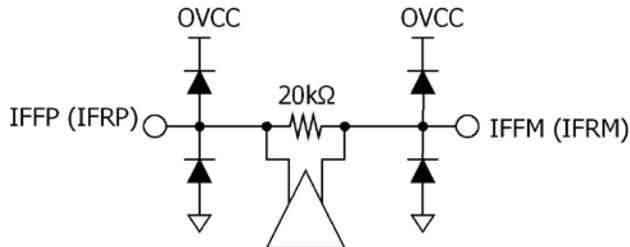


Figure 25. IFFM, IFFP, IFRM, and IFRP Interfaces

### VCM INTERFACE

The VCM interface sets the common-mode voltage level of the IF output amplifiers. This is useful for interfacing with the common-mode input level of many different ADCs to optimize available dynamic range. When the VCM pin is left floating, an internal voltage divider sets the common-mode voltage level to OVCC/2. When externally driven, a low-impedance voltage source should be used to set the voltage on this pin. The tracking range of the VCM pin voltage to the common-mode output voltage is linear over most of the 1 V to 4 V input range. For input voltages less than about 1 V and greater than 4 V the output common-mode voltage is clamped at 1 V and 4 V, respectively.

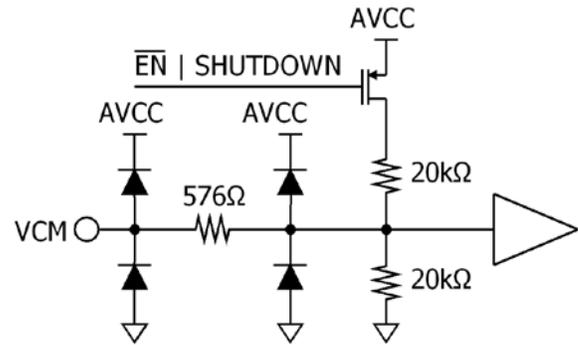


Figure 26. VCM Interface

### LOP AND LOM INTERFACE

The LO interface can be driven differentially or single-ended. The (LOP and LOM) inputs are internally biased at AVCC/2. The internal 100 $\Omega$  termination can be impedance matched using a 2:1 external balun.

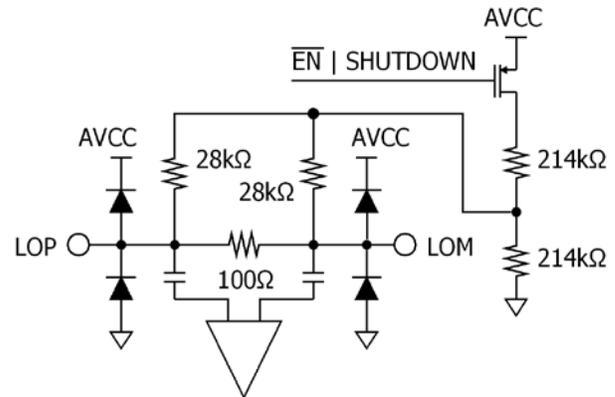


Figure 27. LOP and LOM Interface

### OFFP AND OFM INTERFACE

The offset frequency inputs (OFFP and OFM) have an internal 3.3 V bias, and should be dc blocked externally. The inputs can be driven differentially or single-ended. When driven single-ended, the unused input should be ac grounded with a high value capacitor. A value of 10 nF or higher is recommended for 400 kHz input frequency.

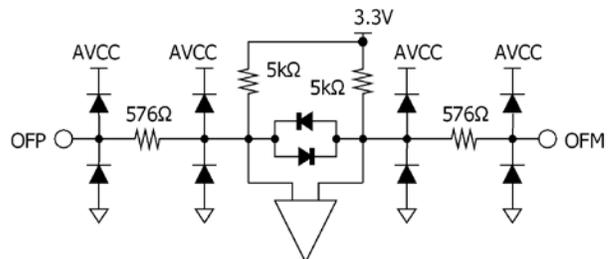


Figure 28. OFFP and OFM Interface

**EN INTERFACE**

The chip is in shutdown if either the SHUTDOWN, Bit 1, in DEVICE\_CONFIG. Register 0x02 is set, or the EN pin is de-asserted. An internal 415 kΩ pull-down ensures the device is off (shutdown) if the pin is left floating.

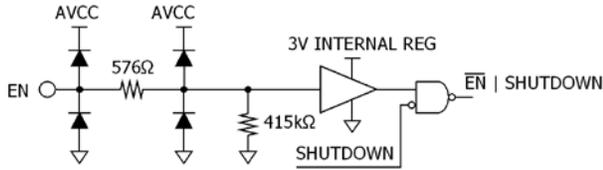


Figure 29. EN Interface

**SYNC OR SCK INTERFACE**

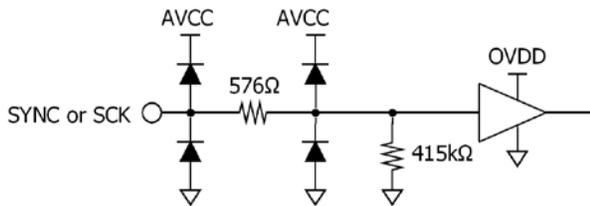


Figure 30. SYNC or SCK Interface

**CS INTERFACE**

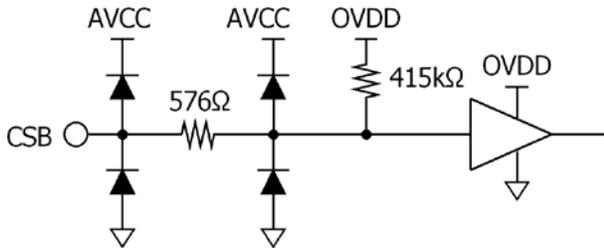


Figure 31. CS Interface

**SDIO INTERFACE**

The ADL5960 implements a 3-wire SPI. For cases where the SPI master is 4-wire, a series current limiting resistor is recommended to isolate the master and slave outputs. This provides protection in the event that both outputs become simultaneously active.

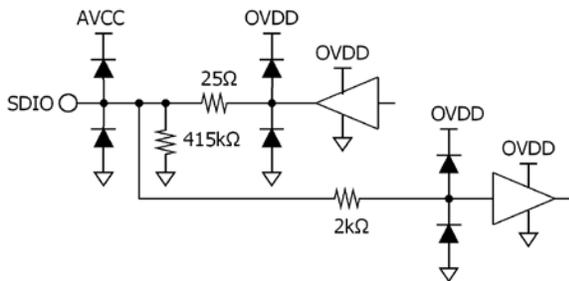
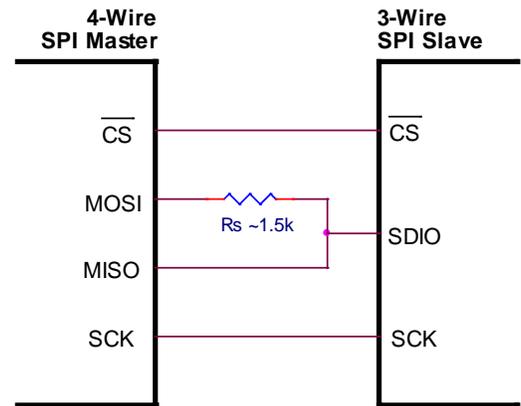


Figure 32. SDIO Interface

For example, see Figure 33.



ADL5960

Figure 33. SPI 4-Wire to 3-Wire Conversion

**TEMP INTERFACE**

In addition to the on-chip digital thermometer, the TEMP pin can be used to monitor the die temperature. A user-chosen reference current of 100uA, results in a nominal voltage of TBD V at 25°C and a temperature slope of -TBD mV/°C.

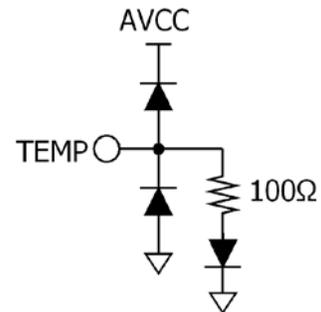


Figure 34. TEMP Interface

## SERIAL PERIPHERAL INTERFACE PROTOCOL

There are two phases to the serial interchange. The first phase is the instruction cycle and is comprised of the controller shifting an instruction to the slave device. This is followed by one or more bytes of data shifted by the controller for a write operation or by the slave for a read operation.

### Instruction

Immediately following the falling edge of  $\overline{CS}$  that initiates a SPI cycle is the instruction phase. The instruction determines the action immediately following its completion. If the instruction is to write data to a target register, the following data bytes will be latched into 8-bit bytes and then routed to the target address starting with the one specified in the instruction phase. If the instruction is to read data from the target device, the address specified is the first address that the device will respond with at the completion of the instruction phase.

The instruction always consists of 16 bits and can directly address 0x7FFF addresses.

### Read/Write

The most significant bit of the instruction phase is the read-write indicator bit. If this bit is set, the instruction represents a read instruction. If this bit is clear, the instruction represents a write instruction.

### Address

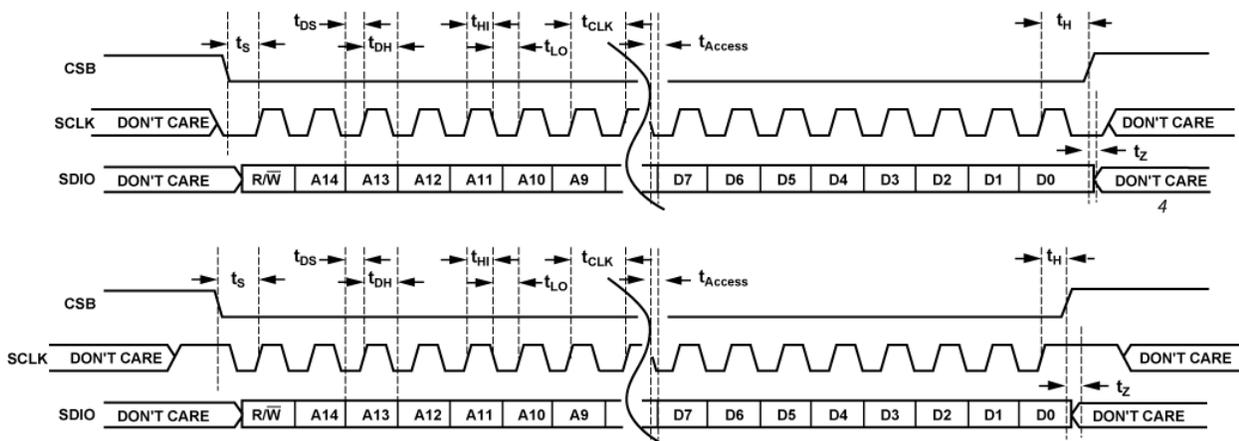
The 15 LSBs of the instruction phase provide direct access to 0x7FFF registers, each representing 8 bits of data.

### Timing

The following figures both represent acceptable timing diagrams. The only difference between the two is the initial state of the clock relative to the state of the  $\overline{CS}$  line. These diagrams do not indicate that the polarity of the clock can be changed to latch data on the rising or falling edge. In both cases, the rising edge of the SCLK is used to latch data.

### Read Cycle

The instruction header is written to the device either MSB or LSB first (depending on the mode) followed by the data. By default, chip readback is sent via the SDIO (3-wire mode). The SDIO pin becomes an output pin after receiving the instruction header with a readback request. In this mode, the SDIO is changed from an input to an output in the  $\frac{1}{2}$  cycle of SCLK between the last rising edge of SCLK of the instruction and the following falling edge. When  $\overline{CS}$  is de-asserted, SDO returns to high impedance until the next read transaction.



Setup and Hold timing measurements  
\*Level must be the same at head and tail.

Figure 35. SPI Timing Diagram

## REGISTER SUMMARY

Registers 0x00 through 0x05 configure the SPI and contain device identifiers. Register 0x20 to Register 0x26 control the analog circuit functionality of the device. Refer to Table 5 for details.

### Interface Configuration Register

Register 0 is the serial interface configuration register and is implemented as a 4-bit palindrome with each nibble a mirror of the other. This ensures that regardless of which way data is

shifting, the device can be programmed should device synchronization be lost. Therefore, when writing to this address, the palindrome is always required to eliminate any ambiguity in configuring this register.

### Soft Reset

Bit 7 and bit 0 implement chip reset. Setting this bit implements a reset function, resetting all SPI registers to their default value.

Table 5. ADL5960 Register Summary

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	R/W	
0x00	SPI_CONFIG_A	[7:0]	SOFTRESET_	LSB_FIRST_	ASCENSION_	RESERVED		ASCENSION	LSB_FIRST	SOFTRESET	0x00	R/W	
0x01	SPI_CONFIG_B	[7:0]	SINGLE_INSTRUCTION	CSB_STALL	MASTER_SLAVE_RB	RESERVED					0x00	R/W	
0x02	DEVICE_CONFIG	[7:0]	RESERVED							SHUTDOWN	RESERVED	0x00	R/W
0x03	CHIPTYPE	[7:0]	CHIPTYPE									0x01	R
0x04	PRODUCT_ID_L	[7:0]	PRODUCT_ID_L									0x60	R
0x05	PRODUCT_ID_H	[7:0]	PRODUCT_ID_H									0x59	R
0x20	LO_CONFIG	[7:0]	RESERVED			BYPASS		IFMODE	LOMODE		0x19	R/W	
0x21	CT2	[7:0]	RESERVED			CT2					0x00	R/W	
0x22	CT4	[7:0]	RESERVED			CT4					0x00	R/W	
0x23	FGAIN	[7:0]	RESERVED	FGAIN							0x00	R/W	
0x24	RGAIN	[7:0]	RESERVED	RGAIN							0x00	R/W	
0x25	CIF2_CIF1	[7:0]	CIF2				CIF1				0x00	R/W	
0x26	TDEG	[7:0]	RESERVED				TDEG				0x00	R	

## REGISTER DETAILS

Table 6. SPI Register Details

Addr	Name	Bits	Bit Name	Description	Reset	Access
0x00	SPI_CONFIG_A	7	SOFTRESET_	Soft Reset. Copy of Bit 0.	0x0	R/W
		6	LSB_FIRST_	LSB First. Copy of Bit 1.	0x0	R/W
		5	ASCENSION_	Address Ascension. Copy of Bit 2.	0x0	R/W
		[4:3]	RESERVED	Reserved.	0x0	R
		2	ASCENSION	Address Ascension. When set causes address ascension address mode to be enabled. When clear, addresses descend. 0: address auto decrement. 1: address auto increment.	0x0	R/W
		1	LSB_FIRST	LSB First. When set causes input and output data to be oriented as LSB first. If this bit is clear, data is oriented as MSB first. 1: LSB first. 0: MSB first.	0x0	R/W
		0	SOFTRESET	Soft Reset. Setting this bit initiates a reset equivalent to a hard reset with the exception that the bits of 0x00 (this register) and the SPI state machine are unaffected. This bit is auto-clearing after the soft reset is complete. 1: reset asserted. 0: reset not asserted.	0x0	R/W
0x01	SPI_CONFIG_B	7	SINGLE_INSTRUCTION	Single Instruction. When this bit is set, streaming is disabled and only one read or write operation is performed regardless of the state of the $\overline{CS}$ line. When this bit is clear, streaming is enabled. If this bit is set and the $\overline{CS}$ remains asserted, the state machine resets after the data byte as if $\overline{CS}$ was de-asserted and awaits the next instruction. This forces each data byte to be preceded with a new instruction even though the $\overline{CS}$ line has not been de-asserted by the SPI master.	0x0	R/W
		6	CSB_STALL	$\overline{CS}$ Stalling. When Single Instruction is enabled and $\overline{CS}$ stalling is enabled, the $\overline{CS}$ signal will not reset the SPI state machine when pulled high. When $\overline{CS}$ stalling is disabled, the SPI state machine always resets when $\overline{CS}$ signal is high.	0x0	R/W
		5	MASTER_SLAVE_RB	Master Slave Readback. Setting this bit will allow readback of the master flip-flop outputs instead of the slave outputs. Clearing this bit will provide access to the slave outputs.	0x0	R/W
		[4:0]	RESERVED	Reserved.	0x0	R
0x02	DEVICE_CONFIG	[7:2]	RESERVED	Reserved.	0x0	R
		1	SHUTDOWN	Device Shutdown. If SHUTDOWN is asserted, the device is powered off. See also the EN Interface section. 0: normal operation. 1: shutdown.	0x0	R/W
		0	RESERVED	Reserved.	0x0	R
0x03	CHIPTYPE	[7:0]	CHIPTYPE	Chip Type, Read Only.	0x1	R
0x04	PRODUCT_ID_L	[7:0]	PRODUCT_ID_L	Product ID Low, Lower 8 Bits.	0x60	R
0x05	PRODUCT_ID_H	[7:0]	PRODUCT_ID_H	Product ID High, Higher 8 Bits.	0x59	R

Addr	Name	Bits	Bit Name	Description	Reset	Access
0x20	LO_CONFIG	[7:5]	RESERVED	Reserved.	0x0	R
		4	BYPASS	Bypass LO Path. When asserted, the LO Chain is configured to have all multipliers and dividers turned off. IFMODE and LOMODE have no effect. The LO inputs are connected to the RF mixers by the LO amplifier only.	0x1	R/W
		[3:2]	IFMODE	IFMODE. Configures the divider in the offset reference frequency interface. 00: $\times 1$ no dividers enabled. 01: divide by 2 mode. 10: divide by 4 Mode. 11: dividers off, offset reference signal disconnected.	0x2	R/W
		[1:0]	LOMODE	LOMODE. Configures the LO chain divider and multipliers. 00: divide by 2. 01: multiply by 1 $\times$ . 10: multiply by 2 (2 $\times$ ). 11: multiply by 4 (4 $\times$ ).	0x1	R/W
0x21	CT2	[7:5]	RESERVED	Reserved.	0x0	R
		[4:0]	CT2	CT2 Filter Setting. Sets the center frequency of the filter in the 2 $\times$ frequency multiplier in the LO interface.	0x0	R/W
0x22	CT4	[7:5]	RESERVED	Reserved.	0x0	R
		[4:0]	CT4	CT4 Filter Setting. Sets the center frequency of the filter in the 4 $\times$ frequency multiplier in the LO interface.	0x0	R/W
0x23	FGAIN	7	RESERVED	Reserved.	0x0	R
		[6:0]	FGAIN	Forward Gain. Configures the gain of the IF amplifier in the Forward path, to the (IFFP, IFFM) output, in 6 dB steps. Decimal register value represents the gain in dB. Refer to Figure TBD.	0x0	R/W
0x24	RGAIN	7	RESERVED	Reserved.	0x0	R
		[6:0]	RGAIN	Reverse Gain. Configures the gain of the IF amplifier in the Reverse path, to the (IFRP, IFRM) output, in 6 dB steps. Decimal register value represents the gain in dB. Refer to Figure TBD.	0x0	R/W
0x25	CIF2_CIF1	[7:4]	CIF2	Narrow-band IF Filter Setting. Sets the corner frequency of the narrow bandwidth IF filter. Refer to Figure 10.	0x0	R/W
		[3:0]	CIF1	Wide-band IF Filter Setting. Sets the corner frequency of the wide bandwidth IF filter. Refer to Figure 9.	0x0	R/W
0x26	TDEG	[7:5]	RESERVED	Reserved.	0x0	R
		[4:0]	TDEG	Thermometer Register (5b). 5-bit thermometer readout. Refer to Figure 18.	0x0	R

OUTLINE DIMENSIONS

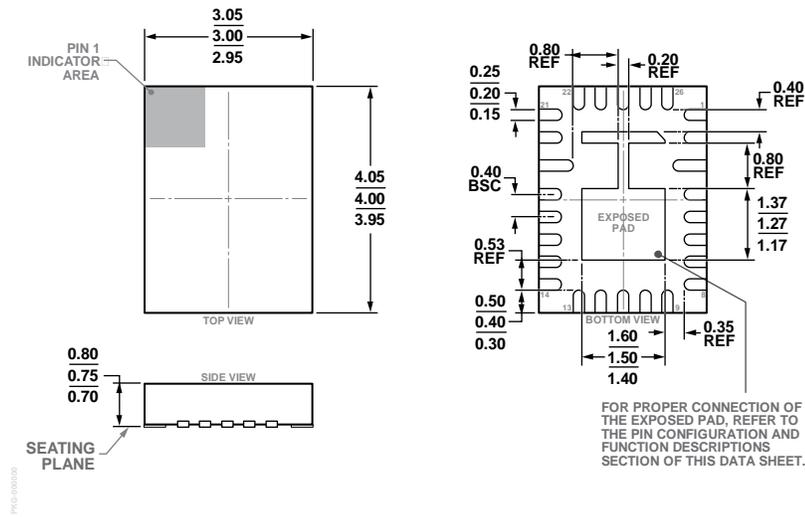


Figure 36. 26-Lead lead Frame Chip Scale Package [LFCSP]  
 3 mm x 4 mm Body and 0.75 mm Package Height  
 (CP-26-1)  
 Dimensions shown in millimeters