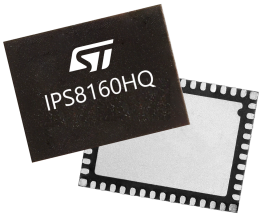
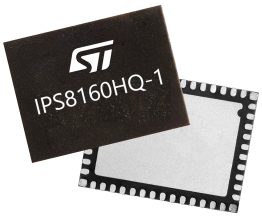
IPS8160HQ, IPS8160HQ-1

Datasheet

Octal channel high-side driver





Product status link
IPS8160HQ
IPS8160HQ-1

Product label

SUSTAINABLE TECHNOLOGY

Features

- Operating output current: 0.7 A (IPS8160HQ) or 1.0 A (IPS8160HQ-1) per channel
- CMOS compatible input
- Very low standby current
- Undervoltage shutdown
- Overload and short-circuit protection with output current limitation
- Junction overtemperature protection
- Case overtemperature protection for thermal independence of the channels
- Protection against loss of ground
- Thermal shutdown diagnostic pin
- Designed to meet IEC 61000-4-2, IEC 61000-4-4, IEC 61000-4-5
- Package: QFN48L 8x6x0.9 mm

Applications

- Programmable logic control
- Vending machines
- Industrial PC peripheral input/output
- Numerical control machines
- General high-side switch applications

Description

The IPS8160HQ and IPS8160HQ-1 are monolithic devices designed with STMicroelectronics VIPower M0-3 technology, intended to drive any kind of load with one side connected to ground. They can be driven by using a 3.3 V logic supply.

They are suitable for applications with up to 0.7 A (IPS8160HQ) or 1 A (IPS8160HQ-1) steady-state operating current.

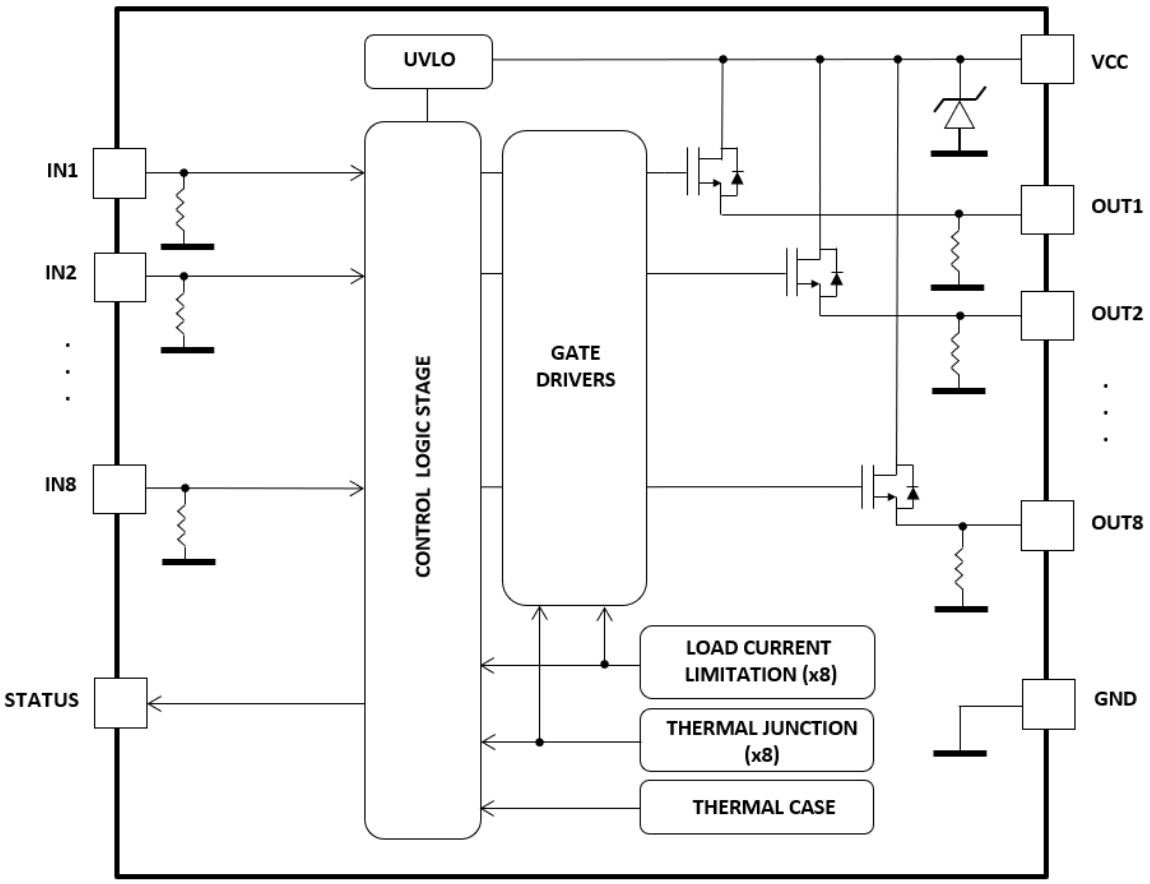
Active current limitation combined with thermal shutdown and automatic restart protect the devices against overload. In overload conditions, the channel turns OFF and ON again automatically to maintain the junction temperature between T_{JSD} and T_R. If this condition causes the case temperature to trigger T_{CSD}, then overloaded channels are turned OFF and can be turned back ON only when the case temperature decreases down to T_{CR}. Non-overloaded channels continue to operate normally.

The devices automatically turn OFF in case of ground pin disconnection.

Devices are especially suitable for industrial applications conforming to IEC 61131.

1 Block diagram

Figure 1. **IPS8160HQ, IPS8160HQ-1 block diagram**



2 Pin connections

Figure 2. **Connection diagram (top through view)**

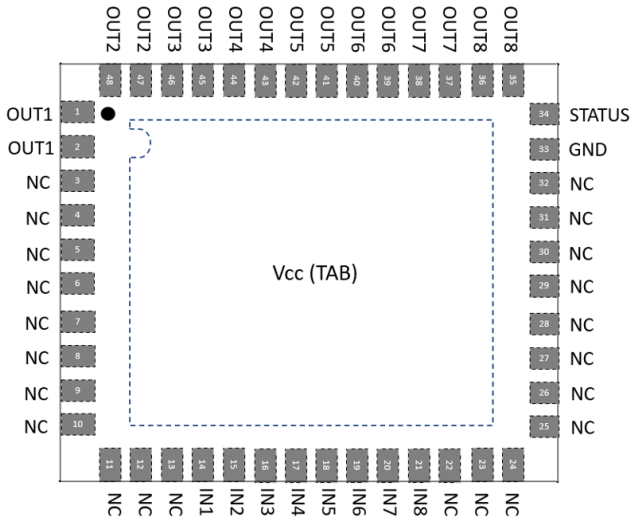


Table 1. **Pin functions**

Pin	Symbol	Description
1, 2	OUT1	Channel 1 power output
3 to 13, 22 to 32	N.C.	Not connected
14	IN1	Channel 1 input
15	IN2	Channel 2 input
16	IN3	Channel 3 input
17	IN4	Channel 4 input
18	IN5	Channel 5 input
19	IN6	Channel 6 input
20	IN7	Channel 7 input
21	IN8	Channel 8 input
33	GND	Output power ground
34	STATUS	Common open source diagnostic for overtemperature
35, 36	OUT8	Channel 8 power output
37, 38	OUT7	Channel 7 power output
39, 40	OUT6	Channel 6 power output
41, 42	OUT5	Channel 5 power output
43, 44	OUT4	Channel 4 power output
45, 46	OUT3	Channel 3 power output
47, 48	OUT2	Channel 2 power output
EP	V_{CC}	Supply voltage

3 Maximum ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	DC supply voltage	45	V
$-I_{GND}$	DC ground reverse current	250	mA
	Transient ground reverse current (pulse duration < 1 ms)	6	A
I_{OUT}	DC output current	Internally limited	A
$-I_{OUT}$	Reverse DC output current	2	A
I_{IN}	DC input current range	-1, +10	mA
V_{IN}	Input voltage range	-0.3, +5.5	V
V_{ESD}	Electrostatic discharge (R = 1.5 KΩ; C = 100 pF)	2000	V
P_{TOT}	Power dissipation at Tc = 25 °C	4	W
EAS	Single pulse Avalanche Energy per channel, all channels driven simultaneously (Tamb = 125 °C, I_{OUT} = 0.6 A per channel)	0.5	J
T_J	Junction operating temperature	Internally limited	°C
T_C	Case operating temperature	Internally limited	°C
T_{STG}	Storage temperature range	-40, +150	°C

4 Thermal data

Table 3. Thermal data

Symbol	Parameter	Max. Value	Unit
$R_{th(JC)}$ (1)	Thermal Resistance, Junction-to-case per channel	1.5	°C/W
$R_{th(JA)}$ (2)	Thermal Resistance, Junction-to-ambient	30	

1. *Rth between the die and the bottom case surface measured by cold plate as per JESD51.*
2. *JESD51-7.*

5 Electrical characteristics

10.5 V < V_{CC} < 32 V; -40 °C < T_J < 125 °C; unless otherwise specified.

Table 4. Power section

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{USD}	V_{CC} undervoltage turn-off threshold		7		10.5	V
R_{ON}	ON-state resistance	I_{OUT} ≤ 1 A; T_J = 25 °C; V_{CC} ≤ 36 V I_{OUT} ≤ 1 A; T_J = 125 °C; V_{CC} ≤ 36 V			160 280	mΩ mΩ
I_S	Supply current	OFF-state V_{CC} = 24 V; T_{CASE} = 25 °C			150	µA
		ON-state (all channels ON) V_{CC} = 24 V; T_{CASE} = 100 °C			12	mA
I_{LGND}	Output current at turn-off	V_{CC} = V_{GND} = 24 V; V_{STAT} = V_{IN} = 5 V; V_{OUT} = 0 V; T_J = 25 °C			0.5	mA
		V_{CC} = V_{GND} = 24 V; V_{STAT} = V_{IN} = 5 V; V_{OUT} = 0 V; T_J = 125 °C			0.55	mA
$I_{L(OFF)}$	OFF-state output current	V_{IN} = V_{OUT} = 0 V	0		5	µA
$V_{OUT(OFF)}$	OFF-state output voltage	V_{IN} = 0 V; I_{OUT} = 0 A			3	V

Table 5. Switching (V_{CC} = 24 V)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
t_{ON}	Turn-ON time	R_L = 48 Ω; from 50% V_{IN} to 80% V_{OUT} see Figure 3	20	30	60	µs
t_{OFF}	Turn-OFF time	R_L = 48 Ω; from 50% V_{IN} to 10% V_{OUT} see Figure 3	20	40	80	µs
t_{OFF}- t_{ON}	Turn-OFF, Turn-ON matching		-40	10	60	µs
$dV_{OUT}/dt_{(ON)}$	Turn-ON voltage slope	R_L = 48 Ω; from V_{OUT} = 2.4 V to V_{OUT} = 19.2 V see Figure 3		0.7		V/µs
$dV_{OUT}/dt_{(OFF)}$	Turn-OFF voltage slope	R_L = 48 Ω; from V_{OUT} = 21.6 V to V_{OUT} = 2.4 V see Figure 3		1.5		V/µs
$t_{d(VCCON)}$	Power on delay time from VCC rising edge	see Figure 4		1		ms

Figure 3. **Turn-ON and turn-OFF**

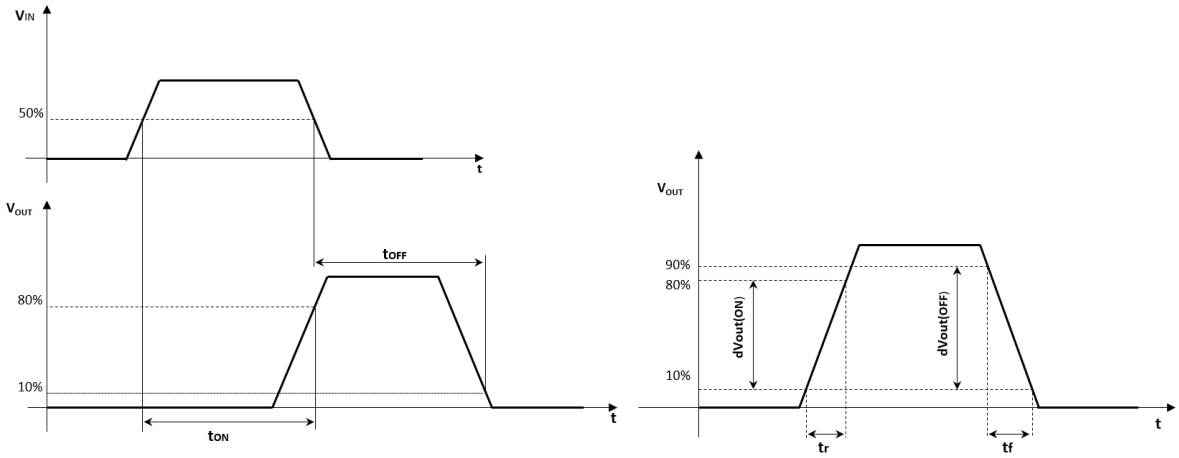


Figure 4. **V_{CC} turn-ON**

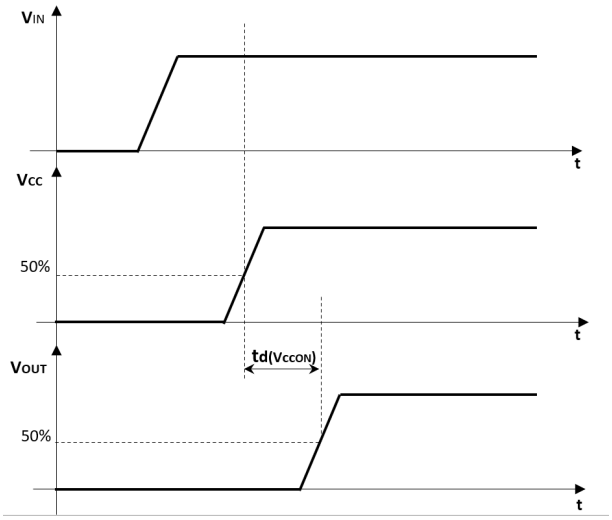


Table 6. **Input pins**

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{INL}	Input low level				1.25	V
I_{INL}	Low level input current	V_{IN} = 1.25 V	1			µA
V_{INH}	Input high level		2.25			V
I_{INH}	High level input current	V_{IN} = 2.25 V			10	µA
$V_{IN(HYST)}$	Input hysteresis voltage		0.25			V
V_{CL}	Input clamp voltage	I_{IN} = 1 mA	6.0	6.8	8.0	V
		I_{IN} = -1 mA		-0.7		

Table 7. Protections

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
T_{CSD}	Case shutdown temperature		125	130	135	°C
T_{CR}	Case reset temperature		110			°C
T_{CHYST}	Case thermal hysteresis		7	15		°C
T_{JSD}	Junction shutdown temperature		150	175	200	°C
T_{R}	Junction reset temperature		135			°C
T_{HYST}	Junction thermal hysteresis		7	15		°C
I_{PEAK}	Maximum DC output current before limitation	V_{CC} = 24 V; R_{LOAD} = 10 mΩ	1.1		2.6	A
I_{LIM}	DC short-circuit current limitation per channel	V_{CC} = 24 V; R_{LOAD} = 10 mΩ	0.7 (1) 1 (2)		1.7	A
V_{DEMAG}	Turn-OFF output clamp voltage	I_{OUT} = 0.5 A; L= 6 mH	V_{CC}-57	V_{CC}-52	V_{CC}-47	V

1. *IPS8160HQ*
2. *IPS8160HQ-1*

Table 8. Status Pin

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
I_{HSTAT}	STATUS pin high level current	V_{CC} = 18 to 32 V; R_{STAT} = 1 kΩ (Fault condition)	2	3	4	mA
I_{LSTAT}	STATUS pin leakage current	Normal operation; V_{CC} = 32 V			0.1	µA
V_{CLSTAT}	STATUS pin clamp voltage	I_{STAT} = 1 mA I_{STAT} = -1 mA	6.0	6.8 -0.7	8.0	V

6 Current, voltage conventions and truth table

Figure 5. **Current and voltage conventions**

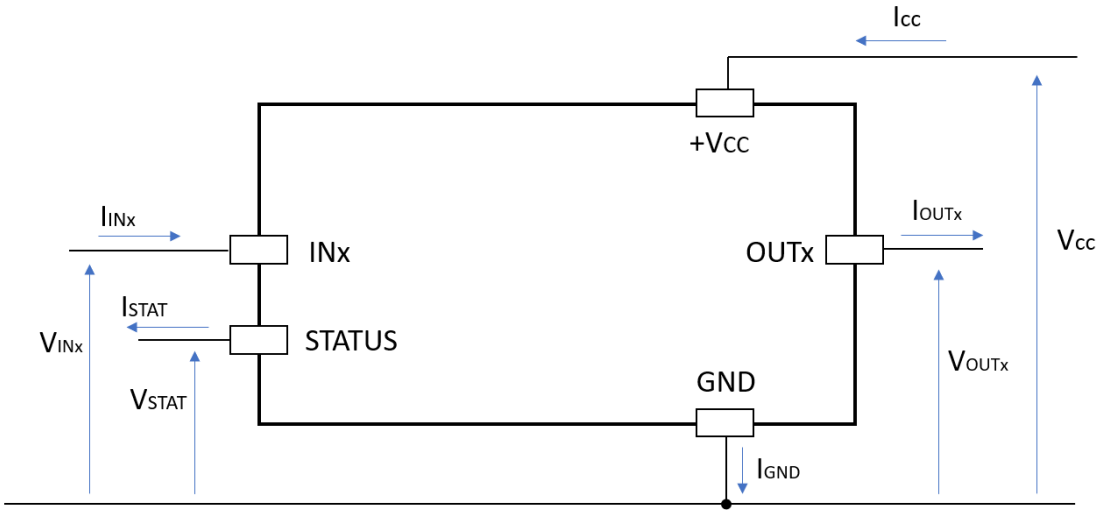


Table 9. **Truth table**

Conditions	INPUTx	OUTPUTx	STATUS
Normal operation	L H	L H	L L
Current limitation	L H	L X(1)	L L
Overtemperature (see Figure 10 and Figure 11)	L H	L L	L H
Undervoltage	L H	L L	X X

1. *Pin voltage = I_{OUT} * R_{LOAD}*

7 Power Section

7.1 Current limitation

Current limitation process is activated when the current sense connected on the output stage measures a current value higher than a fixed threshold.

When this condition is verified, the gate voltage is modulated to prevent the output current from rising above the limitation value.

The following figures show typical output current waveforms with different load conditions.

Figure 6. Switching on resistive and on bulb lamp load

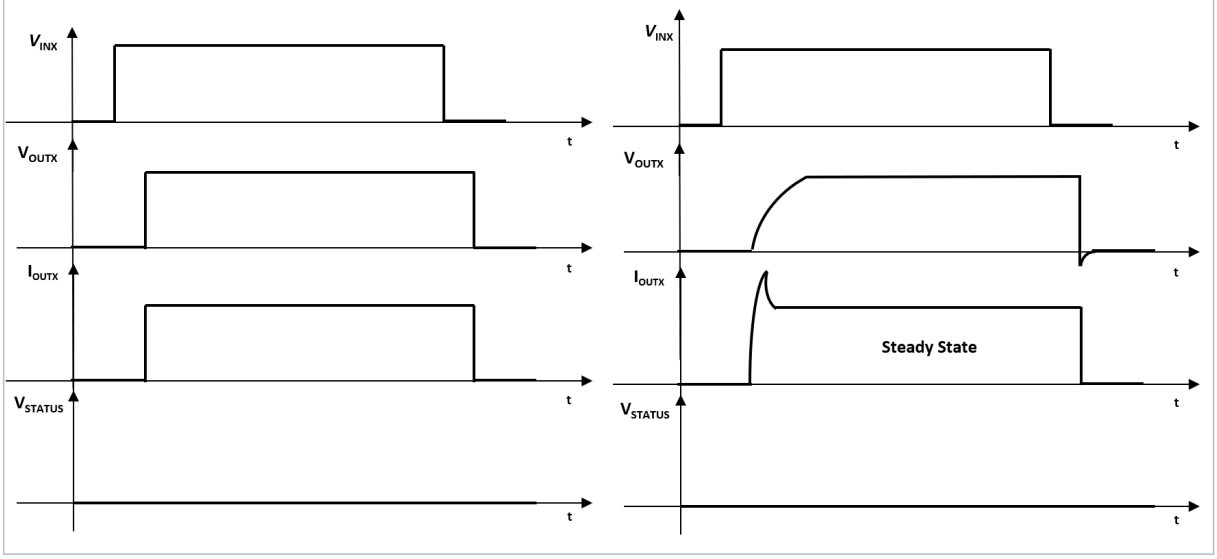


Figure 7. Switching on light and heavy inductive load

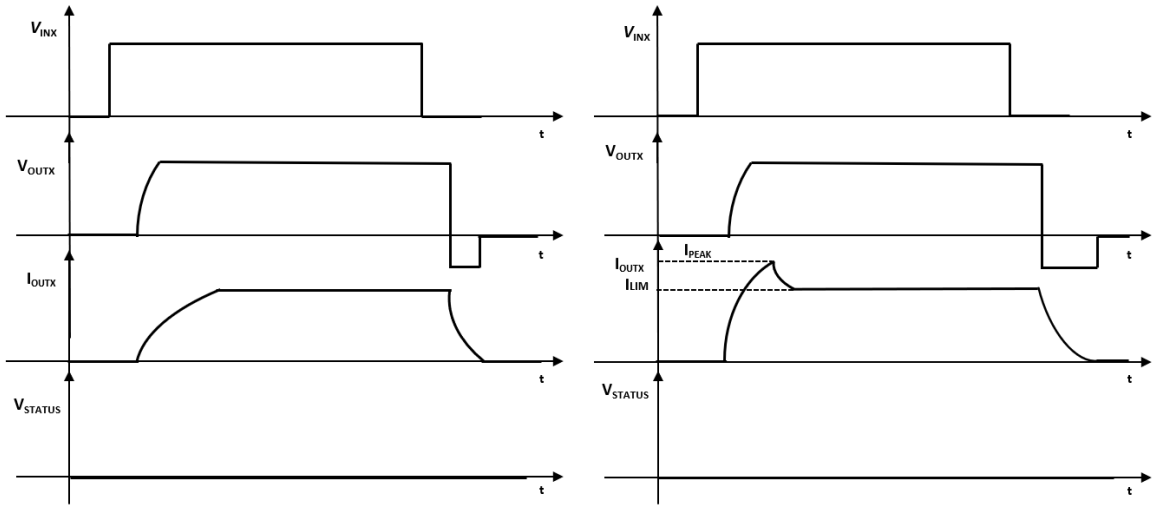
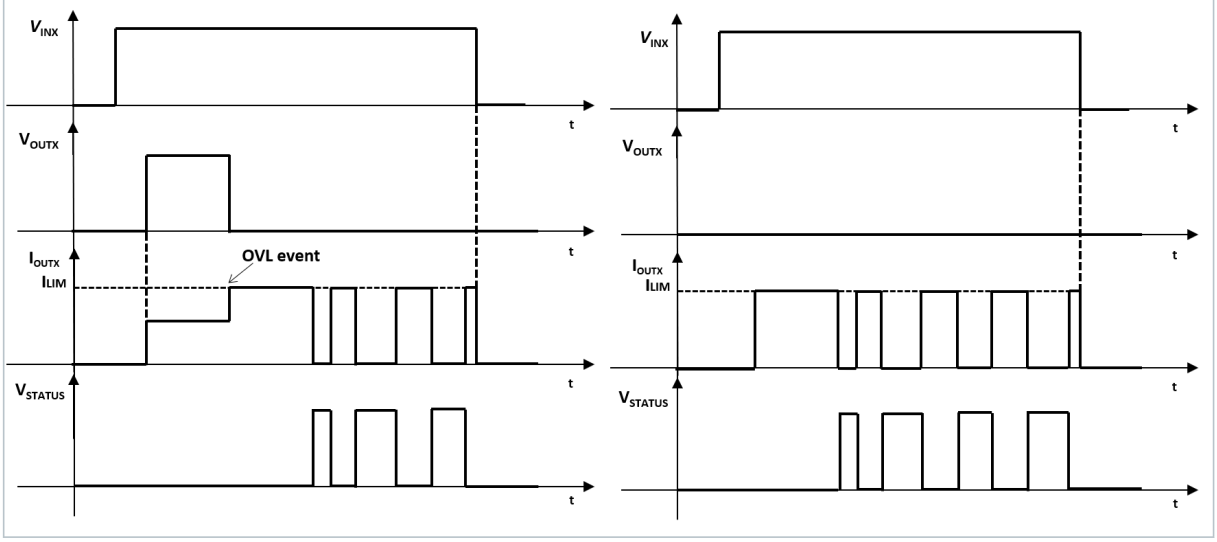


Figure 8. **Short-circuit during ON-state and switching on short-circuit**



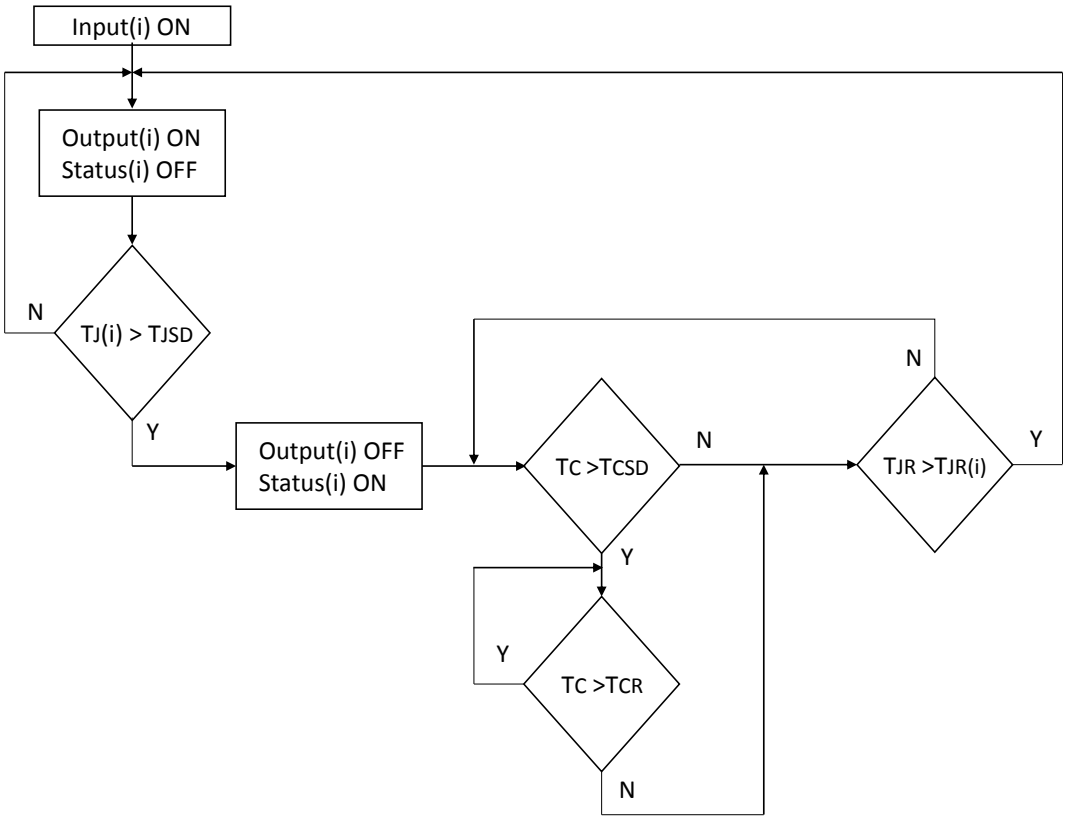
7.2 Thermal protection

The device is protected against overheating due to overload conditions. During the driving period, if the output is overloaded, the device suffers two different thermal stresses, the first is related to the junction, and the second related to the case.

The two faults have different trigger thresholds: the junction protection threshold (T_{JSD}) is higher than the case protection one (T_{CSD}); generally the first protection that is activated in thermal stress conditions is the junction thermal shutdown. The output is turned off when the temperature is higher than the related threshold and turned back on when it goes below the reset threshold (T_{JR}). This behavior continues until the fault on the output is present.

If the thermal protection is active and the temperature of the package increases over the fixed case protection threshold, the case protection is activated and the output is switched off and back on when the junction temperature, of each channel in fault and case temperature, are below the respective reset thresholds.

Figure 9. **Thermal protection flowchart**



7.3 Status indication

The Status pin is an active high common open source output indicating fault conditions. This pin is activated in case of junction overtemperature (T_{JX} >T_{JSD}) of one or more output channels. Figure 10 and Figure 11 show the STATUS behavior when T_{JSD} is triggered before T_{CSD} and when T_{CSD} is triggered before T_{JSD} respectively.

Figure 10. **Thermal protection and STATUS behavior (T_{JSD} triggered before T_{CSD})**

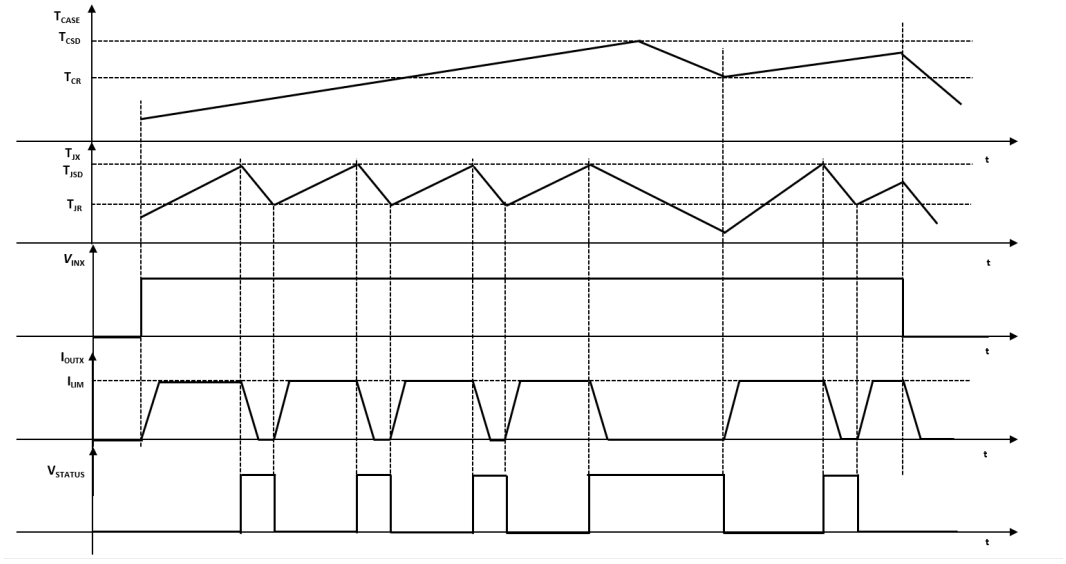
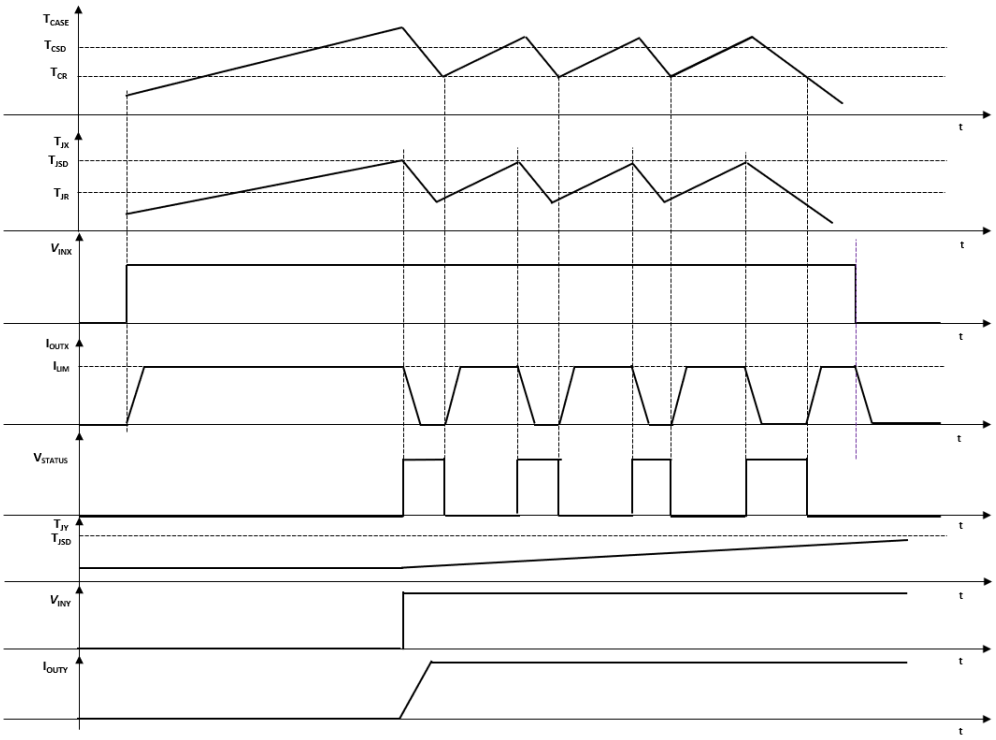


Figure 11. **Thermal protection and STATUS behavior (T_{CSD} triggered before T_{JSD})**



8 Reverse polarity protection

Reverse polarity protection can be implemented on board using two different solutions:

1. Placing a resistor (R_{GND}) between IC GND pin and load GND
2. Placing a diode between IC GND pin and load GND

If option 1 is selected, the minimum resistance value has to be selected according to the following equation:

$$R_{GND} \geq V_{CC} / I_{GND}$$

where I_{GND} is the DC reverse ground pin current and can be found in Section 3 of this datasheet.

Power dissipated by R_{GND} (when $V_{CC} < 0$, reverse polarity situations) is:

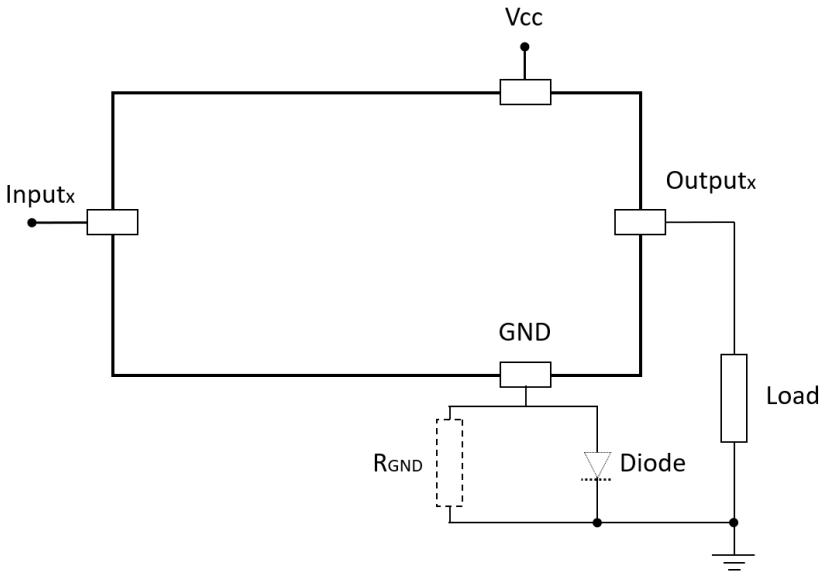
$$P_D = (V_{CC})^2 / R_{GND}$$

If option 2 is selected, the diode has to be chosen by taking into account VRRM > $|V_{cc}|$ and its power dissipation capability:

$$P_D \geq I_S \times V_f$$

Note: In normal operation (no reverse polarity), there is a voltage drop (ΔV) between GND of the device and GND of the system. Using option 1, $\Delta V = R_{GND} \times I_{CC}$; using option 2, ΔV = VF@(IF).

Figure 12. V_{CC} Reverse Polarity Protection



This schematic can be used with any type of load.

9 Active clamp

Active clamp is also known as Fast Demagnetization of inductive loads or Fast Current Decay. When a high-side driver turns off an inductance, an undervoltage on the output is detected.

The OUT pin is pulled down to V_{CC}-V_{DEMAG}. The conduction state is modulated by an internal circuitry in order to keep the OUT pin voltage at ~V_{DEMAG} until the load energy has been dissipated. The energy is dissipated in both IC internal switch and load resistance.

Figure 13. Active clamp typical waveforms

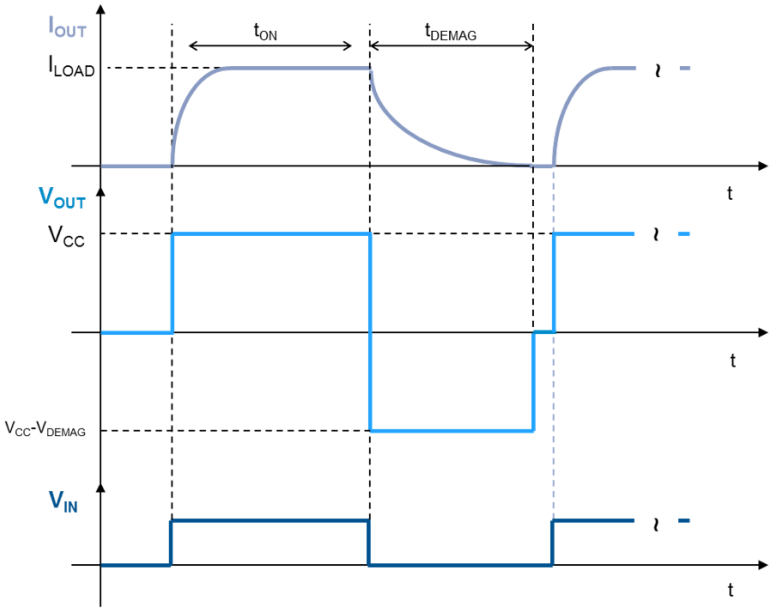
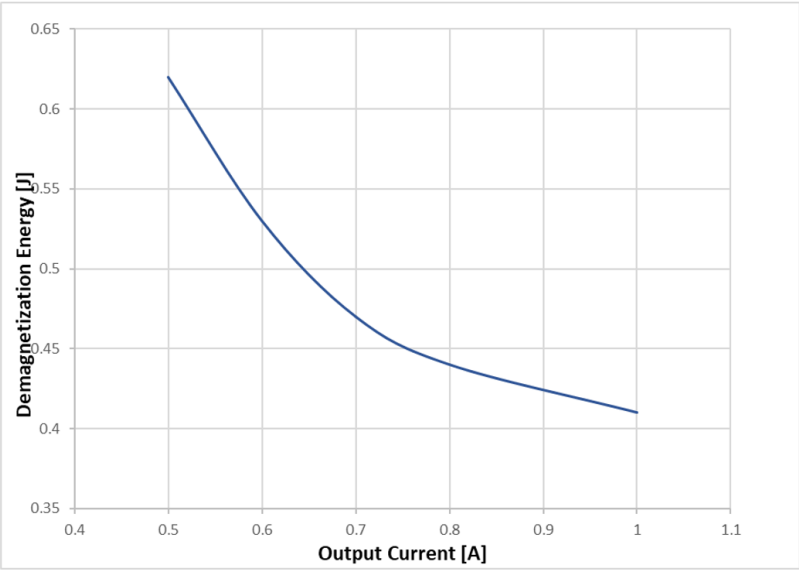


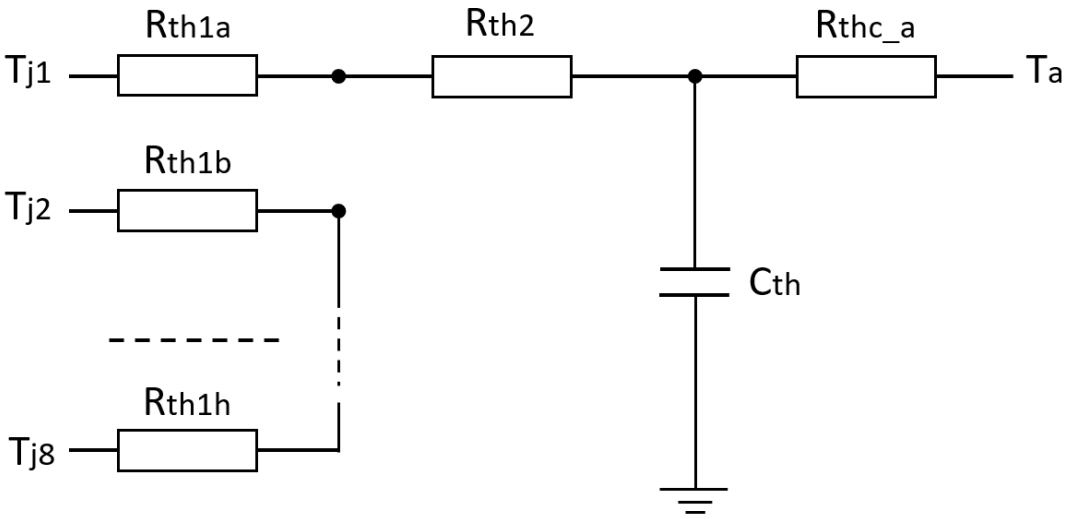
Figure 14. Typical demagnetization energy (single pulse, all channels) at V_{CC} = 24 V and T_{AMB} = 125 °C



10 Thermal information

10.1 Thermal impedance

Figure 15. **Simplified thermal model of the process stage**



11 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com

ECOPACK is an ST trademark.

11.1 QFN48L 8x6 mm package mechanical data

Figure 16. QFN48L 8x6 mm package information

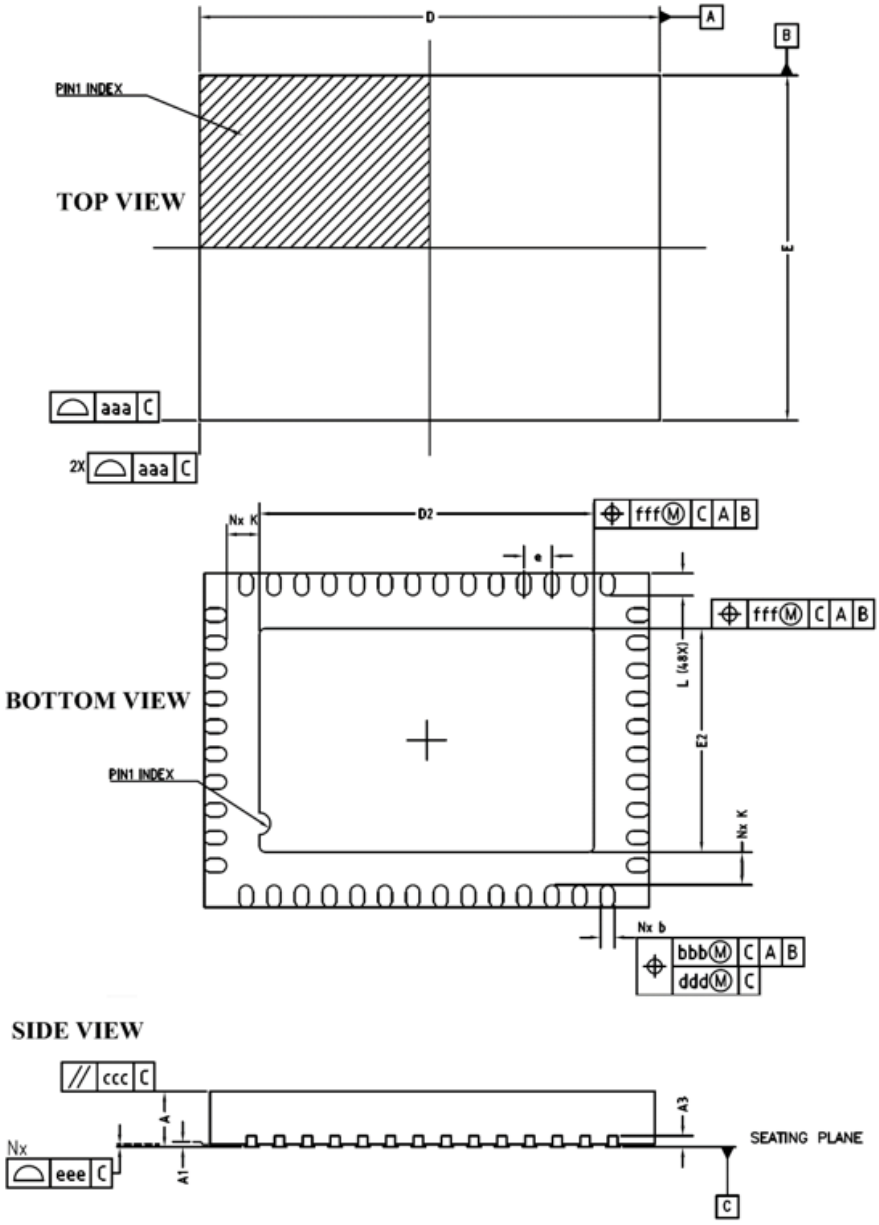


Table 10. QFN48L 8x6 mm package mechanical data

Symbol	[mm]			Note
	Min.	Nom.	Max.	
A	0.80	0.85	0.90	12
A1	0.00	-	0.05	9, 12
A3		0.2 REF		
b	0.20	0.25	0.30	5, 6, 7, 12, 13
D		8 BSC		4, 12
e		0.50 BSC		
E		6.00 BSC		4, 12
D2	5.97	6.02	6.07	
E2	3.97	4.02	4.07	
L	0.365	0.40	0.435	12, 13
k	0.53			
N		48		8

Table 11. Tolerance of forms and positions

Symbol	Tolerance of form and position	
aaa	0.10	
bbb	0.10	
ccc	0.10	
ddd	0.05	
eee	0.08	
fff	0.10	
Note	1,12	
REF		

NOTES (to be reported on column "Note" of package mechanical data table)

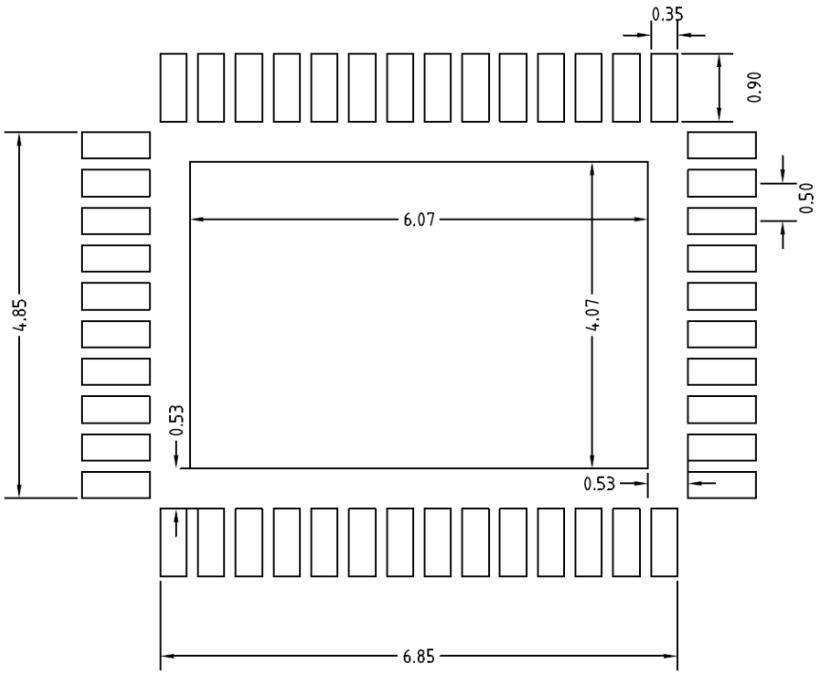
1. Dimensioning and tolerancing schemes conform to ASME Y14.5M-1994.
2. All the dimensions are in mm.
3. Terminal A1 identifier and terminal numbering convention shall conform to JEP95 SPP-002. Terminal A1 identifier must be located within the zone indicated on the outline drawing. Topside terminal A1 indicator may be molded, or metalized feature. Optional indicator on bottom surface may be a molded, marked, or metallized feature.
4. Outlines with "D" and "E" increments less than 0.5 mm should be registered as "standalone" outlines. These outlines should use as many of the algorithms and dimensions states in the design standard as possible to ensure predictability in manufacturing.
5. Dimension "b" applies to the metalized terminal and is measured between 0.15 mm and 0.30 mm from the terminal tip. If the terminal has the optional radius on the other end of the terminal, the dimension "b" should not be measured in that radius area.
6. Inner edge of corner terminals may be chamfered or rounded in order to achieve minimum gap "k". This feature should not affect the terminal with "b", which is measured L/2 from the edge of the package body.
7. Exact shape of the leads at the edge of the package is optional.

8. "N" is the maximum number of terminal positions for the specified body size. Depopulation is allowed, but only under the following conditions:
   – Depopulation scheme must be consistent in each quadrant of the package
   – Non-symmetric variations should be broken out as separate mechanical outline variations, including depopulation graphics.
9. A1 is defined as the distance from the seating plane to the lowest point on the package body (standoff).
10. Dimension D2 and E2 refer to exposed pad. For exposed pad dimensions see Variation Table.
11. For tolerance of form and position see Table below.
12. Critical dimensions:
   – A
   – A1
   – D & E
   – b & L
   – e
   – D2 & E2
13. Dimensions "b" and "L" are measured at terminal plating surface.
14. Depending on the method of lead termination at the edge of the package, pull back (L1) maybe present. L minus L1 to be equal to or greater than 0.3 mm.
15. For Symbols, Recommended Values and Tolerances see Table below: (ACCORDING TO PACKAGE OR JEDEC SPEC IF REGISTERED).

Table 12. Definitions

Symbol	Definition	Notes
aaa	The bilateral profile tolerance that controls the position of the plastic body sides. The centers of the profile zones are defined by the basic dimensions D and E.	
bbb	The tolerance that controls the position of the entire terminal pattern with respect to Datum's A and B. The center of the tolerance zone for each terminal is defined by basic dimension "e" as related to Datum's A and B.	
ccc	The tolerance located parallel to the seating plane in which the top surface of the package must be located.	
ddd	The tolerance that controls the position of the terminals to each other. The centers of the profile zones are defined by basic dimension "e"	This tolerance is normally compounded with tolerance zone defined by bbb.
eee	The unilateral tolerance located above the seating plane where in the bottom surface of all terminals must be located.	This tolerance is commonly known as the "coplanarity" of the package terminals.
fff	The tolerance that controls the position of the exposed metal heat feature. The center of the tolerance zone is the datum's defined by the centerlines of the package body.	

Figure 17. **QFN48 8x6 mm suggested footprint [mm]**



STMicroelectronics is not responsible for PCB-related issues. The footprint shown in the above figure is a suggestion which may differ from the customer PCB supplier design rules.

12 Packing information

Figure 18. **QFN48L 8x6 mm reel shipment reference**

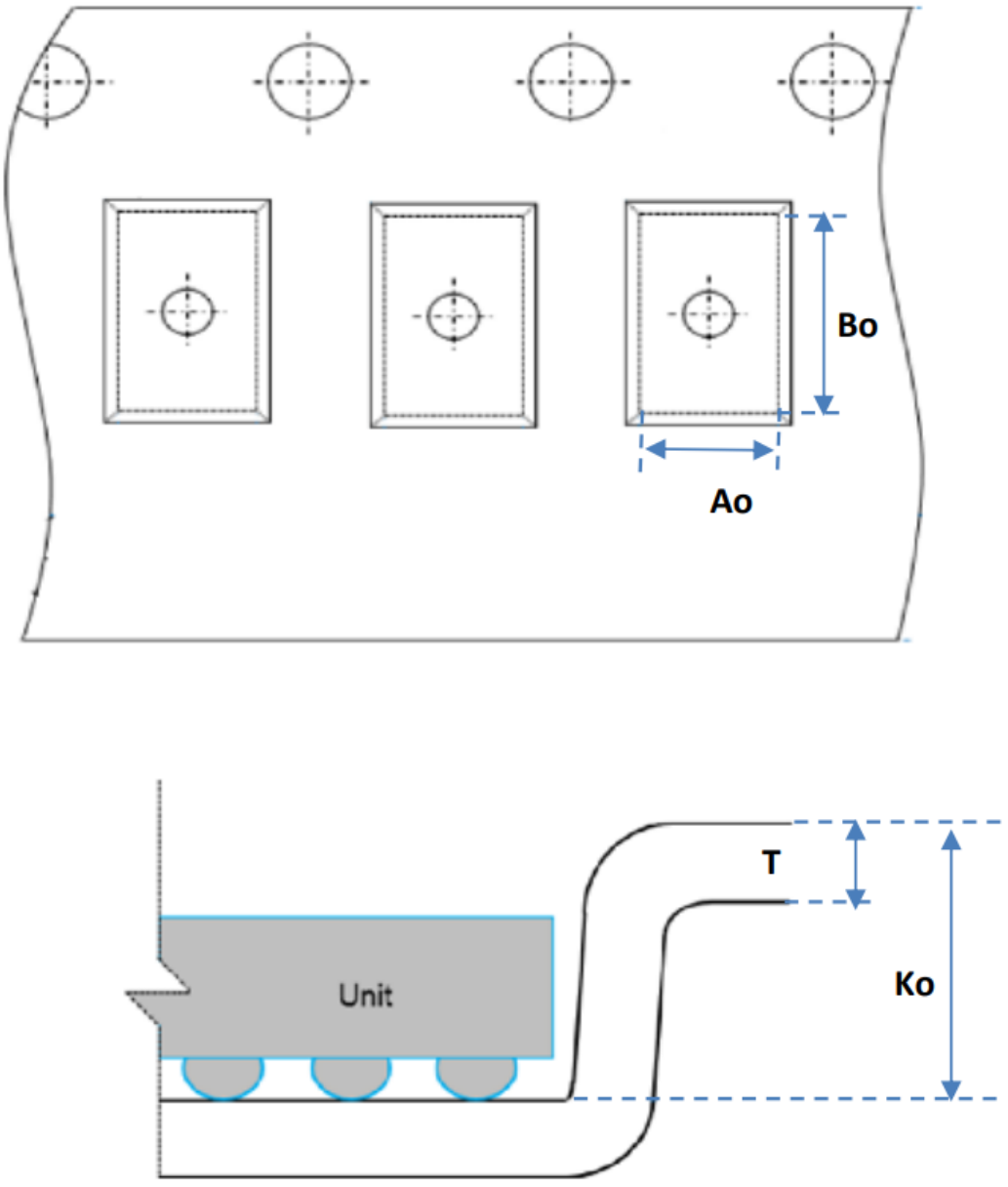
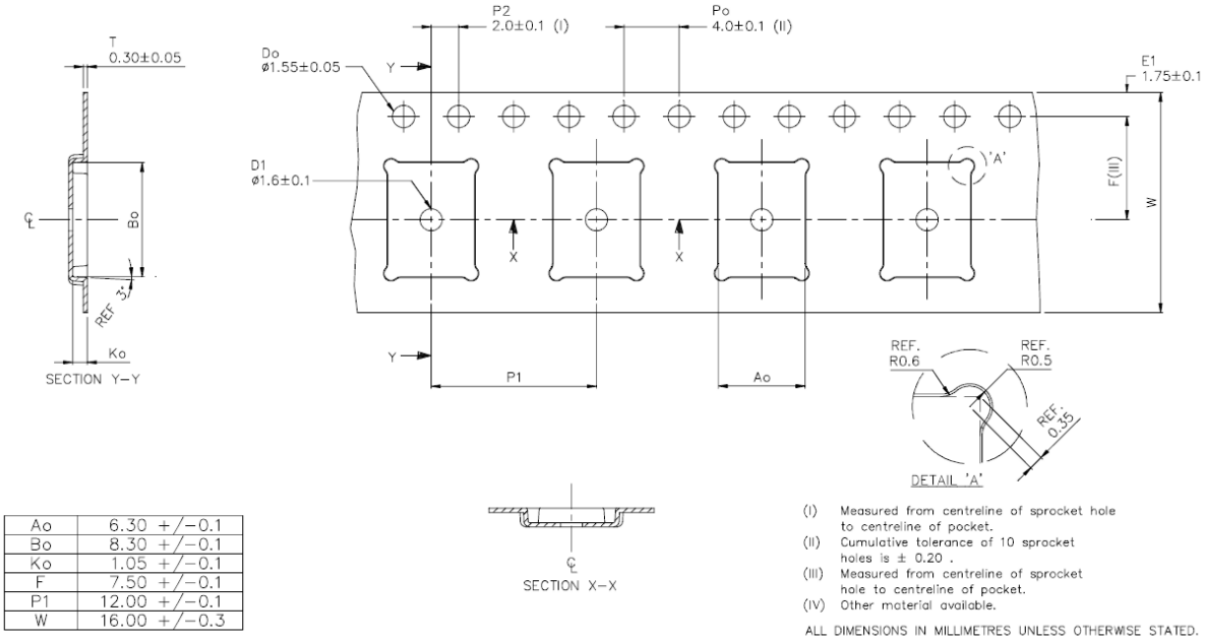


Table 13. **Standard SPC parameters**

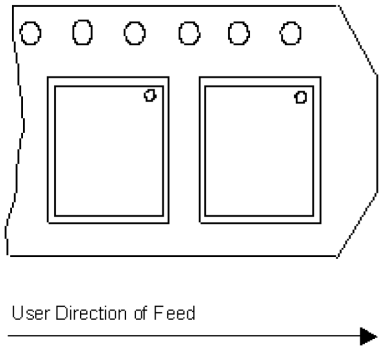
Item	Description
Ao	Pocket Length
Bo	Pocket Width
Ko	Pocket Depth
T	Tape Thickness

Figure 19. **QFN48L 8x6 mm tape dimensions**



Ao	6.30 +/−0.1
Bo	8.30 +/−0.1
Ko	1.05 +/−0.1
F	7.50 +/−0.1
P1	12.00 +/−0.1
W	16.00 +/−0.3

Figure 20. **QFN48L 8x6 mm tape, Pin 1 indication**



13 Ordering information

Table 14. **Ordering information**

Part number	Package	Packaging
IPS8160HQ	QFN48L 8x6 mm	Tape and reel
IPS8160HQ-1		

Revision history

Table 15. **Document revision history**

Date	Version	Changes
23-Dec-2022	1	Initial release.

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