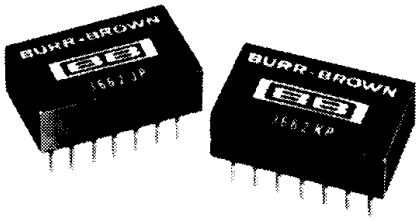
BURR-BROWN

3662



Low Offset Voltage INSTRUMENTATION AMPLIFIER

FEATURES

- **PRESERVES SIGNAL INTEGRITY**
  - **Input Impedance 2 x $10^{10}\Omega$**
  - **Gain Nonlinearity < ±0.025%**
  - **CMR > 104dB @ G = 1000**
- **REDUCES TEMPERATURE ERRORS**
  - **Voltage Drift < 2.4μV/°C @ G = 1000**
  - **Bias Current Drift < 2nA/°C**
- **EASY TO USE**
  - **Single Resistor Gain Adjust 1V/V to 1000V/V**
  - **Usually No Trimming Needed**

DESCRIPTION

The 3662 is an integrated circuit instrumentation amplifier. It is a differential input amplifier with a transfer function of

$$V_{OUT} = (e_2 - e_1)\ 100k\Omega/R_g$$

where R_g is the single external gain settling resistor.

Instrumentation amplifiers differ from operational amplifiers in that they are committed closed-loop devices. As such they only (but very accurately) amplify and have no summing junction. Their high input impedance ($2 \times 10^{10}\Omega$), large gain (1000V/V), easy gain adjustment (1V/V to 1000V/V), high common-mode rejection (> 104dB at G = 1000V/V), and low voltage drift (< 2.4μV/°C at G = 1000) eliminate the problems and compromises of trying to use operational amplifiers to realize the same gain function. Modern hybrid integrated circuit design and state-of-the-art laser-trimming techniques reduce the offset voltage to a point where the need for additional nulling by the user is normally eliminated.

The excellent performance, small size, low cost, and integrated circuit reliability make the 3662 a natural choice for applications such as thermocouples, strain gages, bridges and other low level transducers.

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

PDS-344A

DISCUSSION

NOT AN OP AMP

An instrumentation amplifier differs fundamentally from an operational amplifier. An op amp is an open loop uncommitted device whose closed loop performance depends on the external networks used to close the loop. While an op amp can be used to get the same basic transfer function as an instrumentation amplifier, it is generally difficult (often impossible) to achieve the same level of performance. The use of an op amp usually leads to design tradeoffs when it is necessary to amplify low level signals in the presence of common-mode voltages while maintaining high input impedances.

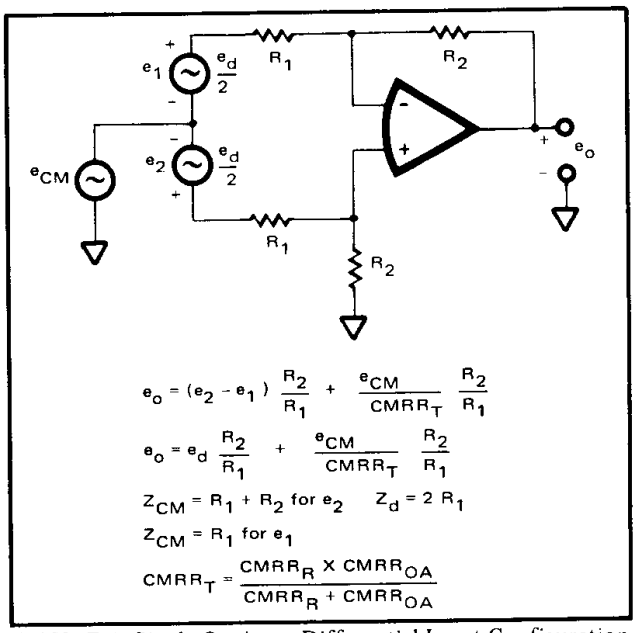


FIGURE 1 Single Op Amp, Differential Input Configuration.

When a single op amp is used (see Figure 1), there are opposing constraints if there is a need for both high gain ($R_2 \div R_1 >> 0$, i.e. R_1 small) and high input impedances (R_1 large). Also, the common-mode rejection ratio of the total circuit, $CMRR_T$, is a function of the op amps rejection, $CMRR_{OA}$, and the effective rejection caused by resistor mismatches, $CMRR_R$. [For example, ±0.1% resistors in a gain of 10 circuit can have a CMR of only 69 dB (CMR (dB) = 20 $\log_{10}$ CMRR (V/V))].

INSTRUMENTATION AMPLIFIERS

The 3662 is an integrated circuit instrumentation amplifier. It is a closed loop differential input gain block – a committed circuit whose primary function is to accurately amplify the voltage applied to its inputs. Ideally, the instrumentation amplifier responds only to the difference between the two input signals ($e_2 - e_1$) and exhibits extremely high impedance between the two input terminals (differential input impedance) and from each input to ground (common-mode input impedance). Figure 2 shows the simple model of an instrumentation amplifier which eliminates most of the problems of using op amps.

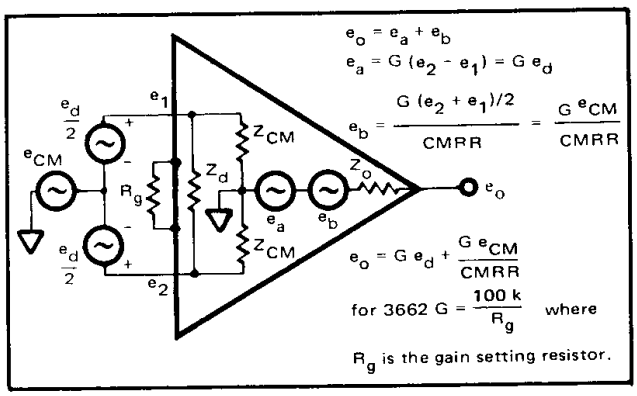


FIGURE 2. Model of an Instrumentation Amplifier.

THEORY OF OPERATION

Figure 3 is a simplified schematic of the 3662. It shows that the amplifier is basically a two stage device. It has a fixed gain output stage (shown as the op amp symbol) and a variable gain input stage (adjusted by R_g). The two stage nature of the design is the reason that many of the specifications consist of two components, one of which is a function of gain.

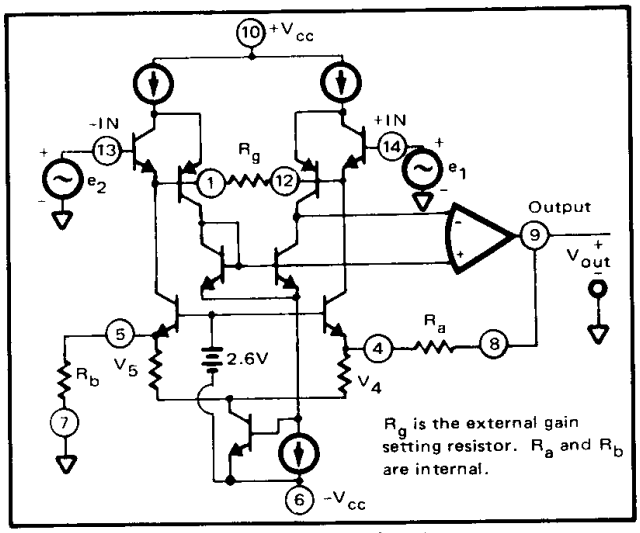


FIGURE 3. Simplified Schematic of 3662.

An analysis of the circuit in Figure 3 is straightforward but lengthy even with simplifying assumptions. Therefore, only the results are given below:

$$V_{out} = (e_1 - e_2)\frac{2R_a}{R_g} + R_a\left(\frac{V_4}{R_a} - \frac{V_5}{R_b}\right) \qquad (1)$$

Equation (1) consists of two parts. The first part is the desired gain equation where R_g is the gain setting resistor and R_a is the output stage feedback resistor (internal 50kΩ). The second part is an output component of offset voltage whose magnitude is dependent on the matching of R_a and R_b. In the 3662 this component of error is significantly reduced by the use of advanced laser trimming techniques and hybrid construction. In fact, the entire offset voltage is reduced to the point where the user nulling usually required with other instrumentation amplifiers is normally not necessary with the 3662.

SPECIFICATIONS

ELECTRICAL

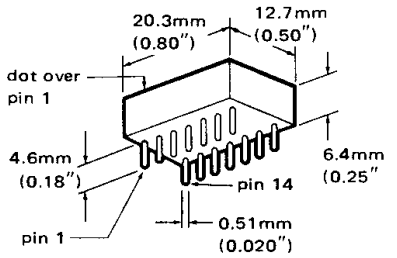
Specifications typical at 25°C and ±15 VDC Power Supply Unless Otherwise Noted.

MODELS	3662JP	3662KP
GAIN		
Range of Gain, min	G = 1 to 1000 V/V	
Gain Equation	$G = \frac{100\ k\Omega}{R}$ V/V	
Error from Equation (may be zeroed)	(±0.5 -0.003G)%	
Gain Temp. Coefficient	±(50 +0.05G)ppm/°C	
Nonlinearity (1) G = 1 - 1000, max	0.1%	0.05%
OUTPUT		
Rated output, min	±10 V, ±10 mA	
Output Impedance	0.15 Ω	
INPUT		
Input Impedance, Differential	$\frac{2 \times 10^{10}}{G}$ Ω ‖ 9 pF	
Common-Mode	2×10^{10} Ω ‖ 3 pF	
Input Voltage Range, min	±10 V	
CMR, DC to 60 Hz with 1kΩ source unbalance		
G = 1, min	60 dB	66 dB
G = 10, min	76 dB	84 dB
G = 100, min	86 dB	94 dB
G = 1000, min	96 dB	104 dB
OFFSETS AND DRIFT (RTI)		
Input Offset, max (2) (may be zeroed)	$\pm(0.4 + \frac{100}{G})$mV	$\pm(0.2 + \frac{30}{G})$mV
vs temperature, max	$\pm(5 + \frac{1000}{G})\mu V/^{\circ}C$	$\pm(2 + \frac{400}{G})\mu V^{\circ}C$
vs Supply	$\pm(8 + \frac{5000}{G})\mu V/V$	
vs Time	$\pm(2 + \frac{1500}{G})\mu V/mo$	
Input Bias Current, max (either input)	+300nA	
vs Temperature, max	-2nA/°C	
vs Supply	±0.25nA/V	
Input Difference Current, max	±80nA	±30nA
vs Temperature, max	±0.8nA/°C	±0.3nA/°C
INPUT NOISE (RTI) (2)		
Voltage, p-p 0.01 Hz -10 Hz	$(3 + \frac{900}{G})\mu V$ p-p	
RMS, 10 Hz -10 kH	$(1 + \frac{130}{G})\mu V$ RMS	
Current, p-p 0.01 Hz -10 Hz	150 pA p-p	
RMS 10 Hz -10 kHz	50 pA RMS	
DYNAMIC RESPONSE		
Small Signal, ±3 dB Flatness		
G = 1	800 kHz	
G = 10	95 kHz	
G = 100	74 kHz	
G = 1000	27 kHz	
Small Signal, ±1% Flatness		
G = 1	20 kHz	
G = 10	15 kHz	
G = 100	10 kHz	
G = 1000	3 kHz	
Full Power, G = 1 - 100	28 kHz	
Slew Rate, G = 1 - 100	1.8V/μs	
Settling Time (0.1%)		
G = 1	17 μs	
G = 10	19 μs	
G = 100	20 μs	
G = 1000	50 μs	
POWER SUPPLY		
Rated Voltage	±15 V	
Voltage Range	±7 VDC to ±20 VDC	
Quies. Supply Current, max	6mA	
TEMPERATURE RANGE		
Specifications	0 to +70°C	
Operation	-55 to +125°C	
Storage	-65 to 150°C	

(1) Peak deviation from a best straightline, expressed as a percent of peak-to-peak full scale output.

(2) RTI = referred to input. May be referred to output by multiplying by gain G.

MECHANICAL



Row Spacing: 7.6mm (0.300")
Weight: 3.4 grams (0.12 oz.)
Connector: 14-pin DIP
0145MC

Pin material and plating composition conform to Method 208 (solderability) of Mil-Std-202.

PIN CONNECTIONS

1. Gain	8. Sense
2. V_{OSI}	9. Out
3. V_{OSI}	10. $+V_{CC}$
4. V_{OSO}	11. Make No Connection
5. V_{OSO}	12. Gain
6. $-V_{CC}$	13. -In
7. Ref	14. +In

CONNECTION DIAGRAM

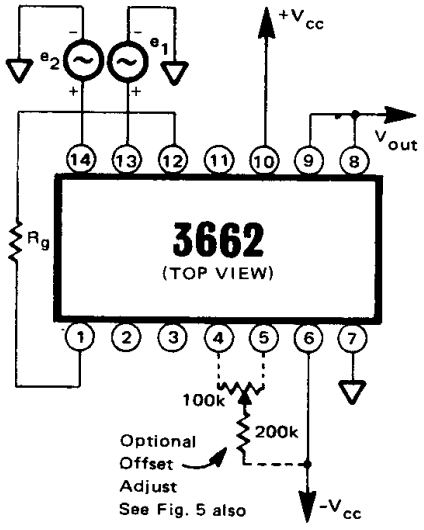
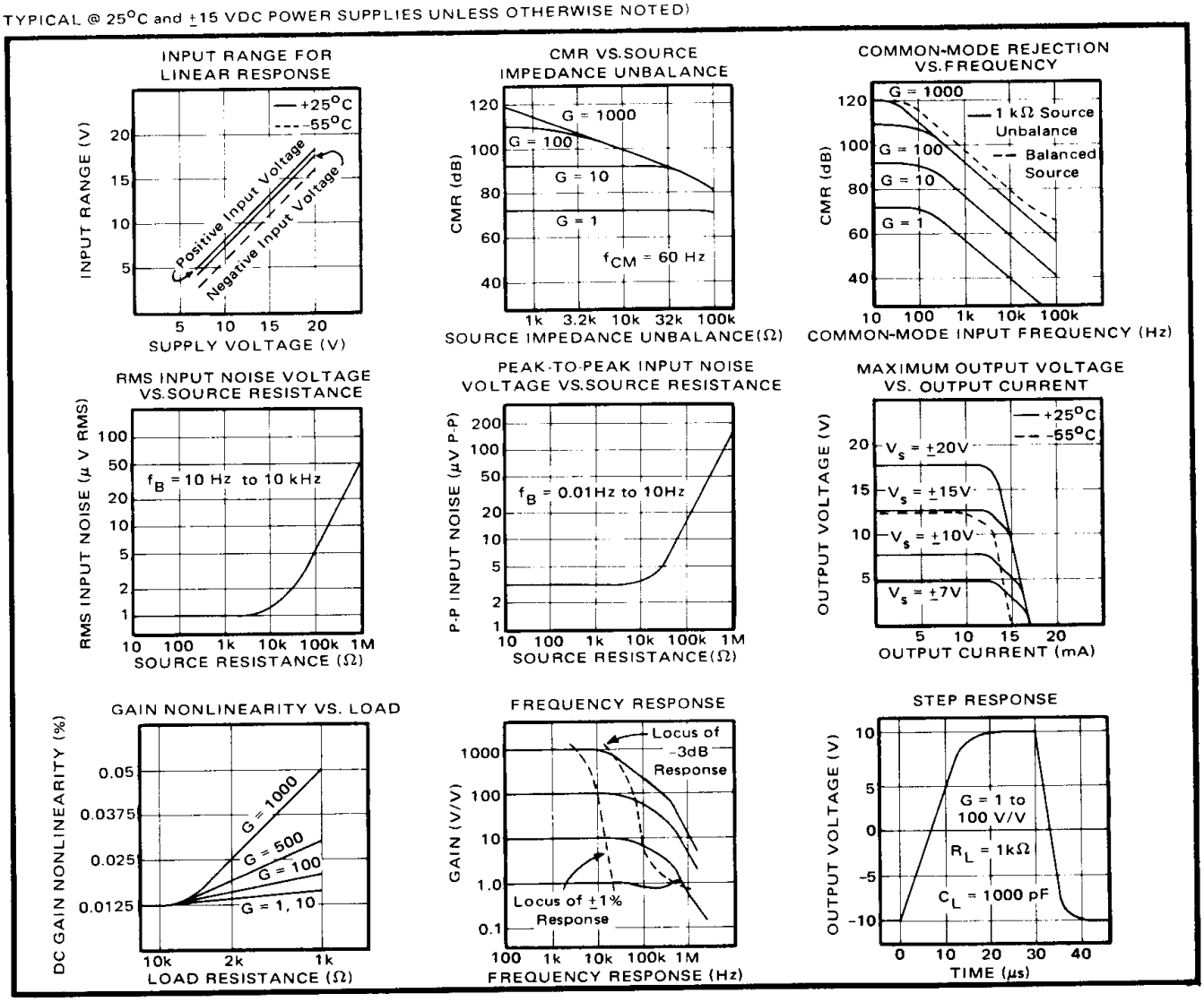


FIGURE 4

TYPICAL PERFORMANCE CURVES

(TYPICAL @ 25°C and ±15 VDC POWER SUPPLIES UNLESS OTHERWISE NOTED)



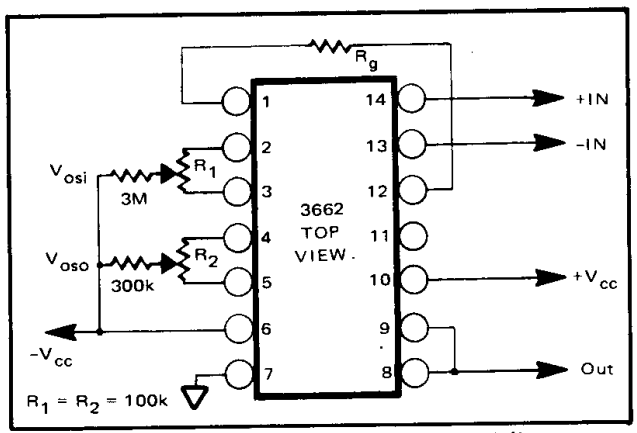


FIGURE 5. Alternate Optional Offset Voltage Adjustment.

The circuit in Figure 4 uses a single adjustment to trim both input and output components of offset voltage. Because of this the output voltage will change when the gain is varied. The circuit in Figure 5 trims the two components separately and minimizes the gain change problem. Adjust R_2 at minimum gain and then adjust R_1 at maximum gain.

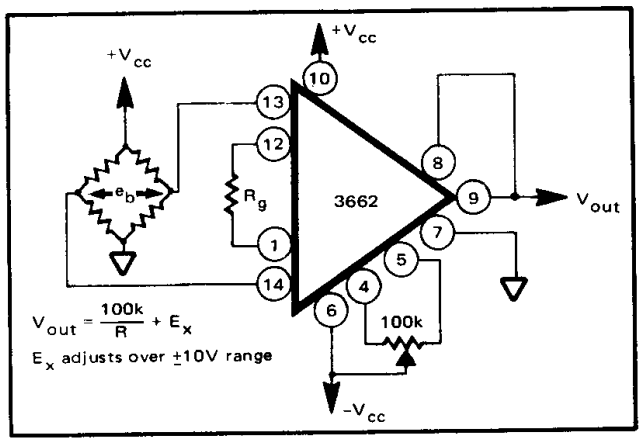


FIGURE 6. Output Biasing.

When it is desired to bias the output over a large range (such as chart recorder bias) the circuit in Figure 6 may be used.