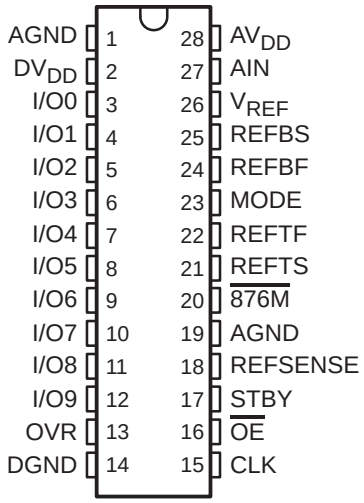
- **10-Bit Resolution 30 MSPS Analog-to-Digital Converter:**
- **Configurable Input: Single-Ended or Differential**
- **Differential Nonlinearity: ±0.3 LSB**
- **Signal-to-Noise: 57 dB**
- **Spurious Free Dynamic Range: 60 dB**
- **Adjustable Internal Voltage Reference**
- **Out-of-Range Indicator**
- **Power-Down Mode**
- **Pin Compatible with TLC876**

28-PIN TSSOP/SOIC PACKAGE
(TOP VIEW)



description

The THS1030 is a CMOS, low power, 10-bit, 30 MSPS analog-to-digital converter (ADC) that can operate with a supply range from 2.7 V to 3.3 V. The THS1030 has been designed to give circuit developers more flexibility. The analog input to the THS1030 can be either single-ended or differential. The THS1030 provides a wide selection of voltage references to match the user's design requirements. For more design flexibility, the internal reference can be bypassed to use an external reference to suit the dc accuracy and temperature drift requirements of the application. The out-of-range output is used to monitor any out-of-range condition in THS1030s input range.

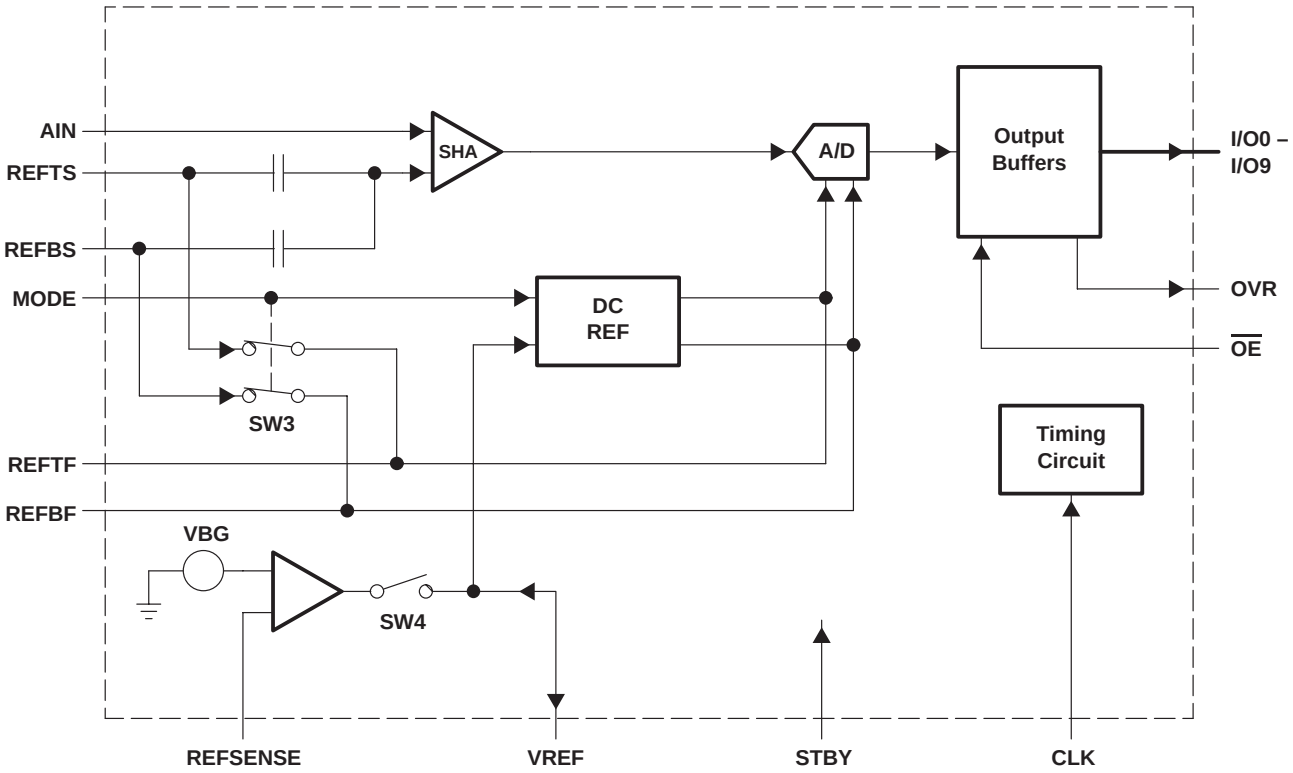
The speed, resolution, and single-supply operation of the THS1030 are suited for applications in STB, video, multimedia, imaging, high-speed acquisition, and communications. The speed and resolution ideally suit charge-couple device (CCD) input systems such as color scanners, digital copiers, digital cameras, and camcorders. A wide input voltage range between REFBS and REFTS allows the THS1030 to be applied in both imaging and communications systems.

The THS1030I is characterized for operation from –40°C to 85°C

AVAILABLE OPTIONS

T_A	PACKAGED DEVICES	
	28-TSSOP (PW)	28-SOIC (DW)
0°C to 70°C	THS1030CPW	THS1030CDW
–40°C to 85°C	THS1030IPW	THS1030IDW

functional block diagram



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
AGND	1, 19	I	Analog ground
AIN	27	I	Analog input
AV_{DD}	28	I	Analog supply
CLK	15	I	Clock input
DGND	14	I	Digital ground
DV_{DD}	2	I	Digital driver supply
I/O0	3	I/O	Digital I/O bit 0 (LSB)
I/O1	4		Digital I/O bit 1
I/O2	5		Digital I/O bit 2
I/O3	6		Digital I/O bit 3
I/O4	7		Digital I/O bit 4
I/O5	8		Digital I/O bit 5
I/O6	9		Digital I/O bit 6
I/O7	10		Digital I/O bit 7
I/O8	11		Digital I/O bit 8
I/O9	12		Digital I/O bit 9 (MSB)
MODE	23	I	Mode input
$\overline{OE}$	16	I	HI to the 3-state data bus, LO to enable the data bus
OVR	13	O	Out-of-range indicator
REFBS	25	I	Reference bottom sense
REFBF	24	I	Reference bottom decoupling
REFSENSE	18	I	Reference sense
REFTF	22	I	Reference top decoupling
REFTS	21	I	Reference top sense
STBY	17	I	HI = power down mode, LO = normal operation mode
V_{REF}	26	I/O	Internal and external reference for ADC
$\overline{876M}$	20	I	HI = THS1030 mode, LO = TLC876 mode (see section 4 for TLC876 mode)

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage: AV_{DD} to AGND, DV_{DD} to DGND . . . . . –0.3 to 6.5 V
AGND to DGND . . . . . –0.3 to 0.3 V
AV_{DD} to DV_{DD} . . . . . –6.5 to 6.5 V
Mode input MODE to AGND . . . . . –0.3 to AV_{DD} + 0.3 V
Reference voltage input range REFTF, REFTB, REFTS, REFBS to AGND . . . . . –0.3 to AV_{DD} + 0.3 V
Analog input voltage range AIN to AGND . . . . . –0.3 to AV_{DD} + 0.3 V
Reference input V_{REF} to AGND . . . . . –0.3 to AV_{DD} + 0.3 V
Reference output V_{REF} to AGND . . . . . –0.3 to AV_{DD} + 0.3 V
Clock input CLK to AGND . . . . . –0.3 to AV_{DD} + 0.3 V
Digital input to DGND . . . . . –0.3 to DV_{DD} + 0.3 V
Digital output to DGND . . . . . –0.3 to DV_{DD} + 0.3 V
Operating junction temperature range, T_J . . . . . 0°C to 150°C
Storage temperature range, T_{STG} . . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 in) from case for 10 seconds . . . . . 300°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

digital inputs

	MIN	NOM	MAX	UNIT
High-level input voltage, V_{IH}	2.4			V
Low-level input voltage, V_{IL}			0.2 x DV_{DD}	V

analog inputs

	MIN	NOM	MAX	UNIT
Analog input voltage, $V_{I(AIN)}$	REFBS		REFTS	V
Reference input voltage, $V_{I(VREF)}$	1		2	V
Reference input voltage, $V_{I(REFTS)}$	1		AV_{DD}	V
Reference input voltage, $V_{I(REFBS)}$	0		AV_{DD}–1	V

power supply

			MIN	NOM	MAX	UNIT
Supply voltage	Maximum sampling rate = 30 MSPS	AV_{DD}	2.7	3	5.5	V
		DV_{DD}	2.7	3	5.5	

REFTS, REFBS reference voltages (MODE = AV_{DD})

PARAMETER		MIN	NOM	MAX	UNIT
REFTS	Reference input voltage (top)	1		AV_{DD}	V
REFBS	Reference input voltage (bottom)	0		AV_{DD}–1	V
	Differential input (REFTS – REFBS)	1		2	V
	Switched input capacitance on REFTS		0.5		pF

sampling rate and resolution

PARAMETER	MIN	NOM	MAX	UNIT
Fs	5		30	MSPS
Resolution		10		Bits

electrical characteristics over recommended operating conditions, AV_{DD} = 3 V, DV_{DD} = 3 V, Fs = 30 MSPS/50% duty cycle, MODE = AV_{DD}, 2 V input span from 0.5 V to 2.5 V, external reference, T_A = –40°C to 85°C (unless otherwise noted)

analog inputs

PARAMETER		MIN	TYP	MAX	UNIT
$V_{I(AIN)}$	Analog input voltage	REFBS		REFTS	V
C_I	Switched input capacitance		1.2		pF
FPBW	Full power BW (–3 dB)		150		MHz
	DC leakage current (input = ±FS)		60		µA

VREF reference voltages

PARAMETER	MIN	TYP	MAX	UNIT
Internal 1 V reference (REFSENSE = V_{REF})	0.95	1	1.05	V
Internal 2 V reference (REFSENSE = AV_{SS})	1.90	2	2.10	V
External reference (REFSENSE = AV_{DD})	1		2	V
Reference input resistance		18		kΩ

REFTF, REFBF reference voltages

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Differential input (REFTF – REFBF)			1		2	V
Input common mode (REFTF + REFBF)/2		AV_{DD} = 3 V	1.3	1.5	1.7	V
		AV_{DD} = 5 V	2	2.5	3	
REFTF (MODE = AV_{DD})	V_{REF} = 1 V	AV_{DD} = 3 V		2		V
		AV_{DD} = 5 V		3		
	V_{REF} = 2 V	AV_{DD} = 3 V		2.5		V
		AV_{DD} = 5 V		3.5		
REFBF (MODE = AV_{DD})	V_{REF} = 1 V	AV_{DD} = 3 V		1		V
		AV_{DD} = 5 V		0.5		
	V_{REF} = 2 V	AV_{DD} = 3 V		2		V
		AV_{DD} = 5 V		1.5		
Input resistance between REFTF and REFBF				600		Ω

dc accuracy

PARAMETER		MIN	TYP	MAX	UNIT
INL	Integral nonlinearity		±1	±2	LSB
DNL	Differential nonlinearity		±0.3	±1	LSB
	Offset error		0.4	1.4	%FSR
	Gain error		1.4	3.5	%FSR
	Missing code	No missing code assured			

electrical characteristics over recommended operating conditions, AV_{DD} = 3 V, DV_{DD} = 3 V, Fs = 30 MSPS/50% duty cycle, MODE = AV_{DD}, 2 V input span from 0.5 V to 2.5 V, external reference, T_A = –40°C to 85°C (unless otherwise noted) (continued)

dynamic performance

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ENOB	Effective number of bits	f = 3.5 MHz	8.4	9		Bits
		f = 3.5 MHz, AV_{DD} = 5 V		9		
		f = 15 MHz, 3 V		7.8		
		f = 15 MHz, AV_{DD} = 5 V		7.7		
SFDR	Spurious free dynamic range	f = 3.5 MHz	56	60.6		dB
		f = 3.5 MHz, AV_{DD} = 5 V		64.6		
		f = 15 MHz		48.5		
		f = 15 MHz, AV_{DD} = 5 V		53		
THD	Total harmonic distortion	f = 3.5 MHz		–60	–56	dB
		f = 3.5 MHz, AV_{DD} = 5 V		–66.9		
		f = 15 MHz		–47.5		
		f = 15 MHz, AV_{DD} = 5 V		–53.1		
SNR	Signal-to-noise	f = 3.5 MHz	53	57		dB
		f = 3.5 MHz, AV_{DD} = 5 V		56		
		f = 15 MHz		53.1		
		f = 15 MHz, AV_{DD} = 5 V		49.4		
SINAD	Signal-to-noise and distortion	f = 3.5 MHz	52.5	56		dB
		f = 3.5 MHz, AV_{DD} = 5 V		56		
		f = 15 MHz		48.6		
		f = 15 MHz, AV_{DD} = 5 V		48.1		

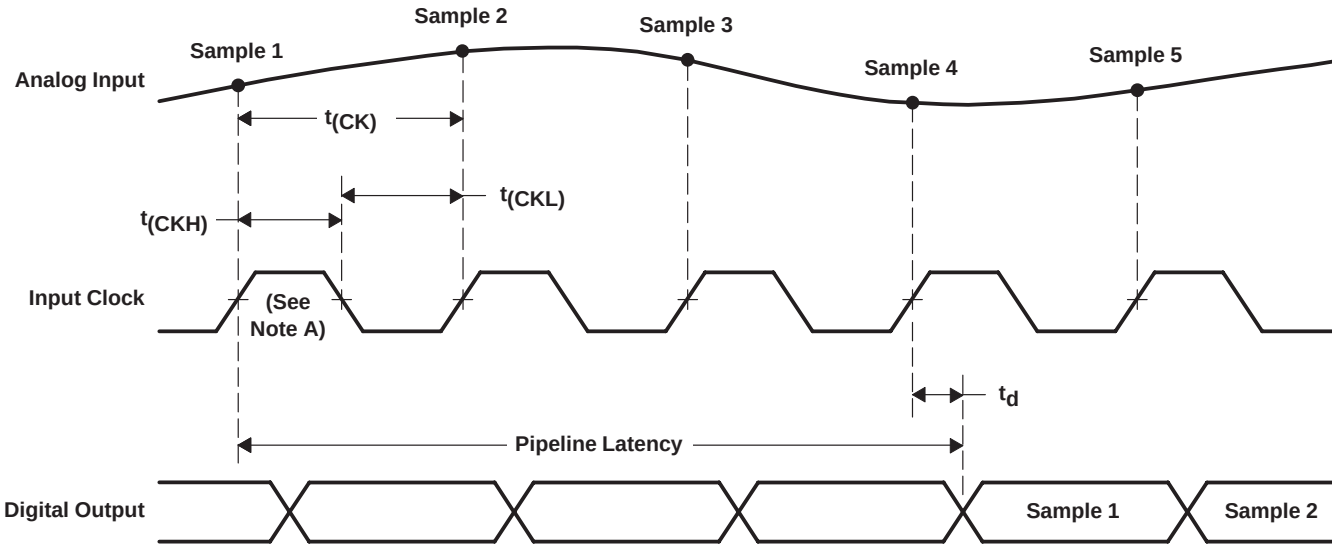
clock

PARAMETER		MIN	TYP	MAX	UNIT
$t_{(CK)}$	Clock period	33			ns
$t_{(CKH)}$	Pulse duration, clock high	15	16.5		ns
$t_{(CKL)}$	Pulse duration, clock low	15	16.5		ns
t_d	Clock to data valid			20	ns
	Pipeline latency		3		Cycles
$t_{(ap)}$	Aperture delay		4		ns
	Aperture uncertainty (jitter)		2		ps

power supply

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CC}	Operating supply current	AV_{DD} =DV_{DD} = 3 V, MODE = AGND		29	40	mA
P_D	Power dissipation	AV_{DD} = DV_{DD} = 3 V		87	120	mW
		AV_{DD} = DV_{DD} = 5 V		150		
P_D(STBY)	Standby power	AV_{DD} =DV_{DD} = 3 V, MODE = AGND		3	5	mW

PARAMETER MEASUREMENT INFORMATION



NOTE A: All timing measurements are based on 50% of edge transition.

Figure 1. Digital Output Timing Diagram

TYPICAL CHARACTERISTICS

POWER
vs
SAMPLING FREQUENCY

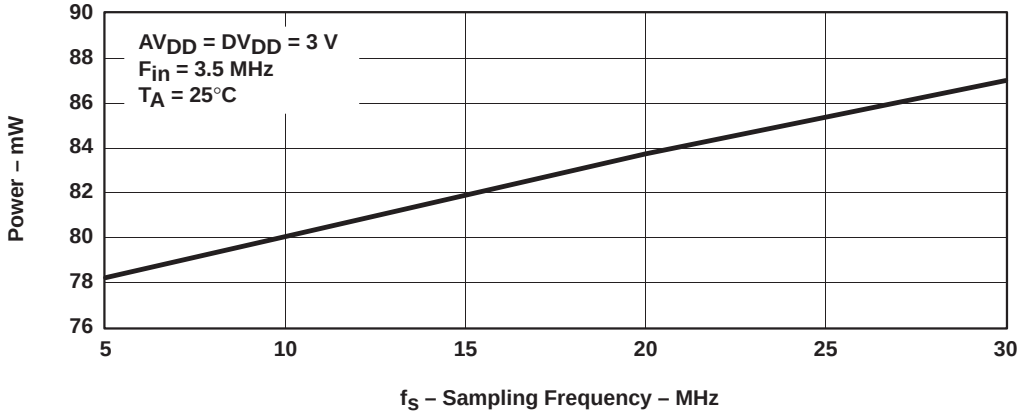


Figure 2

EFFECTIVE NUMBER OF BITS
vs
TEMPERATURE

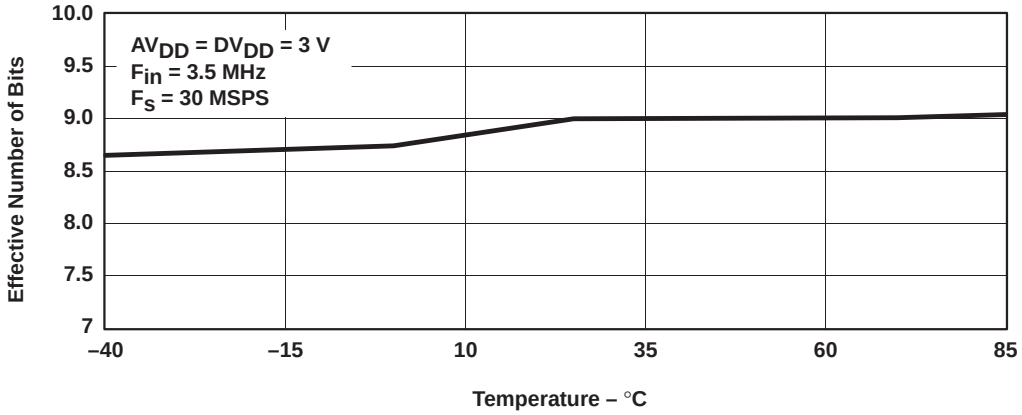


Figure 3

TYPICAL CHARACTERISTICS

EFFECTIVE NUMBER OF BITS
vs
FREQUENCY

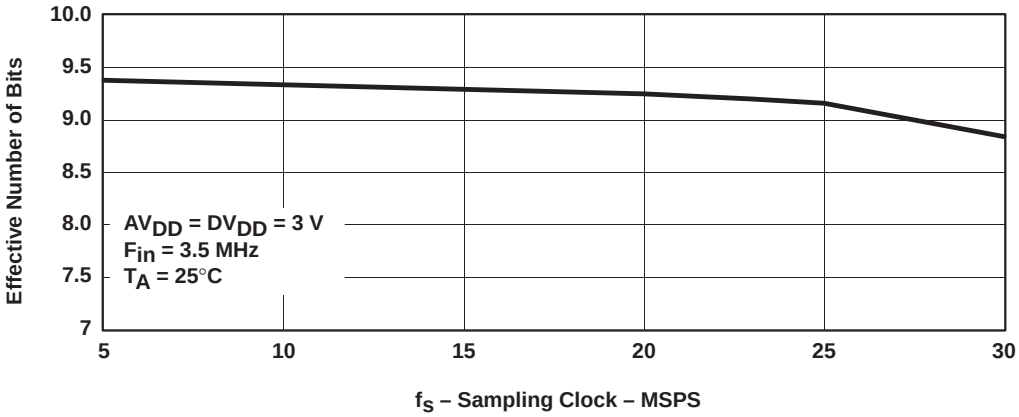


Figure 4

EFFECTIVE NUMBER OF BITS
vs
FREQUENCY

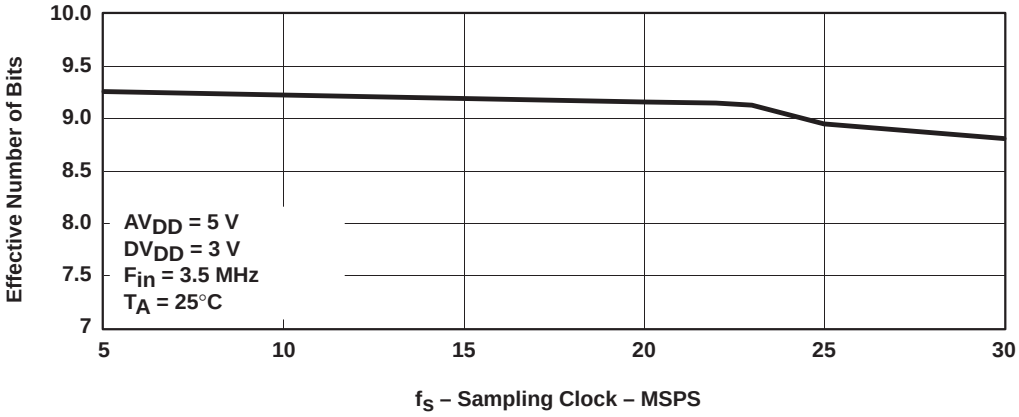


Figure 5

TYPICAL CHARACTERISTICS

EFFECTIVE NUMBER OF BITS
vs
FREQUENCY

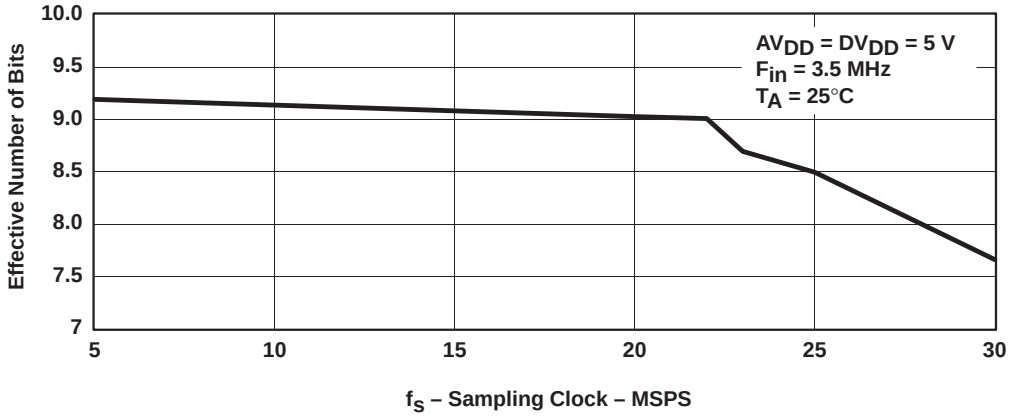


Figure 6

DIFFERENTIAL NONLINEARITY
vs
INPUT CODE

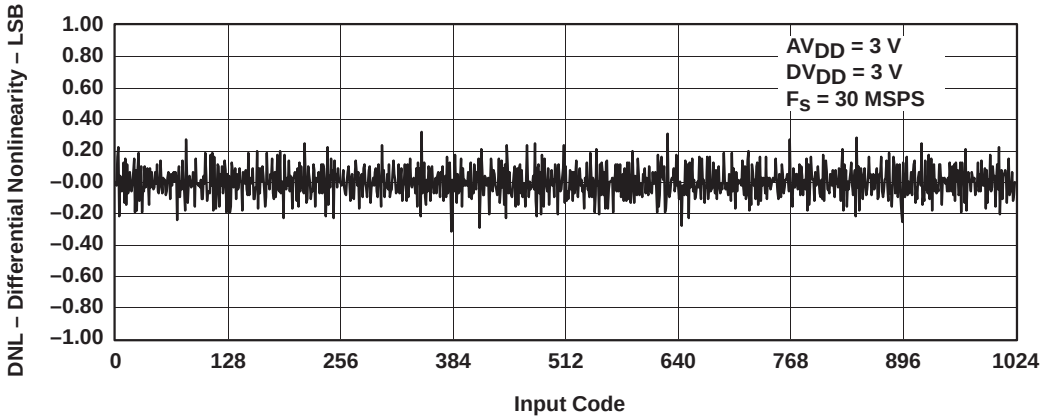


Figure 7

TYPICAL CHARACTERISTICS

INTEGRAL NONLINEARITY
vs
INPUT CODE

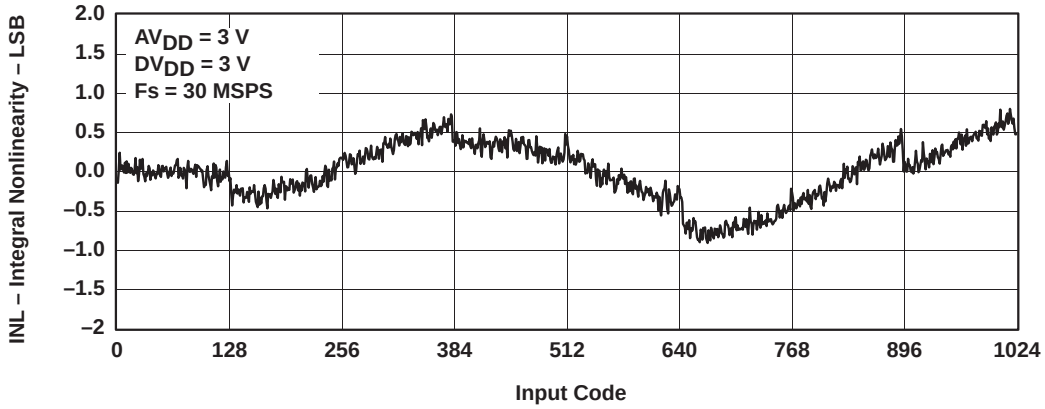


Figure 8

FFT
vs
FREQUENCY

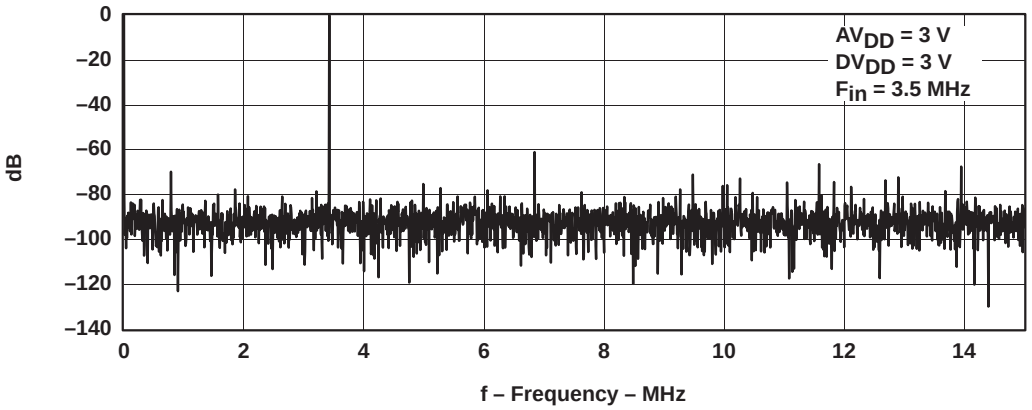


Figure 9

PRINCIPLES OF OPERATION

Table 1. Mode Selection

MODES	ANALOG INPUT	INPUT SPAN	MODE PIN	REFSENSE PIN	VREF PIN	REFTS PIN	REFBS PIN	FIGURE
Top/bottom	AIN	1 V	AV_{DD}	Short together			AGND	7, 14
	AIN	2 V	AV_{DD}	AGND	Short together		AGND	8, 15
	AIN	$1+R_a/R_b$	AV_{DD}	Mid R_a & R_b	Short together to R_a		AGND	9, 14, 15
	AIN	External V_{REF}	AV_{DD}	AV_{DD}	NC	NC	AGND	10, 14, 15
Center span	AIN	1 V	$AV_{DD}/2$	Short together		Short together to the common mode voltage		7, 13
	AIN	2 V	$AV_{DD}/2$	AGND	NC			8, 13
	AIN	$1+R_a/R_b$	$AV_{DD}/2$	Mid R_a & R_b	R_a			9, 13
	AIN	V_{REF}	$AV_{DD}/2$	AV_{DD}	External			10, 13
External reference	AIN	2 V max	AGND	See Note 1	See Note 1	Voltage within supply (REFTS–REBS) = 2 V max		11, 12
Differential input	AIN is input 1 REFTS & REFBS are shorted together for input 2	1 V	AV_{DD}	Short together		Short together $AV_{DD}/2$		16
		2 V	AV_{DD}	AGND	NC			
		V_{REF}	AV_{DD}	AV_{DD}	External			

NOTE 1: In external reference mode, V_{REF} can be available for external use with CENTER SPAN set-up.

reference operations

V_{REF}-pin reference

The voltage reference sources on the V_{REF} pin are controlled by the REFSENSE pin as shown in Table 2.

Table 2. V_{REF} Reference Selection

REFSENSE	V_{REF}
AGND	2 V
AV_{DD}	The internal reference is disabled and an external reference should be connected to V_{REF} pin.
Short to V_{REF}	1 V
Connect to R_a/R_b	$1+R_a/R_b$

- 1-V reference: The internal reference may be set to 1 V by connecting REFSENSE to V_{REF}.

PRINCIPLES OF OPERATION

V_{REF}-pin reference (continued)

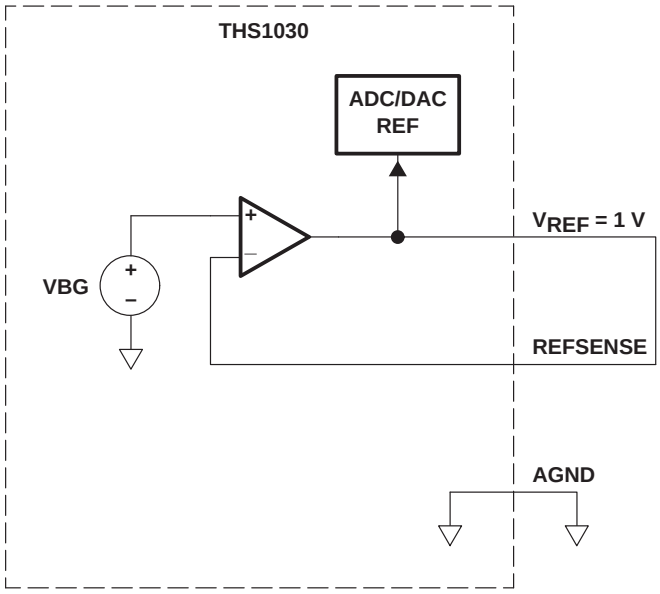


Figure 10. V_{REF} 1-V Reference Mode

- 2-V reference: The internal reference may be set to 2 V by connecting REFSENSE to AGND.

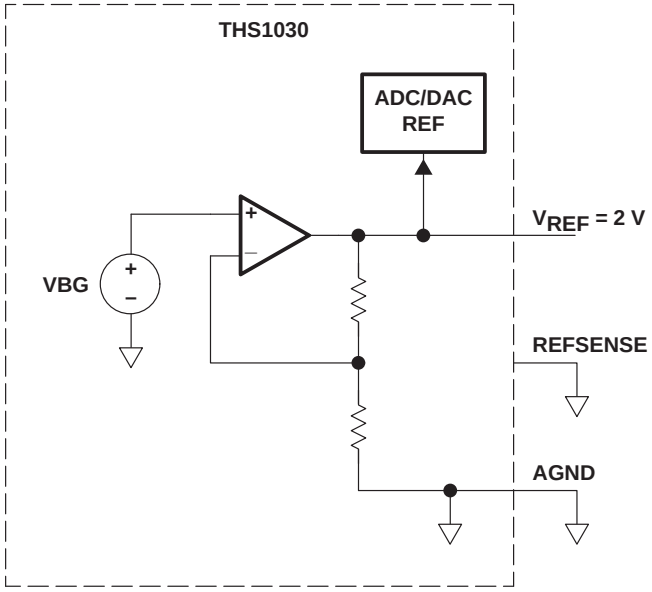


Figure 11. V_{REF} 2-V Reference Mode

- External divider: The internal reference can be set to a voltage between 1 V and 2 V by adding external resistors.

PRINCIPLES OF OPERATION

V_{REF}-pin reference (continued)

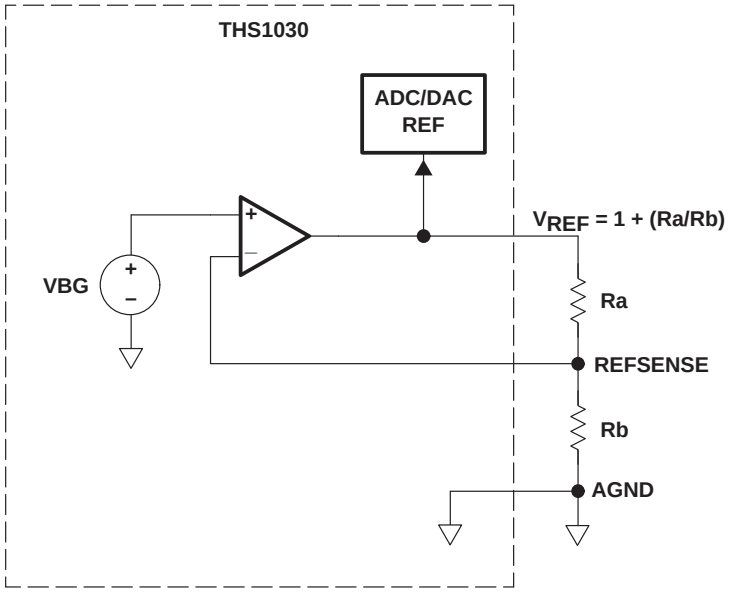


Figure 12. V_{REF} External-Divider Reference Mode

- External reference: The internal reference may be overridden by using an external reference. This condition is met by connecting REFSENSE to AV_{DD} and an external reference circuit to the V_{REF} pin.

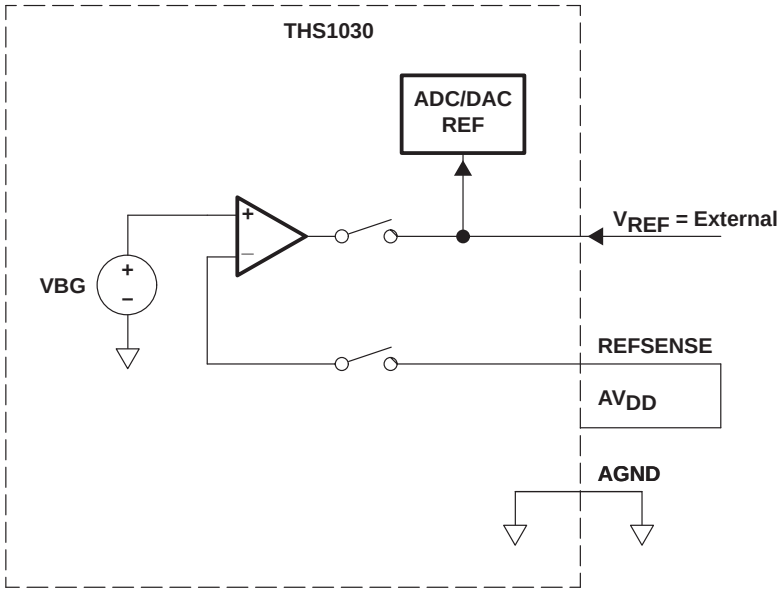


Figure 13. V_{REF} External Reference Mode

PRINCIPLES OF OPERATION

ADC reference

The MODE pin is used to select the reference source for the ADC.

- **Internal ADC Reference:** Connect the MODE pin to AV_{DD} to use the reference source for ADC generated on the V_{REF} pin. (See V_{REF} REFERENCE described in Table 2) such that (REFTF–REFBF) = V_{REF} and (REFTF+REFBF)/2 is set to a voltage for optimum operation of the ADC (near $AV_{DD}/2$).
- **External ADC Reference:** To supply an external reference source to the ADC, connect the MODE pin to AGND. An external reference source should be connected to REFTF/REFTS and REFBF/REFBS. MODE = AGND closes internal switches to allow a Kelvin connection through REFTS/REFBS, and disables the on-chip amplifiers which drive on to the ADC references. Differential input is not supported

analog input mode

single-ended input

The single-ended input can be configured to work with either an external ADC reference or internal ADC reference.

- **External ADC Reference Mode**: A single-ended analog input is accepted at the AIN pin where the input signal is bounded by the voltages on the REFTS and REFBS pins. Figure 14 shows an example of applying external reference to REFTS and REFBS pins in which REFTS is connected to the low-impedance 2-V source and REFBS is connected to the low-impedance 2-V source. REFTS and REFBS may be driven to any voltage within the supply as long as the difference (REFTS – REFBS) is between 1 V and 2 V as specified in Table 2. Figure 15 shows an example of an external reference using a Kelvin connection to eliminate line voltage drop errors.

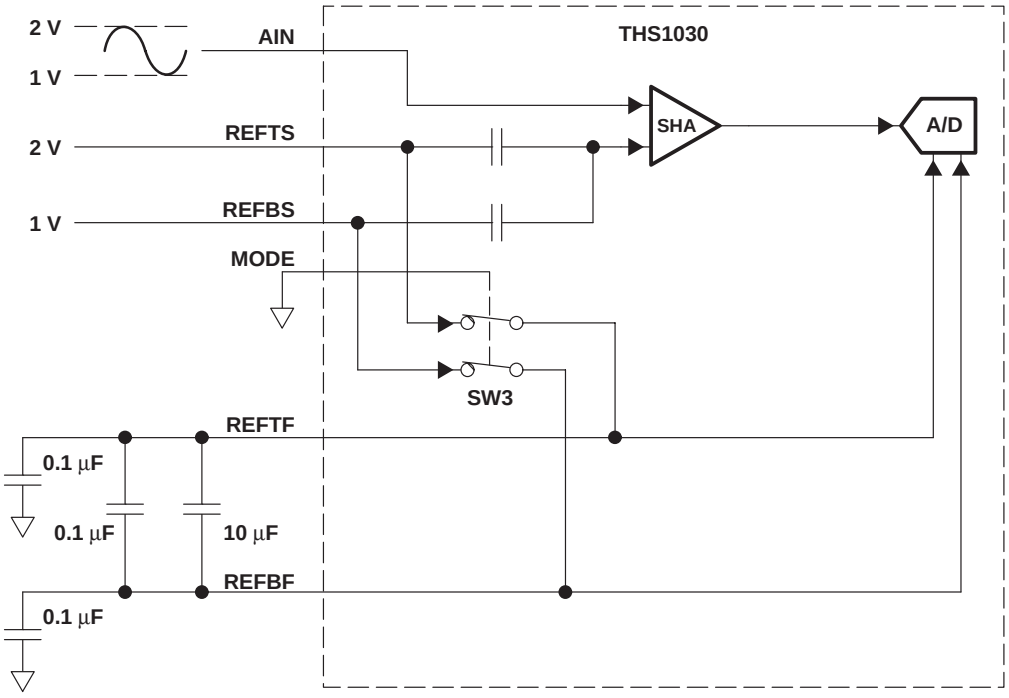


Figure 14. External ADC Reference Mode

PRINCIPLES OF OPERATION

single-ended input (continued)

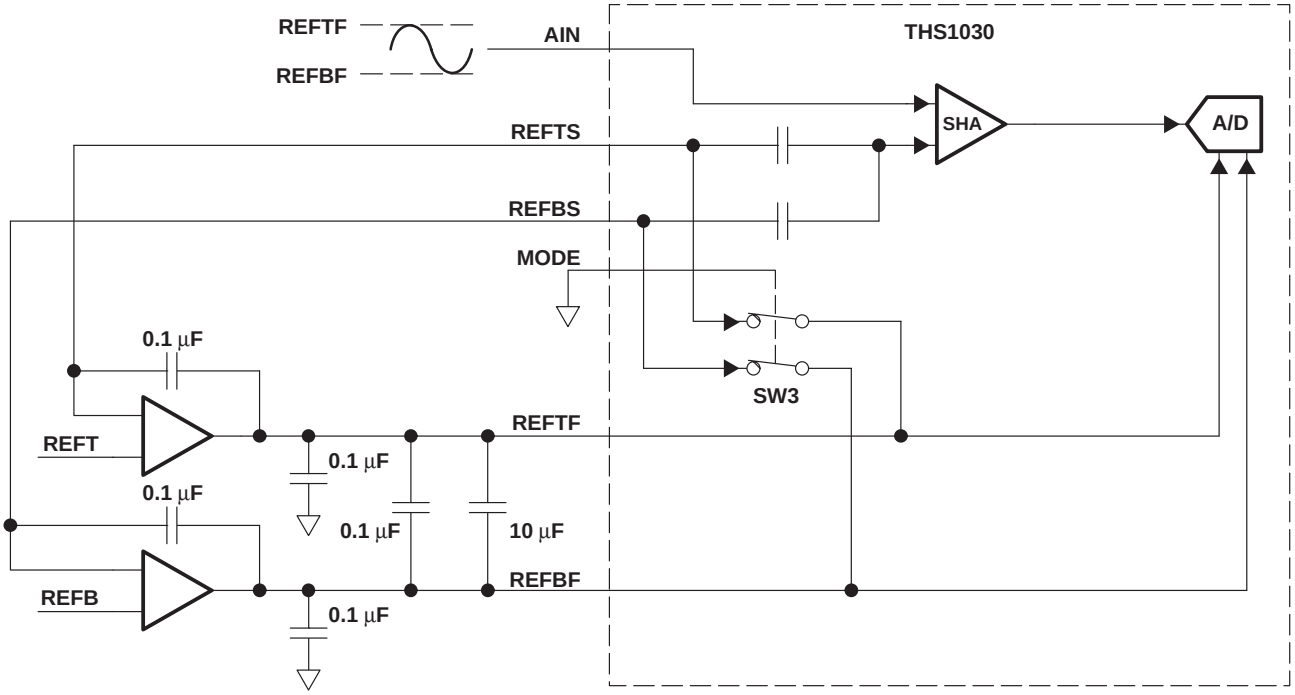


Figure 15. Kelvin Connection With External ADC Reference Mode

- **Internal ADC Reference Mode With External Input Common Mode**: The input common mode is supplied to pins REFTS and REFBS while connected together. The input signal should be centered around this common mode with peak-to-peak input equal to the voltage on the V_{REF} pin. Input can be either dc-coupled or ac-coupled to the same common mode voltage (see Figure 16) or any other voltage within the input voltage range.

PRINCIPLES OF OPERATION

single-ended input (continued)

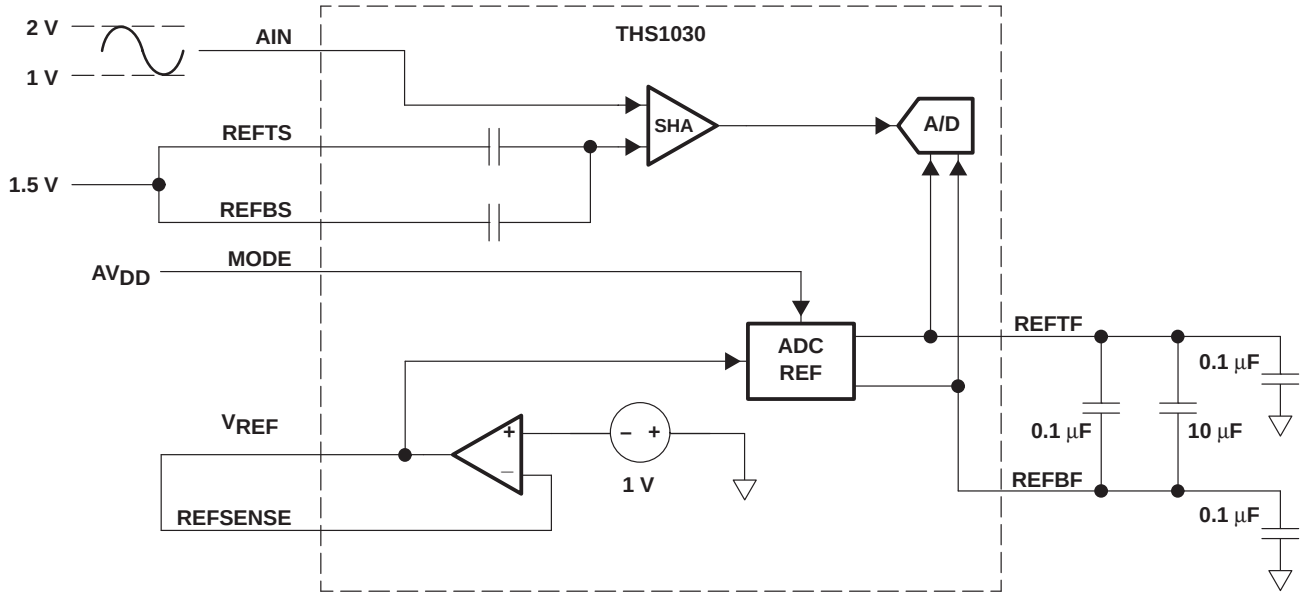


Figure 16. External Input Common Mode

- **Internal ADC Reference Mode With Common Mode Input $V_{REF/2}$**: The input common mode is set to $V_{REF}/2$ by connecting REFTS to V_{REF} and REFBS to AV_{SS}. The input signal at AIN will swing between V_{REF} and AV_{SS}.

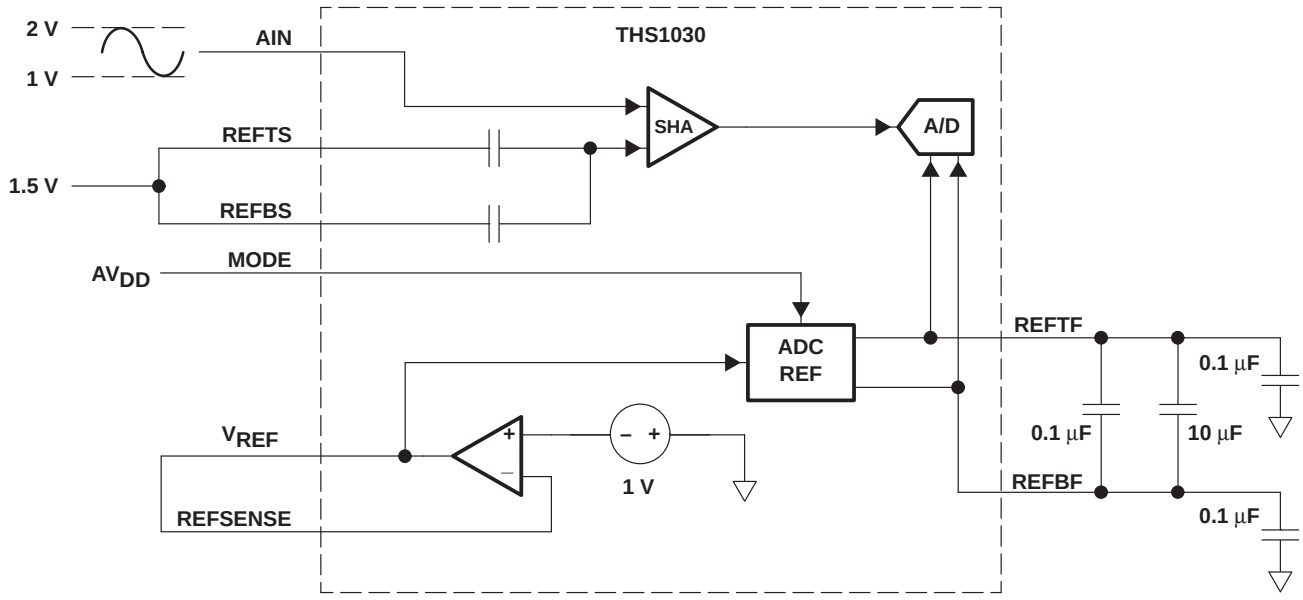


Figure 17. Common Mode Input $V_{REF}/2$ With 1-V Internal Reference

PRINCIPLES OF OPERATION

single-ended input (continued)

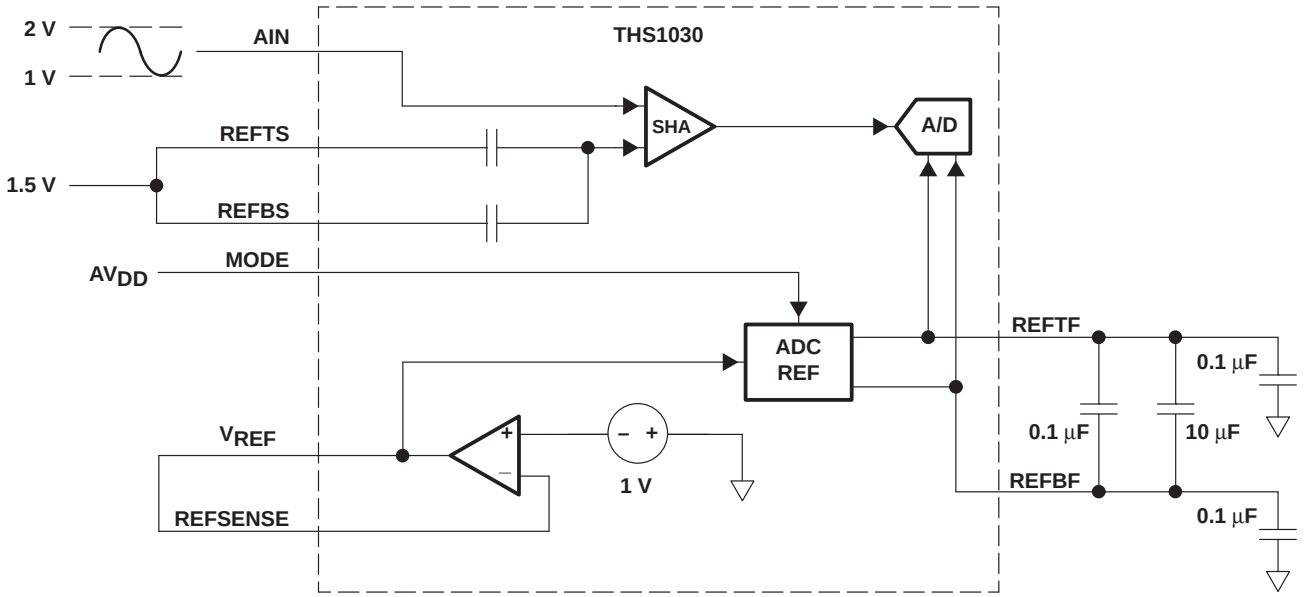


Figure 18. Common Mode Input V_{REF}/2 With 2-V Internal Reference

differential input

In this mode, the first differential input is applied to the AIN pin and the second differential input is applied to the common point where REFTS and REFBS are tied together. The common mode of the input should be set to AV_{DD}/2 as shown in Figure 19. The maximum magnitude of the differential input signal should be equal to V_{REF}.

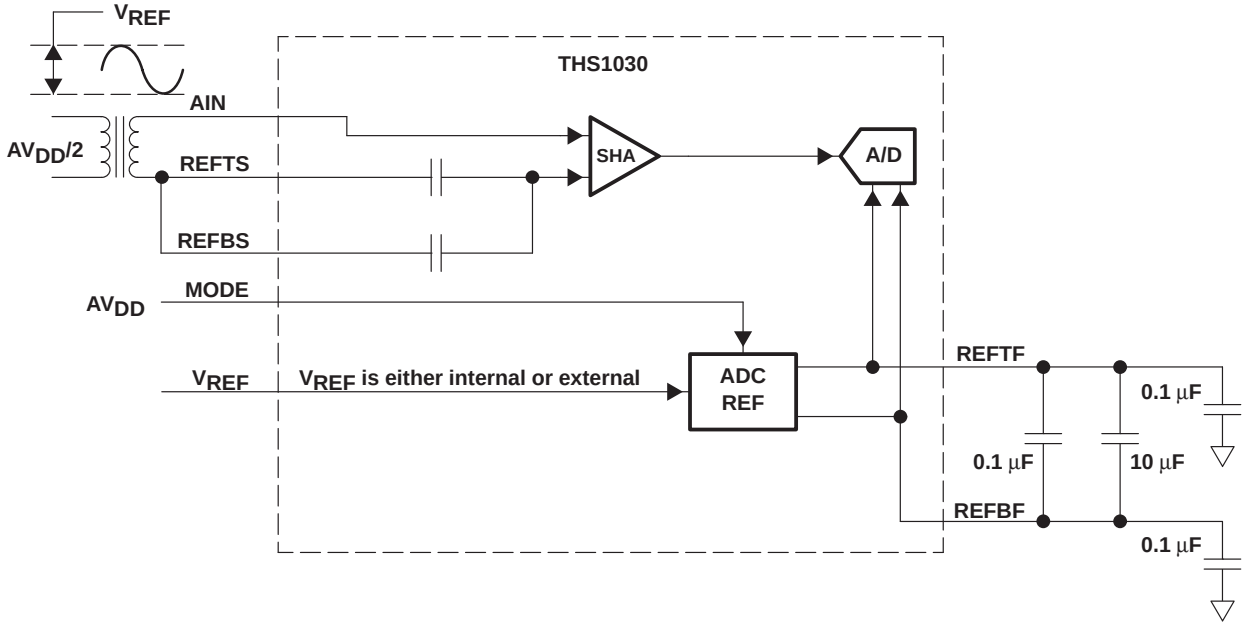


Figure 19. Differential Input

PRINCIPLES OF OPERATION

digital input mode

- **3-State Output:** The digital outputs can be set to high-impedance state by applying a LO logic to the OE pin.
- **Power Down:** The whole device will power down by applying a HI logic to the STBY pin. The ADC will wake up in 400 ns after the pin STBY is reset.

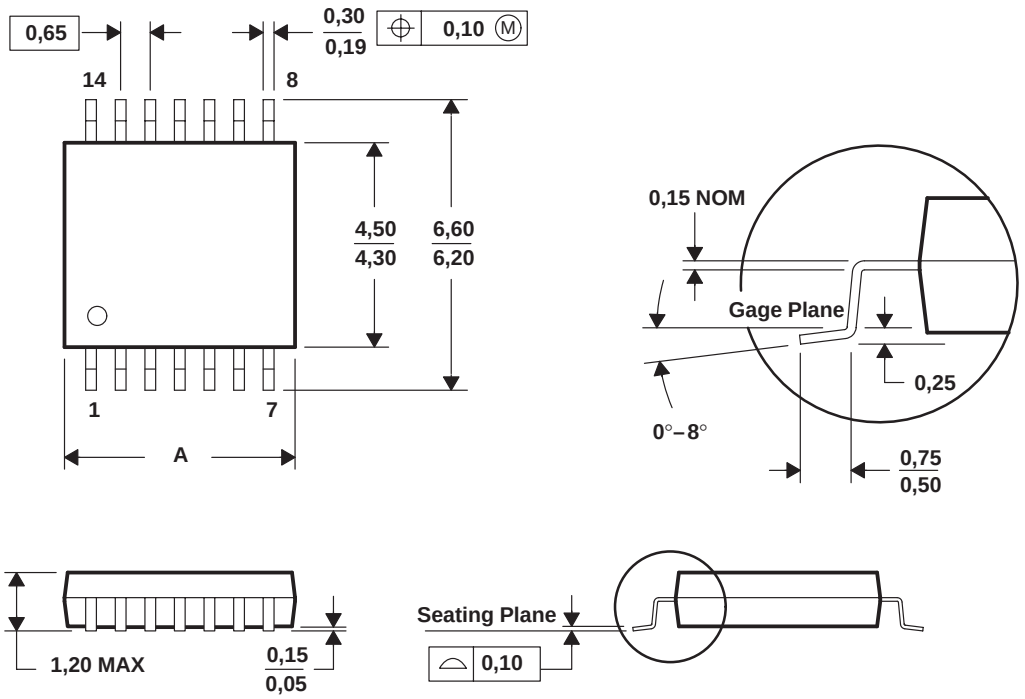
TLC876 mode

The THS1030 is pin compatible with the TI TLC876 and thus enables users of TLC876 to upgrade to higher speed by dropping the THS1030 into their sockets. Floating the MODE pin effectively puts the THS1030 into 876 mode using the external ADC reference. The REFSENSE pin will be connected to DV_{DD} by the TLC876 socket. In the TLC876/AD876 mode, the pipeline latency will be switched to 3.5 cycles to match TLC876/AD876 specifications.

MECHANICAL DATA

PW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

14 PINS SHOWN



DIM \ PINS **	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

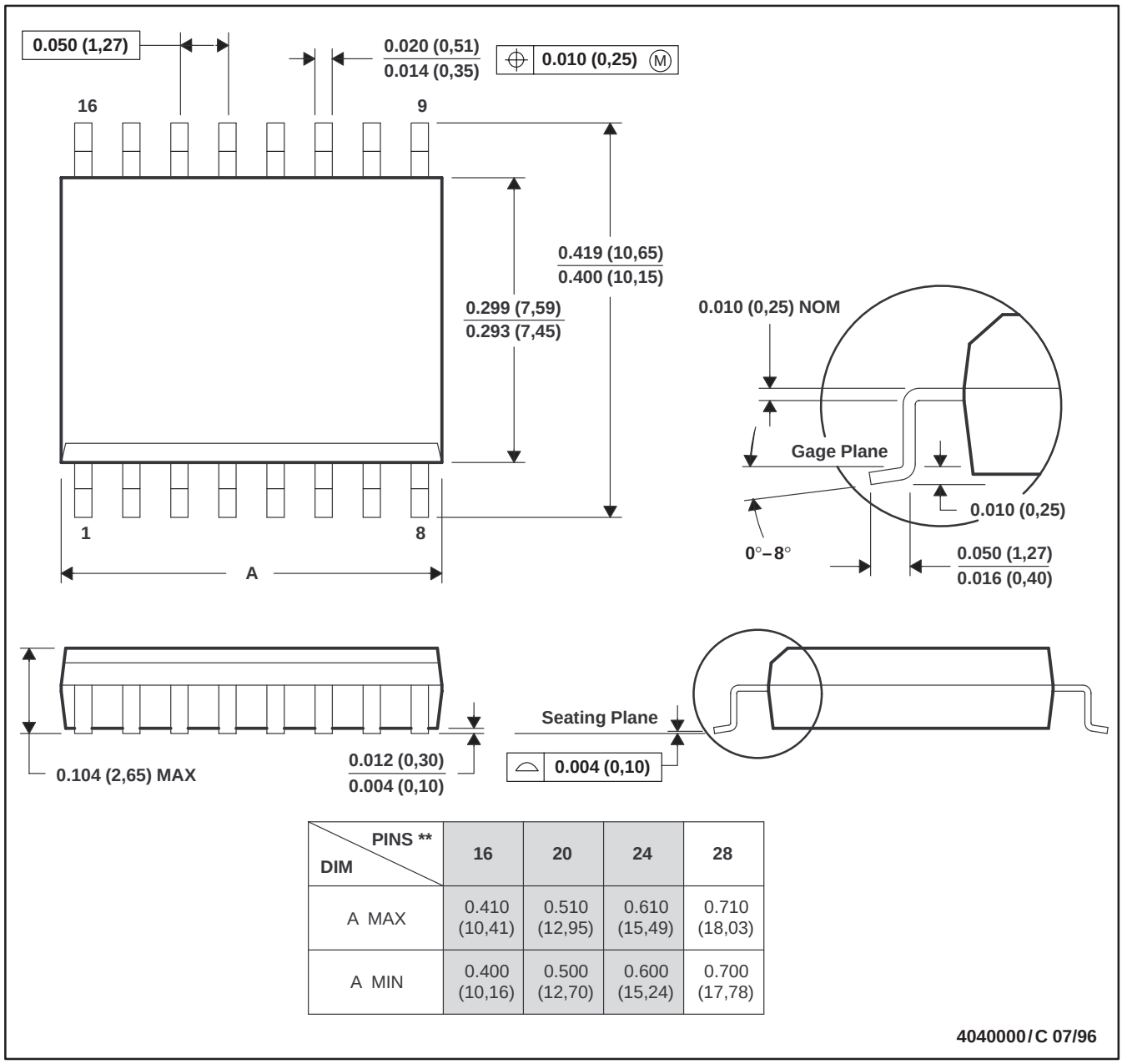
4040064/F 01/97

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

MECHANICAL DATA

DW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

16 PINS SHOWN



DIM \ PINS **	16	20	24	28
A MAX	0.410 (10,41)	0.510 (12,95)	0.610 (15,49)	0.710 (18,03)
A MIN	0.400 (10,16)	0.500 (12,70)	0.600 (15,24)	0.700 (17,78)

4040000/C 07/96

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS-013

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