

March 1992 Revised August 1999

74FR74 • 74FR1074 Dual D-Type Flip-Flop

General Description

The 74FR74 and 74FR1074 are dual D-type flip-flops with true and complement (Q/\overline{Q}) outputs. On the 74FR74, data at the D inputs is transferred to the outputs on the rising edge of the clock input (CPn). The 74FR1074 is the negative edge triggered version of this device. Both parts feature asynchronous clear (CDn) and set (SDn) inputs which are low level enabled.

Features

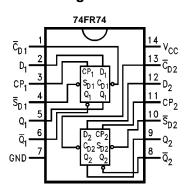
- 74FR74 is pin-for-pin compatible with the 74F74
- True 150 MHz f_{MAX} capability on 74FR74
- Outputs sink 24 mA and source 24 mA
- Guaranteed pin-to-pin skew specifications

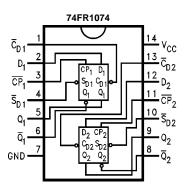
Ordering Code:

Order Number	Package Number	Package Description
74FR74SC	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150 Narrow
74FR74PC	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide
74FR1074SC	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150 Narrow
74FR1074PC	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0,300 Wide

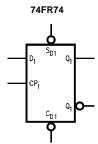
Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

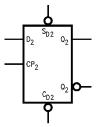
Connection Diagrams



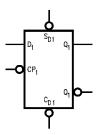


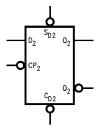
Logic Symbols





74FR1074





Pin Descriptions

Pin Names	Description
D _n	Data Inputs
CP _n	Clock Inputs
S _{Dn}	Asynchronous Set Inputs
C _{Dn}	Asynchronous Clear Inputs
Q _n	True Output
\overline{Q}_n	Complementary Output

Truth Tables

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	Inpu	Out	puts		
SD	CD	СР	D	Q	Q
L	Н	Х	Х	Н	L
Н	L	Χ	Χ	L	Н
L	L	X	X	Н	Н
Н	Н	~	Н	Н	L
Н	Н	~	L	L	Н
Н	Н	L	Χ	Q_0	\overline{Q}_0

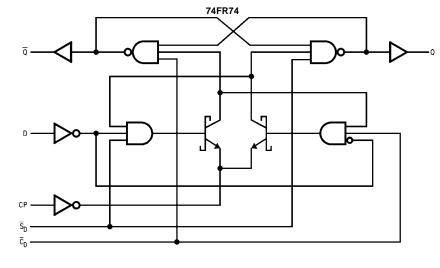
- H = HIGH Voltage Level
 L = LOW Voltage Level
 Z = High Impedance
 X = Immaterial

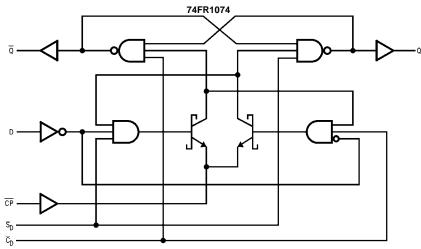
 = Rising Edge
 Q₀ = Previous Q(Q) before LOW-to-HIGH Clock Transition

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	Inp	Out	puts		
SD	CD	CP	D	Q	Q
L	Н	Х	Х	Н	L
Н	L	X	X	L	Н
L	L	X	X	Н	Н
Н	Н	\sim	Н	Н	L
Н	Н	\sim	L	L	Н
Н	Н	L	Χ	Q_0	\overline{Q}_0

Logic Diagrams





Absolute Maximum Ratings(Note 1)

 $\begin{array}{ll} \mbox{Storage Temperature} & -65\mbox{°C to } +150\mbox{°C} \\ \mbox{Ambient Temperature under Bias} & -55\mbox{°C to } +125\mbox{°C} \\ \end{array}$

Voltage Applied to Output

in HIGH State (with $V_{CC} = 0V$)

Standard Output $$-0.5\mbox{V}$\ to \mbox{V}_{\mbox{CC}}$$

Current Applied to Output

in LOW State (Max) $\qquad \qquad \text{twice the rated I}_{\text{OL}} \, (\text{mA})$

ESD Last Passing Voltage (Min)

Recommended Operating Conditions

Free Air Ambient Temperature 0° C to $+70^{\circ}$ C Supply Voltage +4.5V to +5.5V

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

DC Electrical Characteristics

Symbol	Parameter	Min	Тур	Max	Units	v _{cc}	Conditions
/ _{IH}	Input HIGH Voltage	2.0			V		Recognized HIGH Signal
V _{IL}	Input LOW Voltage			0.8	V		Recognized LOW Signal
V _{CD}	Input Clamp Diode Voltage			-1.2	V	Min	I _{IN} = -18 mA
/ _{ОН}	Output HIGH	2.5			V	Min	I _{OH} = -1 mA
	Voltage	2.4			V	Min	$I_{OH} = -3 \text{ mA}$
		2.0			V	Min	I _{OH} = -24 mA
V _{OL}	Output LOW Voltage			0.5	V	Min	I _{OL} = 24 mA
IH	Input HIGH Current			5	μΑ	Max	V _{IN} = 2.7V
BVI	Input HIGH Current Breakdown Test			7	μΑ	Max	V _{IN} = 7.0V
IL	Input LOW Current			-150	μΑ	Max	$V_{IN} = 0.5V (D_n, CP_n)$
				-1.8	mA	Max	$V_{IN} = 0.5V (C_{Dn}, S_{Dn})$
/ _{ID}	Input Leakage Test	4.75			V	0.0	$I_{ID} = 1.9 \mu\text{A},$ All Other Pins Grounded
OD	Output Circuit Leakage Test			3.75	V	0.0	V _{IOD} = 150 mV, All Other Pins Grounded
os	Output Short-Circuit Current	-100		-275	mA	Max	V _{OUT} = 0.0V
CEX	Output HIGH Leakage Current			50	μА	Max	V _{OUT} = V _{CC}
СС	Power Supply Current			24	mA	Max	

AC Electrical Characteristics 74FR74

Units		$T_A = 0^{\circ}C$	T _A = +25°C				
	+5.0V	$V_{CC} = +5.0V$ $C_L = 50 \text{ pF}$		$V_{CC} = +5.0V$		Parameter	Symbol
	0 pF			$\textbf{C}_{\textbf{L}} = \textbf{50 pF}$		r ai ainetei	Symbol
	Max	Min	Max	Тур	Min		
MHz		150		190	150	Maximum Clock Frequency	f _{MAX}
no	5.0	2.5	5.0	3.5	2.5	Propagation Delay	t _{PLH}
ns	6.0	2.5	6.0	4.5	2.5	CP_n to Q_n or \overline{Q}_n	t_{PHL}
ns	5.5	1.5	5.5	3.5	1.5	Propagation Delay	t _{PLH}
	7.0	2.0	7.0	5.5	2.0	\overline{C}_{Dn} or \overline{S}_{Dn} to Q_n or \overline{Q}_n	t_{PHL}
ns	1.0					Pin to Pin Skew	toshl
115	1.0					for HL Transitions	(Note 3)
ns	1.0					Pin to Pin Skew	t _{OSLH}
115	1.0					for LH Transitions	(Note 3)
no	3.0					Pin to Pin Skew	t _{OST}
ns	3.0					for HL/LH Transitions	(Note 3)
	4.0					True/Complement	t _{Q/Q}
ns	1.8					Output Skew	(Note 3)
ns	1.8					Pin (Signal)	t _{PS}
115	1.0					Transition Variation	(Note 3)
	1.8					Output Skew Pin (Signal)	(Note 3)

Note 3: Pin-to-Pin Skew is defined as the absolute value of the difference between the actual propagation delay for any outputs within the same packaged device. The specifications apply to any outputs switching in the same direction either HIGH-to-LOW (t_{OSHL}) or LOW-to-HIGH (t_{OSLH}) or in opposite directions both HL and LH (t_{OST}). t_{OST} is guaranteed by design.

AC Operating Requirements 74FR74

Symbol	Parameter		$T_A = +25$ °C $V_{CC} = +5.0V$ $C_L = 50 \text{ pF}$		$T_A = 0$ °C to $+70$ °C $V_{CC} = +5.0$ V $C_L = 50$ pF	
		Min	Max	Min	Max	
t _S (H)	Setup Time, HIGH or LOW	2.5		2.5		ns
t _S (L)	D _n to CP _n	2.5		2.5		115
t _H (H)	Hold Time, HIGH or LOW	0		0		ns
t _H (L)	D _n to CP _n	0		0		115
t _W (H)	CP _n Pulse Width	3.3		3.3		ns
$t_W(L)$	HIGH or LOW	3.3		3.3		115
(Note 4)						
t _W (L)	\overline{S}_{Dn} or \overline{C}_{Dn} Pulse Width	4.0		4.0		ns
t _{REC}	Recovery Time	2.0		2.0		ns
	\overline{S}_{Dn} or \overline{C}_{Dn} to CP_n					

Note 4: This specification is guaranteed by design.

AC Electrical Characteristics 74FR1074

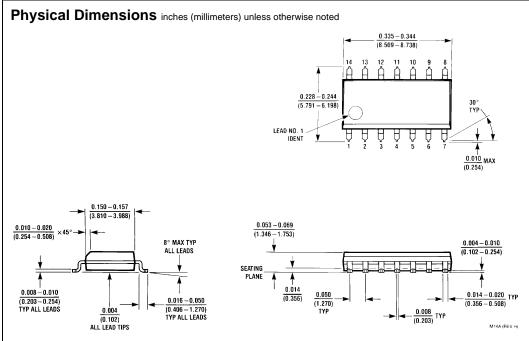
Symbol	Parameter		$T_A = +25^{\circ}C$ $V_{CC} = +5.0V$ $C_L = 50 \text{ pF}$	•	$T_A = 0^{\circ}C \text{ to } +70^{\circ}C$ $V_{CC} = +5.0V$ $C_L = 50 \text{ pF}$		Units
		Min	Тур	Max	Min	Max	
f _{MAX}	Maximum Clock Frequency	120	160		120		MHz
t _{PLH}	Propagation Delay	2.5	4.0	5.5	2.5	5.5	20
t_{PHL}	CP_n to Q_n or \overline{Q}_n	3.0	5.0	6.5	3.0	6.5	ns
t _{PLH}	Propagation Delay	1.5	3.5	5.5	1.5	5.5	ns
t_{PHL}	\overline{C}_{Dn} or \overline{S}_{Dn} to Q_n or \overline{Q}_n	2.0	5.5	7.0	2.0	7.0	
toshl	Pin to Pin Skew					1.5	20
(Note 5)	for HL Transitions					1.5	ns
toslh	Pin to Pin Skew					1.5	ns
(Note 5)	for LH Transitions					1.5	113
t _{OST}	Pin to Pin Skew					3.5	ns
(Note 5)	for HL/LH Transitions					3.3	115
t _{Q/Q}	True/Complement					2.0	
(Note 5)	Output Skew					2.0	ns
t _{PS}	Pin (Signal)					2.0	ns
(Note 5)	Transition Variation					2.0	113

Note 5: Pin-to-Pin Skew is defined as the absolute value of the difference between the actual propagation delay for any outputs within the same packaged device. The specifications apply to any outputs switching in the same direction either HIGH-to-LOW (t_{OSHL}) or LOW-to-HIGH (t_{OSLH}) or in opposite directions both HL and LH (t_{OST}). t_{OST} is guaranteed by design.

AC Operating Requirements 74FR1074

Symbol	Parameter	$T_A = +25$ °C $V_{CC} = +5.0V$		$T_A = 0$ °C = +70°C V_{CC} = +5.0V		Units
		C _L =	50 pF	C _L =	50 pF	
		Min	Max	Min	Max	
t _S (H)	Setup Time, HIGH or LOW	2.0		2.0		ns
t _S (L)	D _n to CP _n	2.0		2.0		115
t _H (H)	Hold Time, HIGH or LOW	0		0		ns
t _H (L)	D _n to CP _n	0		0		115
t _W (H)	CP _n Pulse Width	3.3		3.3		no
t _W (L)	HIGH or LOW	3.3		3.3		ns
(Note 6)						
t _W (L)	S _{Dn} or C _{Dn} Pulse Width	4.0		4.0		ns
t _{REC}	Recovery Time \overline{S}_{Dn} or \overline{C}_{Dn} to CP_n	2.0		2.0		ns

Note 6: This specification is guaranteed by design.



14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150 Narrow Package Number M14A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued) 0.740 - 0.770 (18.80 - 19.56)0.090 (2.286) 14 13 12 11 10 9 8 14 13 12 INDEX AREA 0.250 ± 0.010 (6.350 ± 0.254) PIN NO. 1 PIN NO. 1 IDENT 1 2 3 4 5 6 7 1 2 3 $\frac{0.092}{(2.337)}$ DIA 0.030 MAX (0.762) DEPTH OPTION 1 OPTION 02 $\frac{0.135 \pm 0.005}{(3.429 \pm 0.127)}$ 0.300 - 0.320 $\frac{0.630 - 8.128}{(7.620 - 8.128)}$ 0.060 0.145 - 0.2004° TYP Optional (1.651) (3.683 - 5.080) $\frac{0.008 - 0.016}{(0.203 - 0.406)}$ TYP 0.020 (0.508) 0.125 - 0.150 0.075 ± 0.015 $\overline{(3.175 - 3.810)}$ (1.905 ± 0.381) (7.112) MIN 0.014 - 0.0230.100 ± 0.010 (2.540 ± 0.254) (0.356 - 0.584) $\frac{0.050 \pm 0.010}{(1.270 - 0.254)}$ TYP 0.325 ^{+0.040} -0.015

14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide Package Number N14A

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8.255 + 1.016

N144 (REV.F)

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