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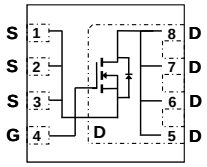
N-Channel CICLON NexFET™ Power MOSFETs
CSD16323Q3

Features

- Optimized for 5V gate drive
- Ultra Low Qg & Qgd
- Low Thermal Resistance
- Avalanche Rated
- Pb Free Terminal Plating
- RoHS Compliant
- Halogen Free

QFN 3.3mm x 3.3mm Plastic Package



Top View

Product Summary

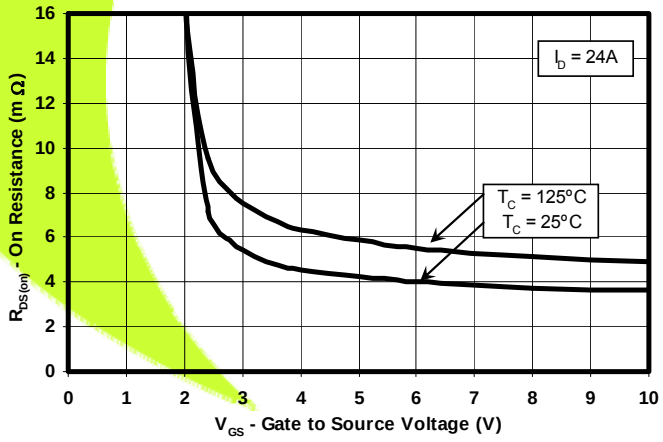
V_{DS}	25		V
Q_g	6.2		nC
Q_{gd}	1.1		nC
$R_{DS(on)}$	V_{GS} = 3.0V	5.4	mΩ
	V_{GS} = 4.5V	4.4	mΩ
	V_{GS} = 8.0V	3.8	mΩ
V_{th}	1.1		V

Maximum Values (T_A = 25°C unless otherwise stated)

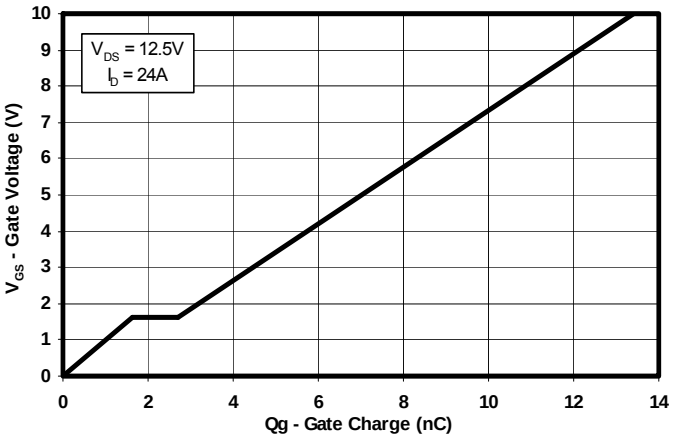
Symbol	Parameter	Value	Units
V_{DS}	Drain to Source Voltage	25	V
V_{GS}	Gate to Source Voltage	+10 / -6	V
I_D	Continuous Drain Current, T_C = 25°C	60	A
	Continuous Drain Current[1]	21	A
I_{DM}	Pulsed Drain Current, T_A = 25°C[2]	112	A
P_D	Power Dissipation[1]	3.0	W
T_J, T_{STG}	Operating Junction and Storage Temperature Range	-55 to 150	°C
E_{AS}	Avalanche Energy, single pulse I_D =50A, L = 0.1mH, R_G = 25Ω	125	mJ

1. $R_{\theta JA}$ = 43°C/W on 1in² Cu (2 oz.) on 0.060" thick FR4 PCB.
2. See Figure 10

$R_{DS(ON)}$ vs. V_{GS}



Gate Charge



Ordering Information

Type	Package	Package Media	Qty	Ship
CSD16323Q3	QFN 3.3 X 3.3 Plastic Package	13 inch reel	2500	Tape and Reel

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Electrical Characteristics (T_A = 25°C unless otherwise stated)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Static Characteristics						
BV_{DSS}	Drain to Source Voltage	V_{GS} = 0V, I_D = 250µA	25	—	—	V
I_{DSS}	Drain to Source Leakage Current	V_{GS} = 0V, V_{DS} = 20V	—	—	1	µA
I_{GSS}	Gate to Source Leakage Current	V_{DS} = 0V, V_{GS} = 10V	—	—	100	nA
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{DS} = V_{GS}, I_D = 250µA	0.9	1.1	1.4	V
$R_{DS(on)}$	Drain to Source On Resistance	V_{GS} = 3.0V, I_D = 24A	—	5.4	6.5	mΩ
		V_{GS} = 4.5V, I_D = 24A	—	4.4	5.5	mΩ
		V_{GS} = 8.0V, I_D = 24A	—	3.8	4.5	mΩ
g_{fs}	Transconductance	V_{DS} = 12.5V, I_D = 24A	—	108	—	S
Dynamic Characteristics						
C_{ISS}	Input Capacitance	V_{GS} = 0V, V_{DS} = 12.5V f = 1MHz	—	1020	1300	pF
C_{OSS}	Output Capacitance		—	740	960	pF
C_{RSS}	Reverse Transfer Capacitance		—	50	65	pF
R_g	Series Gate Resistance		—	1.1	—	Ω
Q_g	Gate Charge Total (4.5V)	V_{DS} = 12.5V, I_D = 24A	—	6.2	8.4	nC
Q_{gd}	Gate Charge Gate to Drain		—	1.1	—	nC
Q_{gs}	Gate Charge Gate to Source		—	1.8	—	nC
$Q_{g(th)}$	Gate Charge at Vth		—	1.0	—	nC
Q_{OSS}	Output Charge	V_{DS} = 12.5V, V_{GS} = 0V	—	14	—	nC
$t_{d(on)}$	Turn On Delay Time	V_{DS} = 12.5V V_{GS} = 4.5V I_D = 24A R_G = 7.0 Ω	—	7	—	ns
t_r	Rise Time		—	18	—	ns
$t_{d(off)}$	Turn Off Delay Time		—	22	—	ns
t_f	Fall Time		—	21	—	ns
Diode Characteristics						
V_{SD}	Diode Forward Voltage	I_S = 24A, V_{GS} = 0V	—	0.85	1.0	V
Q_{rr}	Reverse Recovery Charge	V_{dd}=12.5V, I_F = 24A, di/dt = 300A/µs	—	21	—	nC
t_{rr}	Reverse Recovery Time	V_{dd}=12.5V, I_F = 24A, di/dt = 300A/µs	—	16	—	ns

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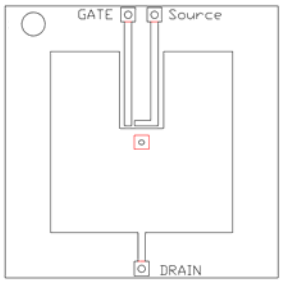
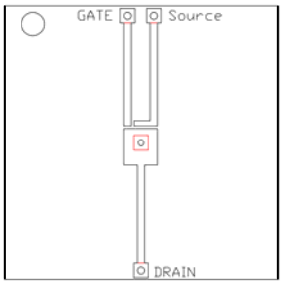
Thermal Characteristics (T_A = 25°C unless otherwise stated)

Symbol	Parameter	Min	Typ	Max	Units
Thermal Characteristics					
$R_{\theta JC}$	Thermal Resistance Junction to Case[3]	—	—	2.7	°C/W
$R_{\theta JA}$	Thermal Resistance Junction to Ambient[3,4]	—	—	58	°C/W

3. $R_{\theta jc}$ is determined with the device mounted on a 1in square 2 oz. Cu pad on a 1.5x1.5 in .060in thick FR4 board. $R_{\theta jc}$ is guaranteed by design while $R_{\theta ca}$ is determined by the user's board design.
4. Device mounted on FR4 Material with 1in^2 of 2 oz. Cu.



Max Rθja = 58°C/W when mounted on 1in^2 of 2 oz. Cu.



Max Rθja = 162°C/W when mounted on min pad area of 2 oz. Cu.

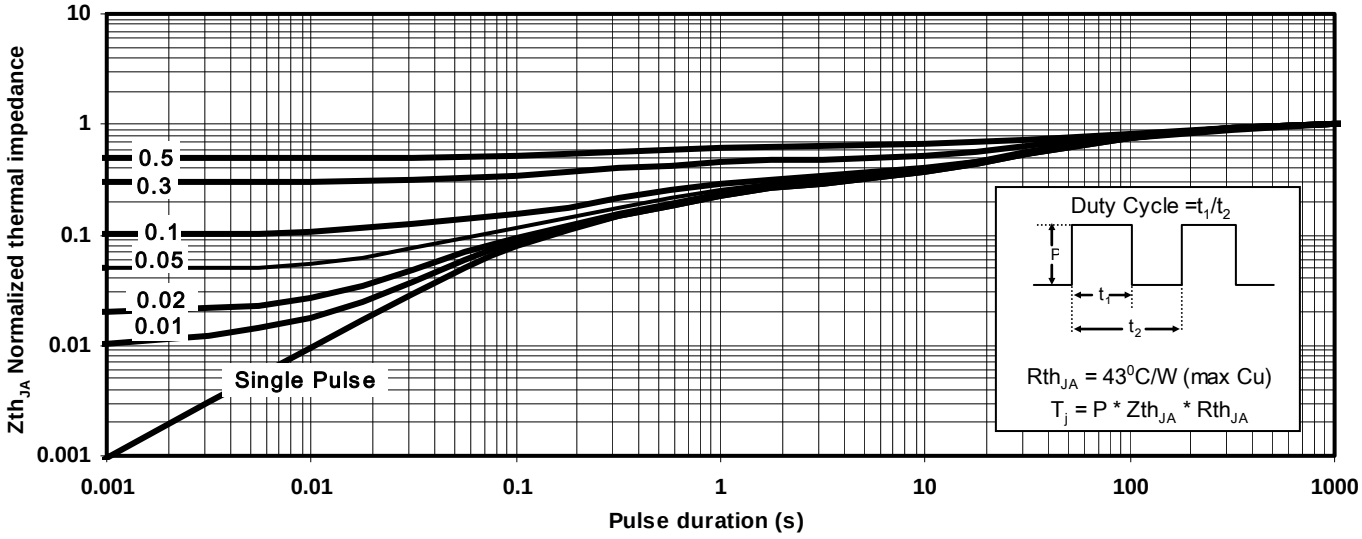


Figure 1: Transient Thermal Impedance

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Typical MOSFET Characteristics (T_A = 25°C unless otherwise stated)

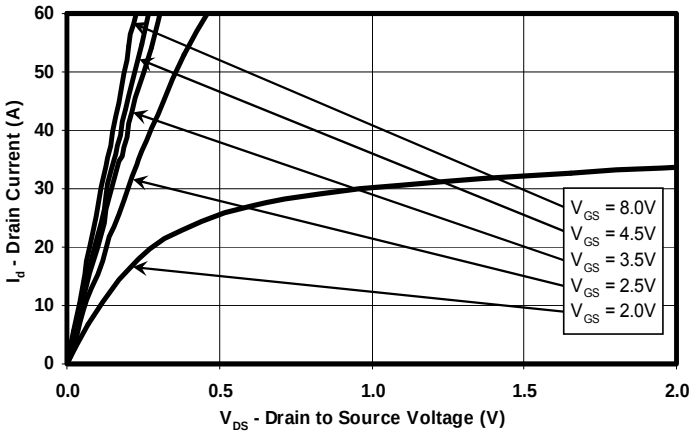

Figure 2: Saturation Characteristics

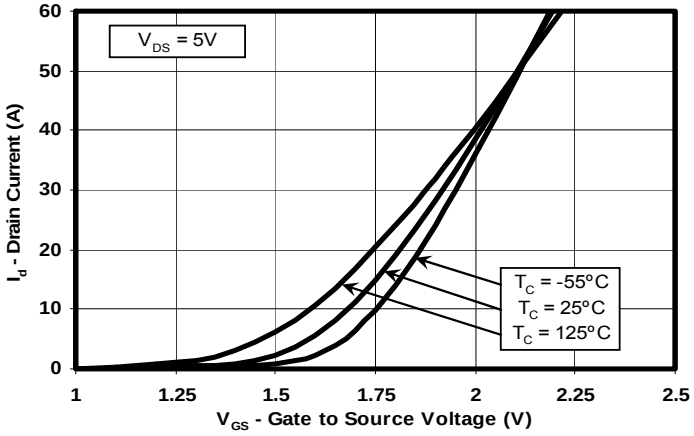

Figure 3: Transfer Characteristics

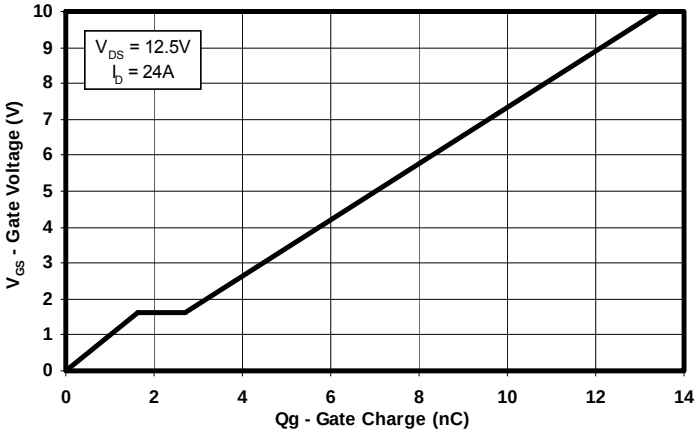

Figure 4: Gate Charge

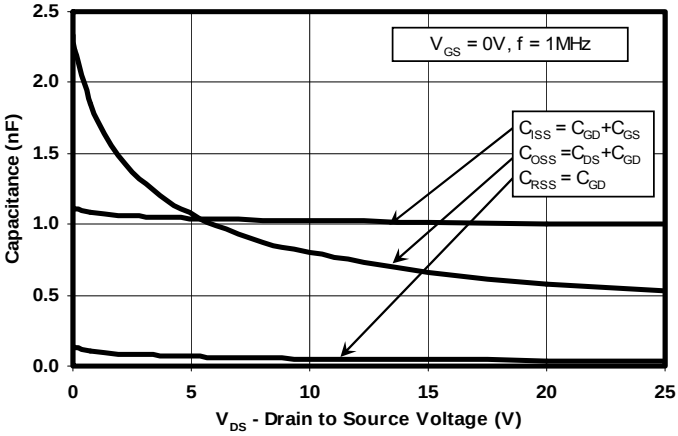

Figure 5: Capacitance

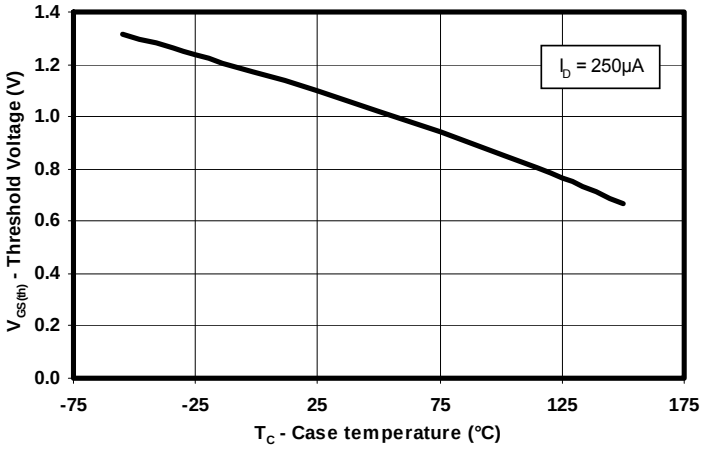

Figure 6: Threshold Voltage vs. Temperature

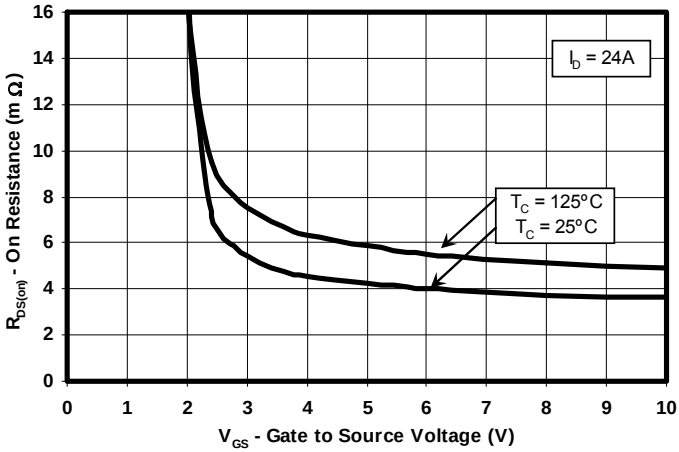

Figure 7: On Resistance vs. Gate Voltage

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Typical MOSFET Characteristics (T_A = 25°C unless otherwise stated)

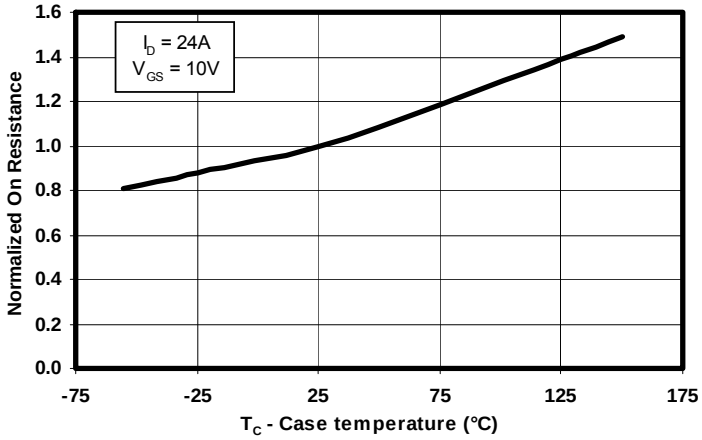

Figure 8: On Resistance vs. Temperature

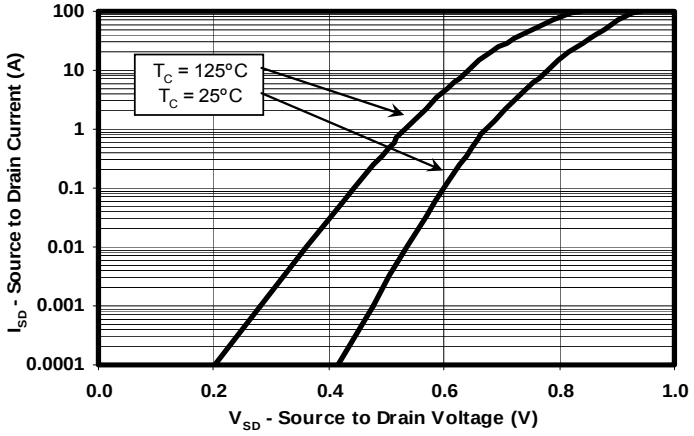

Figure 9: Typical Diode Forward Voltage

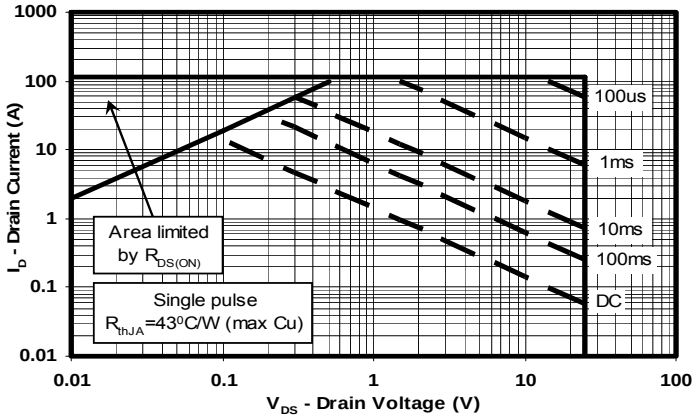

Figure 10: Maximum Safe Operating Area

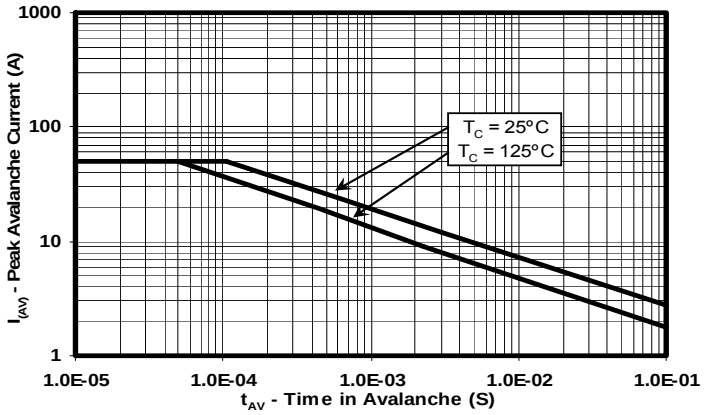

Figure 11: Single Pulse Unclamped Inductive Switching

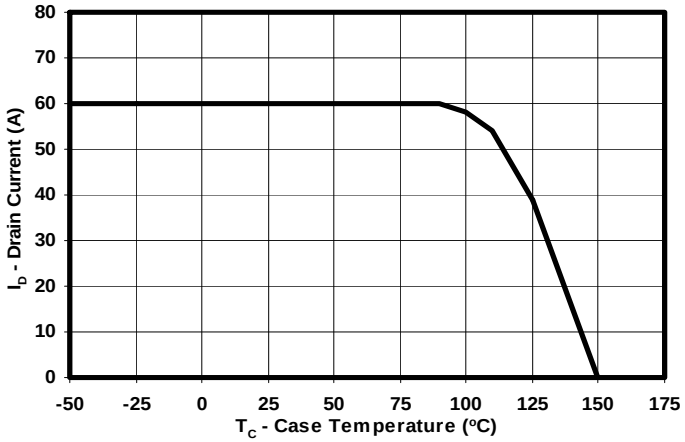

Figure 12: Maximum Drain Current vs. Temperature

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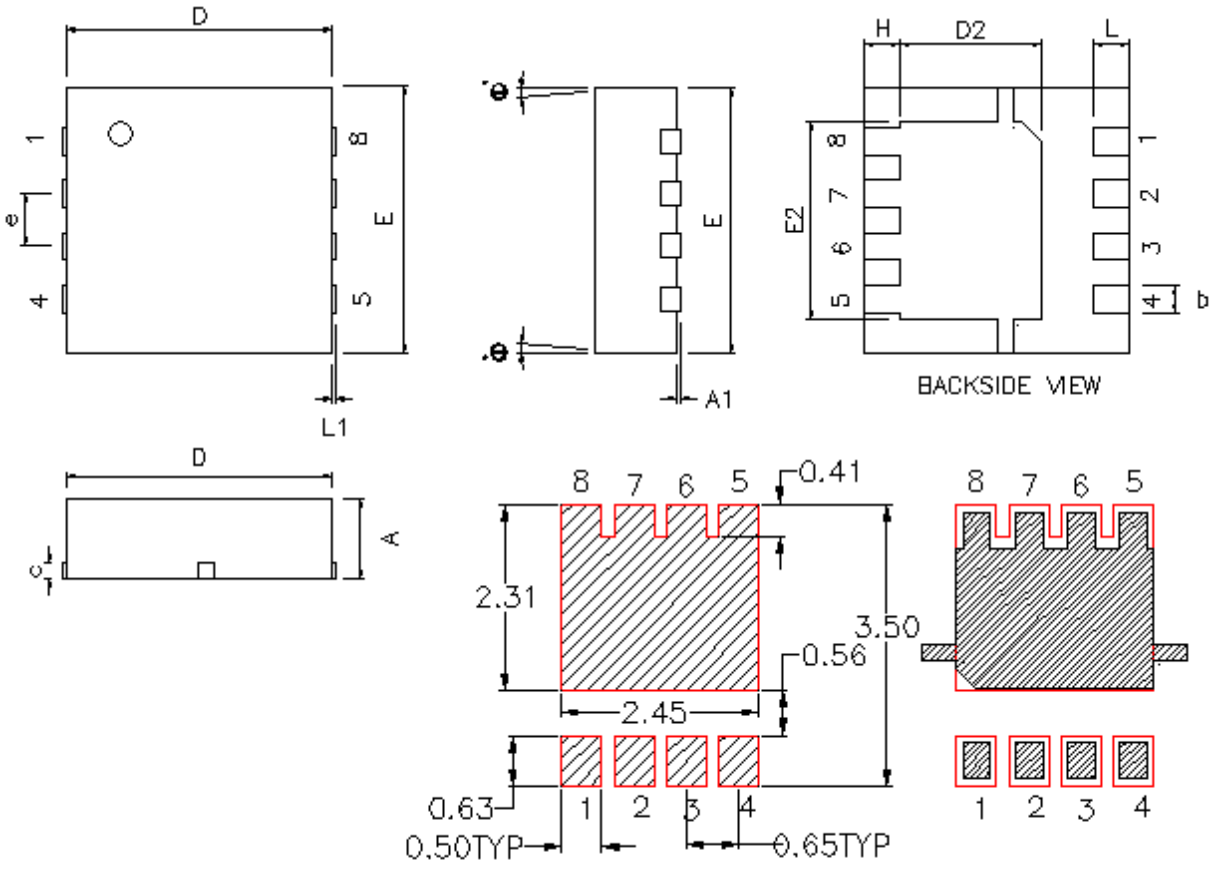
Q3 Package Dimensions



RECOMMENDED PCB LAND PATTERN

DIM	MILLIMETERS			INCHES		
	Min	Nom	Max	Min	Nom	Max
A	0.950	1.000	1.100	0.037	0.039	0.043
A1	0.000	0.000	0.050	0.000	0.000	0.002
b	0.280	0.340	0.400	0.011	0.013	0.016
c	0.150	0.200	0.250	0.006	0.008	0.010
D	3.200	3.300	3.400	0.126	0.130	0.134
D1	-	-	-	-	-	-
D2	1.650	1.750	1.800	0.065	0.069	0.071
E	3.200	3.300	3.400	0.126	0.130	0.134
E1	-	-	-	-	-	-
E2	2.350	2.450	2.550	0.093	0.096	0.100
e	0.650 TYP			0.026		
H	0.35	0.450	0.550	0.014	0.018	0.022
L	0.35	0.450	0.550	0.014	0.018	0.022
L1	-	-	-	-	-	-
θ	-	-	-	-	-	-

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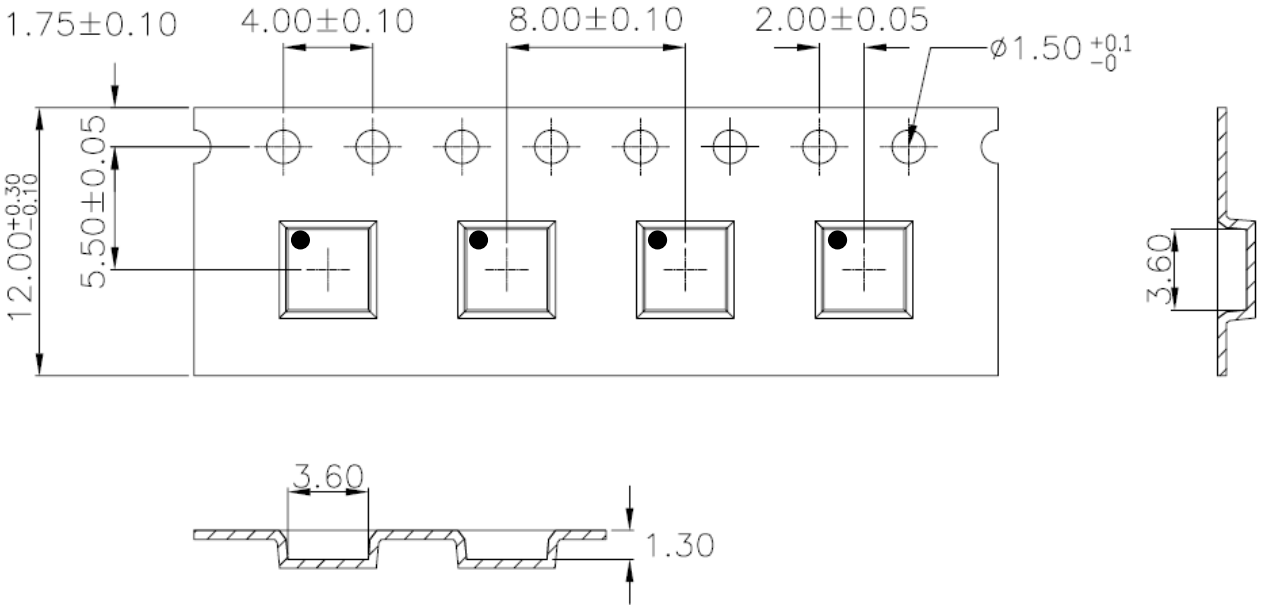
Q3 Tape and Reel Information



Note:

1. 10 SPROCKET HOLE PITCH CUMULATIVE TOLERANCE +/-0.2
2. CAMBER NOT TO EXCEED 1mm IN 100mm, NONCUMULATIVE OVER 250mm
3. MATERIAL:BLACK STATIC DISSIPATIVE POLYSTYRENE
4. ALL DIMENSIONS ARE IN mm (UNLESS OTHERWISE SPECIFIED)
5. THICKNESS: 0.30 +/-0.05mm

Package Marking Information

Location:

1st Line

CSD = Fixed Characters

NNNNN = Product Code

2nd Line (Date Code)

YY = Last 2 digits of the Year

WW = 2-digit Work Week

C = Country of Origin

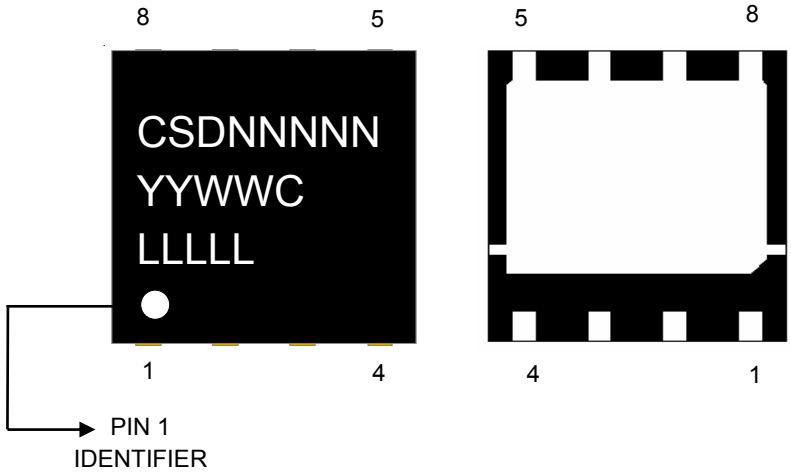
> Philippines = P

> Taiwan = T

> China = C

3rd Line

LLLLL= Last 5 digits of the Wafer Lot #



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CICLON NexFET™ Power MOSFETs

CSD16323Q3

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
CSD16323Q3	ACTIVE	SON	DQG	8	2500	TBD	Call TI	Call TI

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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