CMPA601J025D

6.0 – 18.0 GHz, 25 W GaN HPA

Description

Wolfspeed's CMPA601J025D is a 25 W, MMIC HPA utilizing Wolfspeed's high performance, 0.15um GaN on SiC production process. The CMPA601J025D operates from 6 – 18 GHz and supports a variety of end applications such as electronic warfare, test instrumentation, radar and general amplification. The CMPA601J025D achieves 25 W of saturated output power with 20 dB of large signal gain and 20% power-added efficiency under CW operation.

Figure 1. CMPA601J025D

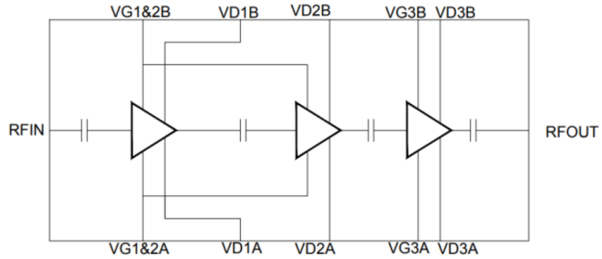

Figure 2. Functional Block Diagram

Features

- Psat: 25 W
- PAE: 20 %
- LSG: 20 dB
- S21: 30 dB
- S11: <-11 dB
- S22: <-7 dB
- CW operation

Note: Features are typical performance across frequency under 25C operation. Please reference performance charts for additional information.

Applications

- Electronic Warfare
- Test Instrumentation
- Radar
- Broadband Amplifiers

RoHS COMPLIANT

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Absolute Maximum Ratings

Parameter	Symbol	Units	Value	Conditions
Drain Voltage	V_d	V	22	25 °C
Gate Voltage	V_g	V	-10, +2	25 °C
Drain Current	I_d	A	5.9	25 °C
Gate Current	I_g	mA	11	25 °C
Input Power	P_{in}	dBm	24	CW operation only
Dissipated Power	P_{diss}	W	130	85 °C
Storage Temperature	T_{stg}	°C	-55, +150	
Mounting Temperature	T_J	°C	320	30 seconds
Junction Temperature	T_J	°C	225	MTTF >=1E6 hours
Output Mismatch Stress	VSWR	Ψ	3:1	

Recommended Operating Conditions

Parameter	Symbol	Units	Typical Value	Conditions
Drain Voltage	Vd	V	22	
Gate Voltage	Vg	V	-1.7	
Drain Current	Idq	A	>1.2	
Input Power	Pin	dBm	24	CW operation only
Case Temperature	Tcase	°C	-40 to 85	

RF Specifications

Test conditions unless otherwise noted: Vd=22 V, Idq= 1.2 A, CW, Tbase=25 °C

Parameter	Units	Frequency	Min	Typical	Max	Conditions
Frequency	GHz		6		18	
Output Power	dBm	6.0 GHz		43.6		Pin = 24 dBm
		9.5 GHz		45.7		
		14.0 GHz		43.7		
		18.0 GHz		43.9		
Power-added Efficiency	%	6.0 GHz		32		Pin = 24 dBm
		9.5 GHz		30		
		14.0 GHz		18		
		18.0 GHz		23		
LSG	dB	6.0 GHz		19.6		Pin = 24 dBm
		9.5 GHz		21.7		
		14.0 GHz		19.7		
		18.0 GHz		19.9		
Small-Signal Gain (S21)	dB	6-11 GHz		32.0		Pin = -25 dBm
		11-18 GHz		29.5		
Input Return Loss (S11)	dB	6-11 GHz		-13.5		Pin = -25 dBm
		11-18 GHz		-11.4		
Output Return Loss (S22)	dB	6-11 GHz		-7.6		Pin = -25 dBm
		11-18 GHz		-7.5		

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Test conditions unless otherwise noted: Vd = 22 V, Idq = 1.2 A, CW, Pin = 24 dBm, T_{base}=25 °C

Figure 3: Pout v. Frequency v. Temperature

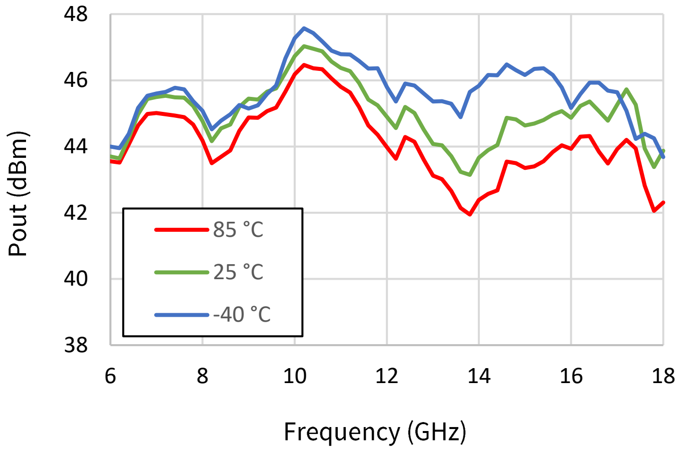


Figure 4: PAE v. Frequency v. Temperature

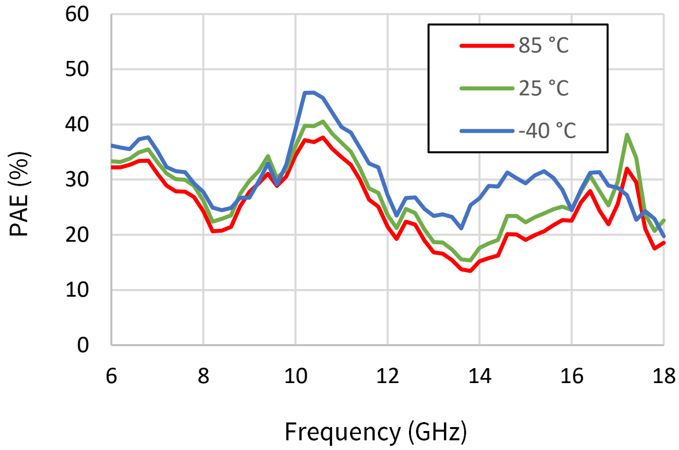


Figure 5: Id v. Frequency v. Temperature

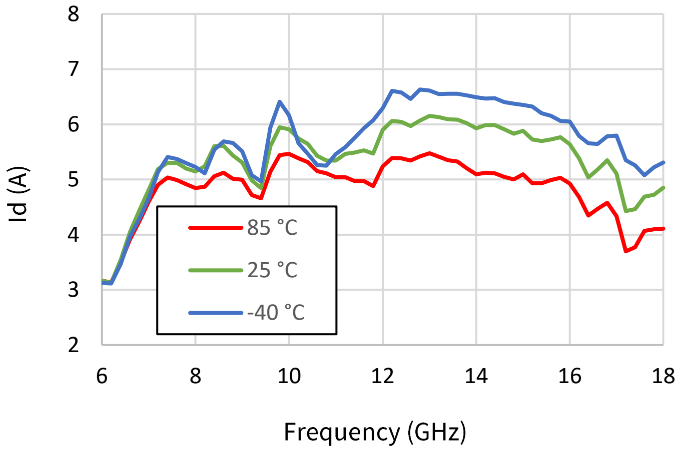


Figure 6: Ig v. Frequency v. Temperature

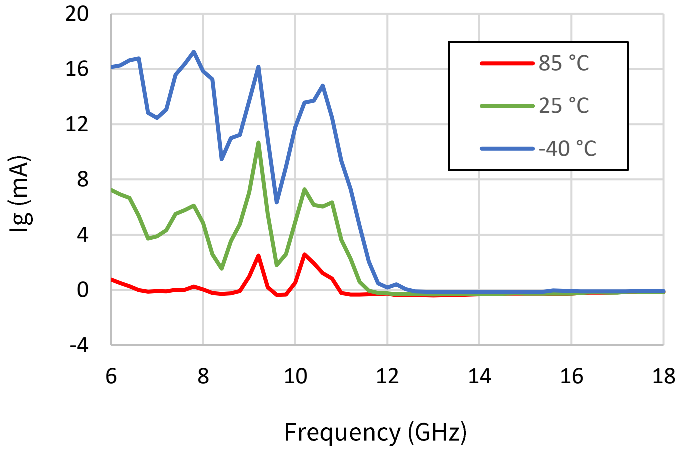
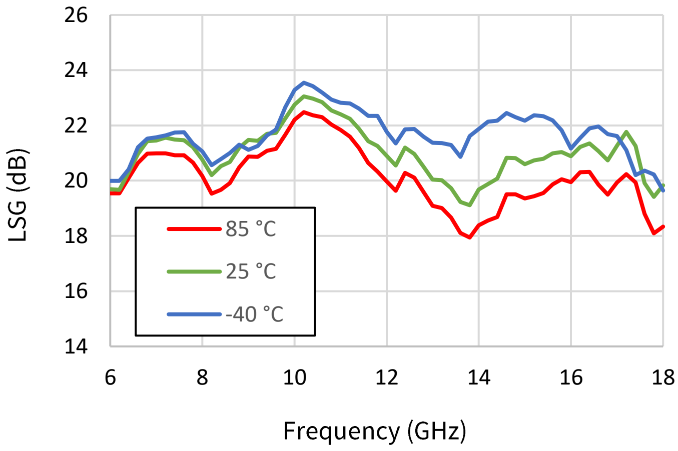


Figure 7: LSG v. Frequency v. Temperature



Test conditions unless otherwise noted: Vd = 22 V, Idq = 1.2 A, CW, Pin = 24 dBm, T_{base}=25 °C

Figure 8: Pout v. Pin v. Frequency

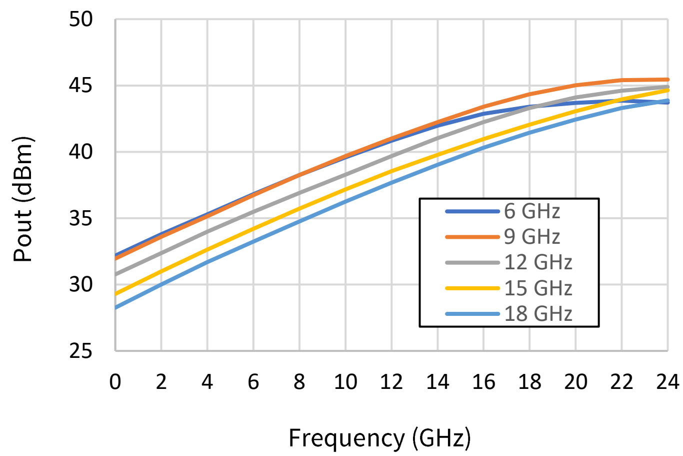


Figure 9: PAE v. Pin v. Frequency

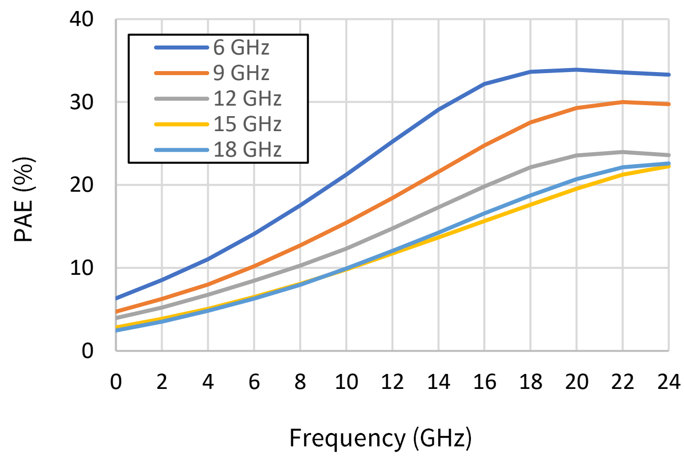


Figure 10: Id v. Pin v. Frequency

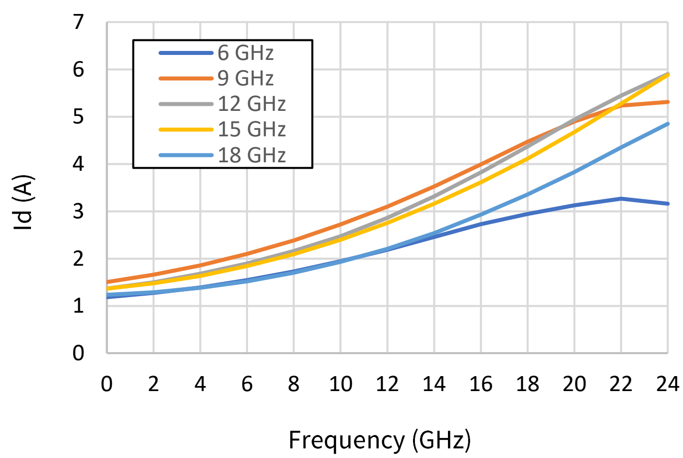


Figure 11: Ig v. Pin v. Frequency

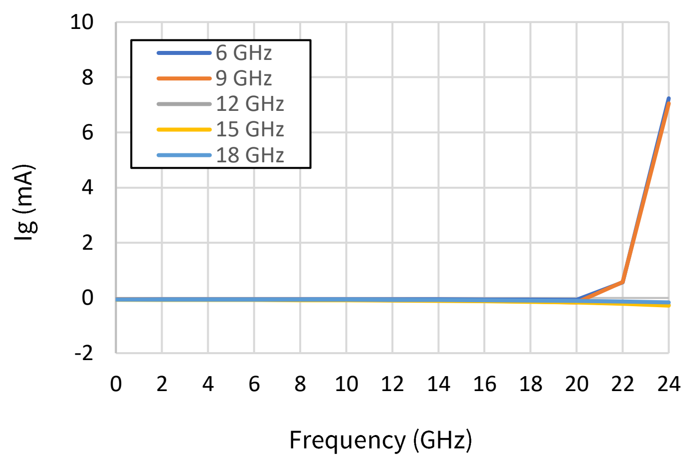
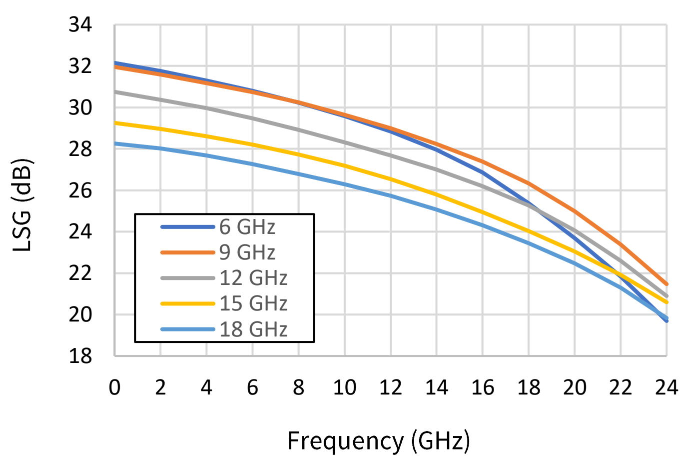


Figure 12: Gain v. Pin v. Frequency



Test conditions unless otherwise noted: Vd = 22 V, Idq = 1.2 A, CW, Pin = 24 dBm, Frequency = 12 GHz, T_{base}=25 °C

Figure 13: Pout v. Pin v. Temperature

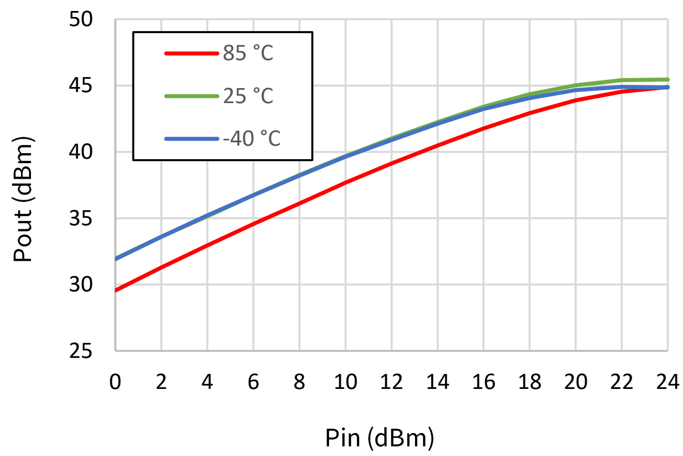


Figure 14: PAE v. Pin v. Temperature

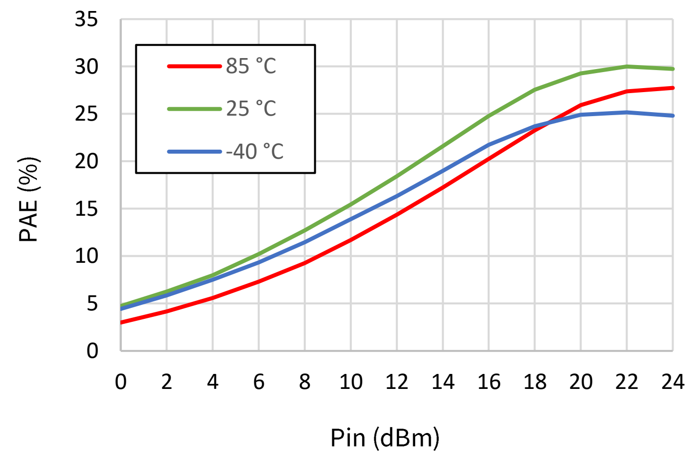


Figure 15: Id v. Pin v. Temperature

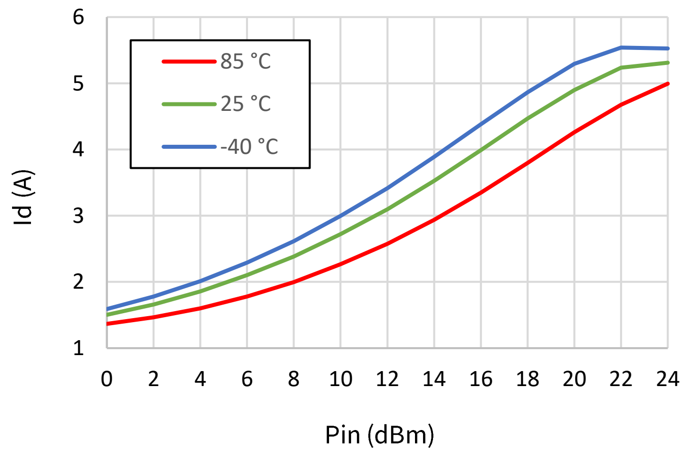


Figure 16: Ig v. Pin v. Temperature

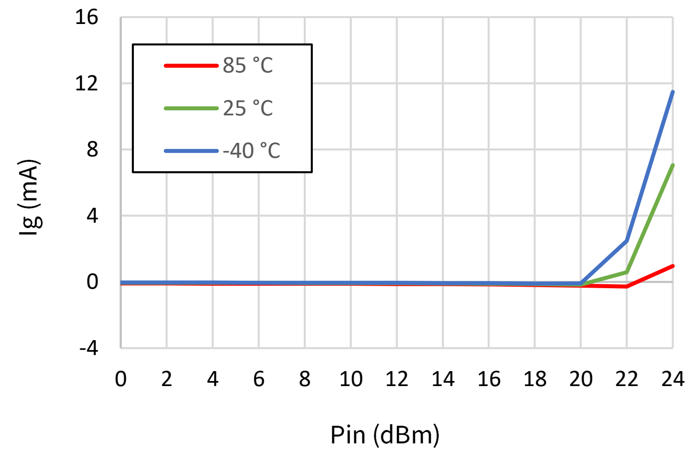
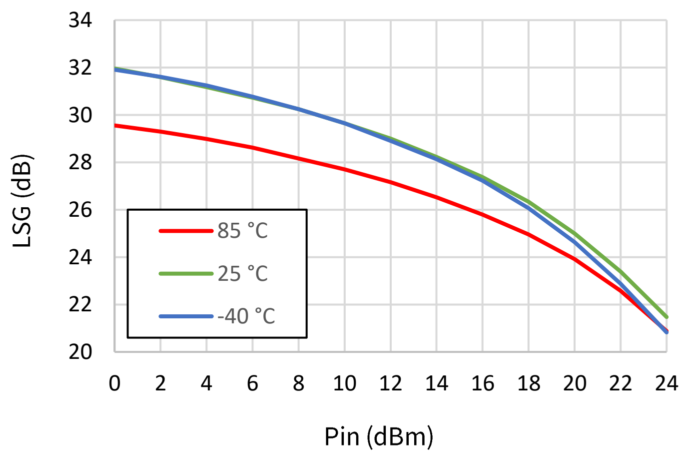


Figure 17: Gain v. Pin v. Temperature



Test conditions unless otherwise noted: Vd = 22 V, Idq = 1.2 A, PW=CW, Pin = -25 dBm, T_{base}=25 °C

Figure 18: S21 v. Frequency v. Temperature

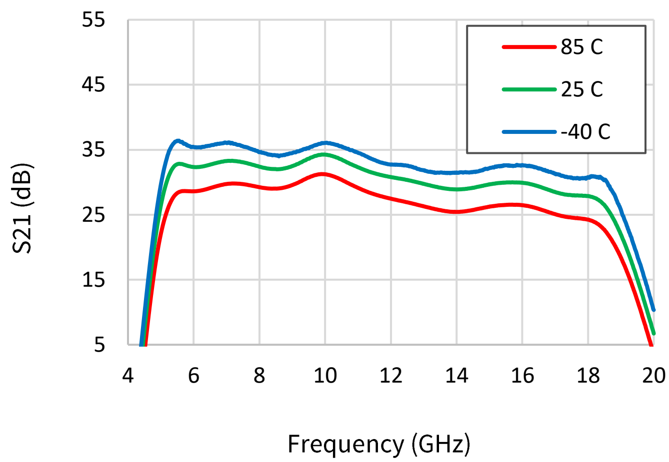


Figure 19: S11 v. Frequency v. Temperature

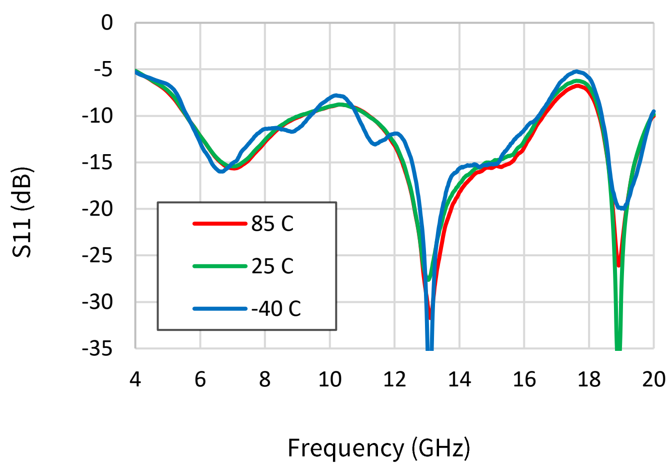
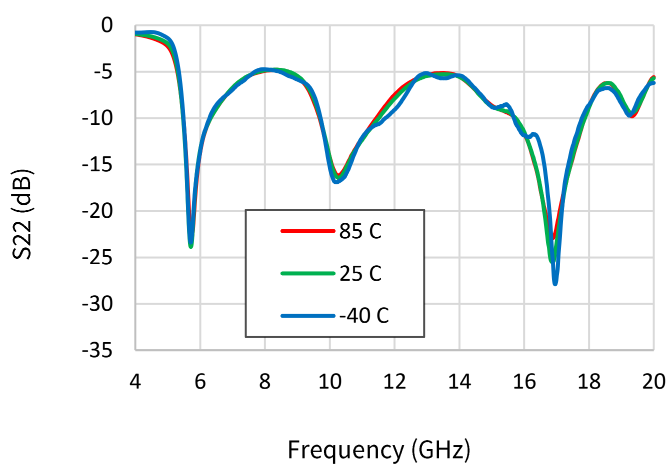


Figure 20: S22 v. Frequency v. Temperature



Test conditions unless otherwise noted: Vd =22 V, Idq = 1.2 A, CW, Pin = 24 dBm,

Figure 21: 2f v. Pout v. Temperature, 6GHz

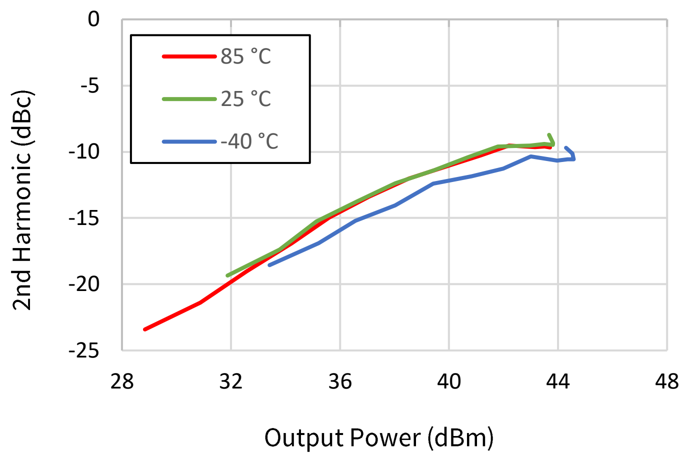


Figure 22: 2f v. Pout v. Temperature, 9GHz

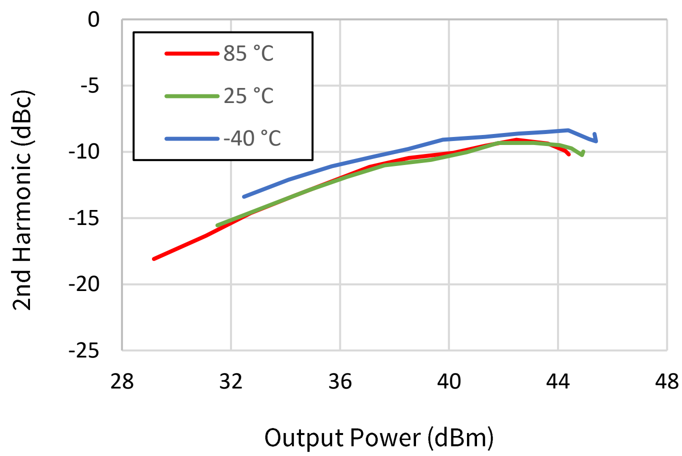
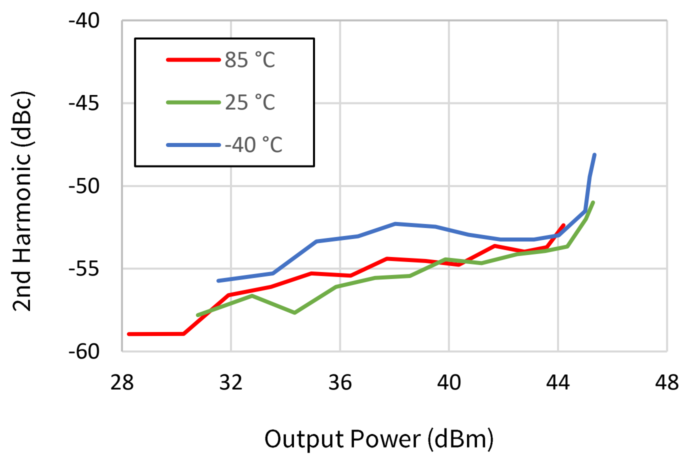


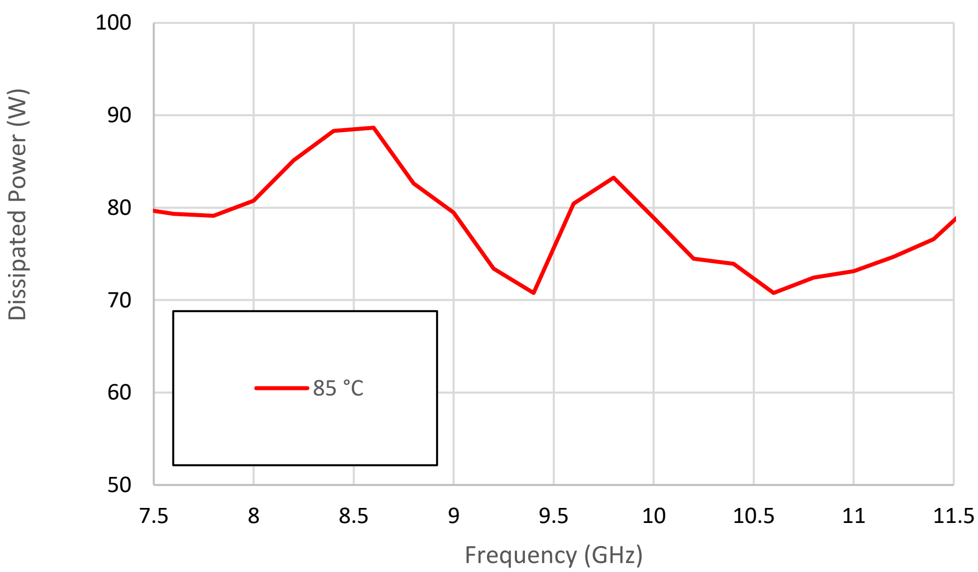
Figure 23: 2f v. Pout v. Temperature, 12GHz



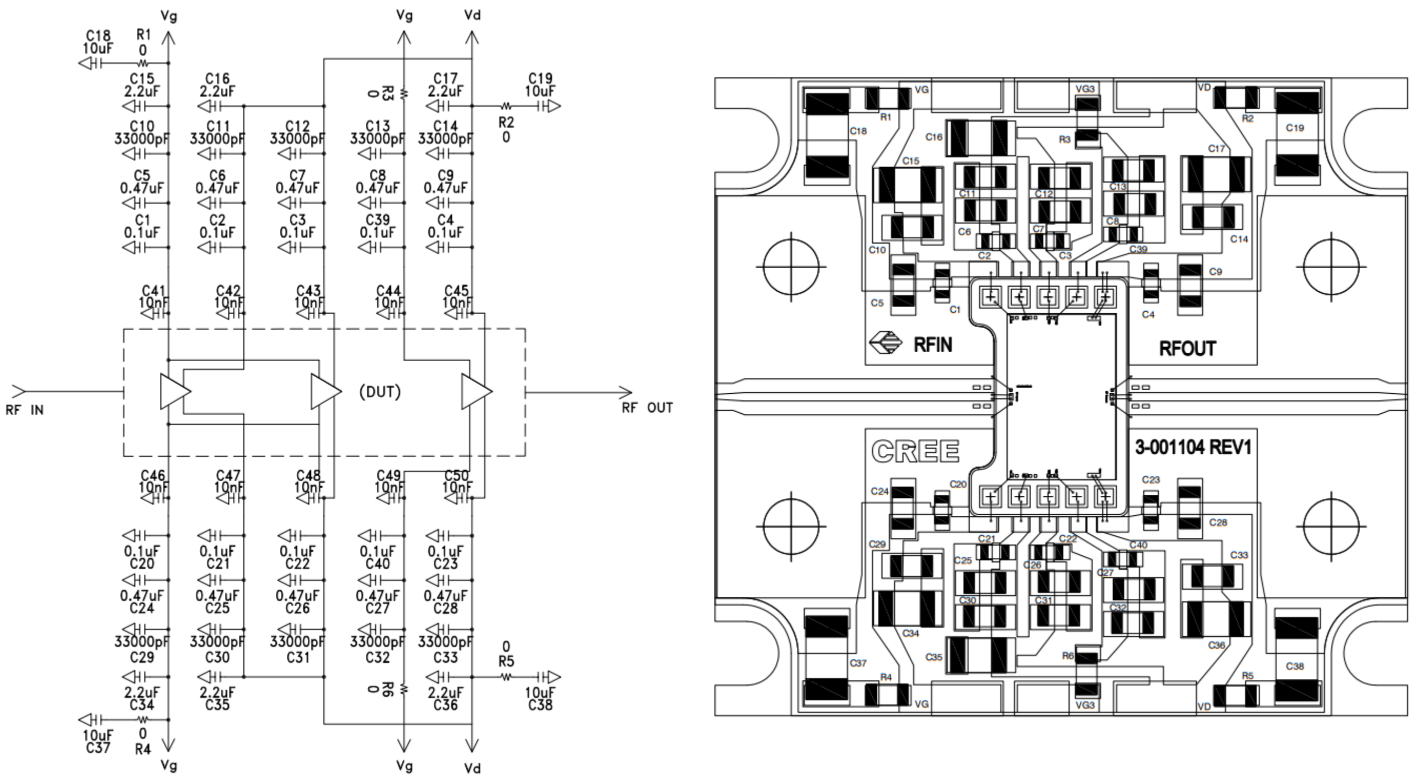
Thermal Characteristics

Parameter	Symbol	Value	Operating Conditions
Operating Junction Temperature	T_J	171	Freq = 9.0 GHz, V_d = 22 V, I_{dq} = 1.2 A, I_{drive} = 5.3 A , P_{in} = 24 dBm, P_{out} = 44.9 dBm, P_{diss} = 80 W, T_{case} = 85 C, CW
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.08	

Power Dissipation v. Frequency (Tcase = 85C)



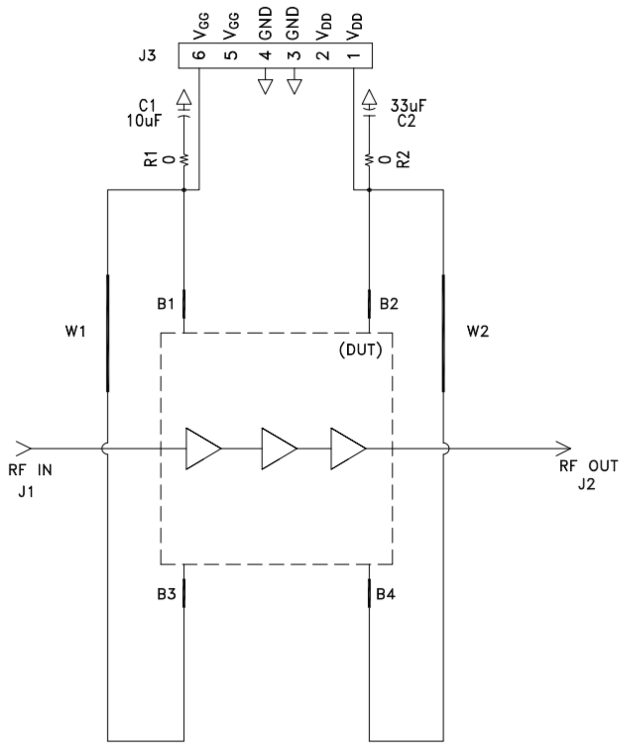
CMPA601J025D-AMP Carrier Schematic and Assembly Drawing

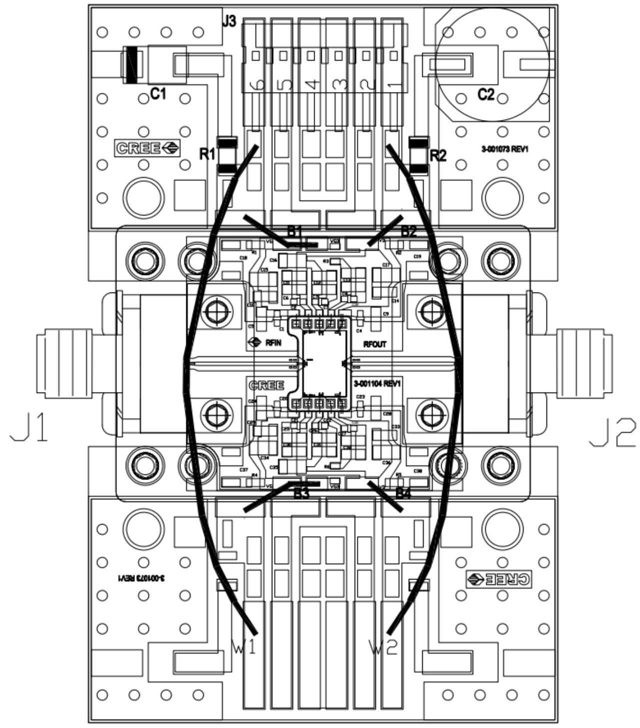


CMPA601J025D-AMP Carrier Bill of Materials

Reference Designator	Description	Qty
C1-C4, C20-C23, C39,C40	CAPACITOR, 0402, 0.1uF, 50V	10
C5-C9, C24-C28	CAPACITOR, 0603, 0.47uF, 50V	10
C10-C14, C29-C33	CAPACITOR, 0603, 33000pF, 50V	10
C15-C17, C34-C36	CAPACITOR, 0805, 2.2uF, 50V	6
C18,C19,C37,C38	CAPACITOR, 1206, 10uF, 50V	4
R1-R6	RESISTOR, 0603, 0 Ohm	6

CMPA601J025D-AMP Evaluation Board Schematic and Drawing





Note: Gate and drain should be biased on both sides of the die, as shown above.

CMPA601J025D-AMP Evaluation Board Bill of Materials

Reference Designator	Description	Qty
J1, J2	2.92mm Female End Launch RF Connector, .007" Pin, .048" Coax	2
J3	6-Pin DC Header, Right Angle	1
R1, R2	0 Ohm Resistors, 1206	2
C1	10uF Tantalum Capacitor	1
C2	33uF Electrolytic Capactitor	1
B1-B4	Jumper Wire	4
W1-W2	WIRE, BLACK, 22 AWG (~2")	2

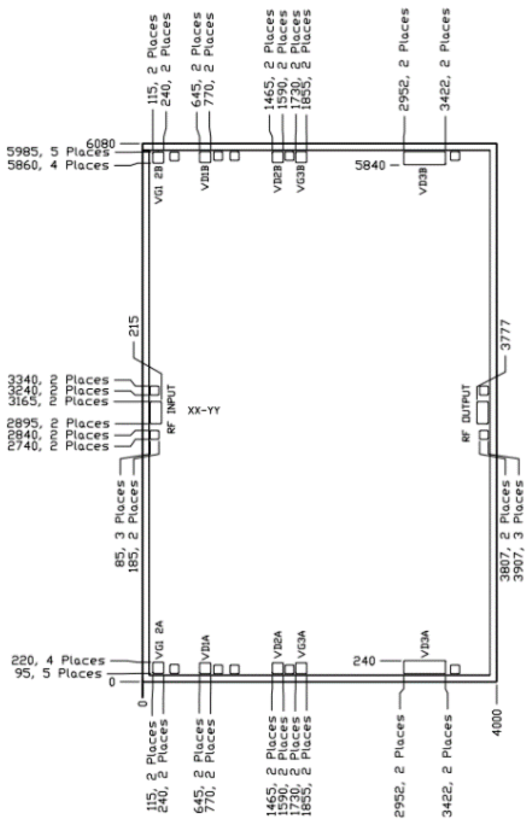
Bias On Sequence

1. Ensure RF is turned-off
2. Apply pinch-off voltage of -5 V to the gate (Vg)
3. Apply nominal drain voltage (Vd)
4. Adjust Vg to obtain desired quiescent drain current (Idq)
5. Apply RF

Bias Off Sequence

1. Turn RF off
2. Apply pinch-off to the gate (Vg=-5V)
3. Turn off drain voltage (Vd)
4. Turn off gate voltage (Vg)

Product Dimensions



Overall die size is 4000 x 6080 (+0/-50) microns, die thickness 75 (+/-10) micron.

Pad Number	Function	Description	Pad Size (um)	Note
1	RF IN	RF Input pad. Matched to 50 ohm. The DC impedance ~ 0 ohm due to matching circuit.	130 x 250	4
2	VG1&2_A	Gate control for stage 1&2A. VG = -1.5 to -2.5 V.	125 x 125	1, 2
3	VG1&2_B	Gate control for stage 1&2B. VG = -1.5 to -2.5 V.	125 x 125	1, 2
4	VD1_A	Drain supply for stage 1A. VD = 22 V.	125 x 125	1
5	VD1_B	Drain supply for stage 1B. VD = 22 V.	125 x 125	1
6	VD2_A	Drain supply for stage 2A. VD = 22 V.	125 x 125	1
7	VD2_B	Drain supply for stage 2B. VD = 22 V.	125 x 125	1
8	VG3_A	Gate control for stage 3A. VG = -1.5 to -2.5 V.	125 x 125	1, 3
9	VG3_B	Gate control for stage 3B. VG = -1.5 to -2.5 V.	125 x 125	1, 3
10	VD3_A	Drain supply for stage 3A. VD = 22 V.	470 x 150	1
11	VD3_B	Drain supply for stage 3B. VD = 22 V.	470 x 150	1
12	RF OUT	RF Output pad. Matched to 50 ohm.	130 x 250	4

Notes:
[1] Attach bypass capacitor to pads 2-11 per application circuit.
[2] VG1&2_A and VG1&2_B are connected internally so it would be enough to connect either one for proper operation.
[3] VG3_A and VG3_B are connected internally so it would be enough to connect either one for proper operation.
[4] The RF Input and Output pad have a ground-signal-ground with a nominal pitch of 10 mil (250 um). The RF ground pads are 100 x 100 microns.

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Electrostatic Discharge (ESD) Classification

Parameter	Symbol	Class	Test Methodology
Human body Model	HBM		JEDEC JESD22 A114-D
Charge Device Model	CDM		JEDEC JESD22 C101-C

Product Ordering Information

Part Number	Description	MOQ Increment	Image
CMPA601J025D	MMIC Die	1 Each	
CMPA601J025D-AMP	Evaluation Board w/ PA	1 Each	

For more information, please contact:

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