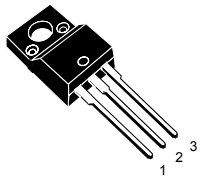
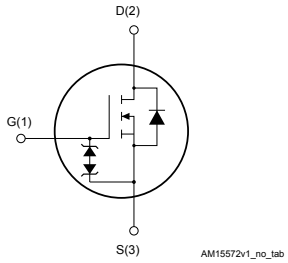
N-channel 650 V, 231 mΩ typ., 12 A, MDmesh DM2 Power MOSFET in a TO-220FP package



TO-220FP



Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D	P_{TOT}
STF18N65DM2	650 V	295 mΩ	12 A	28 W

- Fast-recovery body diode
- Extremely low gate charge and input capacitance
- Low on-resistance
- 100% avalanche tested
- Extremely high dv/dt ruggedness
- Zener-protected

Applications

- Switching applications

Description

This high-voltage N-channel Power MOSFET is part of the MDmesh DM2 fast-recovery diode series. It offers very low recovery charge (Q_{rr}) and time (t_{rr}) combined with low $R_{DS(on)}$, rendering it suitable for the most demanding high-efficiency converters and ideal for bridge topologies and ZVS phase-shift converters.

Product status link
STF18N65DM2

Product summary	
Order code	STF18N65DM2
Marking	18N65DM2
Package	TO-220FP
Packing	Tube

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	±25	V
I_D (1)	Drain current (continuous) at T_C = 25 °C	12	A
	Drain current (continuous) at T_C = 100 °C	7.6	
I_{DM} (2)	Drain current (pulsed)	36	A
P_{TOT}	Total power dissipation at T_C = 25 °C	28	W
dv/dt (3)	Peak diode recovery voltage slope	100	V/ns
dv/dt (4)	MOSFET dv/dt ruggedness	100	
V_{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink (t = 1 s, T_C = 25 °C)	2500	V
T_{stg}	Storage temperature range	-55 to 150	°C
T_j	Operating junction temperature range		

1. *Limited by maximum junction temperature*
2. *Pulse width is limited by safe operating area.*
3. *I_{SD} ≤ 12 A, di/dt=900 A/µs, V_{DS} peak < $V_{(BR)DSS}$, V_{DD} = 400 V*
4. *V_{DS} ≤ 520 V*

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Thermal resistance, junction-to-case	4.5	°C/W
R_{thJA}	Thermal resistance, junction-to-ambient	62.5	

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR} (1)	Avalanche current, repetitive or not repetitive	2.5	A
E_{AS} (2)	Single pulse avalanche energy	482	mJ

1. *Pulse width is limited by T_{Jmax}.*
2. *Starting T_j = 25 °C, I_D = I_{AR}, V_{DD} = 50 V*

2 Electrical characteristics

(T_{case} = 25 °C unless otherwise specified)

Table 4. Static

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V, I_D = 1 mA	650			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = 650 V			1	µA
		V_{GS} = 0 V, V_{DS} = 650 V, T_{case} = 125 °C(1)			100	
I_{GSS}	Gate-body leakage current	V_{DS} = 0 V, V_{GS} = ±25 V			±5	µA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	3	4	5	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 6 A		231	295	mΩ

1. *Defined by design, not subject to production test.*

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 100 V, f = 1 MHz, V_{GS} = 0 V	-	965	-	pF
C_{oss}	Output capacitance		-	42	-	
C_{rss}	Reverse transfer capacitance		-	0.45	-	
$C_{oss\ eq.}$(1)	Equivalent output capacitance	V_{DS} = 0 to 520 V, V_{GS} = 0 V	-	91	-	pF
R_G	Intrinsic gate resistance	f = 1 MHz, I_D = 0 A	-	6.6	-	Ω
Q_g	Total gate charge	V_{DD} = 520 V, I_D = 12 A, V_{GS} = 0 to 10 V (see Figure 14. Test circuit for gate charge behavior)	-	22	-	nC
Q_{gs}	Gate-source charge		-	5.6	-	
Q_{gd}	Gate-drain charge		-	9.3	-	

1. *$C_{oss\ eq.}$ is defined as the constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}.*

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 400 V, I_D = 6 A, R_G = 4.7 Ω, V_{GS} = 10 V (see Figure 13. Test circuit for resistive load switching times and Figure 18. Switching time waveform)	-	16	-	ns
t_r	Rise time		-	11	-	
$t_{d(off)}$	Turn-off delay time		-	40	-	
t_f	Fall time		-	12	-	

Table 7. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		12	A
I_{SDM}(1)	Source-drain current (pulsed)		-		36	A
V_{SD}(2)	Forward on voltage	V_{GS} = 0 V, I_{SD} = 12 A	-		1.6	V
t_{rr}	Reverse recovery time	I_{SD} = 12 A, di/dt = 100 A/µs,	-	89		ns
Q_{rr}	Reverse recovery charge	V_{DD} = 100 V	-	342		nC
I_{RRM}	Reverse recovery current	(see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	6.4		A
t_{rr}	Reverse recovery time	I_{SD} = 12 A, di/dt = 100 A/µs,	-	198		ns
Q_{rr}	Reverse recovery charge	V_{DD} = 100 V, T_J = 150 °C	-	1340		nC
I_{RRM}	Reverse recovery current	(see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	10		A

1. *Pulse width is limited by safe operating area.*
2. *Pulse test: pulse duration = 300 µs, duty cycle 1.5%.*

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

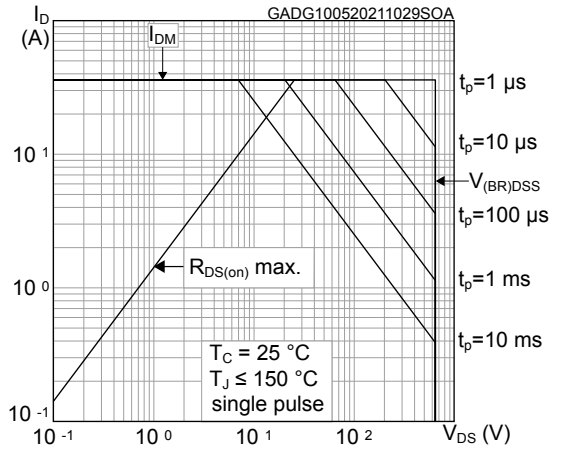


Figure 2. Maximum transient thermal impedance

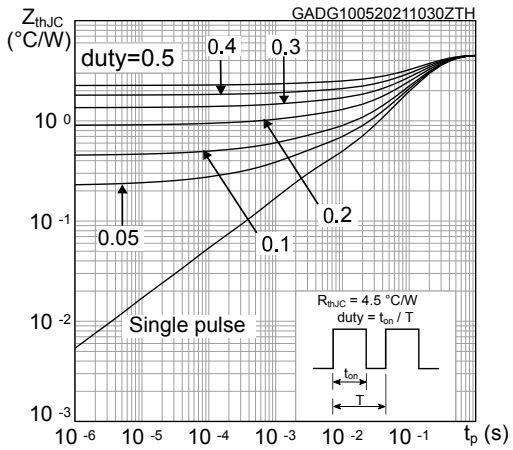


Figure 3. Typical output characteristics

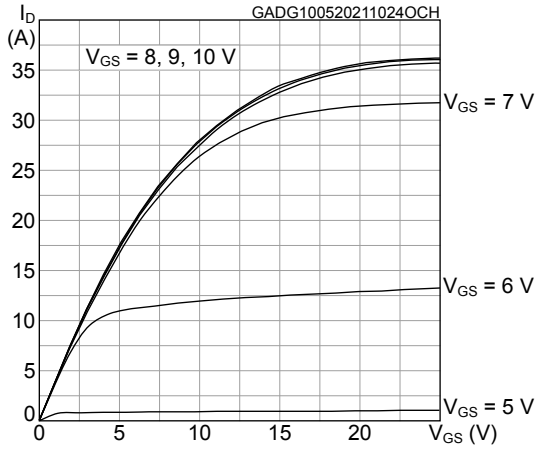


Figure 4. Typical transfer characteristics

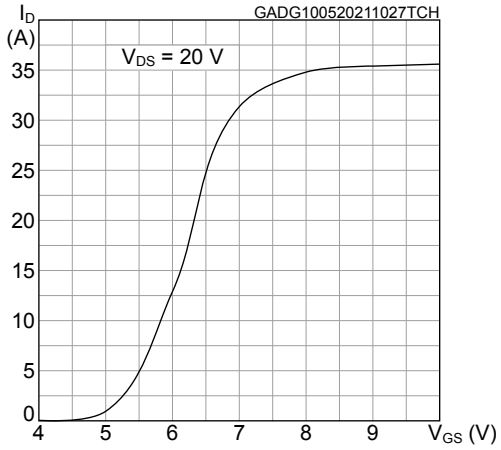


Figure 5. Typical gate charge characteristics

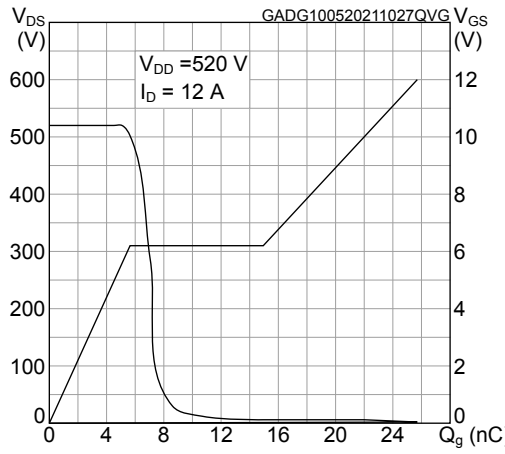


Figure 6. Typical drain-source on-resistance

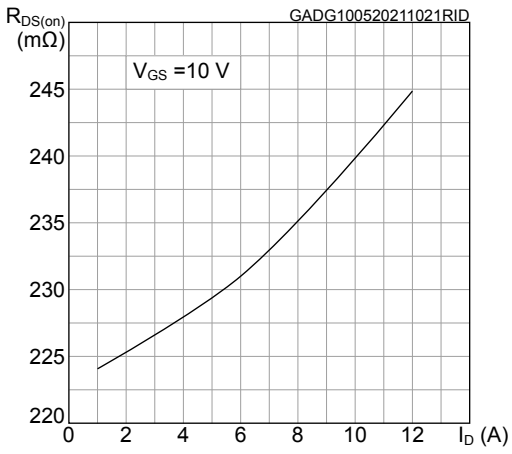


Figure 7. Typical capacitance characteristics

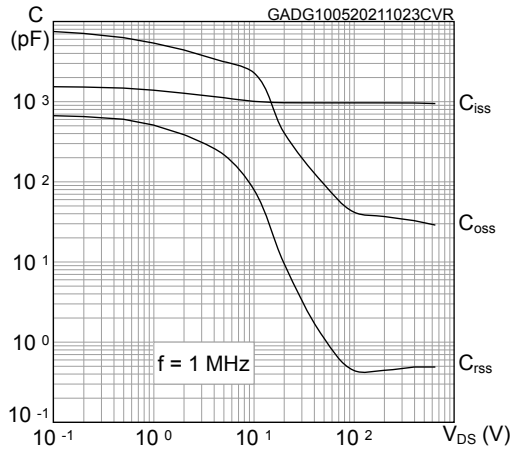


Figure 8. Normalized gate threshold vs temperature

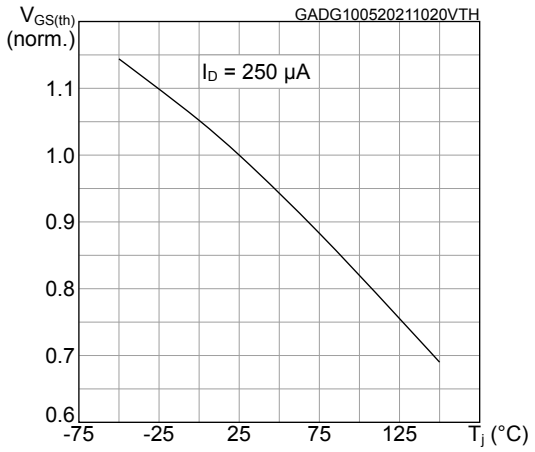


Figure 9. Normalized on-resistance vs temperature

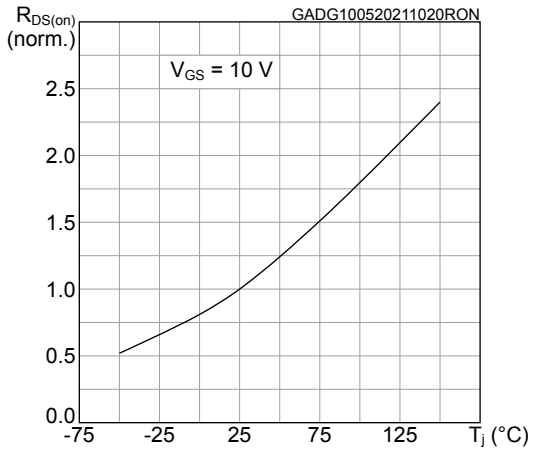


Figure 10. Normalized breakdown voltage vs temperature

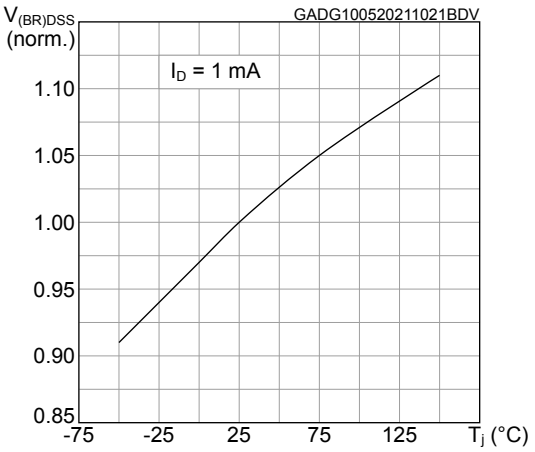


Figure 11. Typical reverse diode forward characteristics

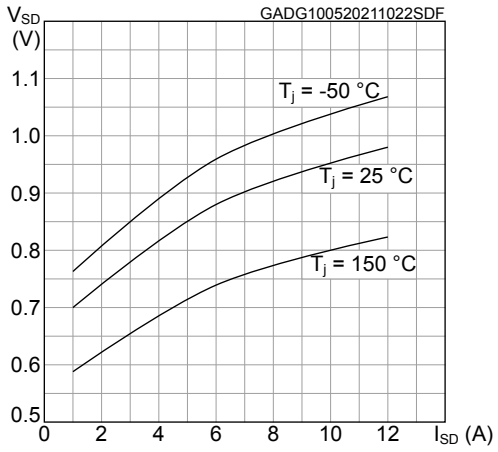
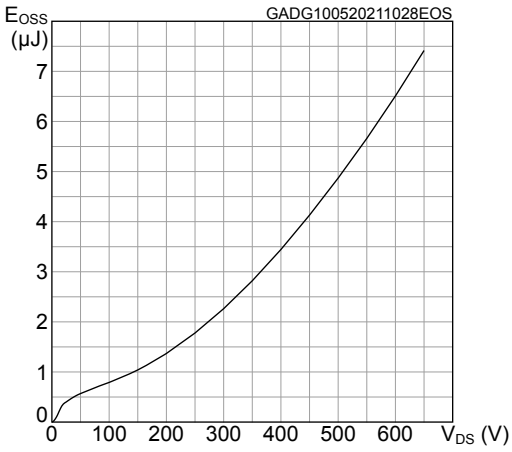


Figure 12. Typical output capacitance stored energy



3 Test circuits

Figure 13. Test circuit for resistive load switching times

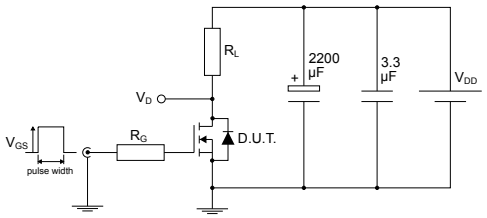


Figure 14. Test circuit for gate charge behavior

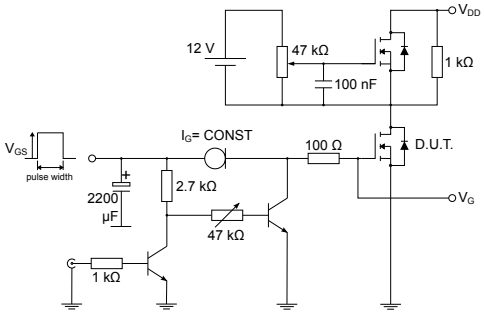


Figure 15. Test circuit for inductive load switching and diode recovery times

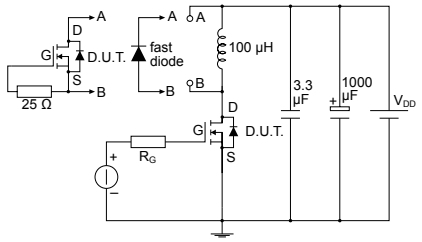


Figure 16. Unclamped inductive load test circuit

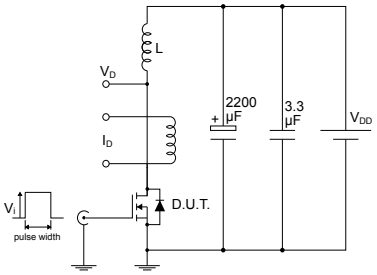


Figure 17. Unclamped inductive waveform

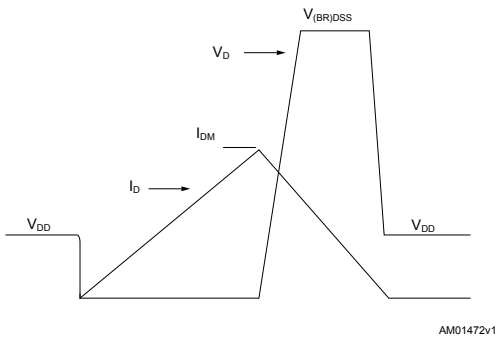
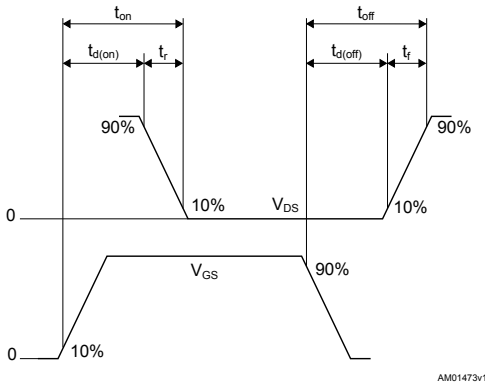


Figure 18. Switching time waveform



4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 TO-220FP package information

Figure 19. **TO-220FP package outline**

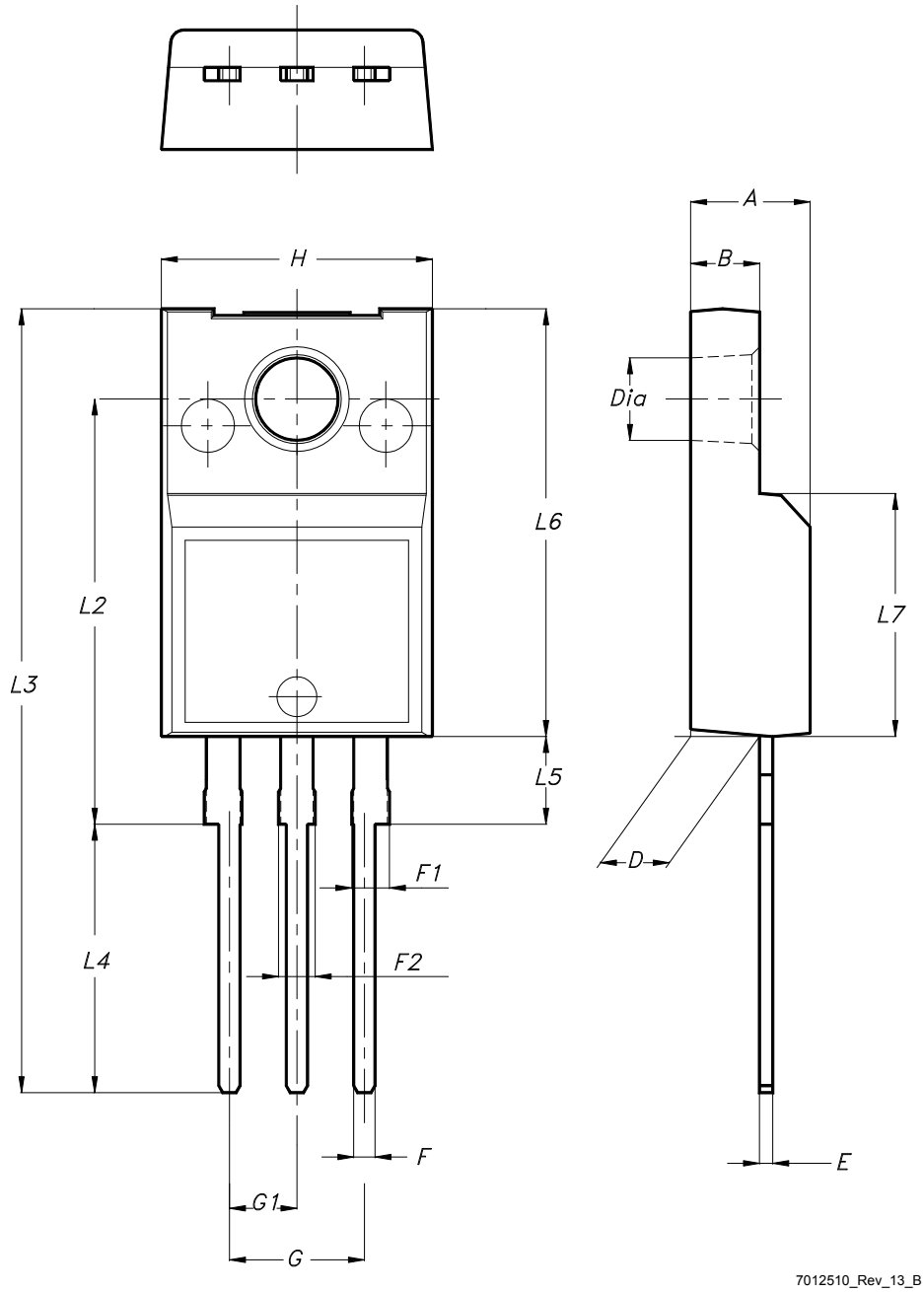


Table 8. **TO-220FP package mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
B	2.50		2.70
D	2.50		2.75
E	0.45		0.70
F	0.75		1.00
F1	1.15		1.70
F2	1.15		1.70
G	4.95		5.20
G1	2.40		2.70
H	10.00		10.40
L2		16.00	
L3	28.60		30.60
L4	9.80		10.60
L5	2.90		3.60
L6	15.90		16.40
L7	9.00		9.30
Dia	3.00		3.20

Revision history

Table 9. **Document revision history**

Date	Version	Changes
15-Mar-2019	1	First release.
10-May-2021	2	Modified features table on cover page. Modified Table 1. Absolute maximum ratings, Table 2. Thermal data, Table 3. Avalanche characteristics, Table 4. Static, Table 5. Dynamic, Table 6. Switching times and Table 7. Source-drain diode. Added Section 2.1 Electrical characteristics (curves). Minor text changes.

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