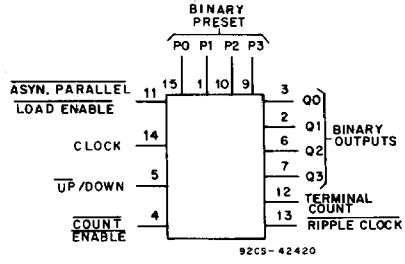
CD54AC193/3A
CD54ACT193/3A

Presettable Synchronous 4-Bit Binary Up/Down Counter with Reset

The RCA CD54AC193/3A and CD54ACT193/3A are up/down binary counters with separate up/down clocks. These devices utilize the new RCA ADVANCED CMOS LOGIC technology. Presetting the counter to the number on preset data inputs (P0-P3) is accomplished by a LOW asynchronous parallel load input ($\overline{PL}$). The counter is incremented on the LOW-to-HIGH transition of the Clock-Up input (and a HIGH level on the Clock-Down input) and decremented on the LOW-to-HIGH transition of the Clock-Down input (and a HIGH level on the Clock-Up input). A HIGH level on the Reset input overrides any other input to clear the counter to its zero state. The $\overline{TCU}$ (carry) output goes LOW half a clock period before the zero count is reached and returns to a HIGH level at the zero count. The $\overline{TCD}$ (borrow) output in the count down mode likewise goes LOW half a clock period before the maximum count (15 counts) and returns to HIGH at the maximum count. Cascading is effected by connecting the $\overline{TCU}$ and $\overline{TCD}$ outputs of a less significant counter to the Clock-Up and Clock-Down inputs, respectively, of the next most significant counter.

The CD54AC193/3A and CD54ACT193/3A are supplied in 16-lead dual-in-line ceramic packages (F suffix).



FUNCTIONAL DIAGRAM & TERMINAL ASSIGNMENT

Package Specifications

See Section 11, Fig. 11

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Static Electrical Characteristics (Limits with black dots (•) are tested 100%.)

CHARACTERISTICS	TEST CONDITIONS		V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C				UNITS
				+25		-55 to +125		
	V_I (V)	I_O (mA)		MIN.	MAX.	MIN.	MAX.	
Quiescent Supply Current (MSI) I_{CC}	V_{CC} or GND	0	5.5	—	8•	—	160•	μA

The complete static electrical test specification consists of the above by-type static tests combined with the standard static tests in the beginning of this section.

ACT INPUT LOADING TABLE

INPUT	UNIT LOAD*
P0 — P3, $\overline{PL}$	0.75
MR, CPU, CPD	0.85

*Unit load is ΔI_{CC} limit specified in Static Characteristics Chart, e.g., 2.4 mA max. @ 25°C.

Burn-In Test-Circuit Connections (Use Static II for /3A burn-in and Dynamic for Life Test.)

Static	STATIC BURN-IN I			STATIC BURN-IN II		
	OPEN	GROUND	V_{CC} (6V)	OPEN	GROUND	V_{CC} (6V)
CD54AC/ACT193	2,3,6,7,12, 13	1,4,5,8-11,14,15	16	2,3,6,7,12, 13	8	1,4,5,9-11,14-16
Dynamic	**OPEN**	**GROUND**	**1/2 V_{CC} (3V)**	**V_{CC} (6V)**	**OSCILLATOR**	
					50 kHz	**25 kHz**
CD54AC/ACT193	—	1,8-10,14,15	2,3,6,7,12,13	4,11,16	5	—

NOTE: Each pin except V_{CC} and Gnd will have a resistor of 2k-47k ohms.

CD54AC193/3A
CD54ACT193/3A

SWITCHING CHARACTERISTICS: AC Series; t_r, t_f = 3 ns, C_L = 50 pF (Worst Case)

CHARACTERISTICS	SYMBOL	V_{CC} (V)	-55 to +125°C		UNITS
			MIN.	MAX.	
Propagation Delays: $\overline{PL}$ to Qn	t_{PLH} t_{PHL}	1.5 3.3* 5†	— — —	200 29 15	ns
CPU to Qn CPD to Qn	t_{PLH} t_{PHL}	1.5 3.3 5	— — —	188 27 14•	ns
CPU to $\overline{TCU}$ CPD to $\overline{TCD}$	t_{PLH} t_{PHL}	1.5 3.3 5	— — —	152 22 11.2	ns
MR to Qn	t_{PLH} t_{PHL}	1.5 3.3 5	— — —	215 30 16	ns
MR to $\overline{TCU}$	t_{PLH} t_{PHL}	1.5 3.3 5	— — —	200 29 15	ns
MR to $\overline{TCD}$	t_{PLH} t_{PHL}	1.5 3.3 5	— — —	245 35 18.2	ns
Pn to Qn	t_{PLH} t_{PHL}	1.5 3.3 5	— — —	222 31 16.5	ns
Power Dissipation Capacitance	C_{PD}§	—	95 Typ.		pF
Input Capacitance	C_I	—	—	10	pF

SWITCHING CHARACTERISTICS: ACT Series; t_r, t_f = 3 ns, C_L = 50 pF (Worst Case)

CHARACTERISTICS	SYMBOL	V_{CC} (V)	-55 to +125°C		UNITS
			MIN.	MAX.	
Propagation Delays: $\overline{PL}$ to Qn	t_{PLH} t_{PHL}	5†	—	15	ns
CPU to Qn		5	—	14•	
CPD to Qn		5	—	14	
CPU to $\overline{TCU}$		5	—	11.2	
CPD to $\overline{TCD}$		5	—	11.2	
MR to QN		5	—	16	
MR to $\overline{TCU}$		5	—	15	
MR to $\overline{TCD}$		5	—	18.2	
Pn to Qn		5	—	16.5	
Power Dissipation Capacitance	C_{PD}§	—	126 Typ.		pF
Input Capacitance	C_I	—	—	10	pF

*3.3 V: min. is @ 3.6 V
max. is @ 3 V

†5 V: min. is @ 5.5 V
max. is @ 4.5 V

(Limits with black dots (•) are tested 100%.)

§C_{PD} is used to determine the dynamic power consumption per package.
For AC, $P_D = C_{PD}V_{CC}^2 f_i + \Sigma (C_L V_{CC}^2 f_o)$
For ACT, $P_D = C_{PD}V_{CC}^2 f_i + \Sigma (C_L V_{CC}^2 f_o) + V_{CC}\Delta I_{CC}$ where f_i = input frequency
f_o = output frequency
C_L = output load capacitance
V_{CC} = supply voltage