REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A	Removed vendor CAGE 61772 as source of supply for case outline letter Z, the F-11A package. Added case outline letters U and T, F-11 and D-15 to the drawing. Editorial changes throughout.	1990 OCT 04	M. A. Frye
B	Changes in accordance with NOR 5962-R042-95.	94-12-15	M. A. Frye
C	Updated boilerplate to reflect current requirements. Corrections to pages 4, 5, 8 and timing waveforms. - glg	01-01-17	Raymond Monnin

THE ORIGINAL FIRST PAGE OF THIS DRAWING HAS BEEN REPLACED.

REV																				
SHEET																				
REV	C	C																		
SHEET	15	16																		

REV STATUS OF SHEETS	REV	C	C	C	C	C	C	C	C	C	C	C	C	C	C
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

PREPARED BY
Kenneth Rice

DEFENSE SUPPLY CENTER COLUMBUS

COLUMBUS, OHIO 43216

STANDARD MICROCIRCUIT DRAWING

CHECKED BY
Ray Monnin

THIS DRAWING IS AVAILABLE FOR USE BY All DEPARTMENTS

APPROVED BY
Michael. A. Frye

MICROCIRCUITS, MEMORY, DIGITAL, CMOS, PARALLEL 512 X 9 FIFO, MONOLITHIC SILICON

AND AGENCIES OF THE DEPARTMENT OF DEFENSE

DRAWING APPROVAL DATE
23 May 1988

AMSC N/A

REVISION LEVEL	SIZE	CAGE CODE	
C	**A**	**67268**	**5962-87531**

SHEET 1 OF 16

DSCC FORM 2233
APR 97

5962-E172-01

1. SCOPE

1.1 Scope. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 Part or Identifying Number (PIN). The complete PIN shall be as shown in the following example:

5962-87531	01	X	X
Drawing number	Device type (see 1.2.1)	Case outline (see 1.2.2)	Lead finish (see 1.2.3)

1.2.1 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit	Access time
01	7201	512 X 9-bit parallel FIFO	30 ns
02	7201	512 X 9-bit parallel FIFO	50 ns
03	7201	512 X 9-bit parallel FIFO	80 ns

1.2.2 Case outline(s). The case outline(s) shall be as designated in MIL-STD-1835, and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	GDIP1-T28 or CDIP2-T28	28	dual-in-line package
Y	CQCC1-N32	32	rectangular chip carrier
Z	CDFP3-F28	28	flat package
U	GDFP2-F28	28	flat package
T	GDIP4-T28 or CDIP3-T28	28	dual-in-line package

1.2.3 Lead finish. The lead finish is as specified in MIL-PRF-38535, appendix A.

1.3 Absolute maximum ratings. 1/

Supply voltage range (V_{CC})	-0.5 V dc to +7.0 V dc
DC output current (I_{OUT})	50 mA
Ambient storage temperature	-65°C to +150°C
Temperature under bias	-55°C to +125°C
Thermal resistance, junction-to-case (Θ_{JC})	See MIL-STD-1835
Maximum power dissipation (P_D):	1.0 W 2/

1.4 Recommended operating conditions. 1/

Supply voltage range (V_{CC})	+4.5 V dc to +5.5 V dc
Ground voltage (V_{SS})	0 V dc
Minimum high level input voltage (V_{IH})	2.0 V dc
Maximum low level input voltage (V_{IL})	0.8 V dc
Case operating temperature range (T_C)	-55°C to +125°C
Rise time	5 ns
Fall time	5 ns

1/ All voltages referenced to V_{SS}.
2/ Must withstand the added P_D due to short circuit test; e.g., I_{OS}.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solicitation.

SPECIFICATION

DEPARTMENT OF DEFENSE

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

DEPARTMENT OF DEFENSE

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

HANDBOOKS

DEPARTMENT OF DEFENSE

MIL-HDBK-103 - List of Standard Microcircuit Drawings (SMD's).
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Unless otherwise indicated, copies of the specification, standards, and handbooks are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturer's approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table. The truth table shall be as specified on figure 2.

3.2.4 Die overcoat. Polyimide and silicone coatings are allowable as an overcoat on the die for alpha particle protection provided that each coated microcircuit inspection lot (see MIL-PRF-38535, appendix A) shall be subjected to and pass the Internal Water-Vapor Content test (test method 1018 of MIL-STD-883). The frequency of the internal water vapor testing may not be decreased unless approved by the preparing activity.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-HDBK-103 (see 6.6 herein). For packages where the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device.

3.5.1 Certification/compliance mark. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, Appendix A.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DSCC-VA shall be required in accordance with MIL-PRF-38535, appendix A.

3.9 Verification and review. DSCC, DSCC's agent and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test (method 1015 of MIL-STD-883).

(1) Test condition C or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or procuring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN} and C_{OUT} measurement) shall be measured only for the initial test and after any design or process changes which may affect capacitance. Sample size is 15 devices with no failures, and all input and output terminals tested.

d. Subgroups 7 and 8 tests shall include verification of the truth table.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $V_{SS} = 0$ V $4.5 \text{ V} \le V_{CC} \le 5.5$ V unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Input leakage current	I_{LI}	$0.4 \text{ V} \le V_{IN} \le V_{CC}$	1, 2, 3	All	-10	10	µA
Output leakage current	I_{LO}	$0.4 \text{ V} \le V_{OUT} \le V_{CC}$, $\overline{R} \ge V_{IH}$	1, 2, 3	All	-10	10	µA
Output low voltage	V_{OL}	$V_{CC} = 4.5$ V, $I_{OL} = 8.0$ mA $V_{IL} = 0.8$ V, $V_{IH} = 2.2$ V	1, 2, 3	All		0.4	V
Output high voltage	V_{OH}	$V_{CC} = 4.5$ V, $I_{OH} = -2.0$ mA $V_{IL} = 0.8$ V, $V_{IH} = 2.2$ V	1, 2, 3	All	2.4		V
Operating supply current	I_{CC1}	f = maximum, outputs open, V_{CC} = maximum	1, 2, 3	All		100	mA
Standby power supply current	I_{CC2}	$\overline{R} = \overline{W} = \overline{RS} = \overline{FL}/\overline{RT} = V_{IH}$, outputs open	1, 2, 3	All		15	mA
Power down current	I_{CC3}	All inputs = $V_{CC} - 0.2$ V, outputs open	1, 2, 3	All		900	µA
Input capacitance 1/	C_I	$V_I = 5.0$ V or GND, f = 1 MHz $T_C = +25°C$, See 4.3.1c	4	All		5	pF
Output capacitance 1/	C_O	$V_O = 5.0$ V or GND, f = 1 MHz $T_C = +25°C$, See 4.3.1c	4	All		7	pF
Functional tests		See 4.3.1d.	7, 8A, 8B	All			

See footnotes at end of table.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 2/ 3/ $-55°C \le T_C \le +125°C$ $V_{SS} = 0$ V $4.5 V \le V_{CC} \le 5.5$ V unless otherwise specified	Group A subgroups	Device types	Limits Min	Limits Max	Unit
Read cycle time	t_{RC}		9, 10, 11	01	40		ns
				02	65		
				03	100		
Access time	t_A		9, 10, 11	01		30	ns
				02		50	
				03		80	
Read recovery time	t_{RR}		9, 10, 11	01	10		ns
				02	15		
				03	20		
Read pulse width	t_{RPW}		9, 10, 11	01	30		ns
				02	50		
				03	80		
Read pulse low to data bus at low-Z	t_{RLZ} 4/		9, 10, 11	All	5		ns
Write pulse low to data bus at low-Z	t_{WLZ} 4/		9, 10, 11	All	5		ns
Data valid from read pulse high	t_{DV}		9, 10, 11	All	5		ns
Read pulse high to data bus at high-Z	t_{RHZ} 4/		9, 10, 11	01		20	ns
				02,03		30	
Write cycle time	t_{WC}		9, 10, 11	01	40		ns
				02	65		
				03	100		
Write pulse width	t_{WPW}		9, 10, 11	01	30		ns
				02	50		
				03	80		
Write recovery time	t_{WR}		9, 10, 11	01	10		ns
				02	15		
				03	20		
Data setup time	t_{DS}		9, 10, 11	01	18		ns
				02	30		
				03	40		
Data hold time	t_{DH}		9, 10, 11	01	0		ns
				02	5		
				03	10		
Reset cycle time	t_{RSC}		9, 10, 11	01	40		ns
				02	65		
				03	100		
Reset pulse width	t_{RS}		9, 10, 11	01	30		ns
				02	50		
				03	80		
Reset recovery time	t_{RSR}		9, 10, 11	01	10		ns
				02	15		
				03	20		

See footnotes at end of table.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 2/ 3/ $-55°C \le T_C \le +125°C$ $V_{SS} = 0$ V $4.5 V \le V_{CC} \le 5.5 V$ unless otherwise specified	Group A subgroups	Device types	Limits Min	Limits Max	Unit
Reset setup time	t_{RSS}		9, 10, 11	01	30		ns
				02	50		
				03	80		
Retransmit cycle time	t_{RTC}		9, 10, 11	01	40		ns
				02	65		
				03	80		
Retransmit pulse width	t_{RT}		9, 10, 11	01	30		ns
				02	50		
				03	80		
Retransmit recovery time	t_{RTR}		9, 10, 11	01	10		ns
				02	15		
				03	20		
Reset to empty flag low	t_{EFL}		9, 10, 11	01		40	ns
				02		65	
				03		100	
Read low to empty flag low	t_{REF}		9, 10, 11	01		30	ns
				02		45	
				03		60	
Read high to full flag high	t_{RFF}		9, 10, 11	01		30	ns
				02		45	
				03		60	
Write high to empty flag high	t_{WEF}		9, 10, 11	01		30	ns
				02		45	
				03		60	
Write low to full flag low	t_{WFF}		9, 10, 11	01		30	ns
				02		45	
				03		60	
Reset to half-full and full flag high	t_{HFH} t_{FFH}		9, 10, 11	01		40	ns
				02		65	
				03		100	
Read/write to $\overline{XO}$ low	t_{XOL}		9, 10, 11	01		30	ns
				02		50	
				03		80	
Read/write to $\overline{XO}$ high	t_{XOH}		9, 10, 11	01		30	ns
				02		50	
				03		80	
$\overline{XI}$ pulse width	t_{XI}		9, 10, 11	01	30		ns
				02	50		
				03	80		
$\overline{XI}$ recovery time	t_{XIR}		9, 10, 11	All	10		ns
$\overline{XI}$ setup time	t_{XIS}		9, 10, 11	All	15		ns

1/ This parameter tested initially and after any design or process change which could affect this parameter, and is therefore guaranteed to the limits specified in table I.
2/ For output load circuit and ac test conditions, see figure 3.
3/ For timing waveforms, see figure 4.
4/ May not be tested, but shall be guaranteed to the limits specified in table I.

Device types	All	
Case outlines	X, Z, U, T	Y
Terminal number	Terminal symbol	
1	$\overline{W}$	NC
2	D_8	$\overline{W}$
3	D_3	D_8
4	D_2	D_3
5	D_1	D_2
6	D_0	D_1
7	$\overline{XI}$	D_0
8	$\overline{FF}$	$\overline{XI}$
9	Q_0	$\overline{FF}$
10	Q_1	Q_0
11	Q_2	Q_1
12	Q_3	NC
13	Q_8	Q_2
14	GND	Q_3
15	$\overline{R}$	Q_8
16	Q_4	GND
17	Q_5	NC
18	Q_6	$\overline{R}$
19	Q_7	Q_4
20	$\overline{XO}$ / $\overline{HF}$	Q_5
21	$\overline{EF}$	Q_6
22	$\overline{RS}$	Q_7
23	$\overline{FL}$ / $\overline{RT}$	$\overline{XO}$ / $\overline{HF}$
24	D_7	$\overline{EF}$
25	D_6	$\overline{RS}$
26	D_5	$\overline{FL}$ / $\overline{RT}$
27	D_4	NC
28	V_{CC}	D_7
29	---	D_6
30	---	D_5
31	---	D_4
32	---	V_{CC}

NC = no connection

FIGURE 1. Terminal connections.

Reset and retransmit
Single device configuration/width expansion mode

Mode	Inputs			Internal status		Outputs		
	$\overline{RS}$	$\overline{RT}$	$\overline{XI}$	Read pointer	Write pointer	$\overline{EF}$	$\overline{FF}$	$\overline{HF}$
Reset	0	X	0	Location zero	Location zero	0	1	1
Retransmit	1	0	0	Location zero	Unchanged	X	X	X
Read/write	1	1	0	Increment 1/	Increment 1/	X	X	X

1/ Pointer will increment if flag is high.

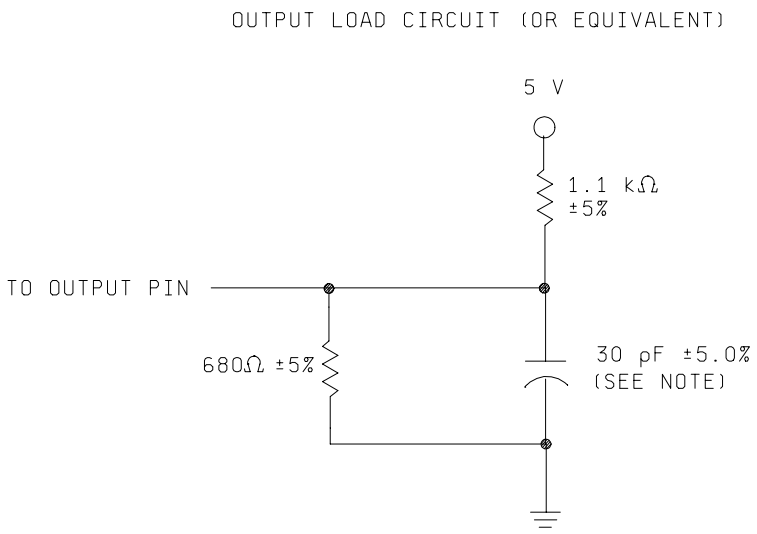
Reset and first load
Depth expansion/compound expansion mode

	Inputs			Internal status		Outputs	
Mode	$\overline{RS}$	$\overline{FL}$	$\overline{XI}$	Read pointer	Write pointer	$\overline{EF}$	$\overline{FF}$
Reset first device	0	0	1/	Location zero	Location zero	0	1
Reset all other devices	0	1	1/	Location zero	Location zero	0	1
Read/write	1	X	1/	X	X	X	X

1/ $\overline{XI}$ is connected to $\overline{XO}$ of previous device.

NOTES: $\overline{RS}$ = Reset input, $\overline{FL}$ / $\overline{RT}$ = First load/retransmit, $\overline{EF}$ = Empty flag output, $\overline{FF}$ = Full flag output, $\overline{XI}$ = Expansion input, and $\overline{HF}$ = Half-full flag output
0 = Low level voltage
1 = High level voltage
X = Don't care

FIGURE 2. Truth tables.



NOTE: C_L includes scope and jig capacitance.

AC test conditions

Input pulse levels	GND to 3.0 V
Input rise and fall times	5 ns
Input timing reference levels	1.5 V
Output reference levels	1.5 V

FIGURE 3. Output load circuit and ac test conditions.

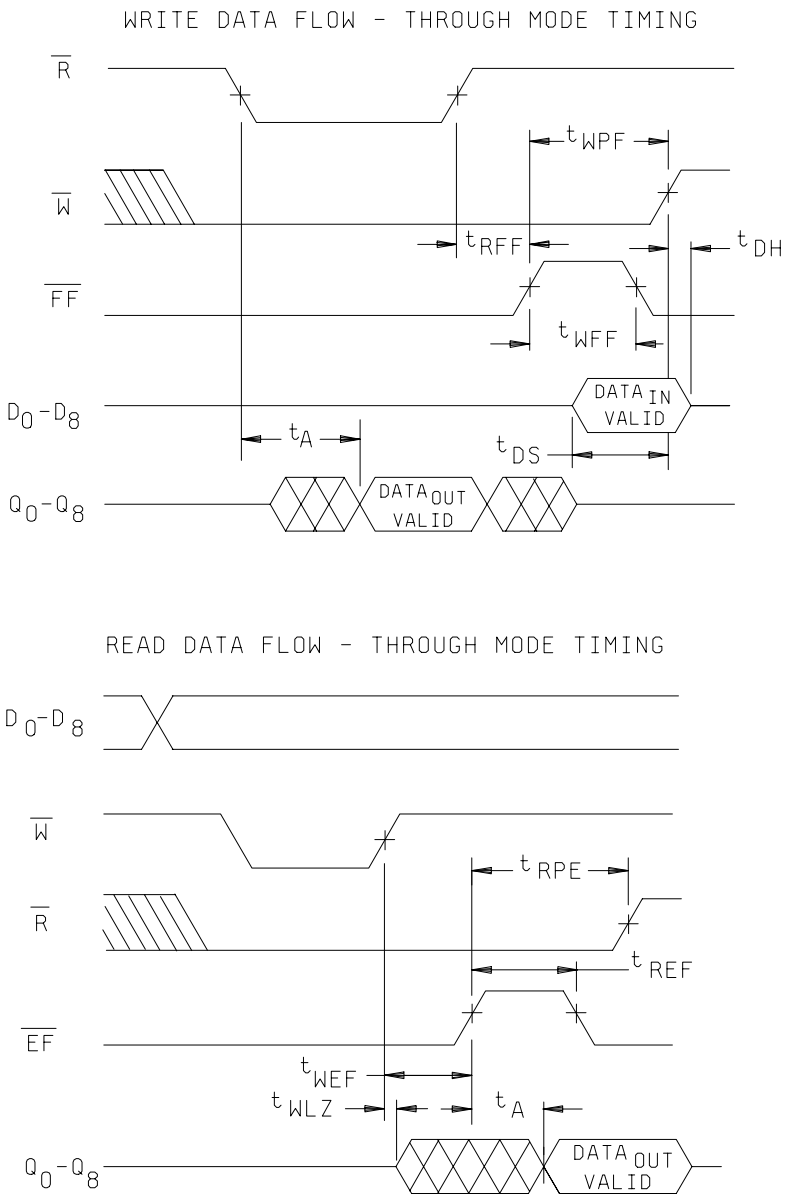
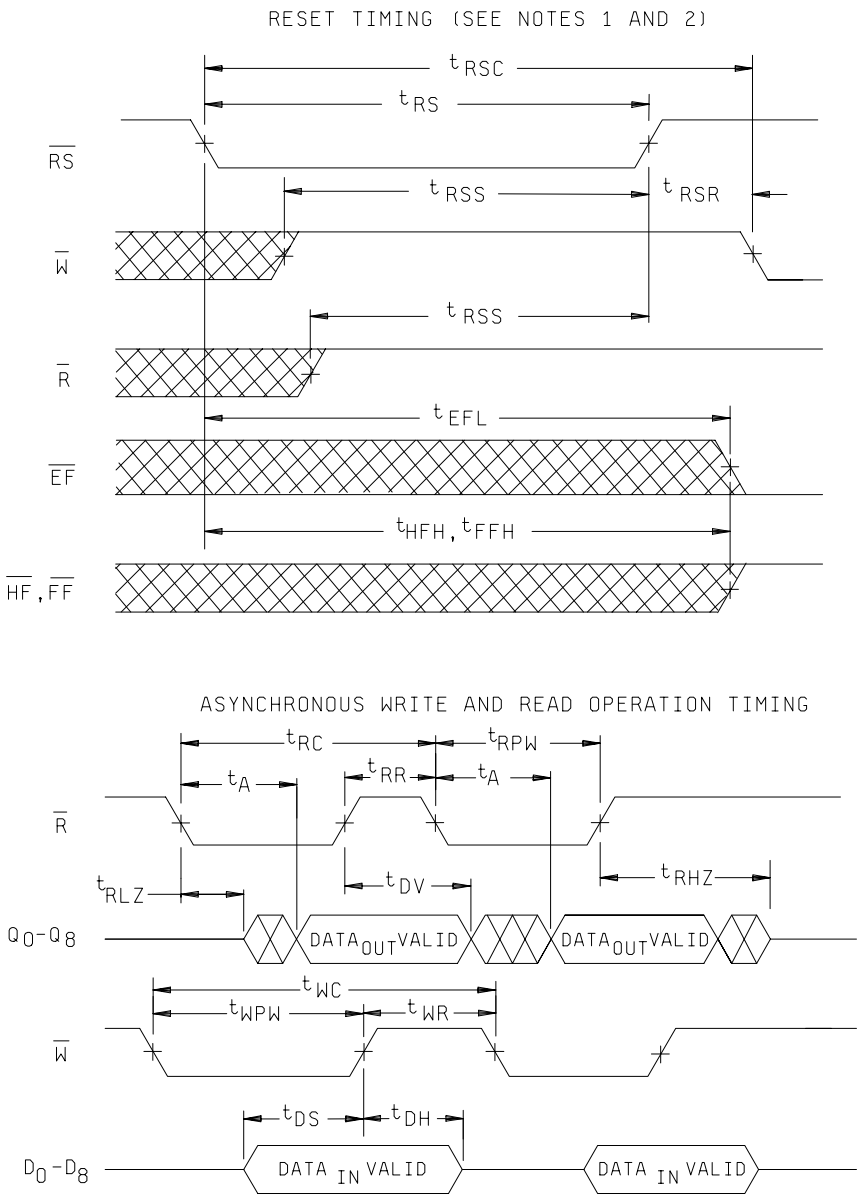


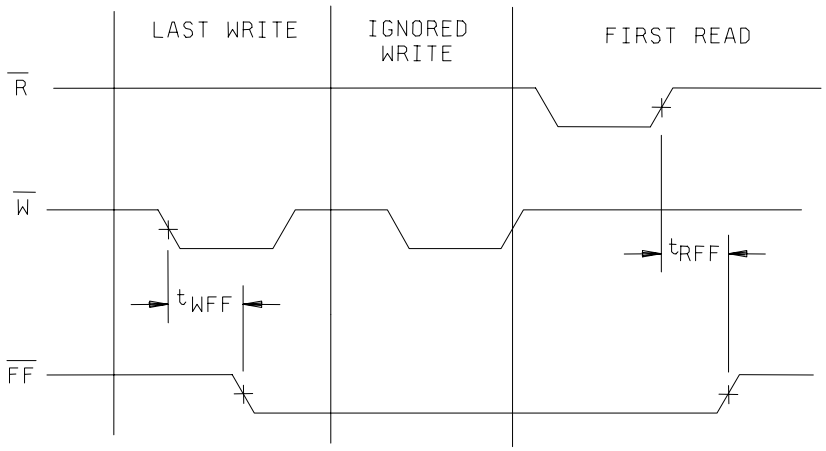
FIGURE 4. Timing waveforms.



Notes:
1. $\overline{EF}$, $\overline{FF}$, and $\overline{HF}$ may change status during RESET but flags will be valid at t_{RSC}.
2. W and R = V_{IH} around the rising edge of RS.

FIGURE 4. Timing waveforms - continued.

FULL FLAG FROM LAST WRITE TO FIRST READ



EMPTY FLAG FROM LAST READ TO FIRST WRITE TIMING

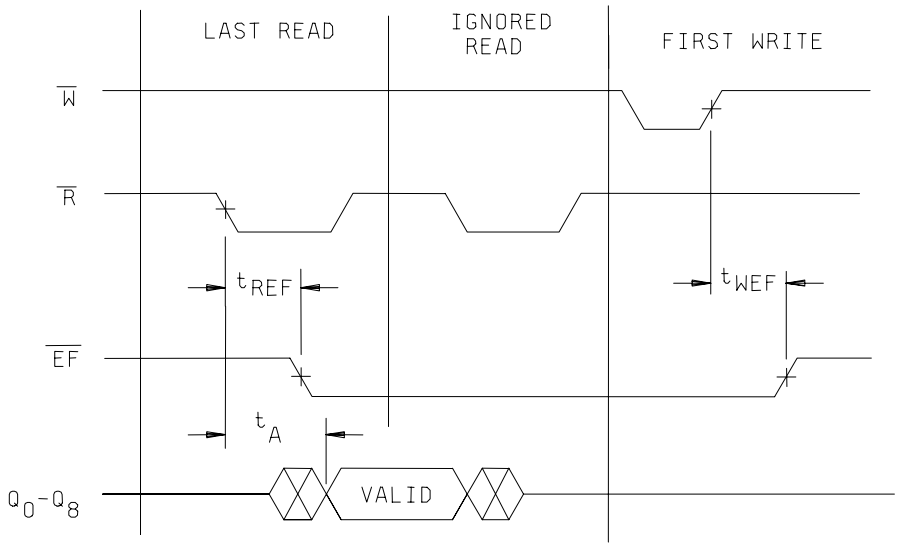
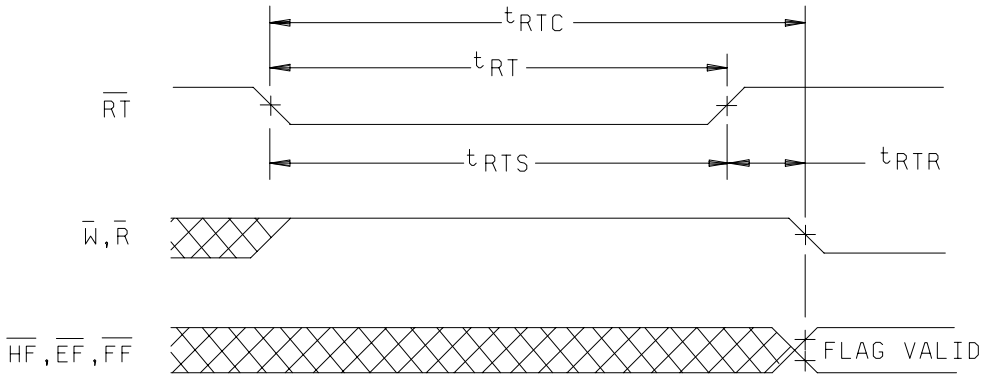
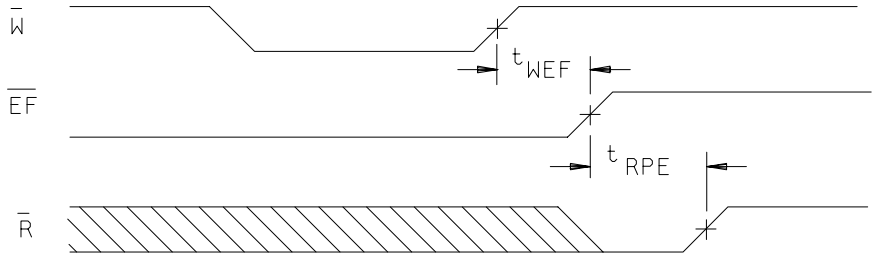


FIGURE 4. Timing waveforms - continued.

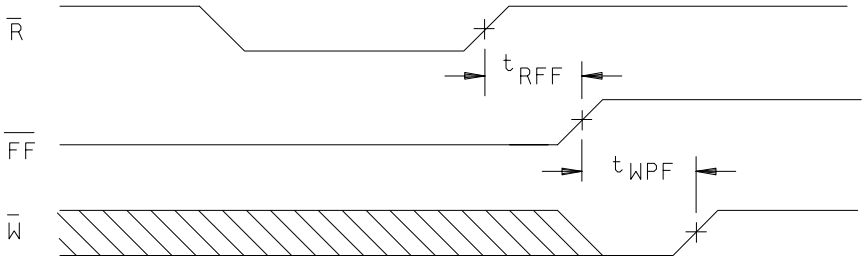
RETRANSMIT TIMING (SEE NOTE 3)



EMPTY FLAG TIMING



FULL FLAG TIMING



Note: $\overline{EF}$, $\overline{FF}$, and $\overline{HF}$ may change status during RETRANSMIT but flags will be valid to t_{RTC}.

FIGURE 4. Timing waveforms - continued.

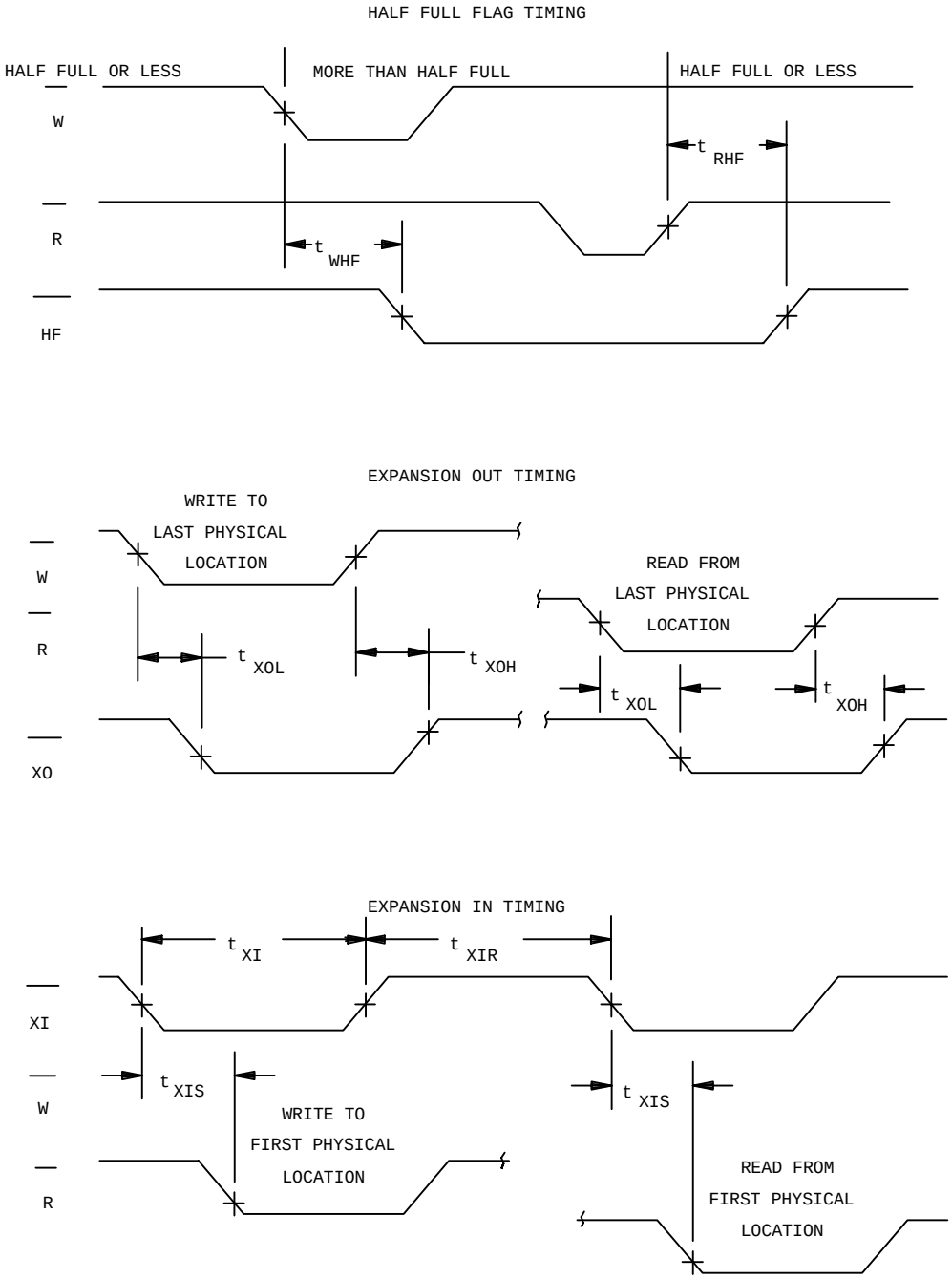


FIGURE 4. Timing waveforms - continued.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition C or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or procuring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

TABLE II. Electrical test requirements. *

MIL-STD-883 test requirements	Subgroups (per method 5005, table I)
Interim electrical parameters (method 5004)	1
Final electrical test parameters (method 5004)	1*, 2, 3, 7*, 8, 9, 10, 11
Group A test requirements (method 5005)	1, 2, 3, 4**, 7, 8, 9, 10, 11
Groups C and D end-point electrical parameters (method 5005)	1, 2, 3, 7, 8A, 8B

* Indicates PDA applies to subgroups 1 and 7.
** See 4.3.1c.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users should inform Defense Supply Center Columbus when a system application requires configuration control and which SMD's are applicable to that system. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0525.

6.5 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43216-5000, or telephone 614-692-0674.

6.6 Approved source of supply. An approved source of supply is listed herein. Additional sources will be added as they become available. The vendor listed herein has agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to DSCC-VA.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 01-01-17

Approved sources of supply for SMD 5962-87531 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535.

Standard microcircuit 1/ drawing PIN	Vendor CAGE number	Vendor similar PIN 2/
5962-8753101XA	61772	IDT7201LA30DB
5962-8753101YA	61772	IDT7201LA30XB
5962-8753101ZA	3/	IDT7201LA30XB
5962-8753101UA	61772	IDT7201LA30XEB
5962-8753101TA	61772	IDT7201LA30TCB
5962-8753102XA	61772	IDT7201LA50DB
5962-8753102YA	61772	IDT7201LA50XB
5962-8753102ZA	3/	IDT7201LA50XB
5962-8753102UA	61772	IDT7201LA50XEB
5962-8753102TA	61772	IDT7201LA50TCB
5962-8753103XA	61772	IDT7201LA80DB
5962-8753103YA	61772	IDT7201LA80XB
5962-8753103ZA	3/	IDT7201LA80XB
5962-8753103UA	61772	IDT7201LA80XEB
5962-8753103TA	61772	IDT7201LA80TCB

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the Vendor to determine its availability.
2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.
3/ No longer available from an approved source.

Vendor CAGE number	Vendor name and address
61772	Integrated Device Technology, Incorporated 2975 Stender Way Santa Clara, CA 95054