10-bit DAC Bi-directional ±100mA H-Bridge Driver

FEATURES

- 2.3V to 5V power supply
- VCM Driver for Auto-Focus
- ±100mA current sink
- Low quiescent current
- 10 bit resolution DAC
- support VRC (VCM Ring Control) modes
- 2 wire I2C serial interface clock rates up to 1MHz(1.8V interface available)
- Power Down mode current consumption less than 1uA
- Thermal Shutdown
- Power on reset
- Small 0.4mm pitch WLCSP 0.73mm x 1.13mm x 0.30mm -6B

APPLICATIONS

Mobile Camera

Digital still camera

Camcorder

Security camera

Web camera

Nano motor

GENERAL DESCRIPTION

The AW8601 is a bidirectional voice coil motor driver chip, which contains a 10-bit DAC. The maximum output current is ±100mA. AW8601 operating voltage from 2.3V to 5V.

The AW8601 is controlled through the I2C serial interface, and its operating frequency can reach up to 1MHz. The device address of the chip is 0x18(7-bit 0x0c), and which can be changed by the factory.

The AW8601 contains VRC mode, which allows programmable configuration of output current waveform to minimize mechanical vibration and can be suitable for different types of voice coil motors.

The AW8601 contains power on reset circuit and power off function. The reset circuit ensures that the digital circuit works well when supply power up. In power down mode, the supply current consumption less than 1μA.

The AW8601 can be used for auto focus applications in mobile cameras, digital still cameras, camcorders, web cameras and action cameras.

The AW8601 is available in a WLCSP 0.73mm x 1.13mm x 0.30mm -6B package.

PIN CONFIGURATION AND TOP MARK

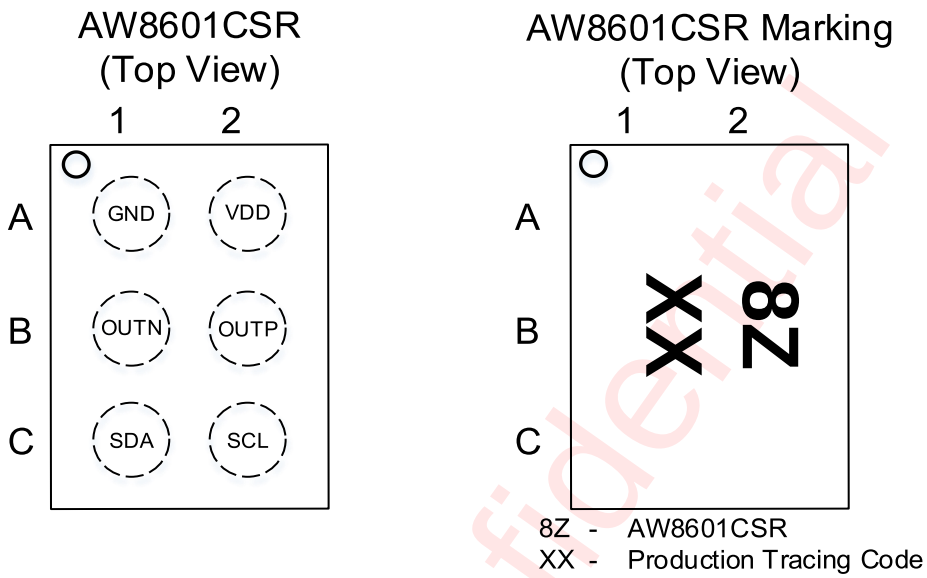


Figure 1 AW8601CSR Pin Configuration and Top Mark

PIN DEFINITION

No.	NAME	DESCRIPTION
A1	GND	Ground
A2	VDD	Chip power supply
B1	OUTN	H bridge negative output
B2	OUTP	H bridge positive output
C1	SDA	I2C bus data input/output
C2	SCL	I2C bus clock input

FUNCTIONAL BLOCK DIAGRAM

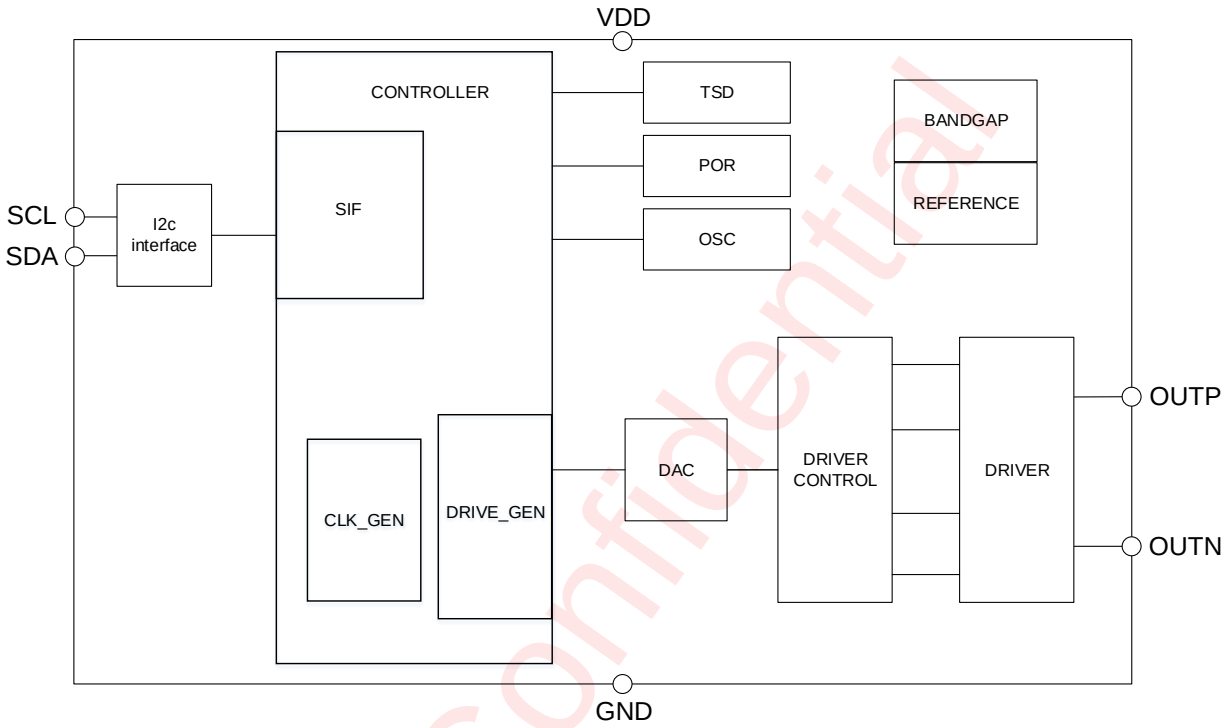


Figure 2 Functional Block Diagram

TYPICAL APPLICATION CIRCUITS

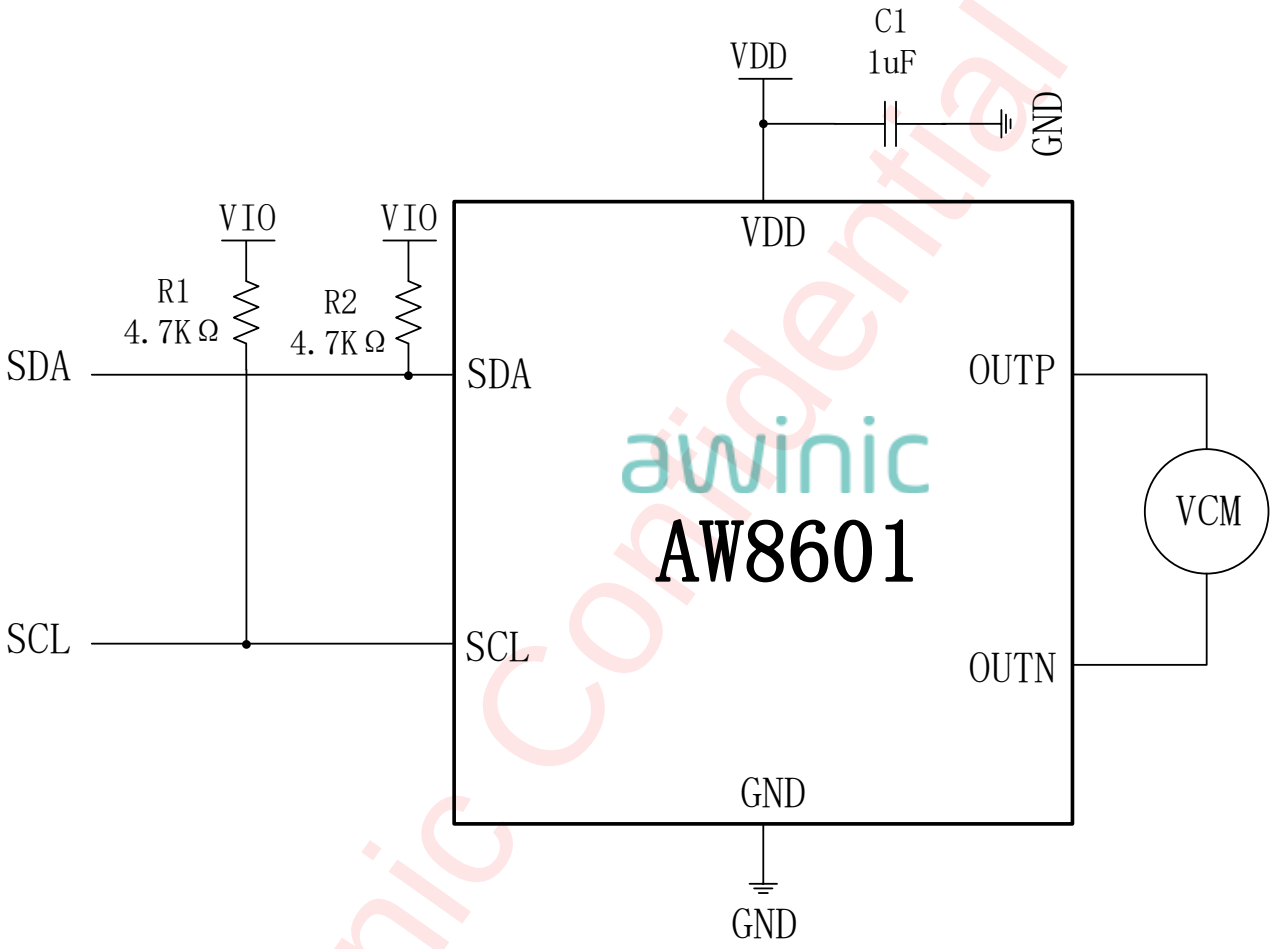


Figure 3 Typical Application Circuit of AW8601

ORDERING INFORMATION

Part Number	Temperature	Package	Marking	Moisture Sensitivity Level	Environmental Information	Delivery Form
AW8601CSR	-40℃～85℃	WLCSP 0.73x1.13x0.30-6B	8Z	MSL1	ROHS+HF	3000 units/ Tape and Reel

ABSOLUTE MAXIMUM RATINGS(NOTE1)

PARAMETERS	RANGE
Supply voltage range V_{DD}	-0.3V to 5.5V
Control input voltage range	-0.3V to VDD+0.3V
Operating free-air temperature range	-40°C to 85°C
Maximum operating junction temperature T_{JMAX}	150°C
Storage temperature T_{STG}	-45°C to 150°C
Lead temperature (soldering 10 seconds)	280°C
ESD	
All PIN(HBM)(NOTE 2)	±2000V
All PIN(CDM)(NOTE 3)	±1500V
Latch-up	
Test method: JESD78E	+IT：200mA -IT：-200mA

NOTE1: Conditions out of those ranges listed in "absolute maximum ratings" may cause permanent damages to the device. In spite of the limits above, functional operation conditions of the device should within the ranges listed in "recommended operating conditions". Exposure to absolute-maximum-rated conditions for prolonged periods may affect device reliability.

NOTE2: The human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin. Test method: ESDA/JEDEC JS-001-2017.

NOTE3: Test method: ESDA/JEDEC JS -002-2018.

ELECTRICAL CHARACTERISTICS

VDD=2.8V, VIO=1.8V, T_A=25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
Overall						
VDD	Power supply voltage	On pin VDD	2.3		5	V
IQ	Quiescent current	DAC≠512	0.25	0.35	0.45	mA
IQz	Quiescent current	DAC=512	0.2	0.3	0.4	mA
ISD	Shutdown current	VDD=3.6	-1	0.1	1	μA
Logic input / output						
I	Input current	VDD=VIN~3.6	-1	0.1	1	μA
VIL	Logic input low level	SCL/SDA			0.5	V
VIH	Logic input high level	SCL/SDA	1.3			V
THSD	Hardware reset time	SCL=SDA=0		2		ms
Tg	Glitch rejection				50	ns
Bi-directional mode						
Imax	Maximum output current		±97	±100	±103	mA
Izero	Zero code current	Code=512	-1	0.1	1	μA
Ipd	Output current for shutdown mode	shutdown mode	-1	0.1	1	μA
Resolution	DAC resolution			10		Bits
INL_P	INL	Positive	-4		4	LSB
INL_N		Negative	-4		4	LSB
DNL_P	DNL	Positive	-1		1	LSB
DNL_N		Negative	-1		1	LSB
Tset	Setup time		100			μs
Uni-directional mode						
Imax	Maximum output current		97	100	103	mA
Izero	Zero code current	Code=0	-1	0.1	1	μA
Ipd	Output current for shutdown mode	shutdown mode	-1	0.1	1	μA
Resolution	DAC resolution			10		Bits
INL	INL		-4		4	LSB
DNL	DNL		-1		1	LSB

I²C INTERFACE

This device supports the I²C serial bus and data transmission protocol in fast mode at 400 kHz and super-fast mode at 1000kHz. This device operates as a slave on the I²C bus. Connections to the bus are made via the open-drain I/O pins SCL and SDA. The pull-up resistor can be selected in the range of 1k~10kΩ and the typical value is 4.7kΩ. This device can support different high level (1.8V~3.6V) of this I²C interface.

DEVICE ADDRESS

The I2C device address is 0x18(7-bit 0x0C) and can be set.

DATA VALIDATION

When SCL is high level, SDA level must be constant. SDA can be changed only when SCL is low level.

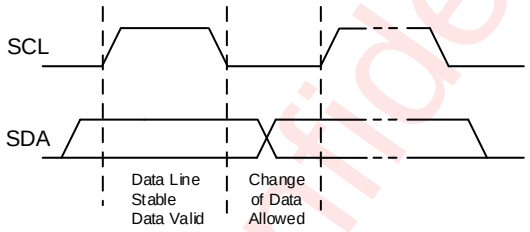


Figure 4 Data Validation Diagram

GENERAL I²C OPERATION

The I²C bus employs two signals, SDA (data) and SCL (clock), to communicate between integrated circuits in a system. The device is addressed by a unique 7-bit address; the same device can send and receive data. In addition, Communications equipment has distinguish master from slave device: In the communication process, only the master device can initiate a transfer and terminate data and generate a corresponding clock signal. The devices using the address access during transmission can be seen as a slave device.

SDA and SCL connect to the power supply through the current source or pull-up resistor. SDA and SCL default is a high level. There is no limit on the number of bytes that can be transmitted between start and stop conditions. When the last word transfers, the master generates a stop condition to release the bus.

START state: The SCL maintain a high level, SDA from high to low level

STOP state: The SCL maintain a high level, SDA pulled low to high level

Start and Stop states can be only generated by the master device. In addition, if the device does not produce STOP state after the data transmission is completed, instead re-generate a START state (Repeated START, Sr), and it is believed that this bus is still in the process of data transmission. Functionally, Sr state and START state is the same. As shown in Figure5.

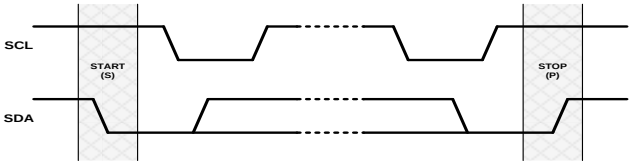


Figure 5 START and STOP state generation process

In the data transmission process, when the clock line SCL maintains a high level, the data line SDA must

remain the same. Only when the SCL maintain a low level, the data line SDA can be changed, as shown in Figure 6. Each transmission of information on the SDA is 9 bits as a unit. The first eight bits are the data to be transmitted, and the first one is the most significant bit (Most Significant Bit, MSB), the ninth bit is an confirmation bit (Acknowledge, ACK or A), as shown in Figure 7. When the SDA transmits a low level in ninth clock pulse, it means the acknowledgment bit is 1, namely the current transmission of 8 bits data are confirmed, otherwise it means that the data transmission has not been confirmed. Any amount of data can be transferred between START and STOP state.

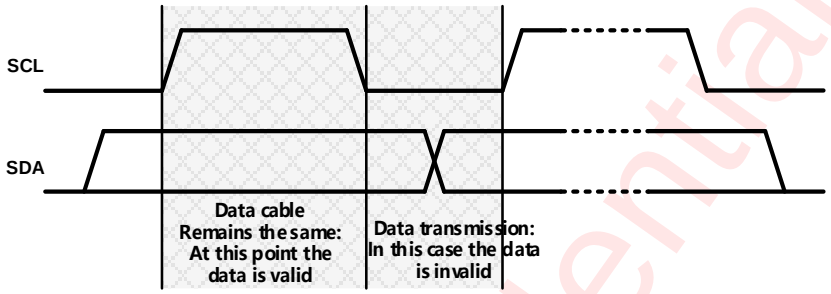


Figure 6 The data transfer rules on the I²C bus

The whole process of actual data transmission is shown in Figure7. When generating a START condition, the master device sends an 8-bit data, including a 7-bit slave addresses (Slave Address), and followed by a "read / write" flag ($R/\overline{W}$). The flag is used to specify the direction of transmission of subsequent data. The master device will produce the STOP state to end the process after the data transmission is completed. However, if the master device intends to continue data transmission, you can directly send a Repeated START state, without the need to use the STOP state to end transmission.

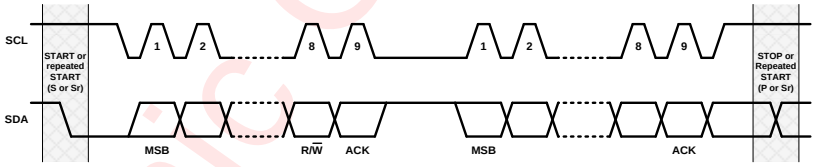


Figure 7 Data transmission on the I²C bus

WRITE PROCESS

Writing process refers to the master device write data into the slave device. In this process, the transfer direction of the data is always unchanged from the master device to the slave device. All acknowledge bits are transferred by the slave device, in particular, the device as the slave device, the transmission process in accordance with the following steps, as shown in Figure 8.

Master device generates START state. The START state is produced by pulling the data line SDA to a low level when the clock SCL signal is a high level.

Master device transmits the 7-bits device address of the slave device, followed by the "read / write" flag (flag $R/\overline{W} = 0$);

The slave device asserts an acknowledgment bit (ACK) to confirm whether the device address is correct;

The master device transmits the 8-bit register address to which the first data byte will written;

The slave device asserts an acknowledgment (ACK) bit to confirm the register address is correct;

Master sends 8 bits of data to register which needs to be written;

The slave device asserts an acknowledgment bit (ACK) to confirm whether the data is sent successfully;

If the master device needs to continue transmitting data by sending another pair of data bytes, just need to repeat the sequence from step 6. In the latter case, the targeted register address will have been auto-incremented by the device.

The master device generates the STOP state to end the data transmission.

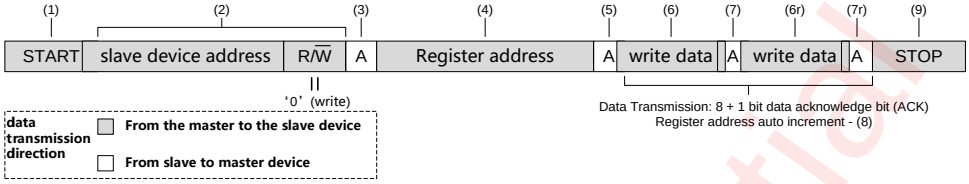


Figure 8 Writing process (data transmission direction remains the same)

READ PROCESS

Reading process refers to the slave device reading data back to the master device. In this process, the direction of data transmission will change. Before and after the change, the master device sends START state and slave address twice, and sends the opposite "read/write" flag. In particular, AW8601 as the slave device, the transmission process carried out by following steps listed in Figure 9.

Master device asserts a start condition;

Master device transmits the 7 bits address of the device, and followed by a "read / write" flag ($R/\overline{W}$ = 0);

The slave device asserts an acknowledgment bit (ACK) to confirm whether the device address is correct;

The master device transmits the register address to make sure where the first data byte will read;

The slave device asserts an acknowledgment (ACK) bit to confirm whether the register address is correct or not;

The master device restarts the data transfer process by continuously generating STOP state and START state or a separate Repeated START;

Master sends 7-bits address of the slave device and followed by a read / write flag (flag $R/\overline{W}$ = 1) again;

The slave device asserts an acknowledgment (ACK) bit to confirm whether the register address is correct or not;

Master transmits 8 bits of data to register which needs to be read;

The slave device sends an acknowledgment bit (ACK) to confirm whether the data is sent successfully;

The device automatically increment register address once after sent each acknowledge bit (ACK);

The master device generates the STOP state to end the data transmission.

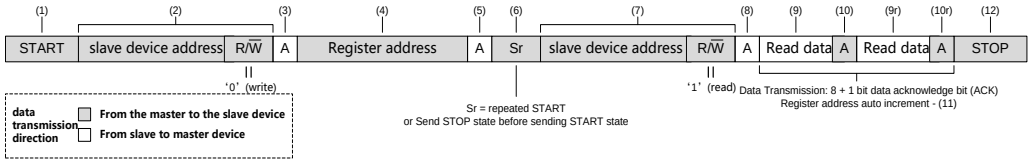


Figure 9 Reading process (data transmission direction remains the same)

I2C TIMING FEATURE

Parameter			Fast mode			Super-fast mode			UNIT
No.	Symbol	Name	MIN	TYP	MAX	MIN	TYP	MAX	
1	f_{SCL}	SCL Clock frequency			400			1000	kHz
2	t_{LOW}	SCL Low level Duration	1.3			0.5			μs
3	t_{HIGH}	SCL High level Duration	0.6			0.26			μs
4	t_{RISE}	SCL, SDA rise time			0.3			0.12	μs
5	t_{FALL}	SCL, SDA fall time			0.3			0.12	μs
6	$t_{SU:STA}$	Setup time SCL to START state	0.6			0.3			μs
7	$t_{HD:STA}$	(repeat-start) start condition hold time	0.6			0.3			μs
8	$t_{SU:STO}$	Stop condition setup time	0.6			0.26			μs
9	t_{BUF}	Time between start and stop condition	1.3			0.5			μs
10	$t_{SU:DAT}$	SDA setup time	0.1			0.05			μs
11	$t_{HD:DAT}$	SDA hold time	0			0			ns

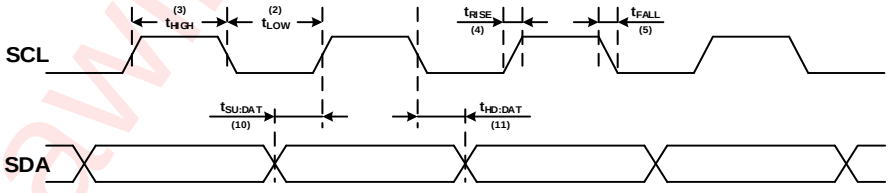


Figure 10 SCL and SDA timing relationships in the data transmission process

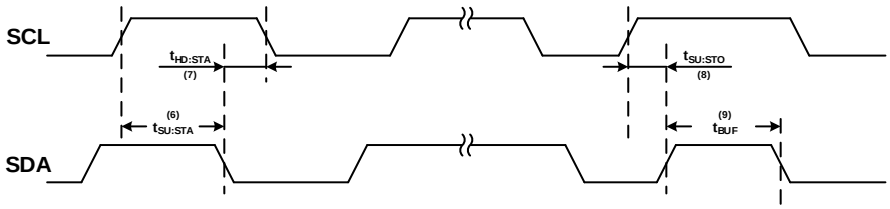


Figure 11 The timing relationship between START and STOP state

POWER UP SEQUENCE

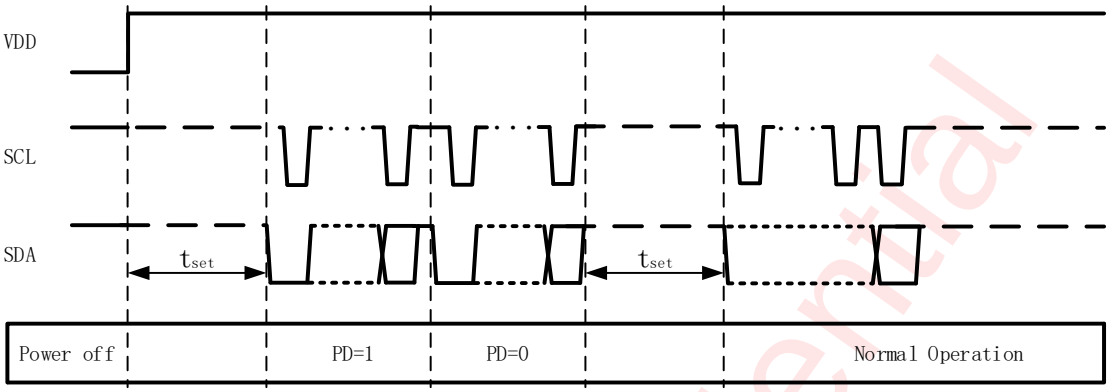


Figure 12 power up sequence

HARDWARE RESET

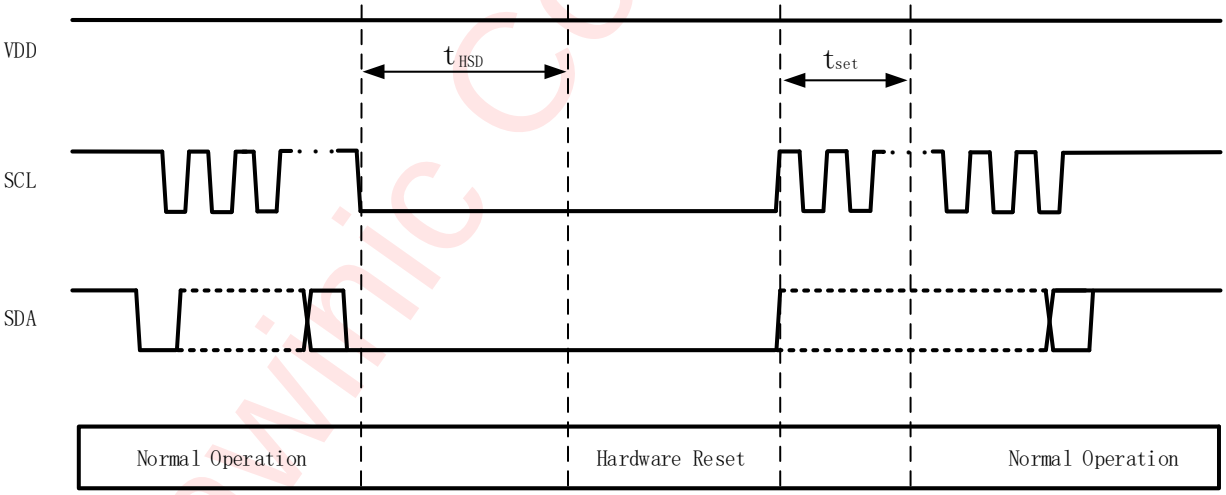


Figure 13 Hardware reset

NOTE1: The AW8601 has hardware reset function, but the default value of hardware reset is disabled. It can be enabled by factory option.

NOTE2: Both SCL and SDA turn low and keep it more than t_{HSD}, AW8601 turns into hardware reset, and all the register are clear.

NOTE3: Either SCL or SDA rise to high level, AW8601 is set to Normal Operation.

NOTE4: During the t_{set}, AW8601 is Initialized Driver IC.

NORMAL MODE

Register List

ADDR	NAME	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Default
0x00	**IC_INFO**	**R**	IC_VENDOR_ID				IC_MODEL				0x01
0x01	**IC_VER**	**R**	Reserved				DESIGN ROUND				0x01
0x02	**Control**	**R/W**							RING	PD	0x00
0x03	**VCM MSB**	**R/W**							D9	D8	0x02
0x04	**VCM LSB**	**R/W**	D7	D6	D5	D4	D3	D2	D1	D0	0x00
0x05	**Status**	**R**				TSD				BUSY	0x00
0x06	**Mode**	**R/W**	VRC1	VRC0						DIV2	0x00
0x07	**TIME**	**R/W**	DIV1	DIV0	VRCT5	VRCT4	VRCT3	VRCT2	VRCT1	VRCT0	0x60

Register Detailed Description

IC_INFO：Chip information Register(Address 0x00) Default: 0x01

Bit	Symbol	R/W	Description	Default
7:4	IC_VENDOR_ID	R	Chip ID	0x00
3:0	IC_MODEL	R	Chip model information	0x01

IC_VER：Chip Version Register(Address 0x01) Default: 0x01

Bit	Symbol	R/W	Description	Default
7:4	RESERVED	R	Reserved	0x00
3:0	DESIGN ROUND	R	DESIGN ROUND	0x01

Control：Chip Control Register(Address 0x02) Default: 0x00

Bit	Symbol	R/W	Description	Default
7:2	RESERVED	RW	Reserved	0x00
1	RING	RW	RING 0 : Direct mode 1 : Algorithm mode	0x00
0	PD	RW	Power down mode 0: normal mode 1: power down mode	0x00

VCM MSB：DAC input Register(Address 0x03) Default: 0x02

Bit	Symbol	R/W	Description	Default
7:2	RESERVED	RW	Reserved	0x00
1:0	VCM MSB	RW	10 bits DAC input	0x02

VCM LSB：DAC input Register(Address 0x04) Default: 0x00

Bit	Symbol	R/W	Description	Default
7:0	VCM LSB	RW	10 bits DAC input D[9:0] current(mA) 0000000000 -100.19 0000000001 -100.00 0000000010 -99.80 … 0111111110 -0.39 0111111111 -0.19 1000000000 0.00 1000000001 0.19 1000000010 0.39 … 1111111110 99.80 1111111111 100.00	0x00

Status：Chip Status Register(Address 0x05) Default: 0x00

Bit	Symbol	R/W	Description	Default
7:5	RESERVED	R	Reserved	0x00
4	TSD	R	TSD : Thermal Shutdown state monitor 0 : Normal operation mode 1 : TSD mode	0x00
3:1	RESERVED	R	Reserved	0x00
0	BUSY	R	BUSY: Ringing control operation state check 0: Ringing control ending 1: Ringing control operating	0x00

Mode：Chip Mode Register(Address 0x06) Default: 0x00

Bit	Symbol	R/W	Description	Default
7:6	VRC[1:0]	RW	Algorithm Control Mode Ring VRC[1:0] MODE 0 0X Direct mode 0 1X LSC mode 1 00 VRC2 mode 1 01 VRC3 mode 1 10 VRC4 mode 1 11 VRC5 mode	0x00
5:1	Reserved	RW	Reserved	0x00
0	DIV2	RW	Divider	0x00

Time：Chip Algorithm time Register(Address 0x07) Default: 0x60

Bit	Symbol	R/W	Description	Default
7:6	DIV[1:0]	RW	Divider DIV[2:0] Tvib 000 T_{ope} X 2 001 T_{ope} X 1 010 T_{ope} X 1/2 011 T_{ope} X 1/4 100 T_{ope} X 8 101 T_{ope} X 4 other Reserved	0x01
5:0	VRCT[5:0]	RW	Algorithm period T_{ope} = 6.3ms + VRCT[5:0] * 0.1ms LSC 1-step period = 252us + (VRCT[5:0]*4)	0x40

Normal algorithm set up Method

mode	VRC operation time[NOTE1]	Tolerance of VCM[NOTE2]
Direct	-	-
LSC	Tvib[NOTE3]	-
VRC2	0.5* Tvib [NOTE3]	± 9 %
VRC3	0.75* Tvib [NOTE3]	± 19 %
VRC4	1.25* Tvib [NOTE3]	± 37 %
VRC5	1.65* Tvib [NOTE3]	± 43 %

NOTE1: The time to reach a target current.
NOTE2: Tolerance can be changed by mechanical characteristics of specific motors.
NOTE3: Tvib = vibration period of motor.

VRC MODE

AW8601 has an VRC mode. It enters its VRC mode by writing 0x08, 0x0A sequentially. The VRC mode adjusts the amplitude and timing of the output current to meet the requirements. The VRC mode adapts to the voice coin motors of different manufacturers. VRC mode effectively reduces motor vibration time.

Register List

ADDR	NAME	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Default
0x00	**IC INFO**	**R**	IC_MANU_ID				IC_MODEL				0x01
0x01	**PHASE0**	**R/W**		PHASE0_AMP			PHASE0_TIME				0x01
0x02	**PHASE1**	**R/W**	PHASE1_AMP			PHASE1_TIME				PD	0x00
0x03	**VCM MSB**	**R/W**							D9	D8	0x02
0x04	**VCM LSB**	**R/W**	D7	D6	D5	D4	D3	D2	D1	D0	0x00
0x05	**STATUS**	**R**				TSD				BUSY	0x00
0x06	**PHASE2**	**R/W**		PHASE2_AMP			PHASE2_TIME				0x00
0x07	**PHASE3**	**R/W**		PHASE3_AMP			PHASE3_TIME				0x60
0x08	**SWITCH**	**R/W**							VRC_CFG		0x02
0x09	**PHASE4**	**R/W**		PHASE4_AMP			PHASE4_TIME				0x00
0x0A	**PHASE5**	**R/W**		PHASE5_AMP			PHASE5_TIME				0x00
0x0F	**PHASE6**	**R/W**		PHASE6_AMP			PHASE6_TIME				0x00
0x10	**PHASE7**	**R/W**		PHASE7_AMP			PHASE7_TIME				0x00
0x11	**PHASE8**	**R/W**		PHASE8_AMP			PHASE8_TIME				0x00
0x12	**PHASE9**	**R/W**		PHASE9_AMP			PHASE9_TIME				0x00
0x13	**PHASEA**	**R/W**		PHASEA_AMP			PHASEA_TIME				0x00
0x14	**TIME_UNIT**	**R/W**	T7	T6	T5	T4	T3	T2	T1	T0	0x00

Register Detailed Description

IC_INFO：Chip information Register(Address 0x00) Default: 0x01

Bit	Symbol	R/W	Description	Default
7:4	IC_MANU_ID	R	Chip ID	0x00
3:0	IC_MODEL	R	Chip model information	0x01

PHASE0：VRC Mode Phase0 Register(Address 0x01) Default: 0x01

Bit	Symbol	R/W	Description	Default
7	RESERVED	RW	Reserved	0x00
6:4	PHASE0_AMP	RW	PHASE0_AMP PHASE0_AMP[2:0] Amplitude 000 0 001 1/4 010 1/2 011 3/4 100 1 other 0	0x00
3:0	PHASE0_TIME	RW	PHASE0_TIME PHASE0_TIME[3:0] TIME 0000 0*TIME_UNIT 0001 1*TIME_UNIT 0010 2*TIME_UNIT … 1110 14*TIME_UNIT 1111 15*TIME_UNIT	0x01

PHASE1：Chip Control Register(Address 0x02) Default: 0x00

Bit	Symbol	R/W	Description	Default
7:5	PHASE1_AMP	RW	PHASE1_AMP PHASE1_AMP[2:0] Amplitude 000 0 001 1/4 010 1/2 011 3/4 100 1 other 0	0x00
4:1	PHASE1_TIME	RW	PHASE1_TIME PHASE1_TIME[3:0] TIME 0000 0*TIME_UNIT 0001 1*TIME_UNIT 0010 2*TIME_UNIT … 1110 14*TIME_UNIT 1111 15*TIME_UNIT	0x00
0	PD	RW	Power down mode 0: normal mode 1: power down mode	0x00

VCM MSB：DAC input Register(Address 0x03) Default: 0x02

Bit	Symbol	R/W	Description	Default
7:2	RESERVED	RW	Reserved	0x00
1:0	VCM MSB	RW	10 bits DAC input	0x02

VCM LSB：DAC input Register(Address 0x04) Default: 0x00

Bit	Symbol	R/W	Description	Default
7:0	VCM LSB	RW	10 bits DAC input D[9:0] current(mA) 0000000000 -100.19 0000000001 -100.00 0000000010 -99.80 … 0111111110 -0.39 0111111111 -0.19 1000000000 0.00 1000000001 0.19 1000000010 0.39 … 1111111110 99.80 1111111111 100.00	0x00

Status：Chip Status Register(Address 0x05) Default: 0x00

Bit	Symbol	R/W	Description	Default
7:5	RESERVED	R	RESERVED	0x00
4	TSD	R	TSD : Thermal Shutdown state monitor 0 : Normal operation mode 1 : TSD mode	0x00
3:1	RESERVED	R	RESERVED	0x00
0	BUSY	R	BUSY: Ringing control operation state check 0: Ringing control ending 1: Ringing control operating	0x00

PHASE2,4-A：VRC Mode Phase Register(Address 0x06 0x09 0x0A 0x0F 0x10 0x11 0x12 0x13) Default: 0x00

Bit	Symbol	R/W	Description	Default
7	RESERVED	RW	Reserved	0x00
6:4	PHASE_AMP	RW	PHASE_AMP PHASE_AMP[2:0] Amplitude 000 0 001 1/4 010 1/2 011 3/4 100 1 other 0	0x00
3:0	PHASE_TIME	RW	PHASE_TIME PHASE_TIME[3:0] TIME 0000 0*TIME_UNIT 0001 1*TIME_UNIT 0010 2*TIME_UNIT … 1110 14*TIME_UNIT 1111 15*TIME_UNIT	0x00

PHASE3：VRC Mode Phase3 Register(Address 0x07) Default: 0x60

Bit	Symbol	R/W	Description	Default
7	RESERVED	RW	Reserved	0x00
6:4	PHASE3_AMP	RW	PHASE3_AMP PHASE3_AMP[2:0] Amplitude 000 0 001 1/4 010 1/2 011 3/4 100 1 other 0	0x06
3:0	PHASE3_TIME	RW	PHASE3_TIME PHASE3_TIME[3:0] TIME 0000 0*TIME_UNIT 0001 1*TIME_UNIT 0010 2*TIME_UNIT … 1110 14*TIME_UNIT 1111 15*TIME_UNIT	0x00

SWITCH：VRC Mode Switch Register(Address 0x08) Default: 0x02

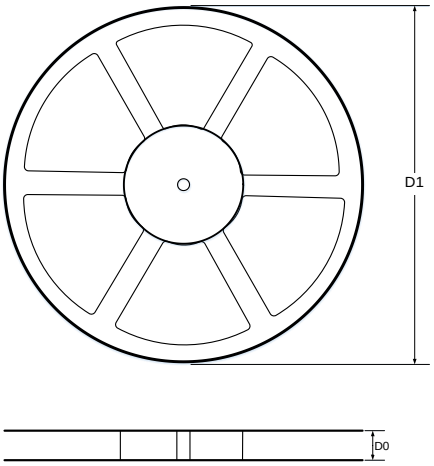
Bit	Symbol	R/W	Description	Default
7:2	RESERVED	RW	Reserved	0x00
1	VRC_CFG	RW	VRC_CFG: VRC mode configuration 0: normal mode 1: VRC mode	0x01
0	RESERVED	RW	Reserved	0x00

TIME_UNIT：VRC Mode Time Unit Register(Address 0x14) Default: 0x00

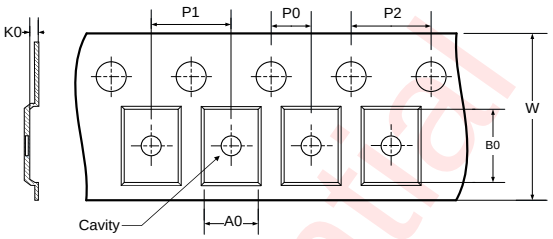
Bit	Symbol	R/W	Description	Default
7:0	TIME_UNIT	RW	TIME_UNIT T[7:0] TIME(us) 00000000 1 00000001 1*8 00000010 2*8 … 11111101 253*8 11111110 254*8 11111111 255*8	0x00

TAPE AND REEL INFORMATION

REEL DIMENSIONS

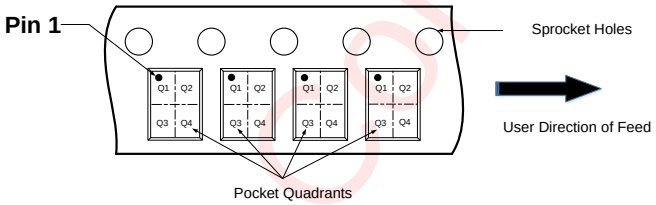


TAPE DIMENSIONS



A0：Dimension designed to accommodate the component width
B0：Dimension designed to accommodate the component length
K0：Dimension designed to accommodate the component thickness
W：Overall width of the carrier tape
P0：Pitch between successive cavity centers and sprocket hole
P1：Pitch between successive cavity centers
P2：Pitch between sprocket hole
D1：Reel Diameter
D0：Reel Width

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

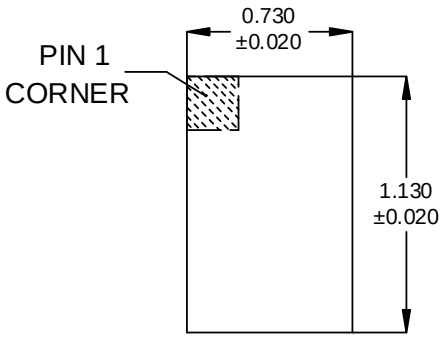


DIMENSIONS AND PIN1 ORIENTATION

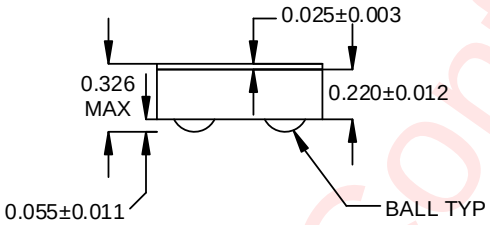
D1 (mm)	D0 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
179.00	9.00	0.83	1.25	0.38	2.00	4.00	4.00	8.00	Q1

All dimensions are nominal

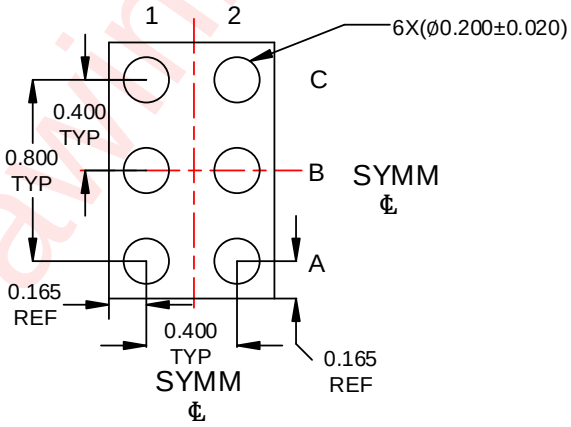
PACKAGE DESCRIPTION



Top View



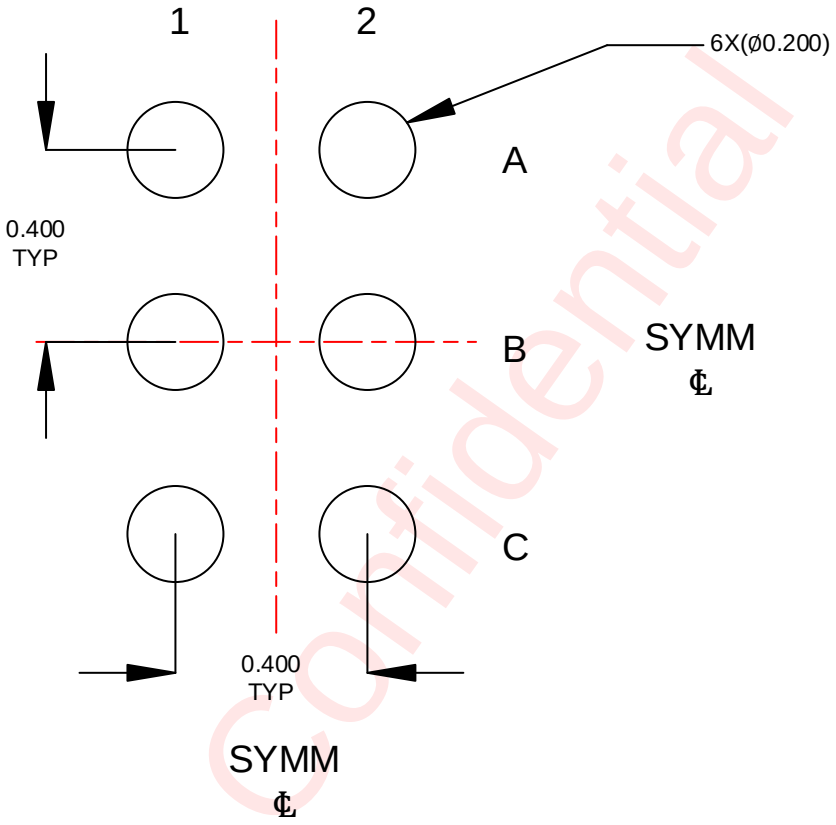
Side View

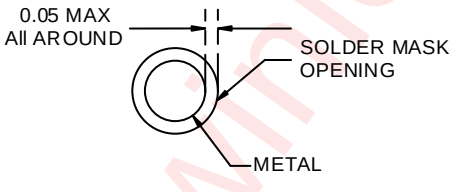


Bottom View

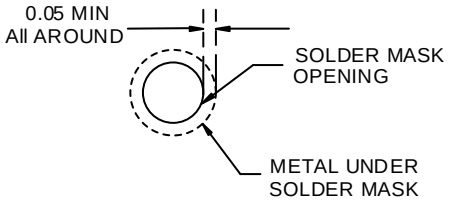
Unit: mm

LAND PATTERN DATA





NON-SOLDER MASK DEFINED



SOLDER MASK DEFINED

Unit: mm

Revision History

Version	Date	Change Record
V1.0	Nov 2019	Officially released
V1.1	Feb 2020	1. Figure 4 changed 2. Device address description changed 3. Fixed incorrect bit setting for register list
V1.2	Aug 2020	1. Device address description changed 2. Change Vin to VIO
V1.3	Oct 2021	1. Add normal mode
V1.4	Nov 2021	1. Change algorithm name 2. Change Algorithm period name

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