Signetics

68172
VMEbus Controller (BUSCON)

Product Specification

Military Customer Specific Products

DESCRIPTION

The Signetics 68172 VMEbus Controller (BUSCON) is an interface device for the VMEbus. It can be used in three different configurations: master-only, slave-only, and master/slave. The 68172 can be used with a processor-type interface or with a DMA controller-type interface. In all configurations, it handles the VMEbus signaling protocol in compliance with revisions B and C of the VMEbus Specification.

CONFIGURATION/VERSION

Applications of the BUSCON are identified as follows (see Figures 1 through 4):

VERSION	APPLICATION
PMS	Processor-type master/slave
DMAC	DMA controller/type master/slave
MS	Either PMS or (DMAC)
M	Master-only
S	Slave-only

All of these applications are handled by the 68172, with unused pins tied to stated logic levels in some of the applications.

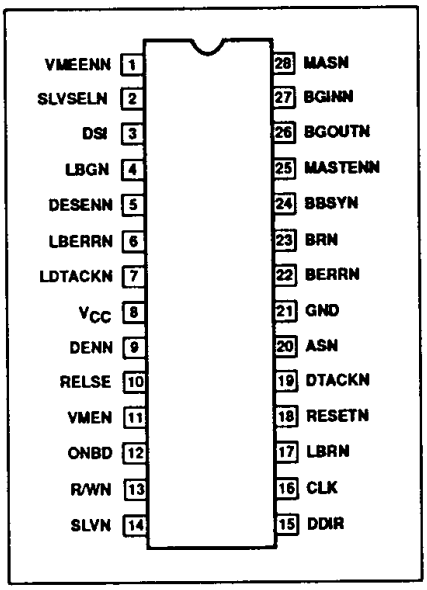
Figure 5 shows a functional model of the 68172 logic. The ASN, MASN, LBRN, BGINN, and RELSE inputs are internally synchronized to CLK before being presented to the state machine which determines the major functions of the device. The SLVN, ONBD, and VMEN signals are used directly in the state machine, although they are highly qualified to prevent metastable conditions on the state machine outputs. the BRN, BBSYN and LBGN signals are direct state machine outputs, while ASN, MASTENN, VMEENN, SLVSELN, and BGOUTN are derived from the state machine outputs plus some combinatorial qualification.

The DSI, R/WN, DTACKN, BERRN, LDTACKN, and LBERRN inputs function largely as direct combinatorial inputs. The DDIR, DTACKN, BERRN, LDTACKN, LBERRN, and (when applicable) MASN outputs are largely derived directly from these direct inputs, with some qualification from the state machine outputs. The DENN and DSENN outputs have complex multi-case logic which uses both the direct inputs and the state machine outputs.

FEATURES

- **Master, slave, or master/slave (dual ported) applications**
- **Helps assure VMEbus compatibility**
- **Allows for address decoding time**
- **Processor or DMA controller interface for master/requester**
- **Master/requester logic allows release on request (ROR) or release when done (RWD) operation, early or intercycle release**
- **Supports and exploits address lookahead**

PIN CONFIGURATION



ORDERING INFORMATION

DESCRIPTION	ORDERING CODE
28–Pin CERDIP	68172/BXA

PIN DESCRIPTION

MNEMONIC	PIN NO.	TYPE	CONFIG	NAME AND FUNCTION
CLK	16	I	All	**Clock:** User-supplied clock signal.
SLVN	14	I	S,MS	**Slave:** Active-low decode of the VMEbus address and address modifier lines indicating that the current cycle is for this board. SLVN should not be qualified with ASN nor VMEENN. It is first sampled on the rising clock edge after the rising edge on which ASN is first detected. It must remain valid until after the next low-going edge on DTACKN or BERRN. In a master-only application, SLVN should be pulled up to V_{CC}.
ASN	20	I/O I	M,MS S	**Address Strobe:** Direct connect to VMEbus ASN.
VMEN	11	I	M,MS	**VME Decode:** Active-low decode of the master's address lines, indicating that the master's current cycle is for a slave on the VMEbus. VMEN should not be qualified with MASN nor MASTENN. It is first sampled on the rising clock edge after the one on which MASN is first detected. Thereafter, it must remain valid until MASN goes false (high). In a slave-only configuration, VMEN should be pulled up to V_{CC}.
LBRN	17	I	M,MS	**Local Bus Request:** Connected to the low-active bus request output of a DMA controller. Typically tied to a high logic level in processor-type interfaces.
ONBD	12	1	MS	**Onboard:** Active-high decode of the master's address lines, indicating that the master's current cycle is for an onboard slave that is dual-ported with the VMEbus. ONBD should not be qualified with MASN or MASTENN. It is first sampled on the rising clock edge after the one on which MASN is first detected. Thereafter, it must remain valid until after MASN goes false (high). In a master-only or slave-only application, ONBD should be grounded. If a master/slave configuration does not contain "local slaves" as shown in Figure 3, VMEN and ONBD should both be connected to an active-low "VME decode". A cycle between the onboard master and a local slave (VMEN high, ONBD low) is ignored by BUSCON, and can proceed concurrently with a cycle between another VMEbus master and an onboard dual-ported slave.
MASN	28	I	M,PMS DMAC	**Master's Address Strobe:** RMW and Sequential VMEbus master cycles are accomplished by holding MASN low across several data strobes. If LBGN is high at the end of the RESETN low time, the state of ASN is driven onto MASN whenever BUSCON does not have control of the VMEbus. In a slave-only application, MASN should be pulled up to V_{CC}.
MASTENN	25	O	MS	**Master Enable:** In a master/slave application, the low state of this signal enables the master onto the shared bus and enables shared-bus responses back t the master. MASTENN also provides the direction control for the VMEbus address transceivers.
VMEENN	1	O	M,MS	**VME Enable:** Active-low enable for the VMEbus address drivers (master-only) or transceivers (master/slave).
SLVSELN	2	O	S,MS	**Slave Select:** Active-low select for the onboard slave resources (the shared/dual ported slaves in a master/slave application). Derived from MASN and ONBD, or from ASN and SLVN. If necessary, MASTENN and VMEENN are cycled to provide address setup time before SLVSELN is asserted.
BRN	23	O	M,MS	**Bus Request:** Active-low, open-collector VMEbus request. Direct connect to the selected level among VMEbus BR0* - BR3*.
BGINN	27	I	M,MS	**Bus Grant In:** Direct connect to the selected level among VMEbus BG0IN* - BG3IN*.
BGOUTN	26	O	M,MS	**Bus Grant Out:** Direct connect to the selected level among VMEbus BG0OUT* - BG3OUT*.
BBSYN	24	O	M,MS	**Bus Busy:** Active-low, open-collector direct connect to VMEbus BBSY*.
LBGN	4	I/O	M,MS	**Local Bus Grant:** Active-low, open-collector. Can be connected to the bus grant input of a DMA controller. Asserted when LBRN is low and the BUSCON has control of the VMEbus. Grounded, or driven low during RESET, to prevent the ASN state being driven onto MASN when the BUSCON is not in control of the VMEbus.
RELSE	10	I	M,MS	**Release:** Active-high signal indicating that the onboard logic wants to release control of the VMEbus. In DMA controller applications, the BGACKN output of the DMAC should be connected to (or positive-logic ANDed into) this signal.
DTACKN	19	I/O O	M,MS S	**Data Transfer Acknowledge:** Active-low, open-collector. Direct connect to VMEbus DTACK*.
BERRN	22	I/O O	M,MS S	**Bus Error:** Active-low, open-collector. Direct connect to VMEbus BERR*.
LDTACKN	7	O, I/O I	M,MS S	**Local DTACK:** Active-low, open-collector. Output to onboard master and/or input from onboard slave.

PIN DESCRIPTION (Continued)

MNEMONIC	PIN NO.	TYPE	CONFIG	NAME AND FUNCTION
LBERRN	6	O, I/O I	M,MS S	**Local Bus Error:** Onboard active-low, open-collector. Output to onboard master and/or input from onboard slave.
DSI	3	I	All	**Data Strobe:** The high-active or of the onboard data strobes, which may be from the on board master or VMEbus master.
DSENN	5	O	M,MS	**Data Strobe Enable:** Low-active, used to enable the onboard data strobes onto the VME bus.
R/WN	13	I	All	**Read/Write:** Onboard R/W signal from the onboard master or VMEbus master.
DDIR	15	O	All	**Data Direction Control:** Direction control for VMEbus data transceivers. A high level indicates the "onboard-to-VMEbus" direction.
DENN	9	O	All	**Data Enable:** Low-active enable for VMEbus data transceivers.
RESETN	18	I	All	**RESET:** Low-active reset. Clears BUSCON logic.
V_{CC}	8	I	All	**Power Supply:** +5 volts.
GND	21	I	All	**Ground:** 0V reference.

ADDRESS DECODING

Both the VMEbus and current high-speed processors provide short address-to-strobe setup times, such that with all but the most simple decode schemes, designers must provide for delaying the strobe until decoder outputs have become valid. However, BUSCON operates as a finite-state machine and must synchronize address strobes and other inputs before it can act on them. The BUSCON design allows this synchronization time to be overlapped with address decoding.

In general, most BUSCON inputs do not have critical timing parameters. Exceptions are the three address decode signals. Figure 6 shows a somewhat simplified model of the VMEbus slave selection logic in the 68172. The ASN signal is qualified and sampled by flip-flops A and B on each rising edge of CLK. Flip-flop C is set when ASN is high between cycles, and cleared by a falling edge on DTACKN or BERRN.

On the rising edge of CLK after flip-flop B samples ASN low, if C is still set and SLVN is low, flip-flop D is set, indicating slave selection. (In reality, there are more terms in the logic to set D.) Once D is set, it remains set until flip-flop A samples ASN high and a similar circuit (not shown) samples DSI low.

Since SLVN is a direct input to flip-flop D, it must meet a setup time to the clock after ASN is sampled low. Viewed asynchronously, SLVN should be valid slightly less than one clock period after ASN goes low, through shortly after DTACKN goes low.

The onboard logic driven by MASN, VMEN, and ONBD is similar, but not as complex. Neither flip-flop C nor a data-strobe-related signal are used, and there are separate flip-flops corresponding to D for each of the VMEN and ONBD signals. VMEN and ONBD should be valid slightly less than one clock period after MASN goes low, through shortly after MASN goes high.

Because ASN and MASN are used directly to clear the corresponding "flip-flop B", their minimum high times are relatively short. However, for consecutive cycles, the inactive time of "flip-flop D" (and signals derived from it) will be at least two clock periods because of the feedback path from "D" to "B".

VMEbus ARBITRATION

BUSCON begins VMEbus arbitration by driving BRN low if MASN, VMEN and ONBD indicate a VMEbus cycle (or if LBRN goes low) and the BUSCON does not have control of the bus.

After driving BRN, BUSCON waits for the BGINN input which is connected to the selected one among the four VMEbus arbitration levels. (During this time it can of course respond t cycles from other VMEbus masters.) When it receives BGINN low while holding BRN low, it drives BBSYN low and thereafter releases BRN. (If it receives BGINN low at any other time, it drives BGOUTN low and continues to do so until BGINN goes high.)

Once BUSCON has driven BBSYN low, it waits for any current VMEbus cycle to complete as evidenced by ASN high. Then it begins to drive ASN (initially high) and drives VMEENN low to enable the address out onto the VMEbus.

If the BRN was initiated by MASN, BUSCON then waits two clock periods for address setup time before driving ASN low. If the bus acquisition was initiated by LBRN, it waits for MASN.

BUSCON will release the BBSYN signal on a rising clock edge at which all of the following conditions are met:

1. It is at least three clock periods after the edge on which BBSYN was asserted, and
2. Any prior master's cycle has completed and VMEENN has been driven low, and
3. The BGINN input was high on the last rising clock edge, and
4. The RELSE input was high on the last rising clock edge, and
5. It is not the clock edge at which BUSCON asserts ASN, and
6. It is not the clock edge at which BUSCON withdraws ASN, and
7. LBRN was high on the last rising clock edge.

If BBSYN is released while BUSCON is not driving ASN low, then VMEENN goes high when BBSYN is released, to release the VMEbus. Otherwise, VMEENN goes high shortly before ASN goes high.

RELSE is provided to allow user determination of the method of VMEbus release. The BGACKN output of a DMA controller can be connected to (or included in) this signal to allow the device to control how long it keeps the bus. The OR of the VMEbus requests can be connected to (or included in) this signal for release on request (ROR) operation. If RELSE is connected to a constant logic high, BUSCON will release the bus as soon as possible, i.e. during the first bus cycle.

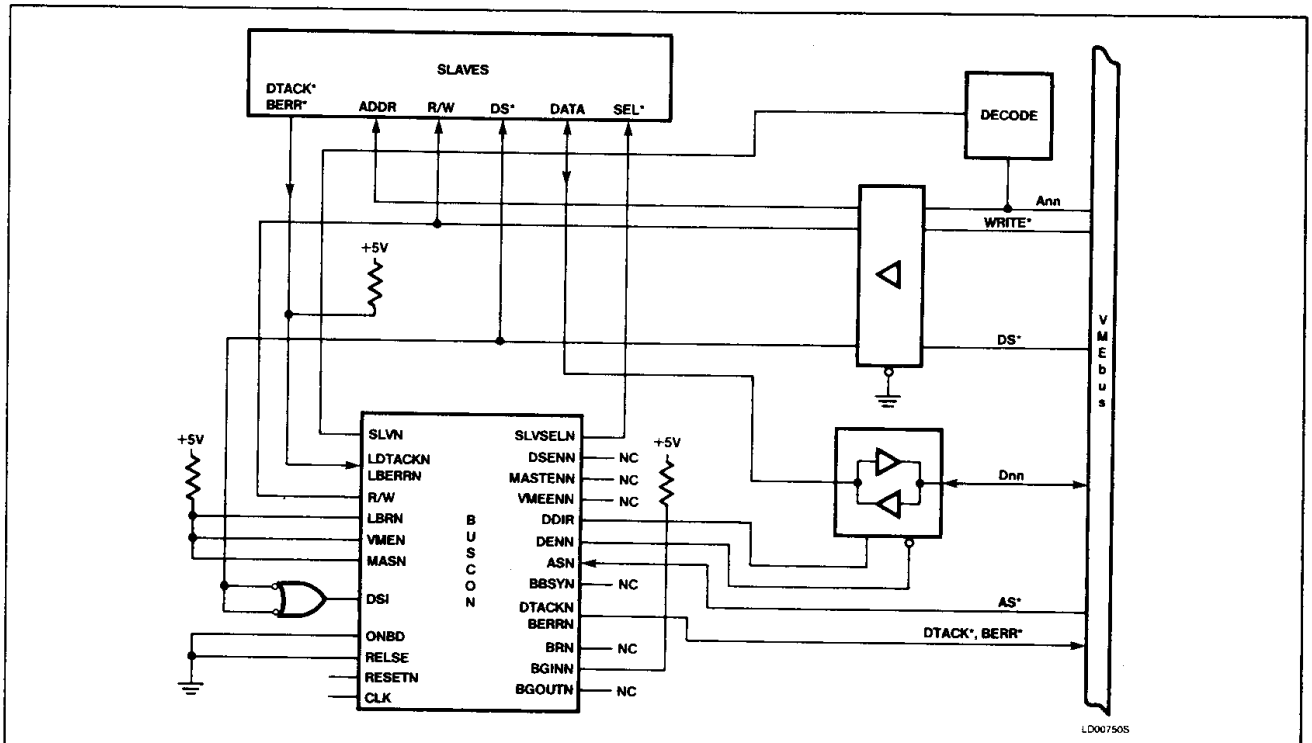


Figure 1. Slave-Only Application

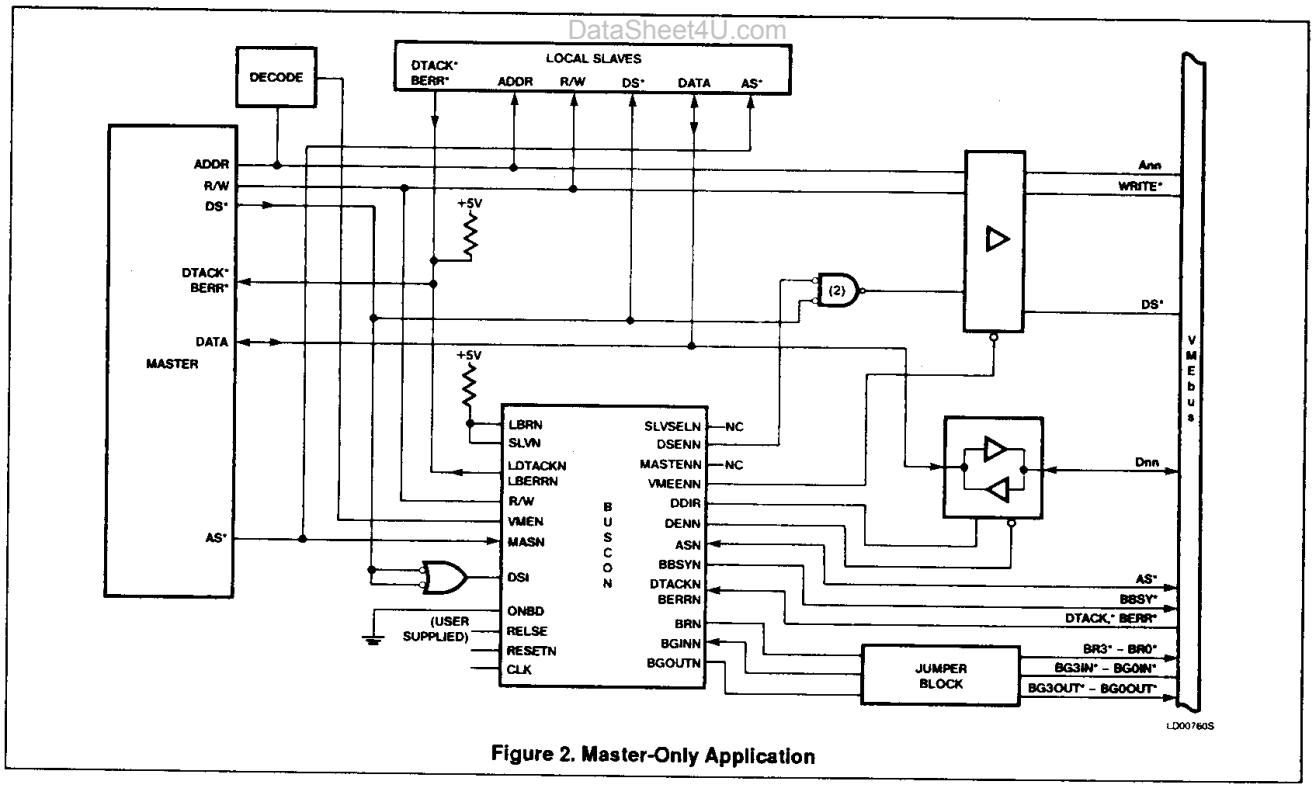


Figure 2. Master-Only Application

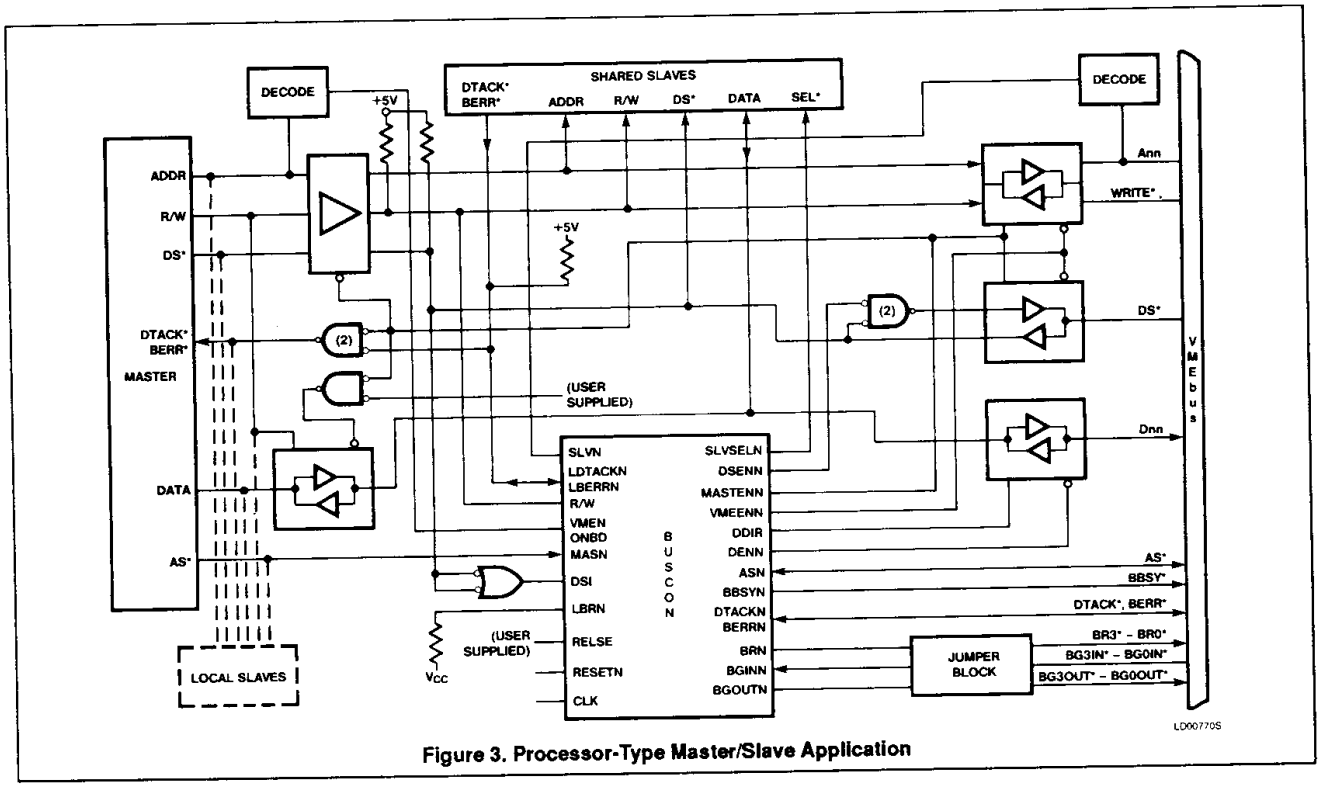


Figure 3. Processor-Type Master/Slave Application

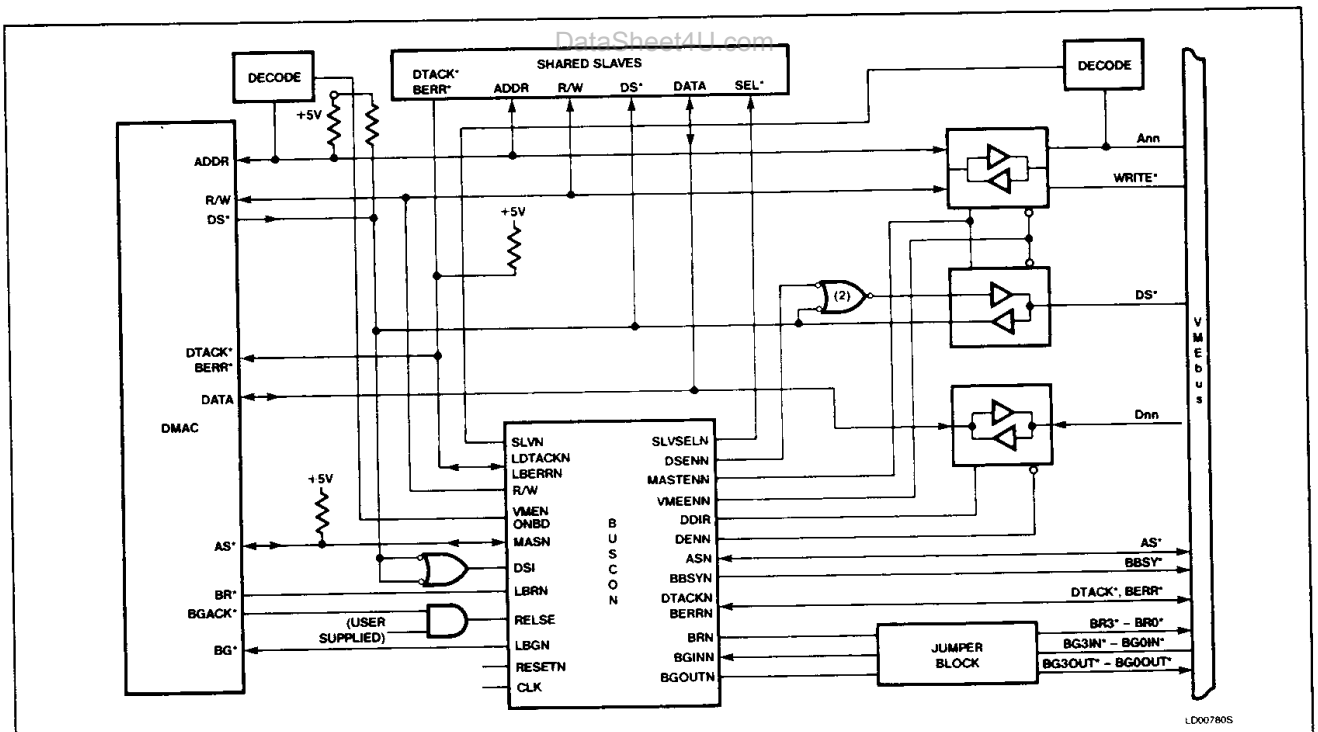


Figure 4. DMAC-Type Master/Slave Application

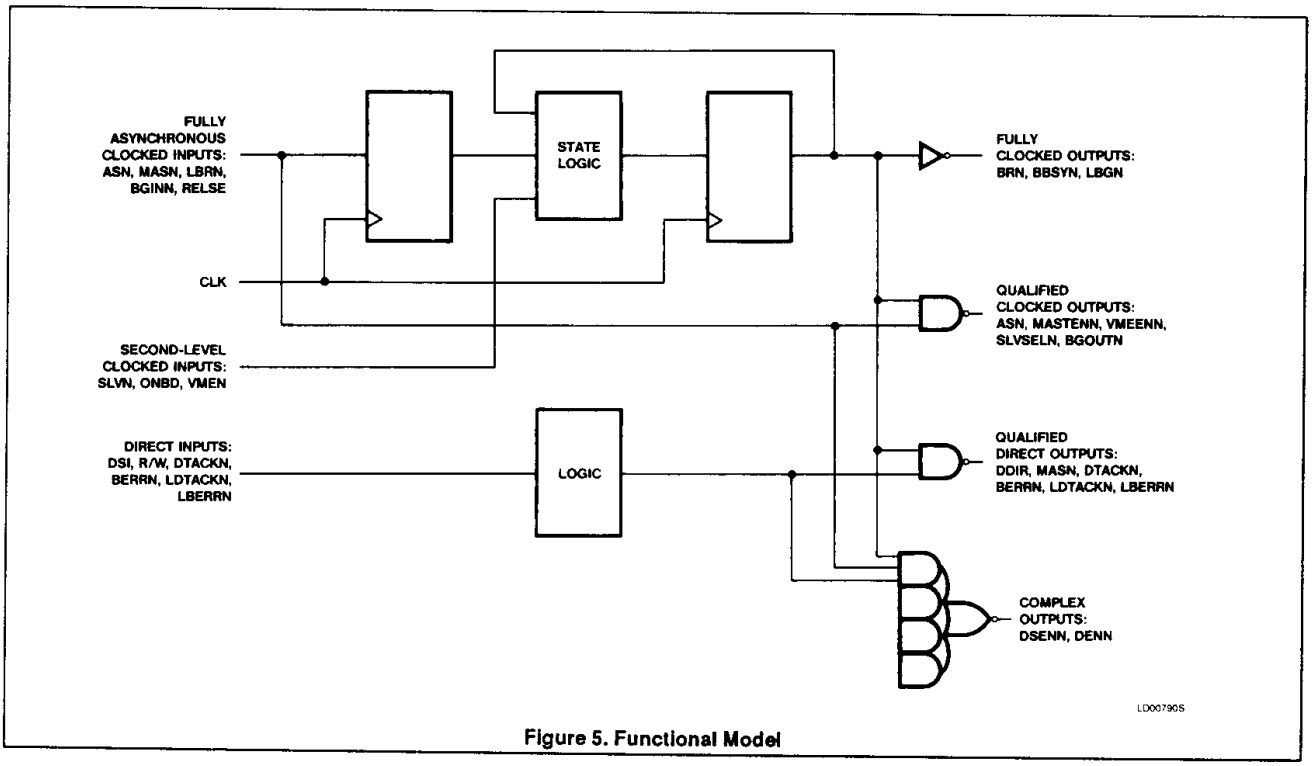


Figure 5. Functional Model

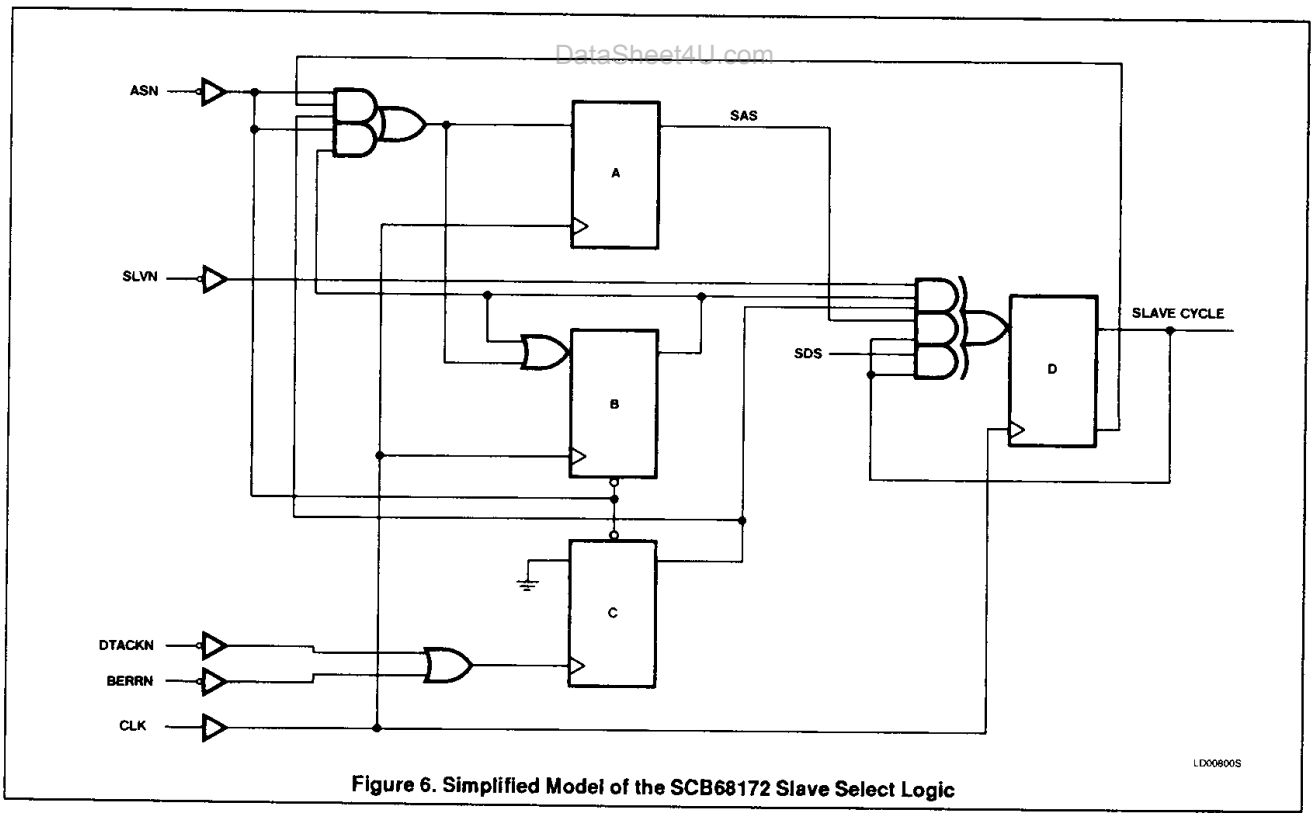


Figure 6. Simplified Model of the SCB68172 Slave Select Logic

VMEbus Controller (BUSCON)

68172

VMEbus MASTER OPERATION

When the BUSCON has VMEbus control, VMEbus cycles indicated on MASN and VMEN produce ASN low on the VMEbus. DDIR and DENN control the VMEbus data transceivers. DDIR reflects the R/WN line.

In a write operation, DENN is driven low to drive data onto the VMEbus whenever the BUSCON has control of the VMEbus, R/WN is low, and the previous VMEbus slave has released DTACKN and BERRN to high. (The DTACKN/BERRN requirement does not apply to subsequent cycles among consecutive writes, if R/WN is maintained continuously low.) DSENN is then driven low when DENN has been low for more than a clock period, and DTACKN and BERRN are high, but not before ASN is driven low. DSENN goes high after DSI goes low or MASN goes high, whichever occurs first. DENN goes high after R/WN goes high, or with VMEENN going high, whichever occurs first.

In a read operation (R/WN is high), DENN goes low to drive data in from the VMEbus after ONBD and VMEN have been sampled, DSI is high, and MASTENN is low. DSENN goes low after DSI, DTACKN, and BERRN are all high, but not before ASN goes low. DSENN and DENN go high after DSI goes low or MASN goes high, whichever occurs first.

DTACKN and BERRN are inputs and drive LDTACKN and LBERRN as outputs. LDTACKN and LBERRN are released when the onboard master makes DSI low. If the VMEbus slave continues to hold DTACKN or BERRN low thereafter, DSENN, LDTACKN and LBERRN are inhibited for the next cycle until the response is released.

MASTENN and VMEENN are kept low while the BUSCON has VMEbus control. The MAS-to-AS delay thus provides automatic address-setup time for subsequent VMEbus cycles.

The need to transceive the data strobes in a master/slave application, plus qualify the on-board master's strobes with DSENN for output, can be accomplished in several ways as shown in Figure 7.

MASTER/SLAVE SWITCHING

BUSCON includes arbitration and switching logic between VMEbus slave cycles and onboard master cycles (to a shared onboard slave or the VMEbus). The logic remains in its previous direction until forced to switch by another cycle. This provides minimum overhead for slave-only or master-only operation, and for consecutive cycles from the same master.

If a master cycle to a shared slave occurs, or BGINN arrives when requesting the VMEbus, after a slave cycle with another VMEbus master, VMEENN goes high to disable the address from the VMEbus. On the next clock edge, MASTENN goes low to enable the master's address back out onto the onboard bus.

For a VMEbus master cycle, if the current VMEbus cycle is also over, VMEENN then goes low to enable the address out onto the VMEbus.

For a master cycle to a shared slave, SLVSELN goes low one clock period after MASTENN goes low, or if the master direction is continuing, after ONBD is sampled high. SLVSELN goes high shortly after MASN goes high. DTACKN and BERRN are isolated from LDTACKN and LBERRN. DSENN is kept high. DENN is kept high except in a write cycle when BUSCON has VMEbus control.

If an onboard master cycle and VMEbus slave cycle both arrive for the shared slaves within the same clock period, the previous direction of the master/slave switch is retained.

VMEbus SLAVE OPERATION

If a VMEbus slave cycle occurs after a master cycle, or while BUSCON is requesting the VMEbus, MASTENN goes high, and on the subsequent clock VMEENN goes low to enable the VMEbus address and control signals onto the board.

SLVSELN goes low one clock period after VMEENN goes low, to signal the shard slave(s) that a cycle is occurring. If the slave mode is continuing, SLVSELN goes low after SLVN is sampled low. SLVSELN goes high shortly after ASN goes high.

DDIR reflects R/WN (in the opposite sense from master operation). LDTACKN and LBERRN are inputs and drive DTACKN and BERRN as outputs.

In write operations, DENN is driven low (to enable data in) whenever R/WN is low and LDTACKN and LBERRN are high. When switching between master and slave operation with R/WN low, DENN sequences line VMEENN.

In read operations, DENN is driven low (to enable data out) after SLVN has been sampled low, and while R/WN and DSI are both high.

SLAVE-ONLY USE

This is the simplest application of the BUSCON. However, handling of board-selection logic from a simple VMEbus address decode, plus driving and sequencing of DTACKN and BERRN, can save VMEbus designers cost and board space even in this application.

SLAVE DESIGN

In the MS and S configurations, slaves operate off the data strobes and SLVSELN rather than address and data strobes. It should be noted that SLVSELN will typically go low after the data strobes go low. Data should not be written nor placed on the data lines until SLVSELN goes low.

68000 DUAL-PORTED OPERATION

BUSCON is ideal for use on a VMEbus board containing a 68000 processor. The obvious approach to dual-porting memory and other slaves, on a board with a 68000, is to use the BRN input of the 68000 to suspend processor operation while another master accesses the onboard slave. This works fine except when the processor has already started a cycle for the VMEbus. This latter coincidence threatens a "deadlock" situation and requires that the processor be "rolled back" off the board's shared bus so that the other master's cycle can occur first. The 68000 has a feature which can be used for this; assertion of both its BERRN and HALTN inputs cause it to suspend operation and retry the cycle when the inputs are released.

The BUSCON does not use these features because there is a flaw in the retry logic. The retry logic does not function during an indivisible RMW sequence (TAS instruction), even in the read cycle. Instead, the assertion of BERRN and HALTN causes an actual bus error exception. It is believed that there is no reliable and general programming solution to the problem of finding the start of the TAS instruction for restart. With 6801x processors, the situation is better because the TAS can be restarted. In any case BUSCON elects to isolate the processor with a few more packages rather than adding complexity tot he error-handling software because of dual-ported design.

DMA USE

The BUSCON can be used for VMEbus boards which contain a DMA controller but no processor. Such DMA applications are always master/slave due to the need to program the DMA controller from the VMEbus. There are two operational features of the 68172 that are intended for use with DMA controllers. First, the LBRN input can be used to request control of the VMEbus directly, rather than waiting for MASN low and VMEN low as in a processor application. Second, the SCB68172 samples the state of the LBGN pin when RESTN is low. If LBGN is low at the end of RESETN, MASN is used as an input only. If LBGN is high (at the end of the RESETN pulse), the BUSCON thereafter drives the state of VMEbus ASN onto MASN whenever it does not have control of the VMEbus.

For 68000 family DMA controllers, MASN is connected directly to the controller's address strobe pin. The VMEbus ASN-to-MASN feature satisfies the requirement of some DMA controllers that ASN be low on cycles which program

them, and also serves to delay the activity of a controller which gets an LBGN response during the last VMEbus cycle by another master.

When LBRN is sampled low, the BUSCON has retained VMEbus control from previous DMA activity, it continues to retain control for the duration of LBRN being low, and drives LBGN low on the next clock.

Otherwise, it drives VMEbus BRN low on the next clock. When BGINN is sampled low, BBSYN is driven low on the next clock. LBGN is driven low on the same clock as BBSYN if VMEbus ASN is high. If ASN is low, LBGN is driven low one clock after BBSYN, except when ASN low and BGINN are both sampled low for the first time in the same clock period and the VMEbus cycle addresses this board — in this last case, LBGN is driven low two clocks after BBSYN. In either of the last two cases, VMEbus ASN low makes MASN low before LBGN goes low, which keeps the DMA controller from starting until the current VMEbus cycle is over.

Note that the local bus request/grant logic and ASN-to-MASN drive feature are separate capabilities, either or both of which can be used in applications not involving a DMA controller. However, note also that when the state of the ASN is driven onto MASN, this is done without conditioning by the state of the master-slave switch. This means MASN can go low before MASTENN and VMEENN have been cycled to bring the VMEbus address onto the board. (The low state of SLVSELN indicates that the VMEbus address is valid on the board.)

DMA applications are always considered master/slave due to the need to program the DMA controller. The BUSCON assumes that it must always have VMEbus control before answering an LBRN with LBGN. If this is not desired, i.e., if the DMA controller will sometimes be programmed to do onboard transfers solely and the designer wishes to optimize for this case, then a processor-type interface should be used, and isolation devices and additional onboard logic are required.

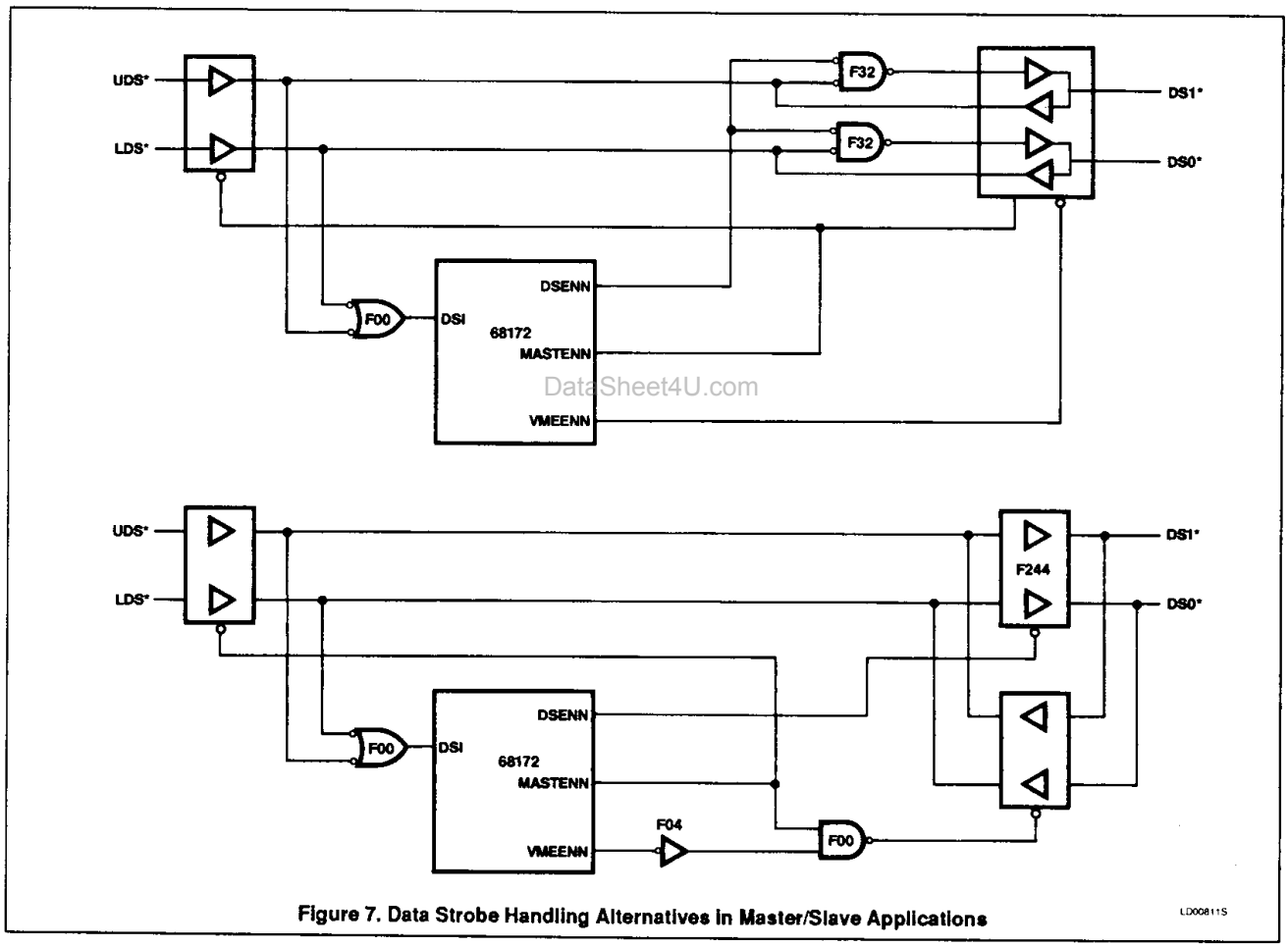


Figure 7. Data Strobe Handling Alternatives in Master/Slave Applications

INTERRUPT HANDLING

When a processor handles interrupts from onboard sources and from the VMEbus, the design must include logic to decide whether an interrupt acknowledge cycle is an onboard or offboard cycle. This logic is quite different from the address decoding logic used to make this decision on other cycles.

Performance can be maximized if the interrupt logic can provide ONBD and VMEN within the specified time after MASN goes low, or if the signals can be made to meet their specified setup and hold times for CLK. In this case ONBD and VMEN need be selected between the IACK and non-IACK sources. Otherwise (i.e., if the interrupt logic presents these signals slowly and asynchronously), MASN must also be selected between the IACK and non-IACK sources.

MASTER BLOCK TRANSFER

The block transfer feature of the VMEbus allows considerable performance improvement for transferring a block of consecutive memory

locations. The BUSCON can be used for block transfer operations in the master role.

Master block transfers are applicable to cache subsystems or block transfer on processor boards, and to DMAC-type designs. The only requirements for master block transfers operation with the BUSCON are that external logic must place a block transfer address modifier (AM) code on the VMEbus, and then hold MASN low across a number of data strobes.(Note that a long block transfer can compromise the operation of other VMEbus masters. One strategy to avoid such problems could be to do a minimum of 4 or 8 transfers without interruption, and then switch to release on request (ROR) operation.)

A sample circuit for master block transfers is shown in Figure 8. Here, a block transfer is triggered whenever the DMAC accesses a certain range of addresses. The SEQ signal could of course be generated in other ways.

SLAVE BLOCK TRANSFERS

VMEbus slaves that are capable of block transfers latch the bus address into a set of counters on the leading edge of ASN, and then increment the address for each data transfer. The 68172 can be used on such slave boards in accordance with revision C of the VMEbus specification.

The revision C specification introduces a limitation on block transfers, namely that a master is not allowed to continue a block transfer across a 256-byte boundary. This limitation has a number of advantages, including reducing the number of counter devices needed on slave boards, allowing straightforward use of page or static column modes on dynamic memories, providing periodic windows in a long block transfer in which higher-priority masters can gain bus control, and (effectively) preventing a block transfer from crossing from one slave board to another.

It is this last advantage that is of particular importance for the 68172. It means that VMEbus slaves can make a positive selection-decision after ASN goes low, and this decision will remain valid for the duration of the cycle even if it is a block transfer cycle.

In a block transfer which selects an 68172-bused slave board, SLVSELN remains low through the block, until ASN goes high. The onboard slave logic then uses the data strobes to define each data transfer.

The data strobe and acknowledge signals are handled in a high-speed combinatorial fashion by the 68172 in both the master and slave roles. Block transfers are inherently faster on the VMEbus because the address need be passed and decoded only once, and because the slave can look ahead (pipeline) subsequent transfers in a block read cycle. With the 68172, this inherent speed advantage is augmented by the advantage of combinatorial over sequential (arbitrated) logic.

3-STATE ENABLE SWITCHING (MASTENN, VMEENN, DENN)

As a result of speed optimization of master/slave switching, some parts used in PMS applications may exhibit short high-going transients on MASTENN, VMEENN, and/or DENN, if requests for access to the shared slave(s) arrive closely in time from both the onboard master and the VMEbus master. These transients should pose no problem as long as the signals are used as intended (i.e., as 3-State enables). The following points apply:

1. A transient will occur only when SLVSELN has been high for at least one clock period, and at least one clock period before a subsequent low on SLVSELN.
2. A transient will occur only if the current master/slave direction is maintained.
3. Low-going transients (which could cause 3-State conflicts) do not occur.
4. Commonly such transients will be eliminated by external capacitance, and/or rejected by receivers on other parts. In any case the logic levels on signals controlled by these enable signals should not be affected.
5. Edge-sensitive use of these signals is inadvisable in a PMS application.

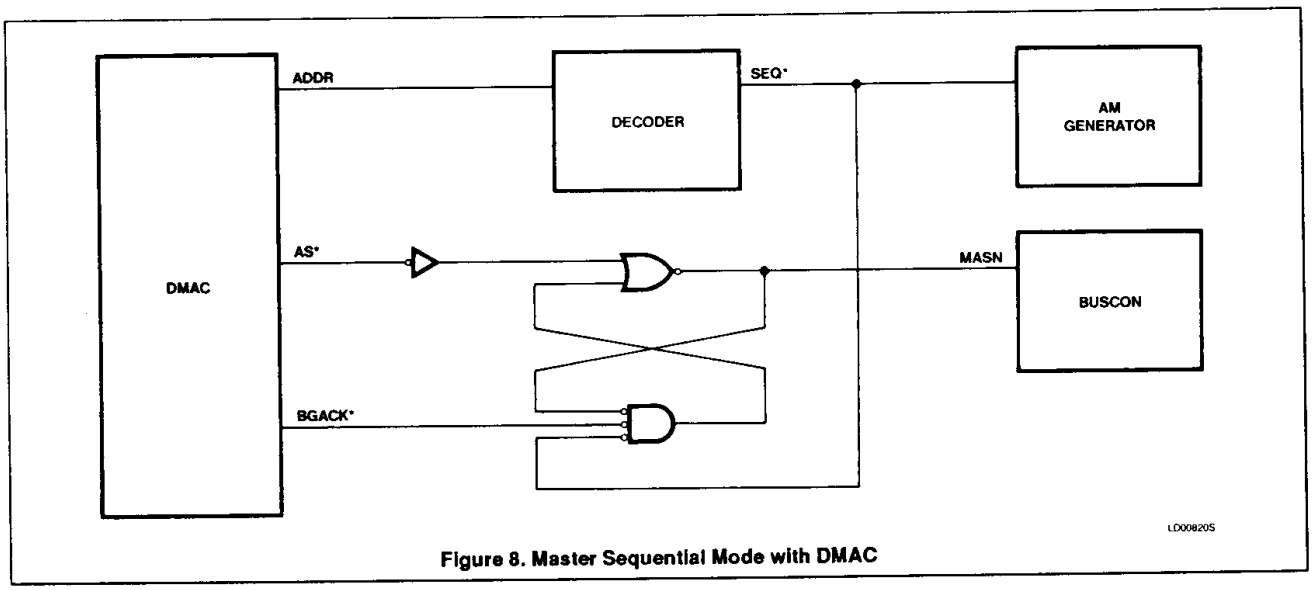
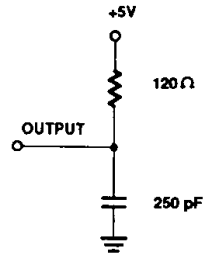


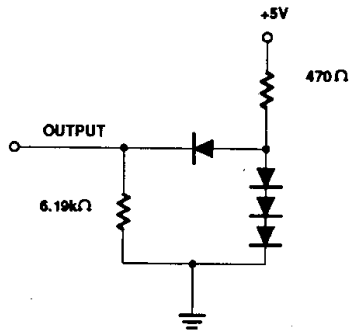
Figure 8. Master Sequential Mode with DMAC

TEST CONDITIONS unless otherwise noted, the timing parameters are based on loading as follows:

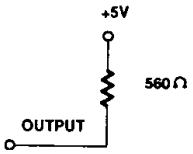
LOAD TYPE A



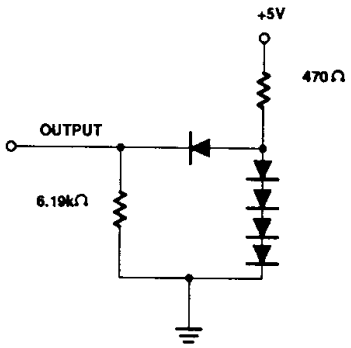
LOAD TYPE B



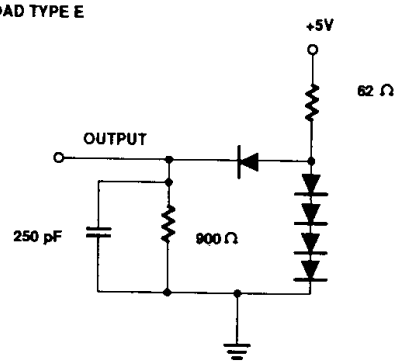
LOAD TYPE C



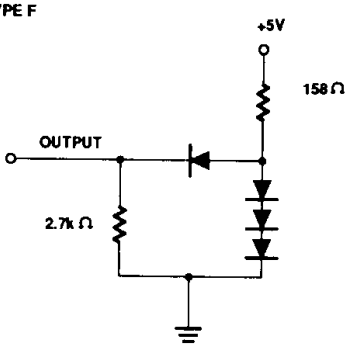
LOAD TYPE D



LOAD TYPE E



LOAD TYPE F



SIGNALS	LOAD TYPE
BBSYN,BERRN,BRN,DTACKN	A
BGOUTN,DDIR,DENN,DSENN,SLVSELN,VMEENN	B
LBERRN,LBGN,LDTACKN	C
MASN	D
ASH	E
MASTENN	F

NOTE: All capacitive loads calculated with 50pf board capacitance.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage range	-0.5 to +7.0	V
V_I	Input voltage range	-0.5 to +5.5	V
T_{STG}	Storage temperature range	-65 to +150	°C

DC ELECTRICAL CHARACTERISTICS V_{CC} = 5.0V ± 5%, T_A = -55°C to +125°C[2, 3, 4]

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			Min	Max	
DSI, ONBD, SLVN, VMEN, LBRN, RELSE, RESETN					
I_{IL}	Input low current	V_I = 0.4V		-400	µA
I_{IH}	Input high current	V_I = 2.7V		20	µA
V_{IL}	Input low voltage			0.8	V
V_{IH}	Input high voltage		2.0		V
ASN, MASN, BGINN, DTACKN, BERRN, LDTACKN, LBERRN					
I_{IL}	Input low current	V_I = 0.4V		-400	µA
I_{IH}	Input high current	V_I = 2.7V		20	µA
V_{IL}	Input low voltage			0.8	V
V_{IH}	Input high voltage		2.0		V
R/WN, CLK					
I_{IL}	Input low current	V_I = 0.4V		-800	µA
I_{IH}	Input high current	V_I = 2.7V		40	µA
V_{IL}	Input low voltage			0.8	V
V_{IH}	Input high voltage		2.0		V
BGOUTN, VMEENN, SLVSELN, DSENN, DENN, DDIR (low current totem pole)					
V_{OL}	Output low voltage	I_{OL} = 8mA, V_{CC} = 4.75V		0.5	V
V_{OH}	Output high voltage	I_{OH} = -0.4mA, V_{CC} = 4.75V	2.7		V
MASTENN (high current totem pole)					
V_{OL}	Output low voltage	I_{OL} = 24mA, V_{CC} = 4.75V		0.5	V
V_{OH}	Output high voltage	I_{OH} = -1mA, V_{CC} = 4.75V	2.7		V
MASN (low current 3-State)					
V_{OL}	Output low voltage	I_{OL} = 8mA, V_{CC} = 4.75V		0.5	V
V_{OH}	Output high voltage	I_{OH} = -0.4mA, V_{CC} = 4.75V	2.7		
ASN (high current 3-State)					
V_{OL}	Output low voltage	I_{OL} = 64mA, V_{CC} = 4.75V		0.5	V
V_{OH}	Output high voltage	I_{OH} = -3mA, V_{CC} = 4.75V	2.7		
LDTACKN, LBERRN, LBGN (low current open-collector)					
V_{OL}	Output low voltage	I_{OL} = 8mA, V_{CC} = 4.75V		0.5	V
I_{OH}	Output leakage current	V = 5.25V		100	µA
DTACKN, BERRN, BRN, BBSYN (high current open-collector)					
V_{OL}	Output low voltage	I_{OL} = 48mA, V_{CC} = 4.75V		0.6	V
I_{OH}	Output leakage current	V = 5.5V		250	µA
I_{CC}	V_{CC} Supply current	V_{CC} = 5.25V		250	mA

AC ELECTRICAL CHARACTERISTICS V_{CC} = 5.0V ± 5%, T_A = -55°C to +125°C.

NO.	FIGURE	CHARACTERISTIC	LIMITS		UNIT	NOTES
			Min	Max		
Clock and general parameters						
1	9 - 18, 20	CLK cycle time (CLK)	40		ns	
2	9 - 18, 20	CLK low time	15		ns	
3	9 - 18, 20	CLK high time	15		ns	
Asynchronous input setup time to CLK high						
4	9, 10, 11, 12, 13, 18, 20	ASN, MASN low	30		ns	5
5	9, 10, 11, 13	ASN, MASN high	25		ns	5
6	9, 10, 11, 12, 13, 20	SLVN, VMEN low	20		ns	6
7	11, 17, 18	SLVN, VMEN high	33		ns	6
8	9, 10, 13	ONBD low	25		ns	6
9	18	ONBD high	20		ns	6
10	13, 16, 20	LBRN, RELSE, BGINN low	23		ns	5
11	14, 15	LBRN, RELSE, BGINN high	10		ns	5
12	11, 12, 13	DSI low (end of slave cycle)	30		ns	5
Asynchronous input hold time from CLK high						
13		ASN, MASN, DSI	0		ns	7
14		ONBD, VMEN	0		ns	8
15		LBRN, RELSE, BGINN	2		ns	7
Propagation, CLK high to:						
16	16	BGOUTN low	20	55	ns	
17	20	LBGN low	20	70	ns	
18		LBGN high	11	46	ns	
19	13, 16, 20	BBSYN, BRN low	17	53	ns	
20	13, 20	BBSYN, BRN high	14	34	ns	
21	9, 10, 13	ASN low	12	41	ns	
22	9, 10	ASN high		40	ns	
23	11, 12, 13, 18, 20	SLVSELN, VMEENN low	14	60	ns	
24	13, 18, 20	MASTENN low	19	42	ns	
Miscellaneous						
25		RESETN width low	6clk		ns	9
27	16	BGINN high to BGOUTN high	5	17	ns	
28	9, 11	R/WN high to DSI high (start of read cycle)	10		ns	39
29	9, 12	DSI low to RWN low (end of ready cycle)	10		ns	39
Address decoding						
33	17	SLVN high after DTACKN low	22		ns	
34	9, 10	VMEN, ONBD valid after MASN high	10		ns	39
35	9, 10	MASN high	15		ns	10
36	9, 10, 11	DSI low	20		ns	
37	11	ASN high	20		ns	10
VMEbus acquisition						
38A	13, 20	ASN low to BGINN low (early release by other master)	10		ns	39
40	13, 20	BBSYN low to BRN high		15	ns	
42	13	ASN high to VMEENN low, DENN low (write)	20	57	ns	12, 13
43A	13, 16, 20	BBSYN or BGOUTN low to BGINN high	0		ns	39

AC ELECTRICAL CHARACTERISTICS (Continued)

NO.	FIGURE	CHARACTERISTIC	LIMITS		UNIT	NOTES
			Min	Max		
VMEbus master cycles						
46	9, 10	ASN low to DSEN low	-1	14	ns	17, 18
47	10, 13	R/WN low to DDIR high		36	ns	
48	10, 13	DDIR high to DENN low (write)	2	11	ns	15
49	10	DTACKN and BERRN high to DENN low (write, 1st bus cycle or preceded by read)	14	41	ns	15
50	10	DENN low to DSENN low (write)	clk+13	2clk+53	ns	17
51	9, 11, 13	R/WN high to DDIR low	13	40	ns	
52	9	DDIR low to DENN low (read)	7	26	ns	16
53	9	DSI high to DENN low (read)	10	30	ns	16
54	9	DSI high to DSENN low (read)	14	45	ns	18
55	9, 10	DTACKN and BERRN high to DSENN low	15	51	ns	17, 18
56	9, 10	DTACKN or BERRN low to LDTACKN or LBERRN low		66	ns	
57	9, 10	LDTACKN or LBERRN low to DSI low or MASN high	0		ns	39
58	9, 10	DSI low to DSENN high		37	ns	19
59	9, 10	MASN high to DSENN high		50	ns	
60	10	R/WN high to DSENN high (after a write)		32	ns	20
62	9	MASN high to DENN high (read)		50	ns	21
63	9	DSI low to DENN high (read)		39	ns	21
64	10	R/WN high to DENN high (write)		30	ns	22
65	9, 10	DSENN high to LDTACKN and LBERRN high		54	ns	23
66	9, 10	DTACKN and BERRN high to LDTACKN and LBERRN high		17	ns	23
VMEbus release						
67	14	BBSYN low	2clk		ns	39
71	14	MASN high to VMEENN high or DENN high (early release, write)	7	46	ns	
73	14	DENN (write) and VMEENN high to ASN high	-6	2	ns	
74	14	ASN high to ASN released (early release)	6	52	ns	
76	15	DENN (write) and VMEENN high to BBSYN high (intercycle release)	0	19	ns	
77	14, 15	BBSYN high to RELSE low	0		ns	39
Master to slave switching						
78		Clock high to MSTEEN high (Clock at which (External) ASN is detected low)	13	30	ns	25
79	11, 13, 20	SLVN low to MASTENN high		18	ns	25
80	11	SLVSELN high to MASTENN high	18	35	ns	25
81A	11, 13	VMEENN low to DDIR change	-1	16	ns	
VMEbus slave cycles						
85	12, 13	R/WN low to DDIR low	16	45	ns	
86	12, 13	DDIR low to DENN low (write)	7	25	ns	27
87	12	LDTACKN and LBERRN high to DENN low (write)	10	35	ns	27
88	12, 13	R/WN high to DDIR high		17	ns	
89	11	DDIR high to DENN low (read)	4	12	ns	28
91	11	DSI high to DENN low (read)		29	ns	28
92	11, 12, 13, 18	SLVSELN low and DSI high to LDTACKN or LBERRN low	0		ns	29, 39
93	11, 12, 13, 18	LDTACKN or LBERRN low to DTACKN or BERRN low		48	ns	
94	12, 13	LDTACKN or LBERRN low to DENN high (write)	10	27	ns	
94A	11, 12, 13, 18	DTACKN or BERRN low to DSI low or ASN high	0		ns	39
95	11	DSI low to DENN high (read)		22	ns	
96	11, 12, 18, 20	ASN high to SLVSELN high	14	35	ns	
97	11, 12, 13	DSI low to DTACKN and BERRN high	14	32	ns	
97A	11	DENN high to DTACKN and BERRN high		20	ns	
98	11, 12, 13, 20	DSI low to DTACKN and LBERRN high	0	35	ns	30, 32, 39
99	11, 12	LDTACKN and LBERRN high to (next) DSI high	0		ns	30, 39

AC ELECTRICAL CHARACTERISTICS (Continued)

NO.	FIGURE	CHARACTERISTIC	LIMITS		UNIT	NOTES
			Min	Max		
Slave to master switching						
100		Clock high to VMEENN, DENN (VMEbus slave write high) (Clock which MASN is detected low)		clk+40	ns	31
101	18	ONBD high to VMEENN, DENN (VMEbus slave write) high	10	40	ns	31
102		VMEN low to VMEENN, DENN (VMEbus slave write) high	9	26	ns	31
103	13, 18, 20	SLVSELN high to VMEENN, DENN (VMEbus slave write) high	0		ns	31
104		Clock high to VMEENN, DENN (VMEbus slave write) high (Clock at which DSI (selected) is detected low)	10	40	ns	31
Onboard cycles						
111	18	MASN high to SLVSELN high	10	40	ns	
DMAC-Type operation						
112	19	Clock high to MASN active (Clock from which BBSYN is driven high)	22	60	ns	34
113	19	ASN high to MASN active		20	ns	34
114	19	ASN low to MASN low	20	49	ns	
115	19	ASN high to MASN high	5	25	ns	
116	19	ASN high to MASN released		48	ns	35
117	19	LBGN low to MASN released		50	ns	35
122	20	LBGN low to LBRN high	0		ns	39

Notes on following page.

NOTES:

1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is stress rating only and functional operation of the device at these or at any other conditions other than those indicated in the Electrical Characteristics section of this data sheet is not implied.
2. For operating at elevated temperatures, the device must be derated based on +150°C maximum junction temperature.
3. Parameters are valid over specified temperature range.
4. All voltage measurements are referenced to ground (V_{SS}). For testing, all signals swing between 0.4V and 2.4V with a transition time of 10ns maximum. All time measurements are referenced at input voltages of 1.5V.
5. These setup times guarantee recognition at a rising edge of CLK, but the device will operate correctly if they are not met. If the asynchronous input is changed between the setup and hold times, the new state of the input may be recognized at this clock or the following clock.
6. These setup times are required on the rising edge of CLK following the one on which ASN or MASN is first recognized low. If parameters 30, 31, and 32 are met, these parameters are automatically guaranteed.
7. These hold times guarantee (continued) recognition of the signal state at a rising edge of CLK, but the device will operate correctly if they are not met.
8. These hold times are required on the rising edge of CLK preceding the one on which MASN is first recognized high. Parameter 34 provides a more straightforward requirement which guarantees these times.
9. This parameter applies after V_{CC} and the clock signal are both within the specified limits.
10. These minimum times are to guarantee recognition. Operation will be limited by 44, 83, and 109 if the strobe is high for less than 2clk.
11. BRN is driven low, and this acquisition sequence applies, only if BBSYN is high.
12. VMEENN is driven low only when 41, 42, and 107 have been met.
13. Applies to ASN or VMEbus cycle which does not select this board as a slave.
14. ASN goes low when 43, 44, and 45 are met. 44 is not applicable on the first cycle after acquiring the VMEbus.
15. In a write operation, DENN goes low when 41, 42, 48, 49, and 107 are met. 49 does not apply for subsequent cycles in a series of writes if R/WN is held low throughout.
16. In a read operation, DENN goes low when all of 52, 53, 53A and (as applicable) 41A and 107A are set.
17. In a write operation, DSENN goes low when 46, 50, and 55 are met. 55 is significant only for subsequent cycles in a series of writes with R/WN held low throughout.
18. In a read operation, DSENN goes low when 46, 54, and 55 are met.
19. DSENN goes high when either 58 or 59 is met.
20. Applies only if R/WN remains low after a write cycle, so that DSENN goes low again.
21. In a read operation, DENN goes high when either 63 or 64 is met.
22. In a write operation, DENN goes high when either 64 or 71 is met
23. LDTACKN and LBERRN go high when either 65 or 66 is met.
24. BBSYN is always released in response to BGINN, RELSE, and LBRN all high. However, if this condition is detected during a clock period in which the decision to change ASN is made, the release of BBSYN is delayed one clock period so that 70 or 75 is met.
25. MASTENN goes high when 78, 79, and 80 are all met.
26. SLVSELN goes low when 82, 83, and 84 (as applicable) are met.
27. In a write operation, DENN goes low when 86 and 87 are met.
28. In a read operation, DENN goes low when 89, 90, and 91 are met.
29. The onboard slave(s) should wait for both SLVSELN and DSI before driving a response.
30. Since BUSCON itself terminates DTACKN and BERRN when DSI goes low, the onboard slaves must meet this requirement to assure that a "lingering" LDTACKN or LBERRN is not presented as DTACKN or BERRN when the next DSI occurs. 99 is the real requirement - 98 max is derived from it, plus the 40ns minimum high time of VMEbus data strobes and an allowance for receiver skew.
31. VMEENN goes high only when 100, (101 or 102), 103, and 104 are met. 104 applies only if a VMEbus slave cycle (with this board) is ending.
32. The onboard slave(s) must meet this requirement so that the local response is not inadvertently presented to the onboard master.
33. SLVSELN goes low when 108, 109, and 110 (as applicable) are met.
34. MASN is driven out of Hi-Z state only when 112 and 113 are met.
35. MASN is released to Hi-Z state only when 116 and 117 are met.
36. The max figure applies only if BUSCON has keep VMEbus control (i.e., if BBSYN is low).
37. LBGN goes high only when 123, 125, and 126 are met, but 125 and 126 apply only if a VMEbus slave cycle (with this board) is in progress.
38. These parameters guarantee parameters 6 through 10, but are not absolute requirements. If these parameters are not met, parameters 6 through 10, and 14 must be met for each clock edge from the one following the edge on which MASN or ASN is recognized low, until MASN or ASN goes high.
39. Guaranteed, but not tested.

DERIVED AC CHARACTERISTICS The following parameters can be derived directly from the AC Electrical Characteristics. These will not be tested or characterized separately.

NO.	FIGURE	CHARACTERISTIC	LIMITS		UNIT	NOTES
			Min	Max		
Miscellaneous						
26	16	BGINN low to BGOUTN low	clk+18	2clk+78	ns	
Address decoding						
30	11, 12, 13, 20	ASN low to SLVN valid		clk-30	ns	38
31	9, 10, 13, 18	MASN low to VMEN valid		clk-30	ns	38
32	9, 10, 13, 18	MASN low to ONBD valid		clk-22	ns	38
VMEbus acquisition						
38	13	MASN low to BRN low	clk+20	2clk+83	ns	11
39	13, 20	BGINN low to BBSYN low	clk+15	2clk+76	ns	
41	13	BGINN low to VMEENN low, DENN low (write)	clk+3	2clk+38	ns	12
41A	13	BGINN low to DENN low (read)	clk+5	2clk+60	ns	16
43	13	VMEENN low to ASN low	clk-11	2clk	ns	14
VMEbus master cycles						
44	9, 10	ASN high (successive VMEbus master cycles)	2clk		ns	14
45	9, 10	MASN low to ASN low (subsequent cycle retaining VMEbus control)	clk+18	2clk+70	ns	14
53A	9	MASN low to DENN low (read)	clk+5	2clk+60	ns	16
61	9, 10	MASN high to ASN high (unless early release)	clk+8	2clk+75	ns	
VMEbus release						
68	14, 15	BGINN high to BBSYN high	clk+12	2clk+35	ns	23
69	14, 15	RELSE high to BBSYN high	clk+12	2clk+42	ns	24
70	14	ASN low to BBSYN high (early release)	clk-8		ns	
75	15	ASN high to BBSYN high (intercycle release)	clk-6		ns	
Master to slave switching						
81	11, 20	MASTENN high to VMEENN low	8	clk+13	ns	
82	11, 13, 20	VMEENN low to SLVSELN low	clk-20	clk	ns	26
VMEbus slave cycles						
83	12	SLVSELN high (successive slave cycles)	3clk+56		ns	26
84	12	ASN low to SLVSELN low (already in slave state)	clk+13	2clk+74	ns	26
90	11	ASN low to DENN low (read)	clk+22	2clk+80	ns	28
Slave to master switching						
105	13, 18, 20	VMEENN high to MASTENN low	-17		ns	
107	13, 20	MASTENN low to VMEENN low, DENN low (write, if next cycle on VMEbus)		0	ns	12, 15
107A	13	MASTENN low to DENN low (read, next cycle on VMEbus)	-5	20	ns	16
108	18	MASTENN low to SLVSELN low (if next cycle on board)	clk-28	clk+17	ns	33
Onboard cycles						
109	18	SLVSELN high (successive onboard cycles)	3clk+22		ns	33
110	18	MASN low to SLVSELN low (MASTENN already low)	clk+11	2clk+63	ns	33
DMAC-Type operation						
118	20	LBRN low to BRN low (if BBSYN released)	clk+15	2clk+76	ns	
119		LBRN low to LBGN low	clk+18	2clk+69	ns	36
120	20	BGINN low to LBGN low (ASN high)	clk+18	2clk+69	ns	
		BGINN low to LBGN low (ASN low)	2clk+18	3clk+69	ns	
121	20	MASN low (output) to LBGN low	clk+38		ns	
123	20	LBRN high to LBGN high	clk+10	2clk+69	ns	37
124	14, 15	LBRN high to BBSYN high	clk+12	2clk+56	ns	24
125	20	ASN high to LBGN high (selected)	2clk+15	3clk+71	ns	37
126	20	DSI low to LBGN high (selected)	2clk+15	3clk+76	ns	37

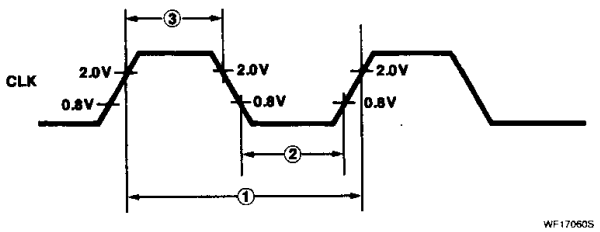


Figure 8.5 CLK Timing

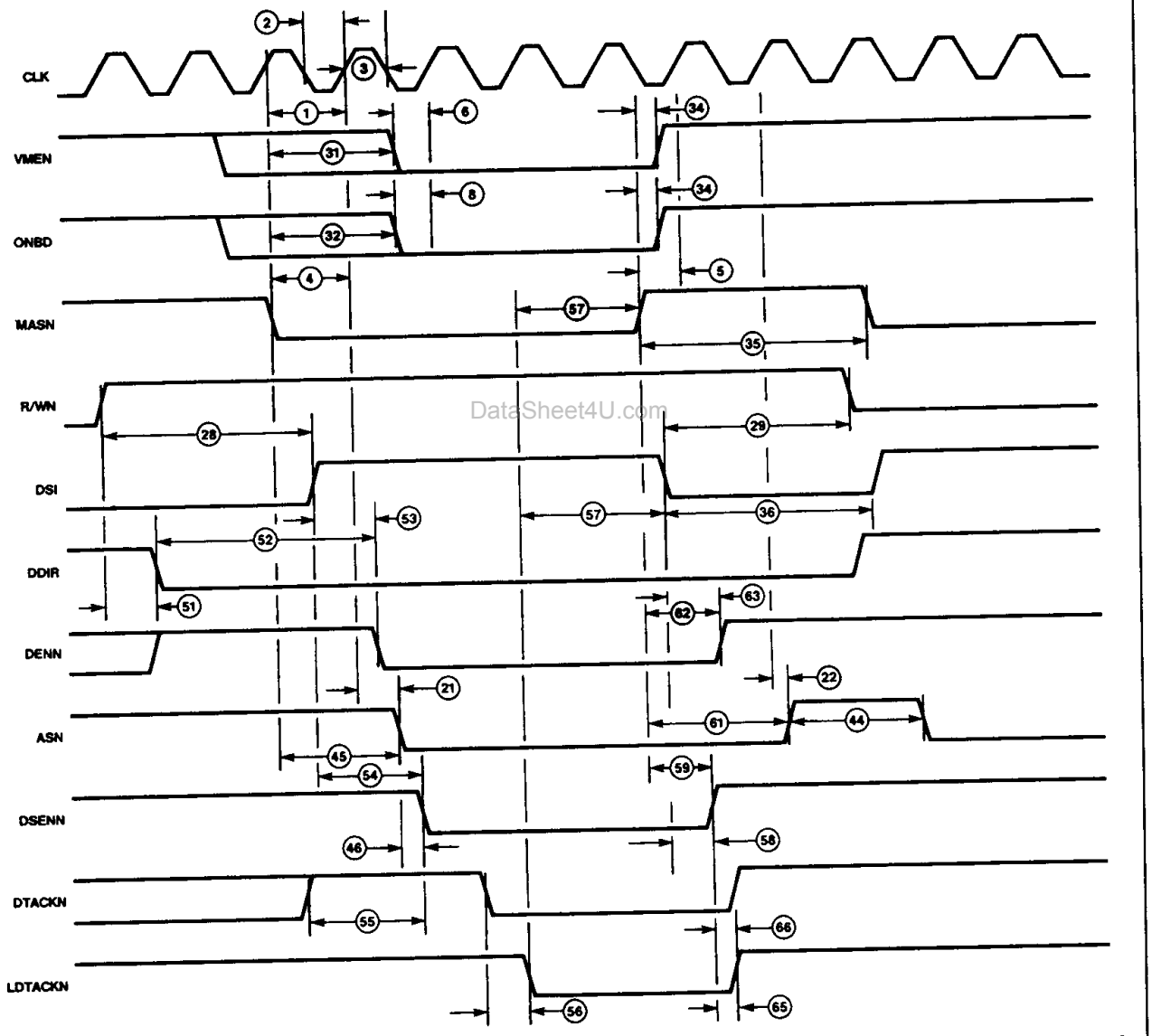


Figure 9. Read Cycle From Onboard Master to VMEbus Slave (Already in Control of VMEbus)

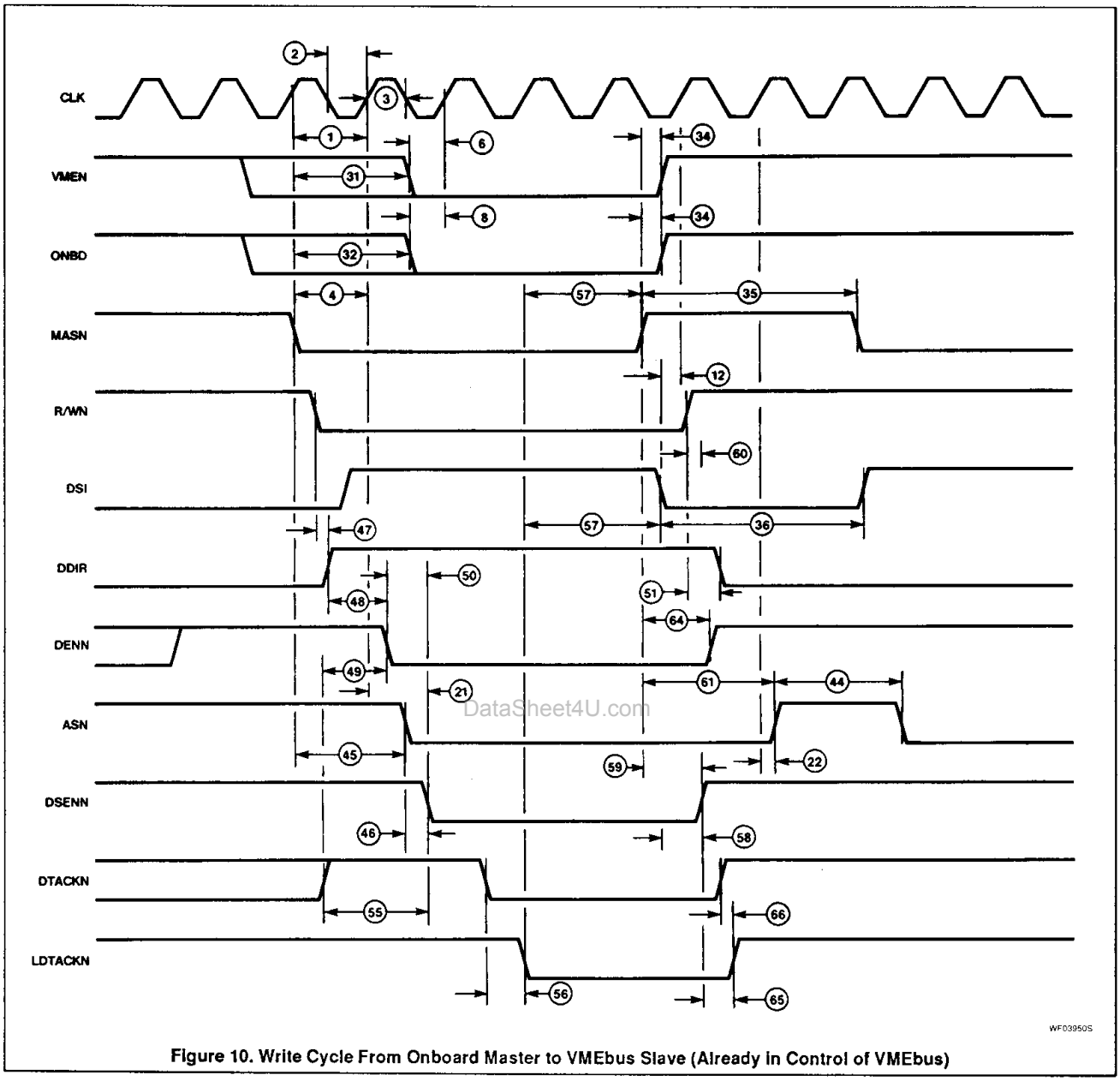


Figure 10. Write Cycle From Onboard Master to VMEbus Slave (Already In Control of VMEbus)

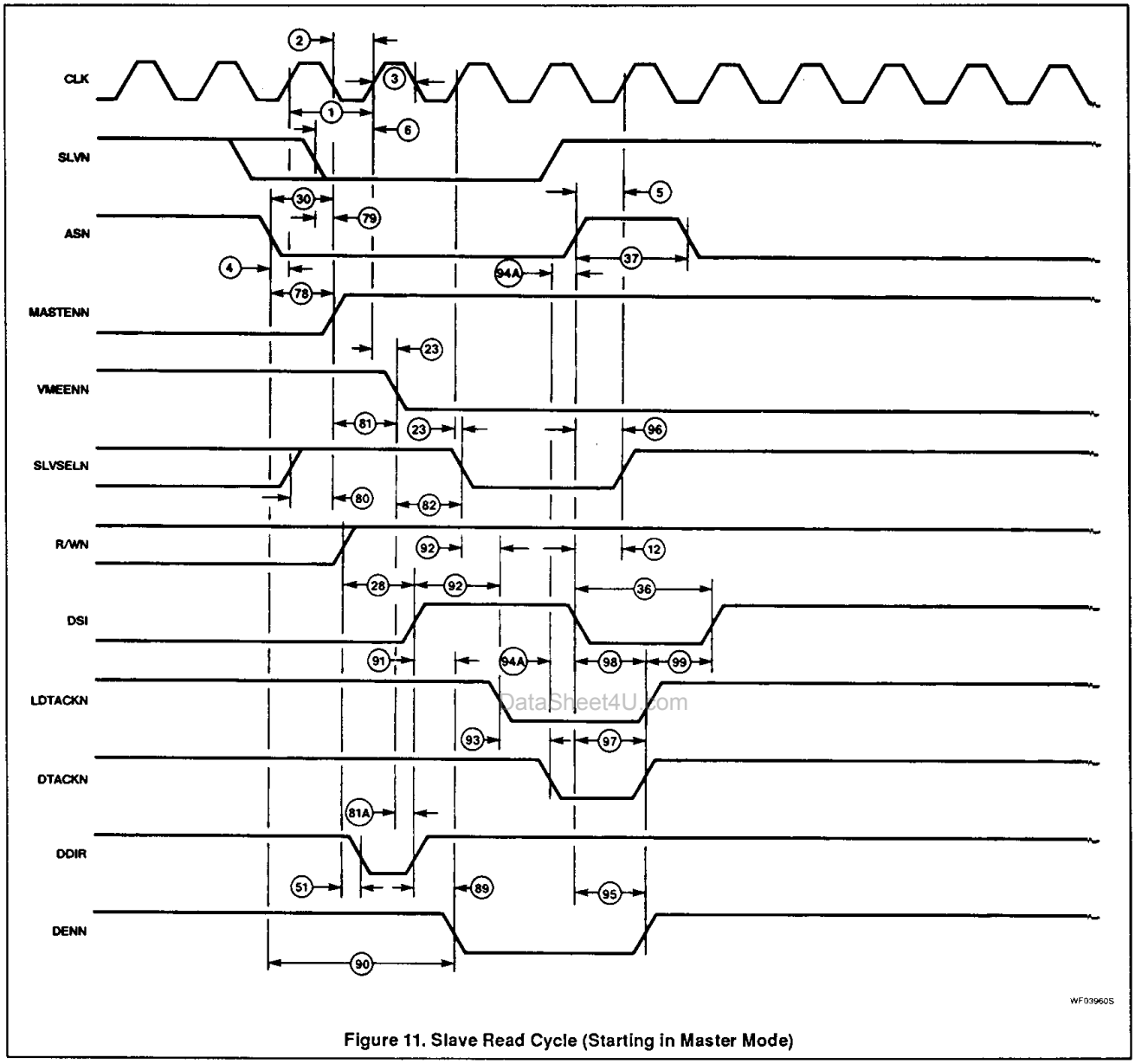


Figure 11. Slave Read Cycle (Starting in Master Mode)

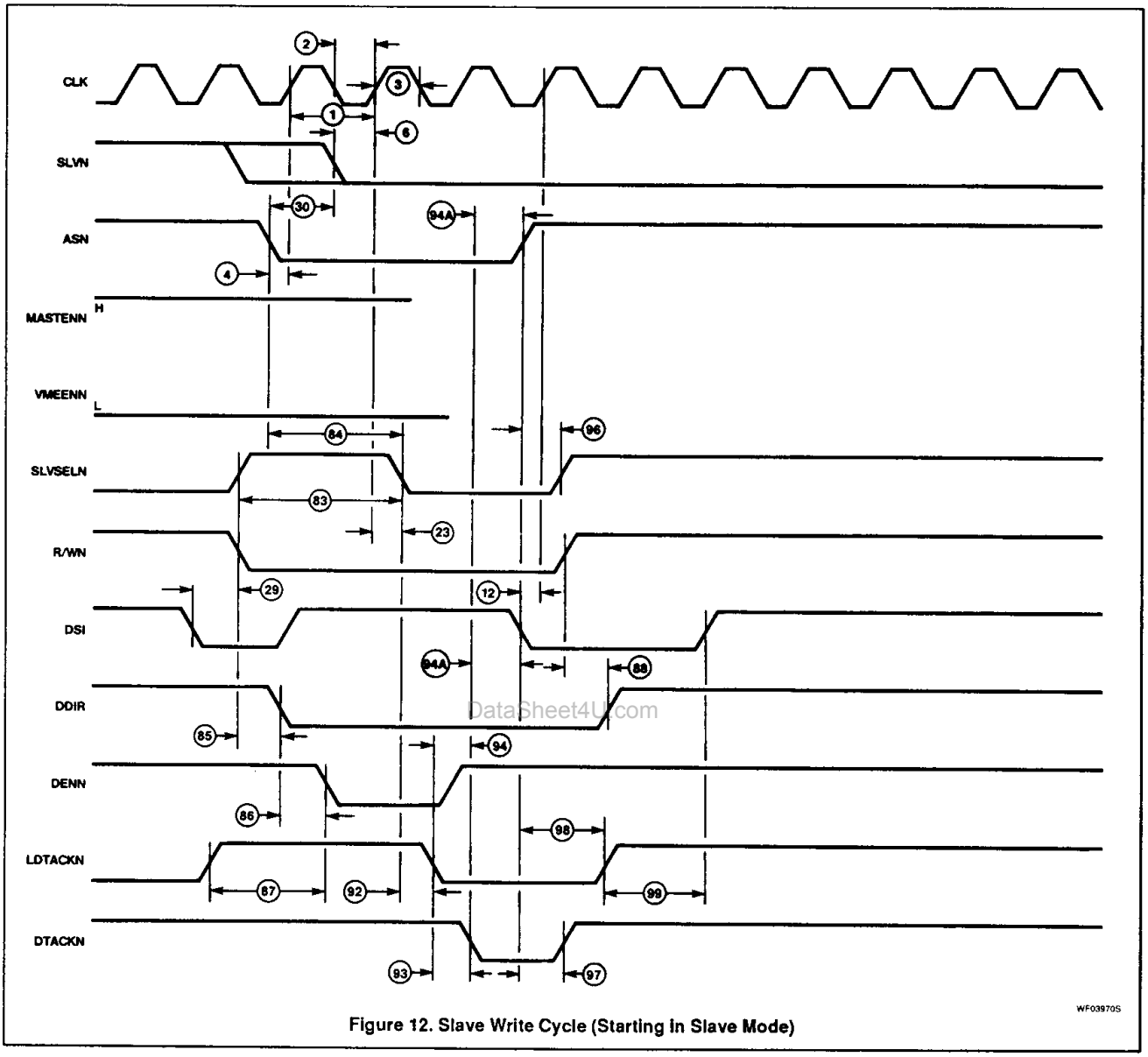


Figure 12. Slave Write Cycle (Starting in Slave Mode)

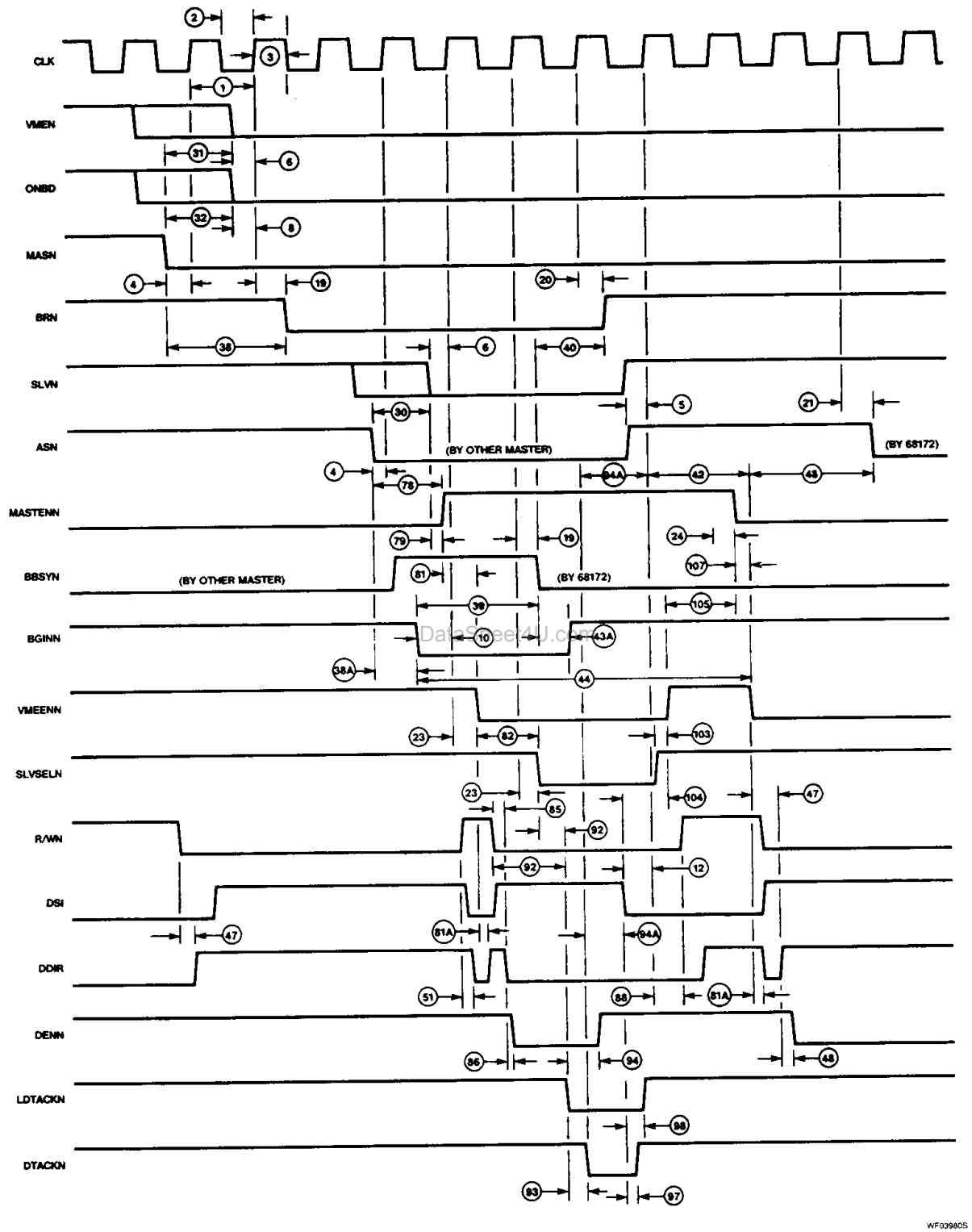


Figure 13. VMEbus Acquisition, Including Slave Write Cycle

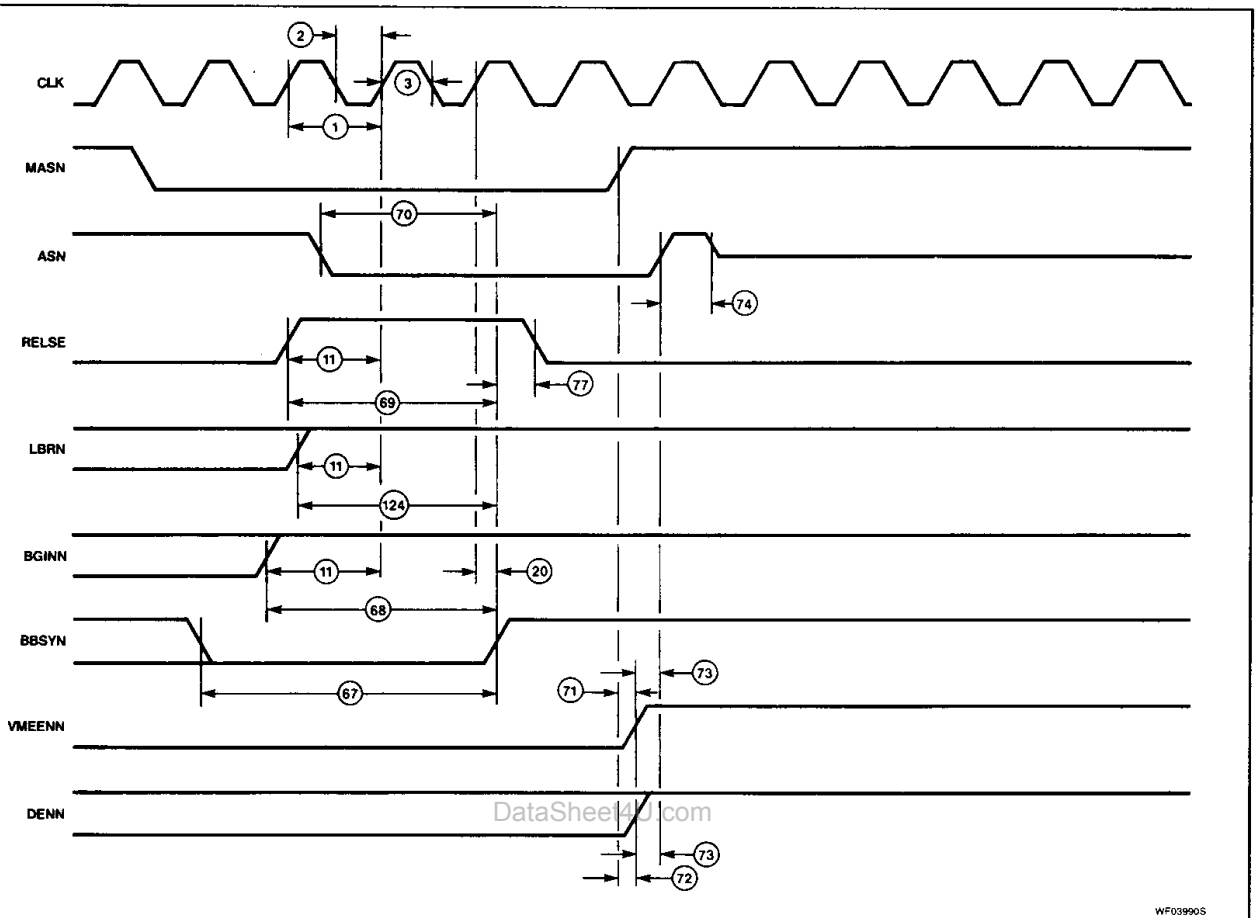


Figure 14. "Early" VMEbus Release

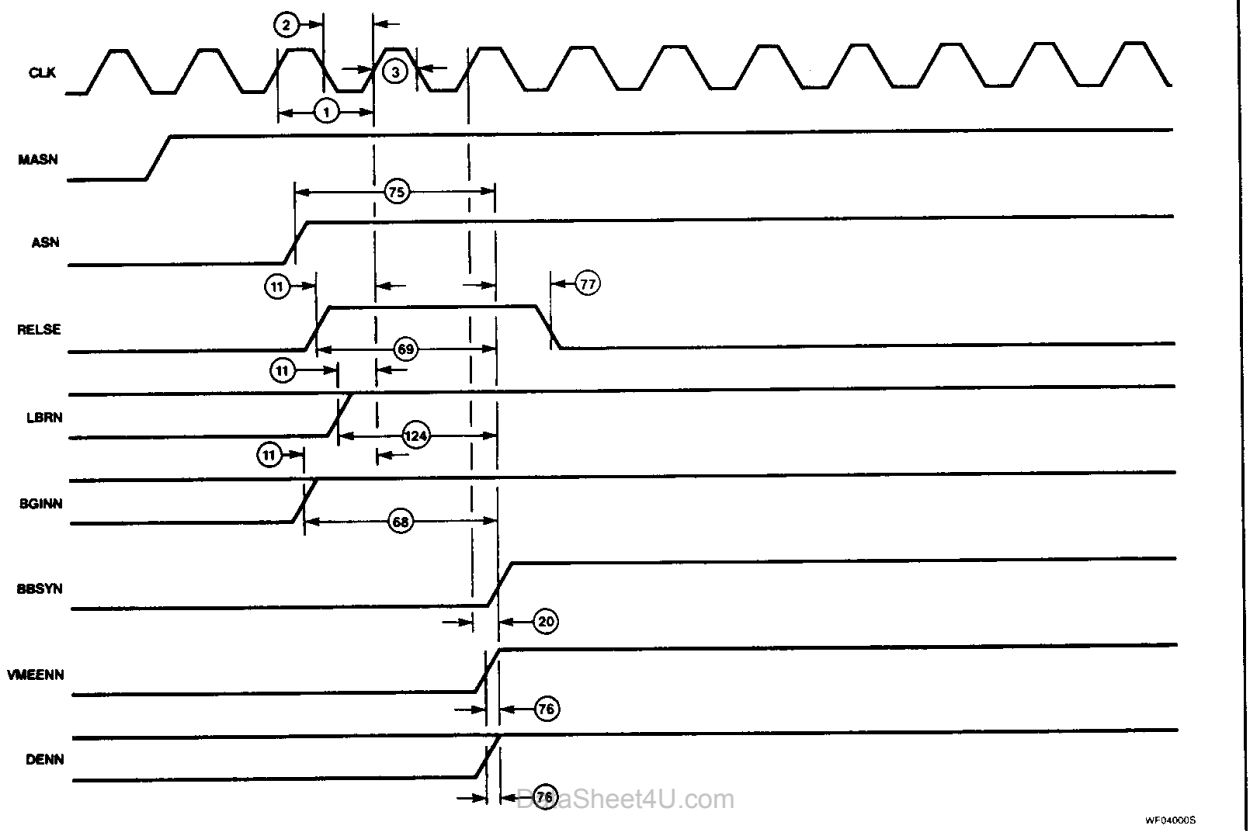


Figure 15. Intercycle VMEbus Release

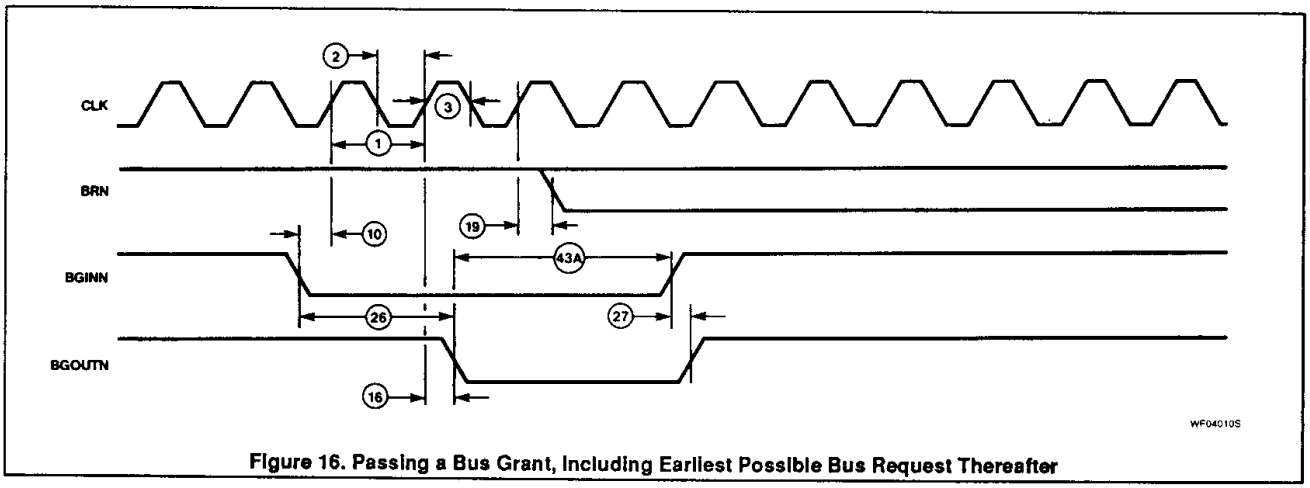


Figure 16. Passing a Bus Grant, Including Earliest Possible Bus Request Thereafter

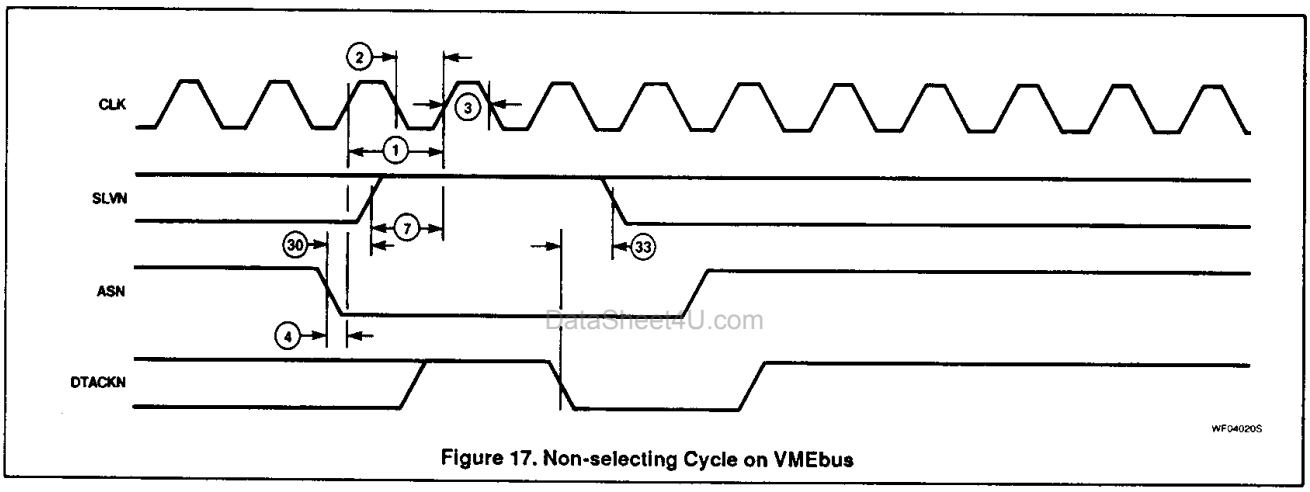


Figure 17. Non-selecting Cycle on VMEbus

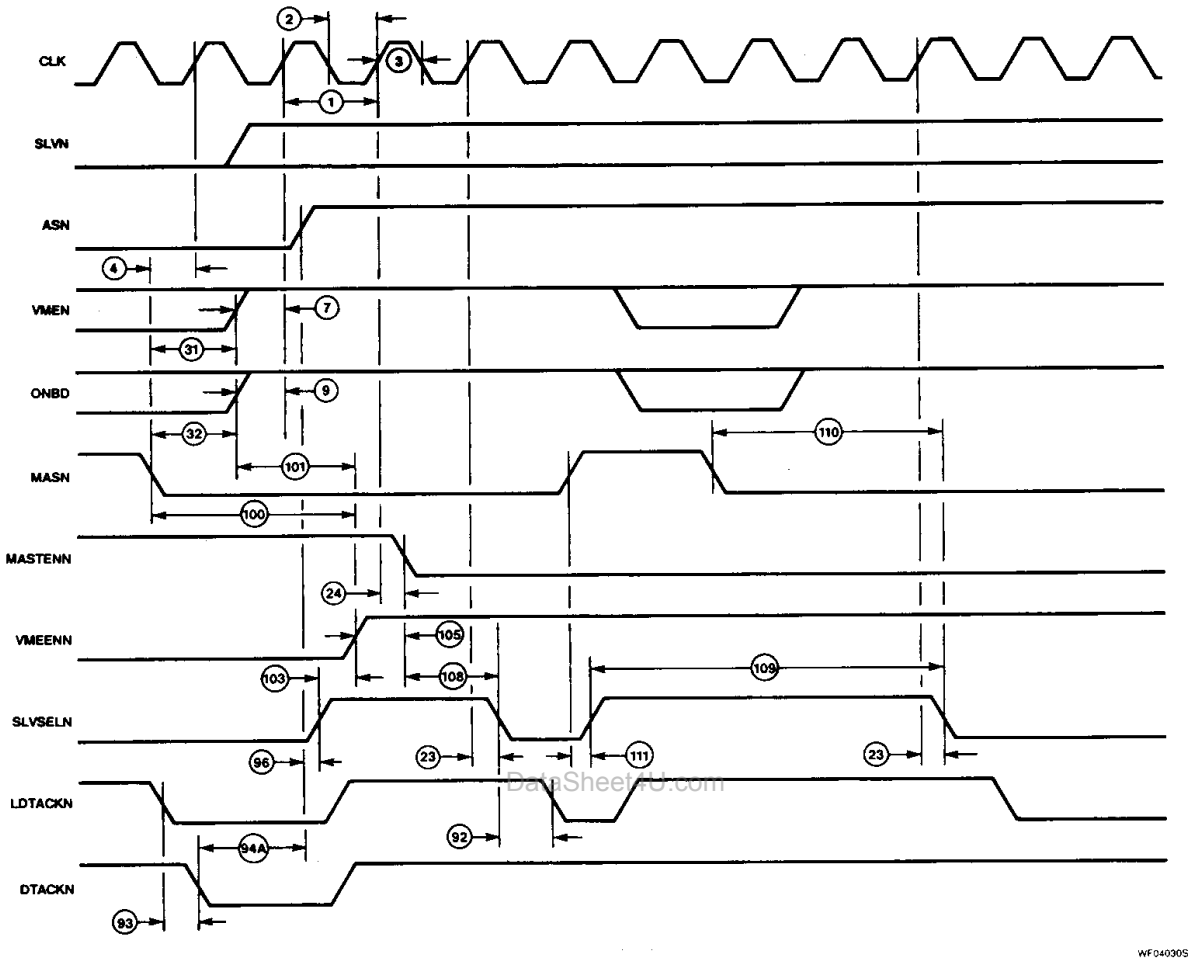


Figure 18. Two Onboard Cycles Following a Slave Cycle

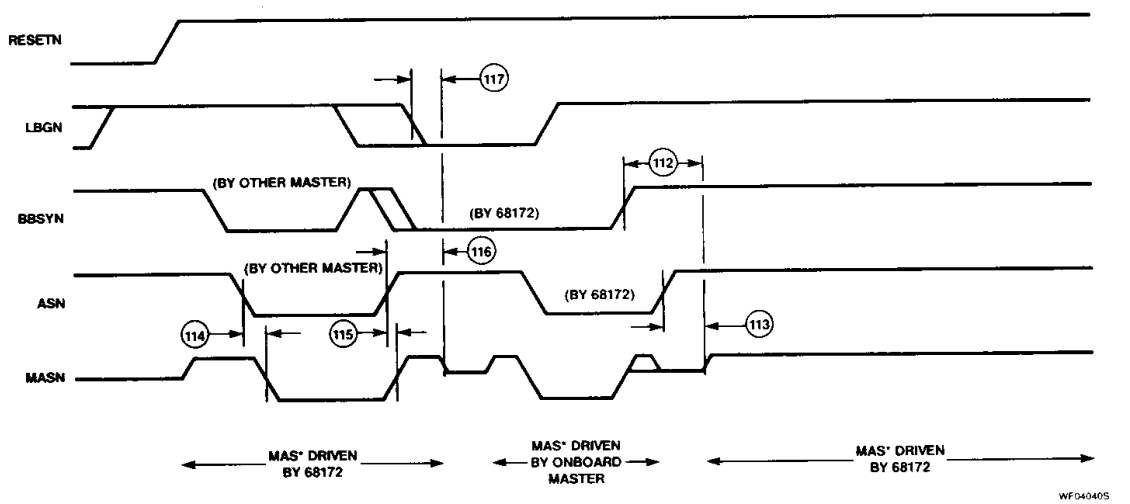


Figure 19. A* to MAS* Drive (DMA-Type Operation)

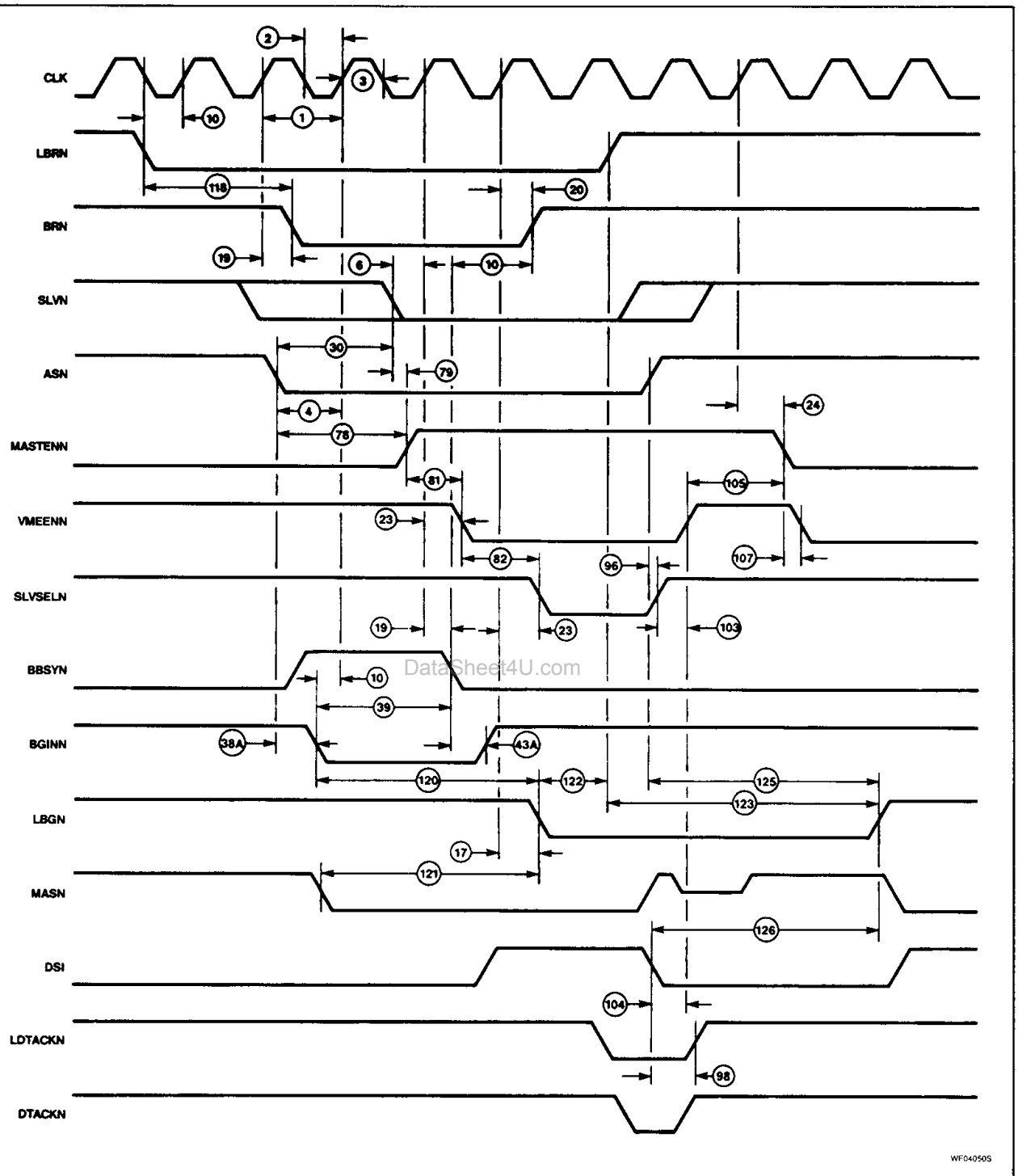


Figure 20. DMA-Type VMEbus Acquisition, With Slave Cycle From Another VMEbus Master

Signetics

Packaging Information

T-90-20

Military Products

SIGNETICS STANDARD PACKAGE DESCRIPTIONS

All Military package case outlines and physical dimensions conform with the current revision MIL-M-38510, Appendix C, except for package types which are not included in that specification.

The physical dimensions for standard package types which are not included in Appendix C are included herein in Appendix C format. Case outline letters are assigned to these packages according to JEDEC Publication 101 as follows:

- U: Leadless chip carriers
- X: Dual-in-line packages
- Y: Flat packages
- Z: All other configurations

A case outline suffix number is assigned herein for identification purposes only, and is not marked on the product.

Signetics Military products are offered in a wide range of package configurations to optimally fit our customer needs.

- Dual-in-line Packages; Frit glass sealed CERDIP (F package family) with 8-40 leads, and side-brazed ceramic (I package family) with 48-64 leads.
- Flat Packages; Frit glass sealed alumina CERPAC (W package family) with 14-28 leads, and brazed leaded ceramic (Q package family) with 52 leads.
- Ceramic Chip Carriers; triple laminated, metal-lidded LCC (G package family) with 20-68 terminals.
- Pin Grid Array; metal-lidded ceramic pin grid (P package family) with 68-100 leads.
- Shown in Table 1 are the case outline letters assigned according to Appendix C of MIL-M-38510 and JEDEC publication 101. Unless otherwise noted, all package types are Configuration 1 and all lead finishes are hot solder dip Finish "A".

Table 1.

Package Description	Type Designation	Case Outline	Theta-JC °C/Watt[4]
8DIP3	D-4	P	28
14DIP3	D-1	C	28
16DIP3	D-2	E	28
18DIP3	D-6	V	28
20DIP3	D-8	R	28
22DIP4	D-7	W	28
24DIP3	D-9	L	28
24DIP4	D-11	X[2]	28
24DIP6	D-3	J	28
28DIP6	D-10	X[2]	28
40DIP6	D-5	Q	28
48DIP6	D-14[1]	X[2]	28
50DIP9	D-12[1]	X[2]	28
64DIP9	D-13[1]	X[2]	28
14FLAT	F-2	D	22
16FLAT	F-5	F	22
18FLAT	F-10	Y[2]	22
20FLAT	F-9	S	22
24FLAT	F-6	K	22
28FLAT	F-11	Y[2]	22
52FLAT	Y-1[1]	Y[2]	22
18LLCC	C-9	U[2]	20
20LLCC	C-2[3]	2	20
28LLCC	C-4[3]	3	20
32LLCC	C-12	U[2]	20
44LLCC	C-5	U[2]	20
68LLCC	C-7	U[2]	20
68PGA	P-AB	Z[2]	20
84PGA	P-AB	Z[2]	20

NOTES:
1. Configuration 2.
2. Per JEDEC publication 101.
3. Dimension A (LLCC thickness) is 75mils maximum.
4. See RADC test report RADC-TR-86-97 for thermal resistance confidence and derating.

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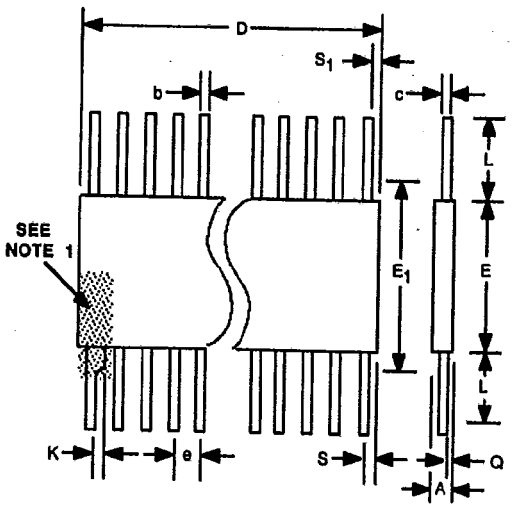
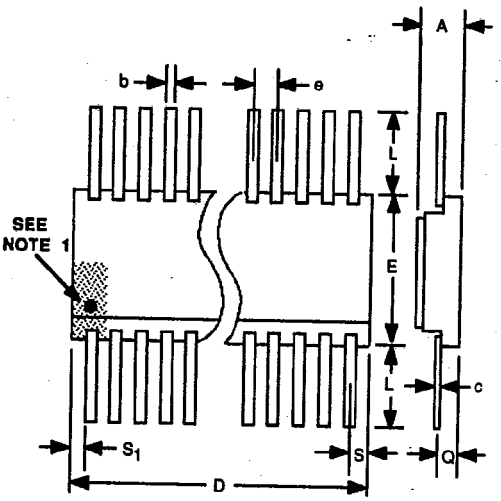
Packaging Information

CASE OUTLINES Y (FLAT PACKAGES)



Configuration 1



Configuration 2

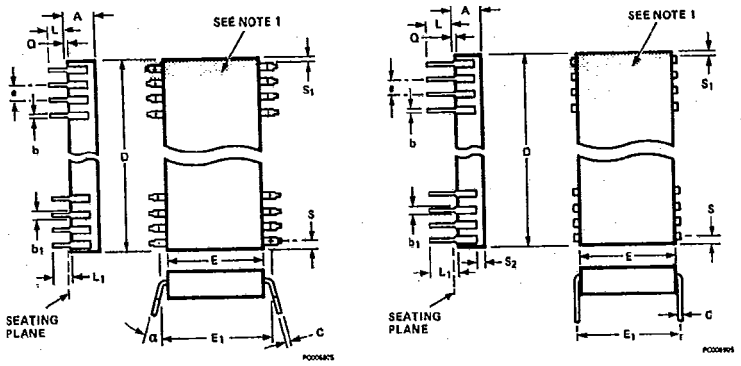
NOTES:

1. A lead tab (enlargement) or index dot is located within the shaded area shown at Pin 1. Other pin numbers proceed sequentially from Pin 1 counterclockwise (as viewed from the top of the device).
2. This dimension allows for off-center lid, meniscus, and glass overrun.
3. The reference pin spacing is 0.050 between centerlines. Each pin centerline is located within ± 0.005 of its logitudinal position relative to the first and last pin numbers.
4. This dimension is measured at the point of exit of the lead body.
5. This dimension applied to all four corner pins.
6. Lead dimensions include 0.003 inch allowance for hot solder dip lead finish.

OUTLINE	Y1		NOTES
CONFIGURATION	2		
NO. LEADS	52		
SIG. PKG.	QP		
SYMBOL	INCHES		
	Min	Max	
A	0.045	0.100	
b	0.015	0.026	6
c	0.008	0.015	6
D	- -	1.330	2
E	0.620	0.660	
e	0.050 BSC		3
L	0.250	0.370	
Q	0.054	0.0666	4
S	-	0.045	5
S1	0.005	-	5

Packaging Information

CASE OUTLINES X (DUAL IN-LINE PACKAGES)



Configuration 1 Configuration 2

1. An index notch is located within the shaded area shown. Pin 1 is adjacent to the notch to the immediate left (as viewed from the top of the device) and other pin numbers proceed sequentially from Pin 1 counterclockwise.
2. The minimum limit for Dimension b1 is 0.023 inches for all four corner pins.
3. This dimension allows for off-center lid, meniscus, and glass overrun.
4. This dimension is measured at the centerline of the leads for Configuration 2.
5. The reference pin spacing is 0.100 between centerlines. Each pin centerline is located within ±0.010 of its longitudinal position relative to the first and last pin numbers.
6. This dimension is measured from the seating plane to the base plane.
7. This dimension applies to all four corner pins.
8. Lead dimensions include 0.003 inch allowance for hot solder dip lead finish.

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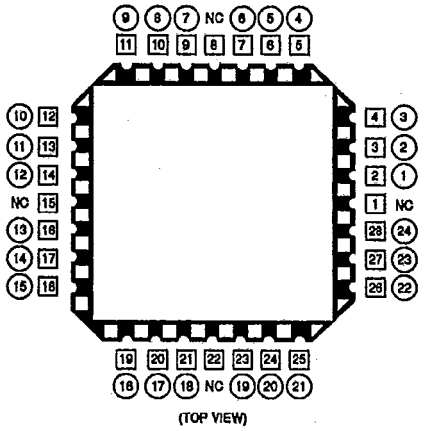
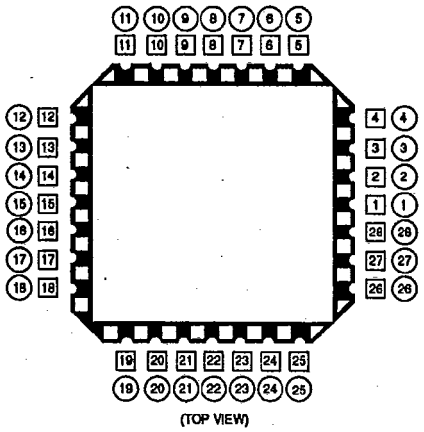
Packaging Information

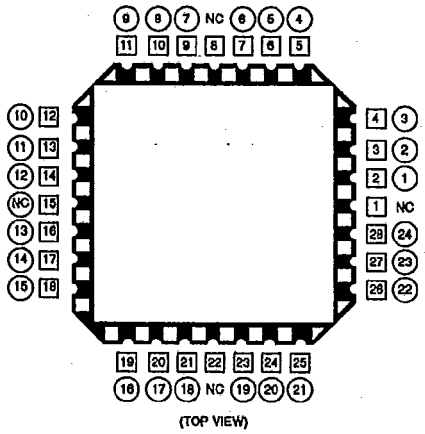
LEADLESS CHIP CARRIER (LLCC) PINOUTS



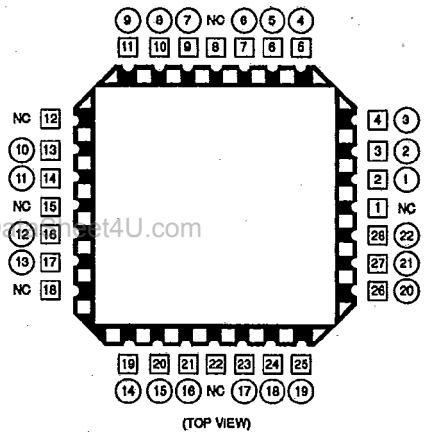
24–Lead Logic Pinout for 28 Terminal Chip Carrier



26–Lead Pinout for 28 Terminal Chip Carrier for all Device Types



24–Lead Memory Pinout for 28 Terminal Chip Carrier



22–Lead Memory Pinout for 28 Terminal Chip Carrier

□ = Chip Carrier Terminal Number
○ = Dual In-Line Lead Number
NC = No Connect