

The ABLIC Inc. HDL6M05585 is an octal, 5-level RTZ, high-voltage, high-speed ultrasound pulser. The HDL6M05585 comprises logic interfaces, level translators, MOSFET gate drive buffers with floating voltage regulators, high-voltage, high-current MOSFETs, and active T/R switches.

Functions

- Octal 5-level pulser with active T/R switch with 2-input per channel

Features

- 0 to $\pm 100V$ output voltage
- $\pm 1.6A$ source and sink peak current for the 1st and 2nd high-voltage pulses ($V_{PP1}/V_{NN1}, V_{PP2}/V_{NN2}$)
- TXSEL to select either V_{PP1}/V_{NN1} or V_{PP2}/V_{NN2} drive commonly for all channels
- $\pm 1.6A$ source and sink peak current for active ground clamp
- 250Ω ($\pm 0.1A$) active ground clamp without blocking diode for anti-leakage (Analog SW type)
- Embedded floating voltage regulators
- Symmetrical positive and negative pulse waveforms for low 2nd order harmonic distortion
- Up to 200MHz LVDS/LVCMOS clock (transparent mode available)
- 12Ω active T/R switch
- 20MHz output frequency @ $\pm 60V$ output, 220pF load
- 1.8V to 5V CMOS logic interface
- Noise-cut diodes at each high-voltage output
- Embedded high-voltage clamp diodes
- 2-mode output current control for the 2nd high-voltage rail
- Automatic thermal protection with indicator
- Power-up/down reset function for free power sequencing and for fail-safe in abrupt power drop
- Latch-up free, low crosstalk between channels by SOI CMOS technology
- 68-lead 10x10mm QFN package (RoHS compliant)

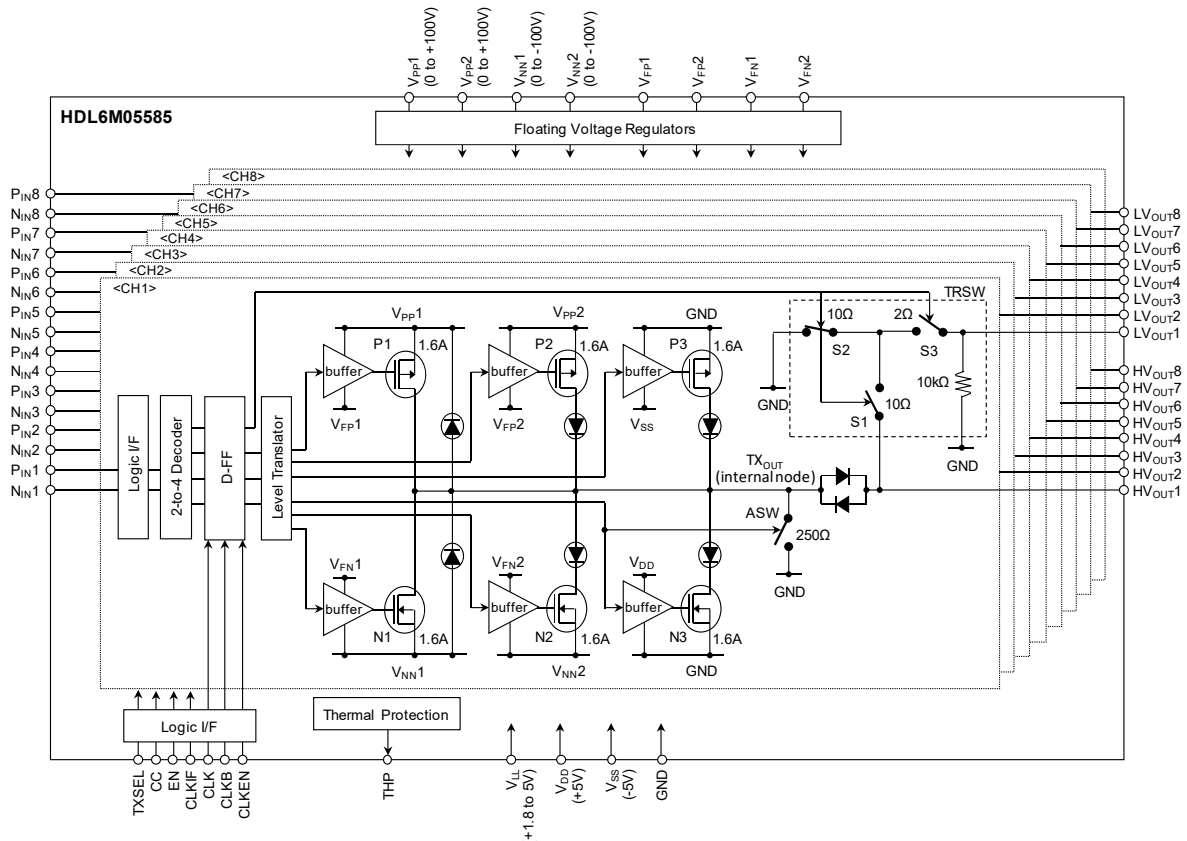


Fig.1 Block diagram

1. Absolute Maximum Ratings

T_A=25°C unless otherwise noted.

Table 1 Absolute Maximum Ratings

No.	Items	Symbol	Value	Units	Condition
1	Logic supply voltage	V _{LL}	-0.4 to +7	V	
2	Positive supply voltage	V _{DD}	-0.4 to +7	V	
3	Negative supply voltage	V _{SS}	-7 to +0.4	V	
4	Positive high-voltage supplies	V _{PP1} , V _{PP2}	-0.5 to +105	V	
5	Negative high-voltage supplies	V _{NN1} , V _{NN2}	-105 to +0.5	V	
6	Positive high-voltage difference	(V _{PP1} -V _{PP2})	-0.5 to +105	V	P _{INX} =1, N _{INX} =0, TXSEL=1
			-105 to +105	V	Other than above
7	Negative high-voltage difference	(V _{NN1} -V _{NN2})	-105 to +0.5	V	P _{INX} =0, N _{INX} =1, TXSEL=1
			-105 to +105	V	Other than above
8	High-voltage outputs (x=1~8)	HV _{OUTX}	-105 to +105	V	
9	Low-voltage outputs (x=1~8)	LV _{OUTX}	-1 to +1	V	
10	THP (Thermal Protection) output	THP	-0.4 to +7	V	
11	All Logic input voltages (x=1~8)	P _{INX} , N _{INX} , EN, CLKEN, CLK, CLKB, CLKIF, CC, TXSEL	-0.4 to +7	V	
12	Operating junction temperature	T _{Jop}	-20 to +150	°C	
13	Storage temperature	T _{STG}	-55 to +150	°C	
14	Maximum power dissipation	P _{Dmax}	4	W	

NOTE: Stresses beyond the absolute maximum ratings may cause permanent damage to the product.

2. Operating Supply Voltages, Logic Inputs, and Power sequencing

2.1 Operating Supply Voltages

Table 2 Operating Supply Voltages

No	Items	Symbol	Min	Typ	Max	Units	Condition
1	Logic supply voltage	V _{LL}	2.4	2.5 to 3.3	3.6	V	Clock mode
			1.7	1.8 to 5	V _{DD}	V	Transparent mode
2	Positive supply voltage	V _{DD}	4.75	5	5.25	V	
3	Negative supply voltage	V _{SS}	-5.25	-5	-4.75	V	
4	Positive high-voltage supplies	V _{PP1} , V _{PP2}	0	-	100	V	
5	Negative high-voltage supplies	V _{NN1} , V _{NN2}	-100	-	0	V	
6	Positive high-voltage difference	(V _{PP1} -V _{PP2})	0	-	100	V	
7	Negative high-voltage difference	(V _{NN1} -V _{NN2})	-100	-	0	V	
8	IC substrate voltage *	V _{SUB}	-	0	-	V	
9	V _{PPX} , V _{NNX} slew rate (x=1,2)	SR _{MAX}	-	-	25	V/ms	
10	Operating free-air Temperature	T _A	0		75	°C	

NOTE: * The package exposed pad internally connected to the chip substrate must be soldered to the ground.

2.2 Logic Inputs

2.2.1 Synchronizing Data Inputs

Clock (CLK) mode synchronizes data inputs P_{INX}, N_{INX} (x=1~8) and TXSEL with a differential LVDS/CMOS clock. Transparent (TP) mode without using clock is also available.

CLK mode:

Set CLKEN=0. P_{INX}, N_{INX}, and TXSEL are decoded, clocked, level-translated, then sent to high-voltage output stage. Differential clock input has two modes as shown below.

- LVDS CLK mode: Set CLKIF=0. Connect external 100Ω between CLK and CLKB. See Table 3 and 4 for the logic inputs, CLK, and CLKB.
- CMOS CLK mode: Set CLKIF=1. See Table 3 for all the logic inputs.

TP mode:

Set CLKEN=CLKIF=1, CLK=CLKB=0. P_{INX}, N_{INX} and TXSEL are decoded, level-translated, then sent to high-voltage output stage. See Table 3 for all the logic inputs.

2.2.2 Selecting Output Drivers

TXSEL selects either P1/N1 or P2/N2 high-voltage output stage commonly for all channels.

- P1/N1-driver selection for all channels: Set TXSEL=0.
- P2/N2-driver selection for all channels: Set TXSEL=1.

See Table 3 for the timing. See also Table 13 for the truth table.

Table 3 Logic Inputs

No	Items	Symbol	Min	Typ	Max	Units	Condition	
1	High-level logic input voltage	V _{IH}	0.8V _{LL}	-	V _{LL}	V		
2	Low-level logic input voltage	V _{IL}	0	-	0.2V _{LL}	V		
3	Logic input capacitance	C _{IN}	-	3	-	pF		
4	Logic input high current	I _{IH}	-10	-	10	μA		
5	Logic input low current *1	I _{IL}	-10	-	10	μA		
6	Input rise/fall time	t _r , t _f	-	-	800	ps	CLK≥100MHz	CMOS CLK mode 10~90% CLK, CLKB, P _{INX} , N _{INX} , TXSEL
			-	-	2.0	ns	CLK<100MHz	
7	Input clock frequency	f _{CLK}	-	-	200	MHz	CMOS CLK mode, CLK, CLKB,	
8	Clock duty cycle	D _{CLK}	40	50	60	%	f _{CLK} =1/T, D _{CLK} =t/T, See Fig.3	
9	Data setup time	t _{SU_D}	1.4	-	-	ns	CLK mode, P _{INX} ,N _{INX} to CLK/CLKB	
10	Data hold time	t _{HLD_D}	1.4	-	-	ns	See Fig.3	
11	TXSEL setup time	t _{SU_S}	1.4	-	-	ns	CLK mode, TXSEL to CLK/CLKB See Fig.3	
			1.4	-	-	ns	TP mode, TXSEL to P _{INX} ,N _{INX} See Fig.3	
12	TXSEL hold time	t _{HLD_S}	1.4	-	-	ns	CLK mode, TXSEL to CLK/CLKB See Fig.3	
			1.4	-	-	ns	TP mode, TXSEL to P _{INX} ,N _{INX} See Fig.3	

NOTE:

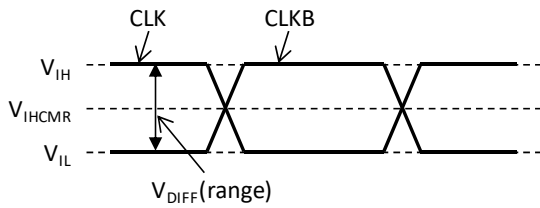
*1) EN, CC, CLKEN, and CLKIF have 50μA leakage at V_{LL}=2.5V due to 50kΩ internal pull-up resistor.

Table 4 LVDS Clock Inputs (CLK, CLKB)

No	Items	Symbol	Min	Typ	Max	Units	Condition
1	High-level input voltage	V_{IH}	1.265	-	-	V	$V_{IHCMR}(Typ)+V_{DIFF}(Min)/2$
2	Low-level input voltage	V_{IL}	-	-	1.135	V	$V_{IHCMR}(Typ)-V_{DIFF}(Min)/2$
3	Differential input voltage range	$V_{DIFF(range)}$	0.13	0.35	0.49	±V	same as CLK,CLKB voltage swing See Fig.2
4	Differential input voltage peak to peak swing	$V_{DIFF(p-p)}$	0.26	0.7	0.98	V_{pp}	$ CLK-CLKB $ differential peak-to-peak voltage swing, See Fig.2
5	Input voltage common mode range	V_{IHCMR}	0.84	1.2	1.56	V	
6	Differential input impedance	R_{IN}	85	100	115	Ω	External 100Ω
7	High-level input current	I_{IH}	-	-	5.8	mA	
8	Low-level input current	I_{IL}	-	-	5.8	mA	
9	Input rise/fall time	t_r, t_f	-	-	600	ps	20% to 80% of V_{DIFF}
10	Input clock frequency	f_{CLK}	-	-	200	MHz	LVDS CLK mode, CLK, CLKB,
11	Clock duty cycle	D_{CLK}	40	50	60	%	$f_{CLK}=1/T, D_{CLK}=t/T$, See Fig.3

NOTE: Please refer to table 3 for the logic inputs other than CLK, CLKB in LVDS CLK mode.

Differential input voltage range ($V_{DIFF(range)}$)



Differential input voltage peak to peak swing ($V_{DIFF(p-p)}$)

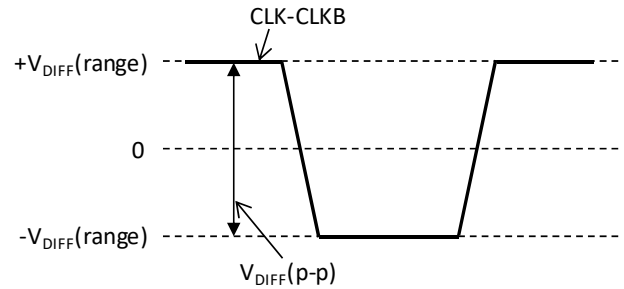
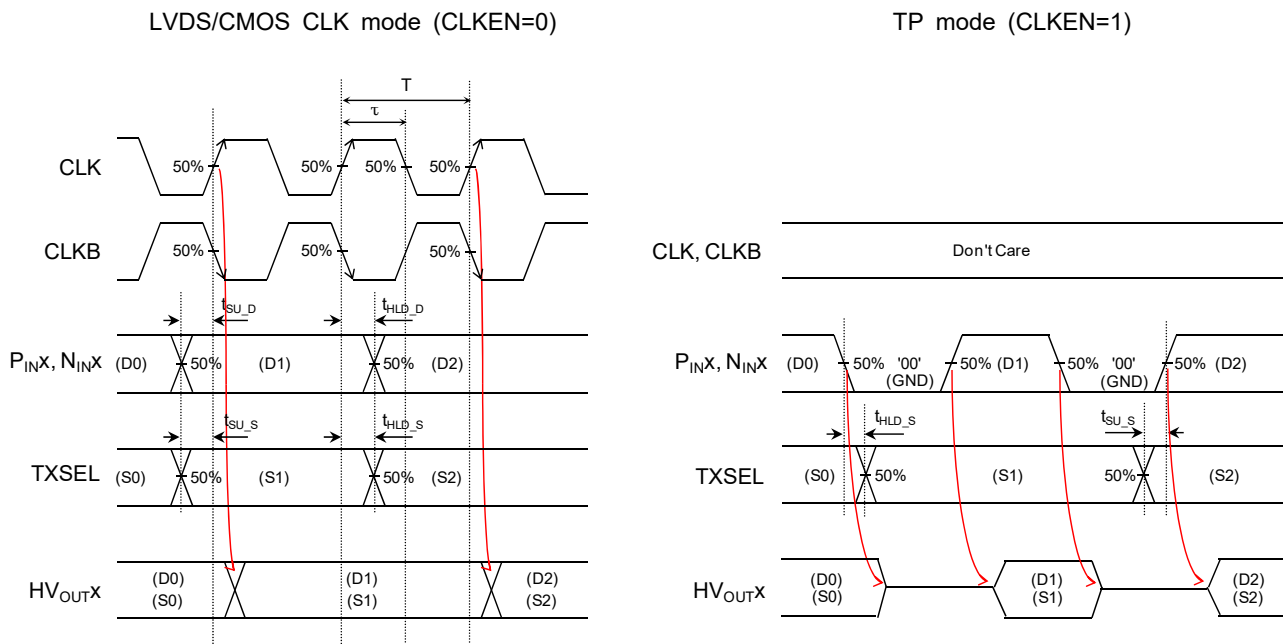


Fig.2 LVDS clock inputs



NOTE: (S_x, x=0,1,2,...) represents the selected drive. Either P1/N1 or P2/N2 drive is commonly selected for all channels.

Fig.3 Setup/Hold Time

2.3 Power Supply Sequencing

Embedded low-voltage (LV) power-up/down reset function provides free power supply sequencing.

It also provides fail-safe system in abrupt LV power supply drop.

When any one of LV power supplies is turned off during operation, all internal circuits will be immediately reset, and both inputs and outputs will be disabled.

Once all LV power supplies are restored, both inputs and output will be enabled.

3. Typical Application Circuit

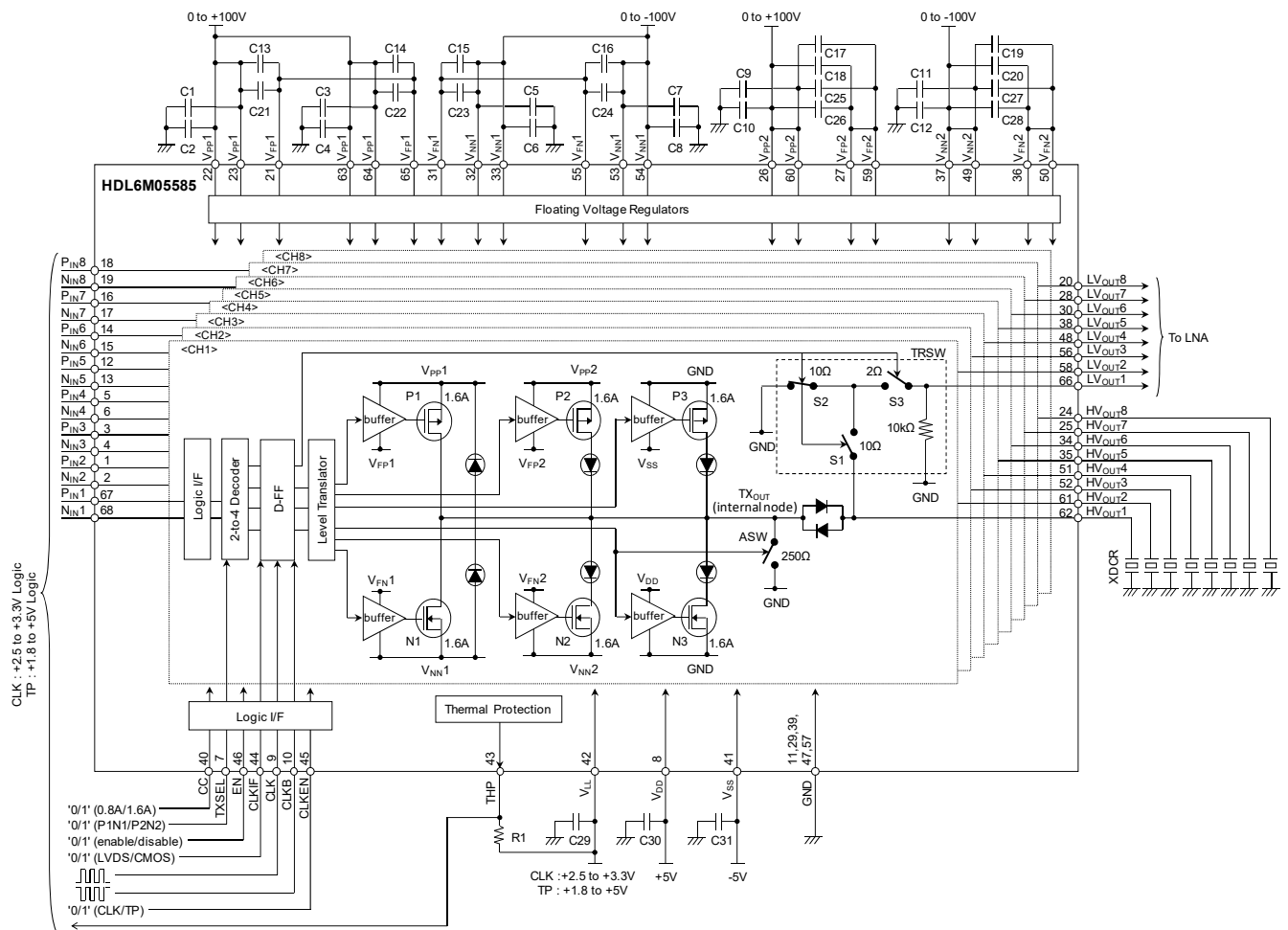


Fig.4 Typical Application Circuit

Note:

1. High-voltage power supply pins, V_{PPX}/V_{NNX} ($x=1,2$), can draw fast transient currents up to $\pm 1.6A$. Therefore, ceramic capacitors of $\geq 200V$ $0.1\mu F$ to $1\mu F$ (C1~12) should be connected as close to the pins as possible for bypassing purpose.
2. Ceramic capacitors of $\geq 16V$ $10\mu F$ (C13~20), $\geq 16V$ $100nF$ (C21~28), and $\geq 16V$ $0.1\mu F$ to $1\mu F$ (C29~31) should also be connected between high-voltage power supply pins and corresponding floating voltage pins V_{FP}/V_{FN} , and low-voltage power supply pins for bypassing purpose. Connect those as close to the pins as possible.
3. It is also important to minimize the trace length and to have enough trace width of those high voltage and floating voltage lines.
4. The thermal tab on the bottom of the package must be soldered to the GND.
5. External 100Ω should be connected between CLK and CLKB in LVDS CLK mode.

4. Electrical Characteristics

4.1 Operating Supply Currents

Table 5 Operating Supply Currents

$V_{LL}=2.5V$, $V_{DD}/V_{SS}=+/-5V$, $T_A=25^{\circ}C$, $CLK=CLKB=100MHz/0(CLKEN=0/1)$,
 HV_{OUT} load= $220pF//200\Omega$, LV_{OUT} load= $47pF//200\Omega$, unless otherwise specified.

No.	Items		Symbol	Spec			Units	Conditions	
				Min	Typ	Max			
1	V _{LL} current	TP	I _{LLQD}	-	0.03	-	mA	Quiescent current-1 EN=1(Disable) P _{INX} =N _{INX} =0 Current mode 1 (CC=1) V _{PP1} /V _{NN1} =+/-100V V _{PP2} /V _{NN2} =+/-100V	
		LVDS CLK		-	0.13	-	mA		
		CMOS CLK		-	0.08	-	mA		
2	V _{DD} current	TP	I _{DDQD}	-	3.3	-	mA		
		LVDS CLK		-	3.3	-	mA		
		CMOS CLK		-	3.3	-	mA		
3	V _{SS} current		I _{SSQD}	-	1.0	-	mA		
4	V _{PP1} current		I _{PP1QD}	-	0.03	-	mA		
5	V _{NN1} current		I _{NN1QD}	-	0.03	-	mA		
6	V _{PP2} current		I _{PP2QD}	-	0.05	-	mA		
7	V _{NN2} current		I _{NN2QD}	-	0.05	-	mA		
8	V _{LL} current	TP	I _{LLQE}	-	0.08	-	mA	Quiescent current-2 EN=0(Enable) P _{INX} =N _{INX} =0 Current mode 1 (CC=1) V _{PP1} /V _{NN1} =+/-100V V _{PP2} /V _{NN2} =+/-100V	
		LVDS CLK		-	0.18	-	mA		
		CMOS CLK		-	0.13	-	mA		
9	V _{DD} current	TP	I _{DDQE}	-	11	-	mA		
		LVDS CLK		-	33	-	mA		
		CMOS CLK		-	30	-	mA		
10	V _{SS} current		I _{SSQE}	-	10	-	mA		
11	V _{PP1} current		I _{PP1QE}	-	0.15	-	mA		
12	V _{NN1} current		I _{NN1QE}	-	0.15	-	mA		
13	V _{PP2} current		I _{PP2QE}	-	0.17	-	mA		
14	V _{NN2} current		I _{NN2QE}	-	0.17	-	mA		
15	V _{LL} current	TP	I _{LLPW}	-	0.18	-	mA		PW operating current EN=0 Current mode 1 (CC=1) 8-channel active Bipolar 3-level 2-cycle P1/N1-drive f=5MHz, PRT=200μs V _{PP1} /V _{NN1} =+/-60V V _{PP2} /V _{NN2} =+/-60V
		LVDS CLK		-	0.18	-	mA		
		CMOS CLK		-	0.13	-	mA		
16	V _{DD} current	TP	I _{DDPW}	-	11	-	mA		
		LVDS CLK		-	37	-	mA		
		CMOS CLK		-	35	-	mA		
17	V _{SS} current		I _{SSPW}	-	10	-	mA		
18	V _{PP1} current		I _{PP1PW}	-	4.0	-	mA		
19	V _{NN1} current		I _{NN1PW}	-	4.6	-	mA		
20	V _{PP2} current		I _{PP2PW}	-	0.17	-	mA		
21	V _{NN2} current		I _{NN2PW}	-	0.17	-	mA		

Table 5 Operating Supply Currents (continued)

No.	Items	Symbol	Spec			Units	Conditions
			Min	Typ	Max		
22	V _{LL} current	TP	-	0.43	-	mA	CW operating current-1 EN=0 Current mode 1 (CC=1) 8-channel active Bipolar 3-level Continuous P2/N2-drive f=5MHz V _{PP1} /V _{NN1} =+/-5V V _{PP2} /V _{NN2} =+/-5V
		LVDS CLK	-	0.53	-	mA	
		CMOS CLK	-	0.48	-	mA	
23	V _{DD} current	TP	-	39	-	mA	
		LVDS CLK	-	60	-	mA	
		CMOS CLK	-	58	-	mA	
24	V _{SS} current	I _{SSCW3}	-	26	-	mA	
25	V _{PP1} current	I _{PP1CW3}	-	0.15	-	mA	
26	V _{NN1} current	I _{NN1CW3}	-	0.15	-	mA	
27	V _{PP2} current	I _{PP2CW3}	-	171	-	mA	
28	V _{NN2} current	I _{NN2CW3}	-	173	-	mA	
29	V _{LL} current	TP	-	0.48	-	mA	CW operating current-2 EN=0 Current mode 0 (CC=0) 8-channel active Bipolar 3-level Continuous P2/N2-drive f=5MHz V _{PP1} /V _{NN1} =+/-5V V _{PP2} /V _{NN2} =+/-5V
		LVDS CLK	-	0.58	-	mA	
		CMOS CLK	-	0.53	-	mA	
30	V _{DD} current	TP	-	31	-	mA	
		LVDS CLK	-	53	-	mA	
		CMOS CLK	-	51	-	mA	
31	V _{SS} current	I _{SSCW1}	-	19	-	mA	
32	V _{PP1} current	I _{PP1CW1}	-	0.15	-	mA	
33	V _{NN1} current	I _{NN1CW1}	-	0.15	-	mA	
34	V _{PP2} current	I _{PP2CW1}	-	153	-	mA	
35	V _{NN2} current	I _{NN2CW1}	-	155	-	mA	

4.2 Static Characteristics

Table 6 Static Characteristics

$V_{LL}=2.5V$, $V_{DD}/V_{SS}=\pm 5V$, $T_A=25^\circ C$, unless otherwise specified.

No.	Items	Symbol	Spec			Units	Conditions
			Min	Typ	Max		
1	HV _{OUTX} output voltage range	HV _{OUTX}	-100	-	+100	V	
2	HV _{OUTX} high-side peak current	I _{OH}	-	1.6	-	A	P1 active, $V_{PP1}/V_{NN1}=V_{PP2}/V_{NN2}=\pm 60V$
			-	1.6	-	A	P2 active, $V_{PP1}/V_{NN1}=V_{PP2}/V_{NN2}=\pm 60V$ Current mode 1 (CC=1)
			-	0.8	-	A	P2 active, $V_{PP1}/V_{NN1}=V_{PP2}/V_{NN2}=\pm 60V$ Current mode 0 (CC=0)
3	HV _{OUTX} high-side GND clamp peak current	I _{OHCL}	-	1.6	-	A	N3 active, $V_{PP1}/V_{NN1}=V_{PP2}/V_{NN2}=\pm 60V$
4	HV _{OUTX} low-side peak current	I _{OL}	-	1.6	-	A	N1 active, $V_{PP1}/V_{NN1}=V_{PP2}/V_{NN2}=\pm 60V$
			-	1.6	-	A	N2 active, $V_{PP1}/V_{NN1}=V_{PP2}/V_{NN2}=\pm 60V$ Current mode 1 (CC=1)
			-	0.8	-	A	N2 active, $V_{PP1}/V_{NN1}=V_{PP2}/V_{NN2}=\pm 60V$ Current mode 0 (CC=0)
5	HV _{OUTX} low-side GND clamp peak current	I _{OLCL}	-	1.6	-	A	P3 active, $V_{PP1}/V_{NN1}=V_{PP2}/V_{NN2}=\pm 60V$
6	HV _{OUTX} high-side on-resistance	R _{ONH}	-	15	-	Ω	P1 active, I _{OH} =100mA
			-	15	-	Ω	P2 active, I _{OH} =100mA Current mode 1 (CC=1)
			-	23	-	Ω	P2 active, I _{OH} =100mA Current mode 0 (CC=0)
7	HV _{OUTX} high-side GND clamp on-resistance	R _{ONHCL}	-	15	-	Ω	N3 active, I _{OHCL} =100mA
8	HV _{OUTX} low-side on-resistance	R _{ONL}	-	15	-	Ω	N1 active, I _{OL} =100mA
			-	15	-	Ω	N2 active, I _{OL} =100mA Current mode 1 (CC=1)
			-	23	-	Ω	N2 active, I _{OL} =100mA Current mode 0 (CC=0)
9	HV _{OUTX} low-side GND clamp on-resistance	R _{ONLCL}	-	15	-	Ω	P3 active, I _{OLCL} =100mA
10	HV _{OUTX} off-capacitance	C _{HVOFF}	-	34	-	pF	TX _{OUTX} =GND, TRSW=off

4.3 Dynamic Characteristics

Table 7 Dynamic Characteristics

$V_{LL}=2.5V$, $V_{DD}/V_{SS}=+/-5V$, $V_{PP1}/V_{NN1}=V_{PP2}/V_{NN2}=+/-60V$, $T_A=25^{\circ}C$, $CC=1$,

$CLK=CLKB=100MHz/0(CLKEN=0/1)$, HV_{OUT} load= $220pF//200\Omega$, LV_{OUT} load= $47pF//200\Omega$, unless otherwise specified.

No.	Items		Symbol	Spec			Units	Conditions	
				Min	Typ	Max			
1	Output frequency		f_{OUT}	-	20	-	MHz		
2	Output rise propagation delay	TP mode	t_{dr}	-	28	-	ns	See Fig.5	
		CLK mode		-	36	-	ns		
3	Output fall propagation delay	TP mode	t_{df}	-	28	-	ns		
		CLK mode		-	36	-	ns		
4	Output rise propagation delay clamp	TP mode	t_{drCL}	-	28	-	ns		
		CLK mode		-	36	-	ns		
5	Output fall propagation delay clamp	TP mode	t_{dfCL}	-	28	-	ns		
		CLK mode		-	36	-	ns		
6	Propagation delay matching		Δt_d	-	± 1	± 3	ns		
7	Output rise time		t_r	-	19	-	ns	P1 active	See Fig.5
				-	19	-	ns	P2 active, CC=1	
				-	36	-	ns	P2 active, CC=0	
8	Output fall time		t_r	-	10	-	ns	P3 active	
				-	19	-	ns	N1 active	
				-	19	-	ns	N2 active, CC=1	
			-	36	-	ns	N2 active, CC=0		
			t_{rCL}	-	10	-	ns	N3 active	
9	2 nd harmonic distortion		HD2	-	-40	-	dBc	Bipolar, 2-cyc, $f_{OUT}=5MHz$	
10	Pulse cancellation		HDPC	-	-40	-	dBc	See Fig.6	
			HDPC2	-	-40	-	dBc		
11	RMS output jitter		t_j	-	10	-	ps	Bipolar CW, $f_{OUT}=5MHz$ $V_{PP1}/V_{NN1}=V_{PP2}/V_{NN2}=+/-5V$	
12	Crosstalk between channels		X_{TLK}	-	-70	-	dB	$f_{OUT}=5MHz$, $10V_{p-p}$, HV_{OUT} load= 50Ω	
13	Output enable time	TP	t_{EN}	-	28	-	ns	See Fig.7	
		LVDS CLK		-	115	-	ns		
		CMOS CLK		-	140	-	ns		
14	Output disable time		t_{DS}	-	36	-	ns		
15	Clock mode enable time		t_{CLKEN}	-	36	-	ns		
16	Clock mode disable time		t_{CLKDS}	-	36	-	ns		

4.4 Integrated Peripheral Circuits Characteristics

T/R Switch

Table 8 T/R Switch Characteristics

$V_{LL}=2.5V$, $V_{DD}/V_{SS}=+/-5V$, $V_{PP1}/V_{NN1}=V_{PP2}/V_{NN2}=+/-60V$, $T_A=25^\circ C$, unless otherwise specified.

No.	Items	Symbol	Spec			Units	Conditions
			Min	Typ	Max		
1	LV _{OUTX} output voltage range	LV _{OUTX}	-0.85	-	0.85	V	
2	TRSW on-resistance	R _{ONTR}	-	12	-	Ω	HV _{OUTX} =100mV, LV _{OUTX} =0V
3	TRSW on-capacitance	C _{ONTR}	-	13	-	pF	LV _{OUTX} =0V
4	TRSW off-resistance on HV _{OUTX}	R _{OFFTRHV}	1	-	-	MΩ	
5	TRSW off-resistance on LV _{OUTX}	R _{OFFTRLV}	8	10	12	kΩ	
6	Spike voltage on HV _{OUTX} and LV _{OUTX}	V _{TRN}	-	-	50	mV _{PP}	50pF//200Ω load on HV _{OUTX} 20pF//200Ω load on LV _{OUTX}
7	TRSW turn-on time	t _{dTRON}	-	300	-	ns	Logic input-to-ready for Rx signal See Fig.8
8	TRSW turn-off time	t _{dTROFF}	-	50	100	ns	See Fig.8
9	Tx setup time	t _{TXSU}	100	-	-	ns	P _{INX} =N _{INX} =0 (GND) for at least 100ns before Tx burst. See Fig.8

Analog Switch

Table 9 Analog Switch Characteristics

$T_A=25^\circ C$

No.	Items	Symbol	Spec			Units	Conditions
			Min	Typ	Max		
1	ASW on-resistance	R _{ONASW}	-	250	-	Ω	

HV Blocking Diode

Table 10 Output HV Blocking Diode Characteristics

$T_A=25^\circ C$

No.	Items	Symbol	Spec			Units	Conditions
			Min	Typ	Max		
1	Forward voltage	V _{FHVD}	-	1.0	-	V	I _F =100mA
			-	1.2	-	V	I _F =200mA
2	Reverse voltage	V _{RHVD}	200	-	-	V	I _R =1μA

LV Noise-cut Diode

Table 11 Output LV Noise-cut Diode Characteristics

$T_A=25^\circ C$

No.	Items	Symbol	Spec			Units	Conditions
			Min	Typ	Max		
1	Forward voltage	V _{FLVD}	-	1.1	-	V	I _F =100mA
			-	1.25	-	V	I _F =200mA

Thermal Protection

Table 12 Thermal Protection Characteristics

$V_{LL}=2.5V$, $V_{DD}/V_{SS}=\pm 5V$, $T_A=25^{\circ}C$, unless otherwise specified.

No.	Items	Symbol	Spec			Units	Conditions
			Min	Typ	Max		
1	THP pull-up voltage	V_{PUTHP}	-	-	5.25	V	Open drain
2	THP output current	I_{THP}	-	1.0	-	mA	-
3	THP output low voltage	V_{OLTHP}	-	-	0.5	V	THP active, $V_{LL}=2.5V$, $I_{THP}=1mA$
4	THP temperature threshold	T_{THP}	90	110	130	$^{\circ}C$	
5	THP reset hysteresis	T_{HYSTHP}	-	10	-	$^{\circ}C$	

5. Switching Time Diagram

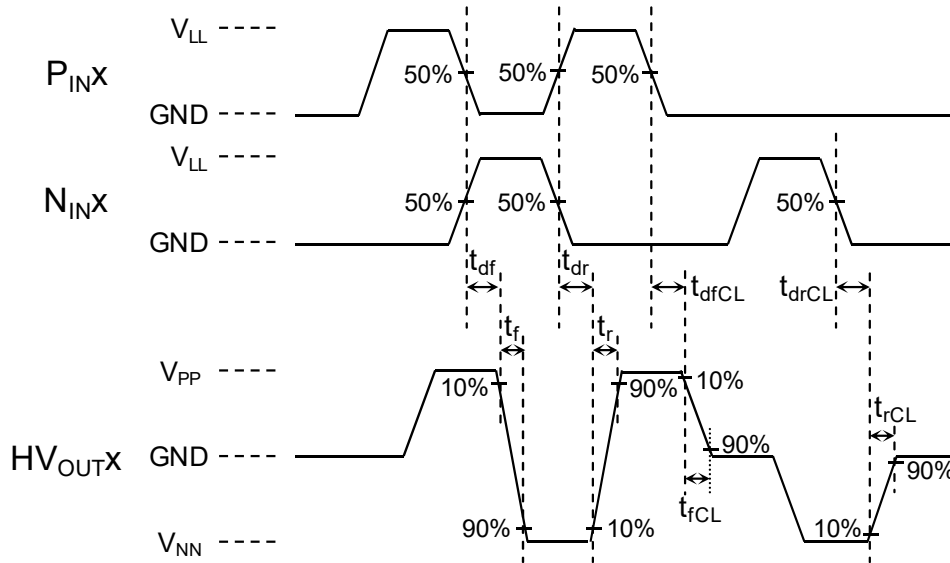
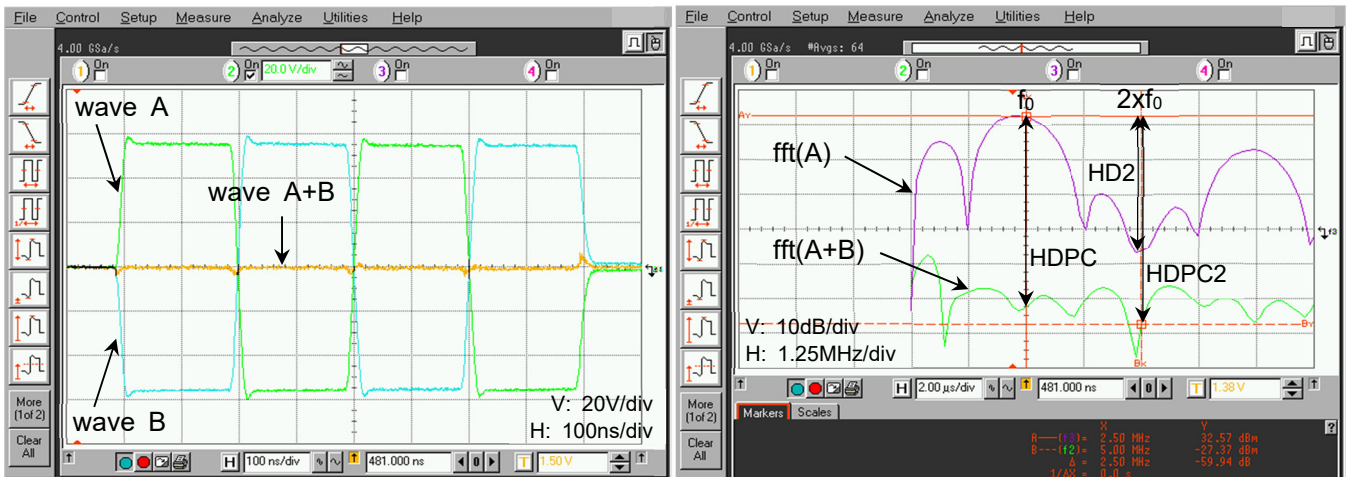


Fig.5 Propagation delay and Output rise/fall time



Example waveforms: $V_{PP}/V_{NN} = \pm 60V$, $f_0 = 2.5MHz$, 2-cycle, HV_{OUT} load = $220pF // 200\Omega$

Fig.6 2nd harmonic distortion and Pulse cancellation

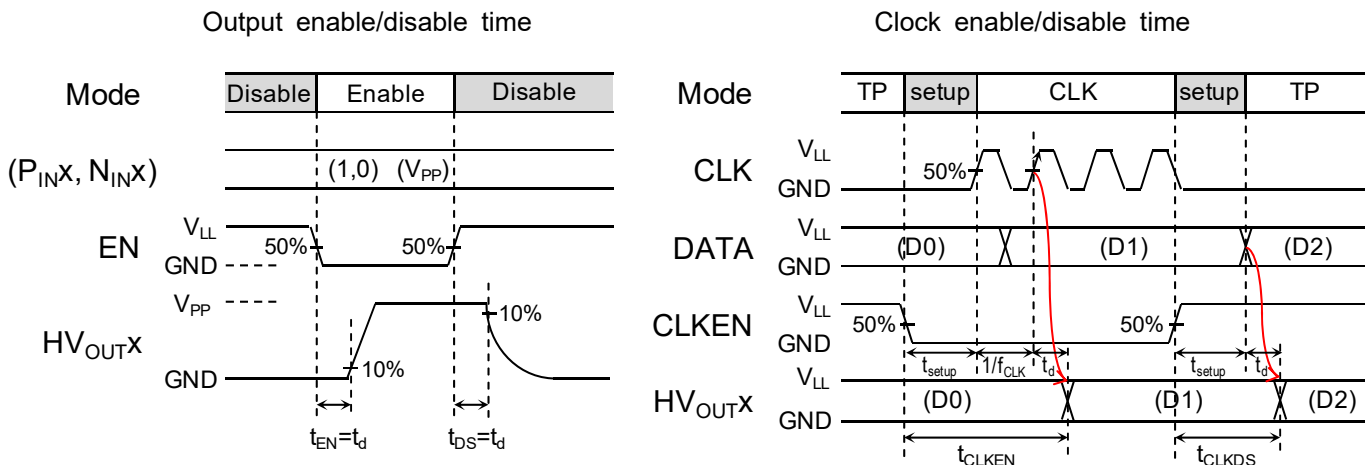


Fig.7 Output enable/disable and Clock enable/disable time

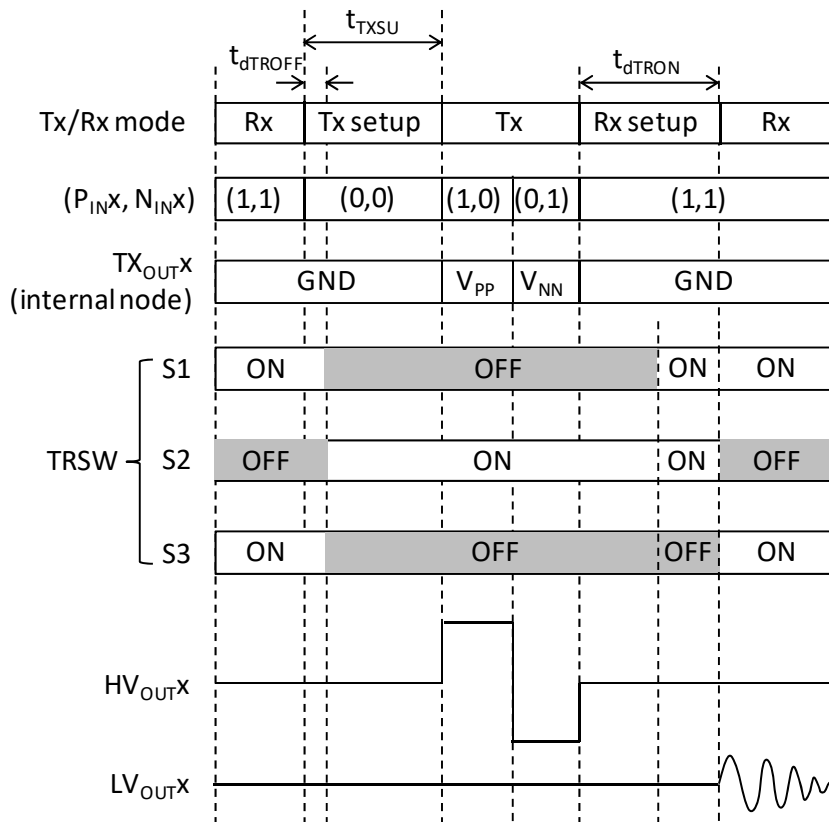


Fig.8 T/R Switch turn-on/off time

6. Truth Table and Mode Control table

Table 13 Truth table

Logic Inputs				Internal MOSFET state										Output state	
EN	TXSEL	P _{INX}	N _{INX}	P1	N1	P2	N2	P3	N3	ASW	TRSW			TX _{OUTX} (internal node)	LV _{OUTX}
				+HV1	-HV1	+HV2	-HV2	GND	GND	GND	S1	S2	S3		
0	0	0	0	OFF	OFF	OFF	OFF	ON	ON	ON	OFF	ON	OFF	GND	10kΩ
0	0	0	1	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	ON	-HV1	10kΩ
0	0	1	0	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	ON	+HV1	10kΩ
0	0	1	1	OFF	OFF	OFF	OFF	ON	ON	ON	ON	OFF	ON	GND	HV _{OUTX}
0	1	0	0	OFF	OFF	OFF	OFF	ON	ON	ON	OFF	ON	OFF	GND	10kΩ
0	1	0	1	OFF	OFF	OFF	ON	OFF	OFF	OFF	OFF	OFF	ON	-HV2	10kΩ
0	1	1	0	OFF	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF	ON	+HV2	10kΩ
0	1	1	1	OFF	OFF	OFF	OFF	ON	ON	ON	ON	OFF	ON	GND	HV _{OUTX}
1	X	X	X	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	ON	HiZ	10kΩ

Note: V_{PP1}/ V_{NN1}=+/-HV1, V_{PP2}/ V_{NN2}=+/-HV2, x=1~8

Table 14 P2/N2 drive current mode

Current Mode	CC	I _{out} [A]	
		P2	N2
0	0	0.8	0.8
1	1	1.6	1.6

Note:

Recommended mode is as follows:

- Current mode 1 for high-amplitude short cycle pulse waveforms, or for driving a heavy load
- Current mode 0 for low-amplitude long pulse train waveforms (e.g. CW), or for driving a light load

7. Pin Configuration

Table 15 Pin Configuration

Pin#	Pin Name	I/O	Function
1	P _{IN2}	I	Logic input of channel 2
2	N _{IN2}	I	Logic input of channel 2
3	P _{IN3}	I	Logic input of channel 3
4	N _{IN3}	I	Logic input of channel 3
5	P _{IN4}	I	Logic input of channel 4
6	N _{IN4}	I	Logic input of channel 4
7	TXSEL	I	Control of output drive selection, Hi=P2/N2, Low=P1/N1
8	V _{DD}	-	Positive low voltage power supply (+5V)
9	CLK	I	Positive clock input (up to 200MHz)
10	CLKB	I	Negative clock Input (up to 200MHz)
11	GND	-	Drive power ground (0V)
12	P _{IN5}	I	Logic input of channel 5
13	N _{IN5}	I	Logic input of channel 5
14	P _{IN6}	I	Logic input of channel 6
15	N _{IN6}	I	Logic input of channel 6
16	P _{IN7}	I	Logic input of channel 7
17	N _{IN7}	I	Logic input of channel 7
18	P _{IN8}	I	Logic input of channel 8
19	N _{IN8}	I	Logic input of channel 8
20	LV _{OUT8}	O	Low voltage output of channel 8
21	V _{FP1}	-	Built-in power supply for P-MOS (P1) gate drive
22	V _{PP1}	-	Positive high voltage power supply 1 (0 to +100V)
23	V _{PP1}	-	Positive high voltage power supply 1 (0 to +100V)
24	HV _{OUT8}	O	High voltage output of channel 8
25	HV _{OUT7}	O	High voltage output of channel 7
26	V _{PP2}	-	Positive high voltage power supply 2 (0 to +100V)
27	V _{FP2}	-	Built-in power supply for P-MOS (P2) gate drive
28	LV _{OUT7}	O	Low voltage output of channel 7
29	GND	-	Drive power ground (0V)
30	LV _{OUT6}	O	Low voltage output of channel 6
31	V _{FN1}	-	Built-in power supply for N-MOS (N1) gate drive
32	V _{NN1}	-	Negative high voltage power supply 1 (0 to -100V)
33	V _{NN1}	-	Negative high voltage power supply 1 (0 to -100V)
34	HV _{OUT6}	O	High voltage output of channel 6

Table 15 Pin Configuration (cont.)

Pin#	Pin Name	I/O	Function
35	HV _{OUT5}	O	High voltage output of channel 5
36	V _{FN2}	-	Built-in power supply for N-MOS (N2) gate drive
37	V _{NN2}	-	Negative high voltage power supply 2 (0 to -100V)
38	LV _{OUT5}	O	Low voltage output of channel 5
39	GND	-	Drive power ground (0V)
40	CC	I	Control of P2/N2 drive current, Hi=1.6A, Low=0.8A (50kΩ internal pull-up resistor)
41	V _{SS}	-	Negative low voltage power supply (-5V)
42	V _{LL}	-	Positive voltage supply of logic input interface (1.8 to 5V)
43	THP	O	Thermal protection output flag, open N-MOS drain
44	CLKIF	I	Control of clock interface, Hi=differential CMOS, Low=LVDS (50kΩ internal pull-up resistor)
45	CLKEN	I	Control of clock enable, Hi=clock disable, Low=clock enable (50kΩ internal pull-up resistor)
46	EN	I	Control of drive output enable, Hi=disable, Low=enable (50kΩ internal pull-up resistor)
47	GND	-	Drive power ground (0V)
48	LV _{OUT4}	O	Low voltage output of channel 4
49	V _{NN2}	-	Negative high voltage power supply 2 (0 to -100V)
50	V _{FN2}	-	Built-in power supply for N-MOS (N2) gate drive
51	HV _{OUT4}	O	High voltage output of channel 4
52	HV _{OUT3}	O	High voltage output of channel 3
53	V _{NN1}	-	Negative high voltage power supply 1 (0 to -100V)
54	V _{NN1}	-	Negative high voltage power supply 1 (0 to -100V)
55	V _{FN1}	-	Built-in power supply for N-MOS (N1) gate drive
56	LV _{OUT3}	O	Low voltage output of channel 3
57	GND	-	Drive power ground (0V)
58	LV _{OUT2}	O	Low voltage output of channel 2
59	V _{FP2}	-	Built-in power supply for P-MOS (P2) gate drive
60	V _{PP2}	-	Positive high voltage power supply 2 (0 to +100V)
61	HV _{OUT2}	O	High voltage output of channel 2
62	HV _{OUT1}	O	High voltage output of channel 1
63	V _{PP1}	-	Positive high voltage power supply 1 (0 to +100V)
64	V _{PP1}	-	Positive high voltage power supply 1 (0 to +100V)
65	V _{FP1}	-	Built-in power supply for P-MOS (P1) gate drive
66	LV _{OUT1}	O	Low voltage output of channel 1
67	P _{IN1}	I	Logic input of channel 1
68	N _{IN1}	I	Logic input of channel 1

■ **Package**

Table 16 Package Drawing Codes

Package Name	Dimension	Tray	Marking	Land	Packing
QFN-68(1010)B	QN068-B-P-SD	QN068-B-T-SD	QN068-B-M-S2	QN068-B-L-SD	QN068-B-K-SD

■ **Storage, Mounting**

1. Storage conditions

- 1.1 The storage location should be kept at 5 to 35°C and 40 to 70% relative humidity. Keeping in a dry box is recommended. Moisture-proof property is assured for 12 months from delivery date for sealed moisture-proof packing, while it is guaranteed for 7 days from unpacked date under the condition above.
- 1.2 When the storage conditions do not conform to those above or other conditions occur indicating moisture exposure, the ICs should be dried to avoid package cracks. A baking process at 125°C lasting for 24 hours results in sufficient dehumidification. The baking is not allowed more than twice, and the ICs should be mounted within 7 days after initial baking or within 10 days of total exposure after the second dehumidification.

2. Reflow soldering

The temperature rise may be different in the resin and a terminal part due to the reflow soldering. It is necessary to check the package surface temperature (resin) before setting the temperature profile.

Fig. 9 shows the resistance to soldering heat condition for package (Reflow method).

Confirm the heat resistance of the package shown below. (Based on JEDEC J-STD-020).

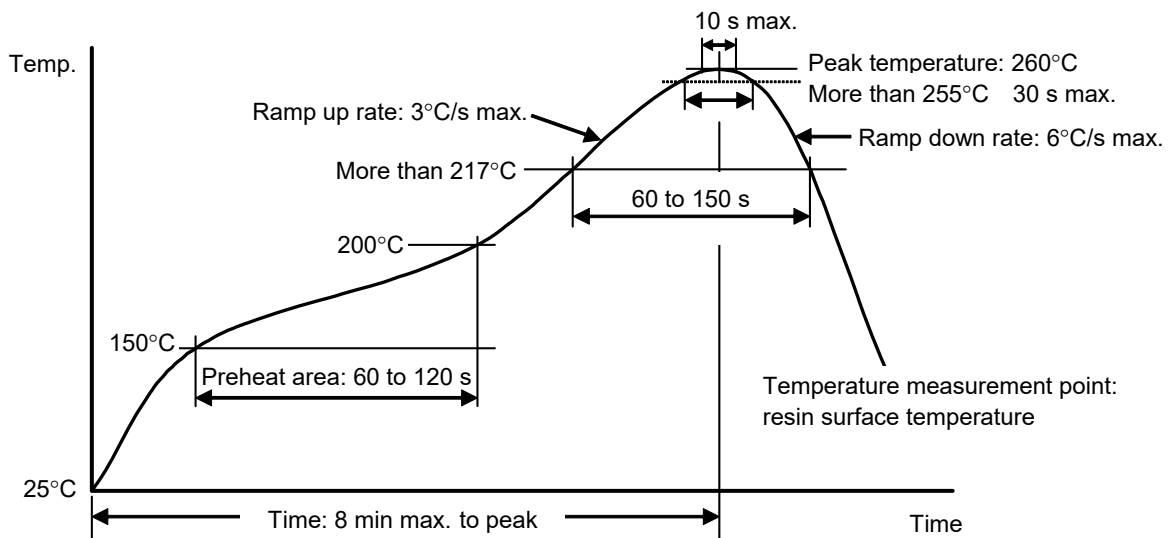


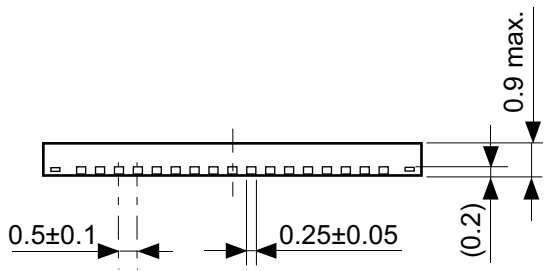
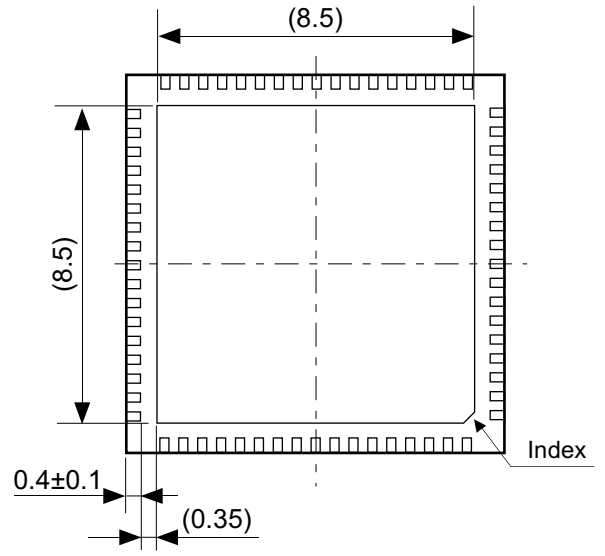
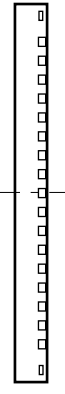
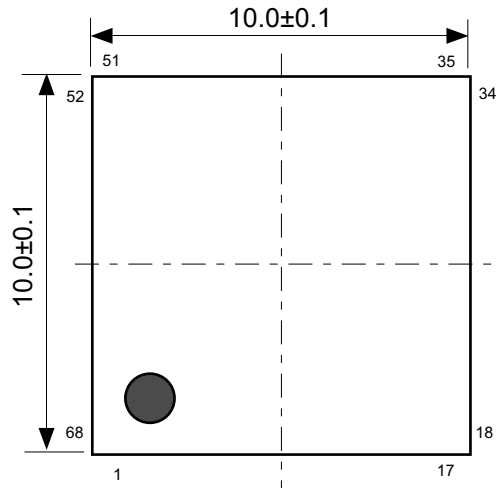
Fig. 9 Resistance to Soldering Heat Condition for Package (Reflow Method)

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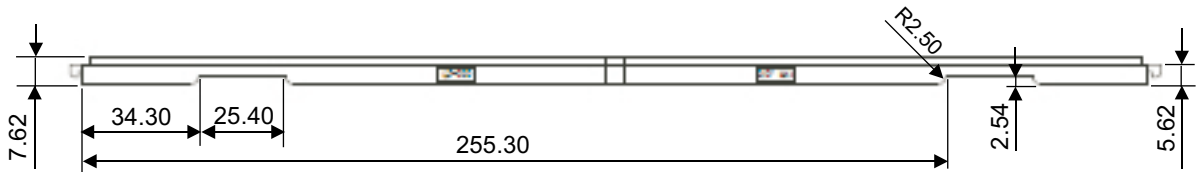
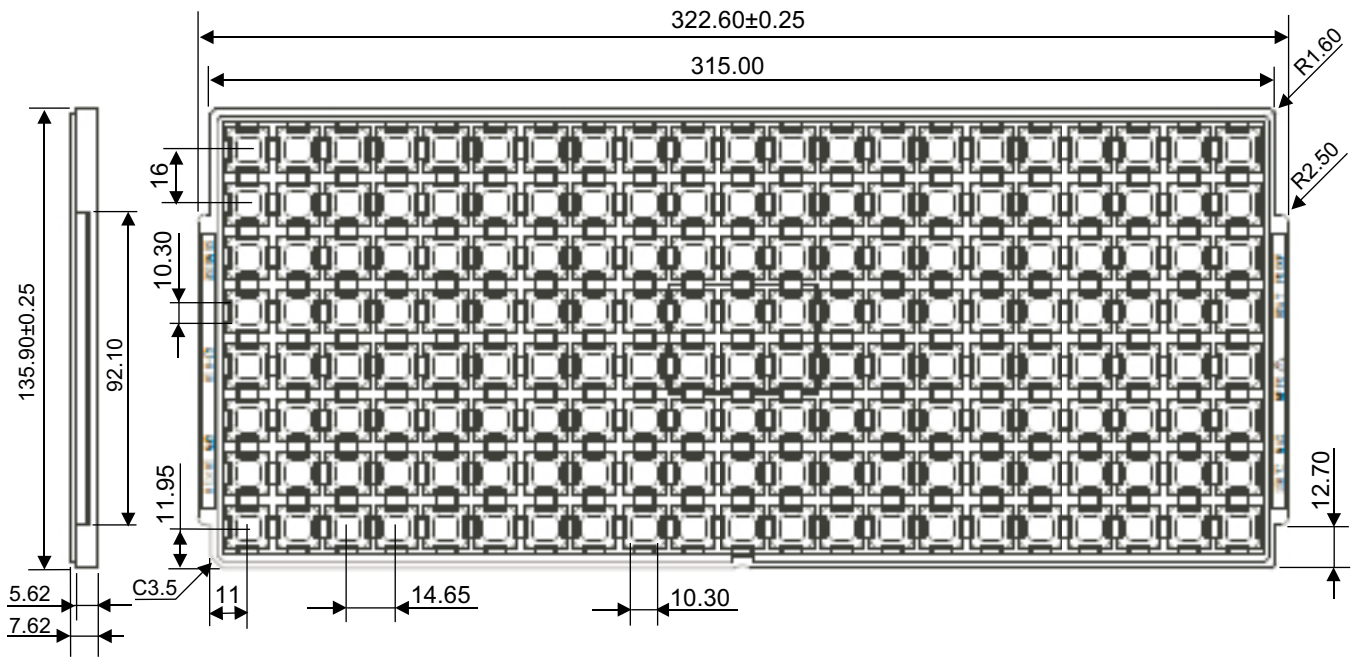
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 - 1.2 Those that touch products, such as work platform, machine, or measurement/test equipment, should be grounded.
 - 1.3 Those who deal with products should be grounded through a large series impedance around 100kΩ to 1MΩ.
 - 1.4 Prevent friction with other materials made with high polymer.
 - 1.5 Prevent vibration or friction when carrying the printed circuit board (PCB) where products are mounted. To short circuit terminals is a recommended countermeasure to keep the same electric potential on the PCB.
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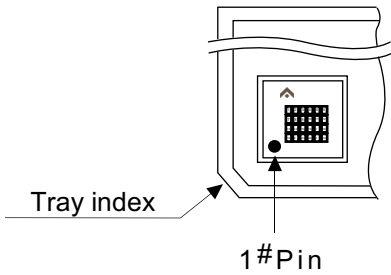


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UNIT	mm
ABLIC Inc.	

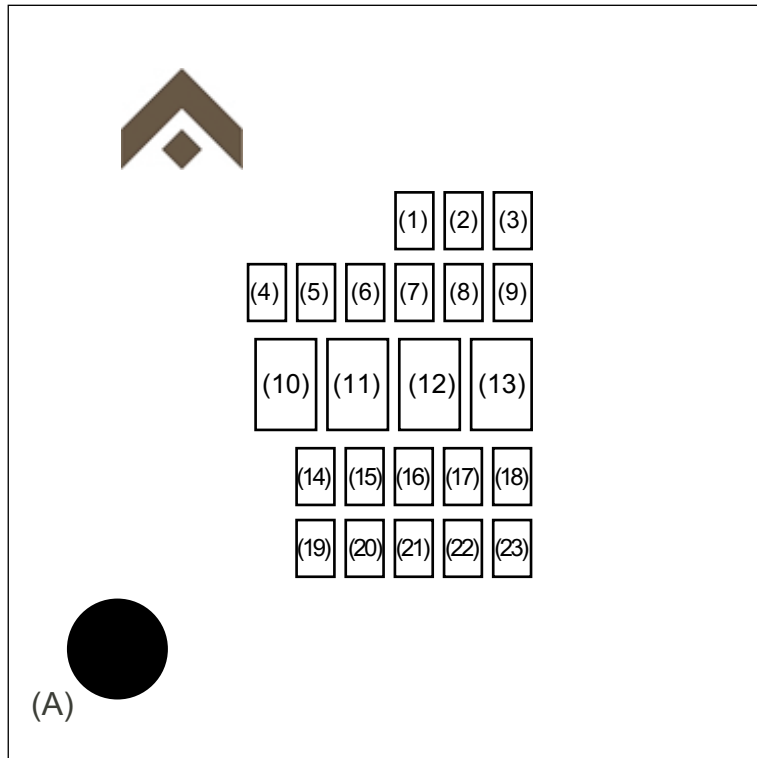


(Direction of IC in tray)



No. QN068-B-T-SD-1.0

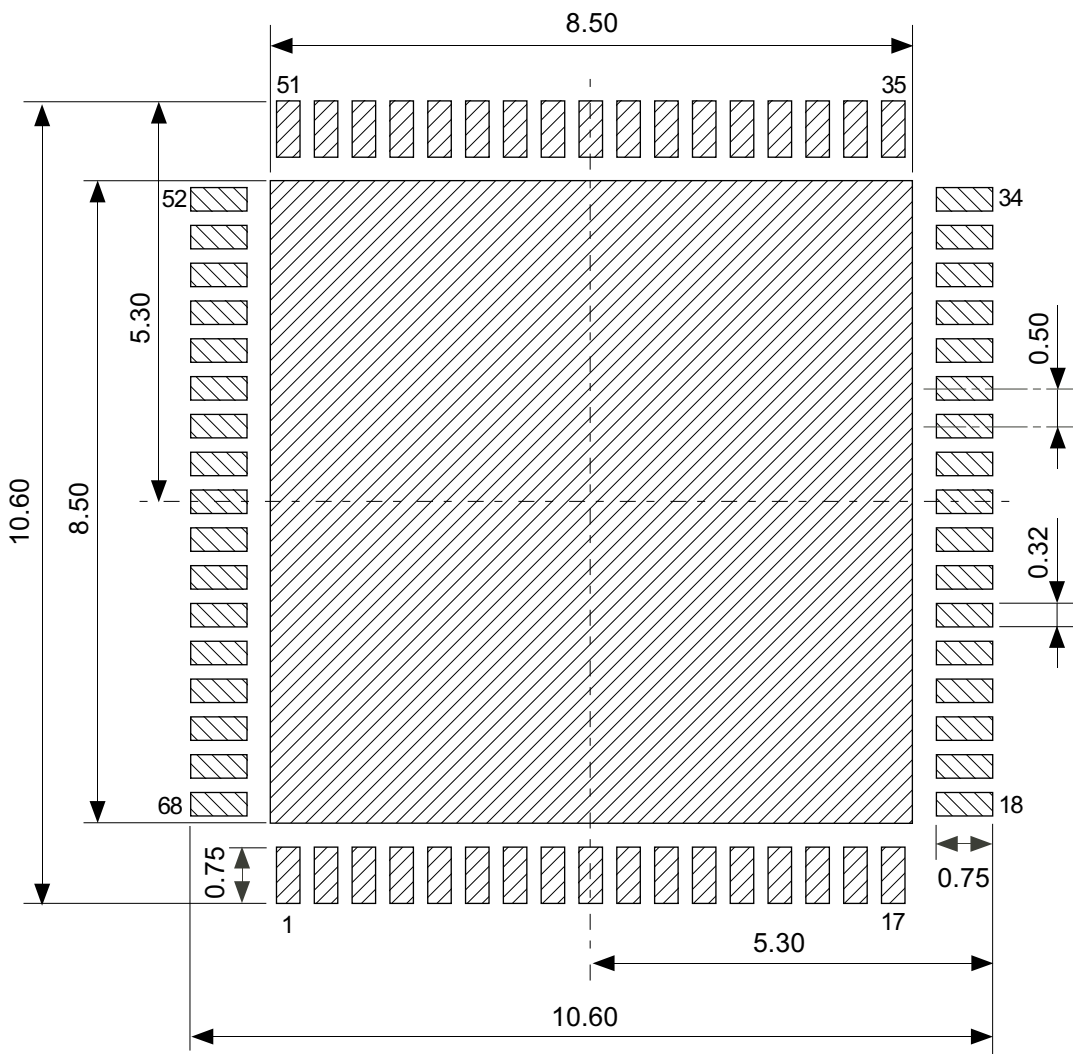
TITLE	QFN68-B-Tray		
No.	QN068-B-T-SD-1.0		
ANGLE		QTY.	168
UNIT	mm		
ABLIC Inc.			



- (1) : Year of assembly
- (2) : Month of assembly
- (3) : Week of assembly
- (4) to (13) : Product code
- (14) to (23) : Quality control code
- (A) : 1-pin mark

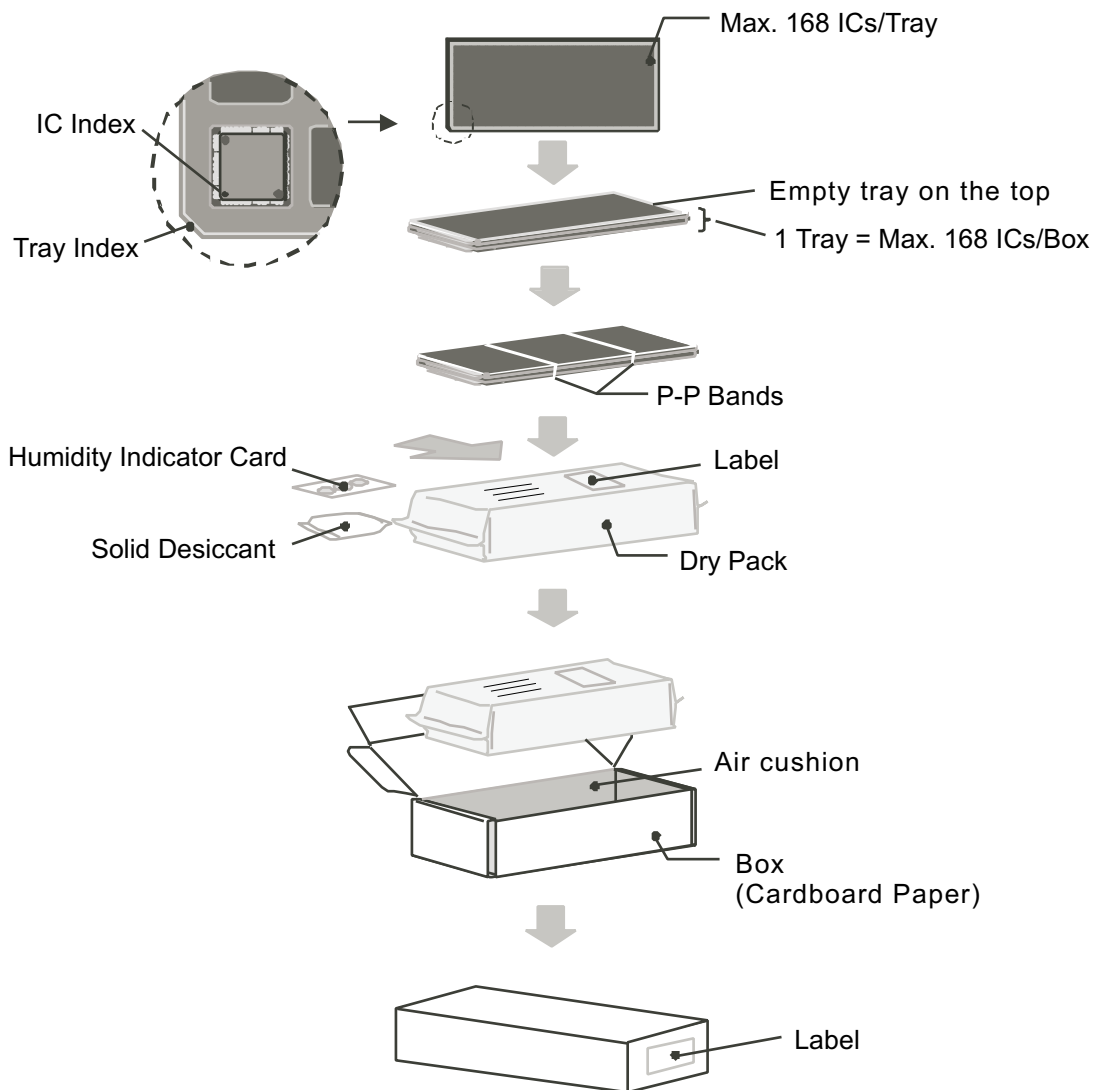
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TITLE	QFN68-B-Markings (S-UM5585)		
No.	QN068-B-M-S2-1.0		
ANGLE			
UNIT		TYPE	LASER
ABLIC Inc.			



No. QN068-B-L-SD-2.0

TITLE	QFN68-B -Land Recommendation
No.	QN068-B-L-SD-2.0
ANGLE	
UNIT	mm
ABLIC Inc.	



No. QN068-B-K-SD-2.0

TITLE	QFN68-B -Packing Procedure
No.	QN068-B-K-SD-2.0
ANGLE	
UNIT	
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