MP9459

17V, 4A, 600kHz, High-Efficiency, Synchronous, Step-Down Converter in an SOT563 Package

DESCRIPTION

The MP9459 is a fully integrated, high-frequency, synchronous, rectified, step-down, switch-mode converter with internal power MOSFETs. The device is a compact solution that achieves 4A of output current over a wide input range with excellent load and line regulation. It uses synchronous mode operation for higher efficiency over the output current load range.

Constant-on-time (COT) control operation provides very fast transient response, easy loop design, and very tight output regulation.

Full protection features include short-circuit protection (SCP), over-current protection (OCP), under-voltage protection (UVP), and thermal shutdown.

The MP9459 requires a minimal number of readily available, standard external components. It is available in a space-saving SOT563 (1.6mmx1.6mm) package.

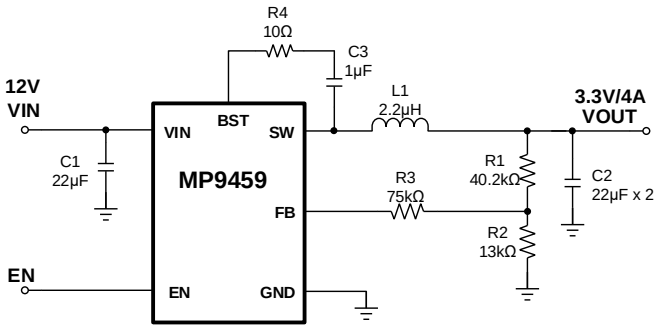
FEATURES

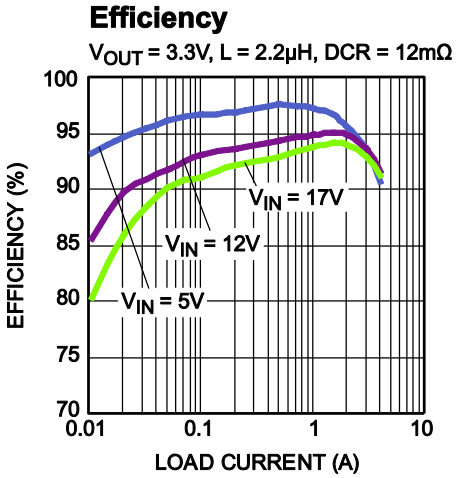
- Wide 4.2V to 17V Operating Input Range
- 60mΩ/30mΩ Low $R_{DS(ON)}$ Internal Power MOSFETs
- 200μA Low Quiescent Current
- High-Efficiency Synchronous Mode Operation
- Power-Save Mode at Light Load
- Fast Load Transient Response
- 600kHz Switching Frequency
- Internal Soft Start (SS)
- Over-Current Protection (OCP) and Hiccup Mode
- Thermal Shutdown
- Output Adjustable from 0.8V
- Available in an SOT563 (1.6mmx1.6mm) Package

APPLICATIONS

- Security Cameras
- Digital Set-Top Boxes
- Flat-Panel Televisions and Monitors
- General Purpose

TYPICAL APPLICATION





ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MP9459GTF	SOT563 (1.6mmx1.6mm)	*See Below*	1

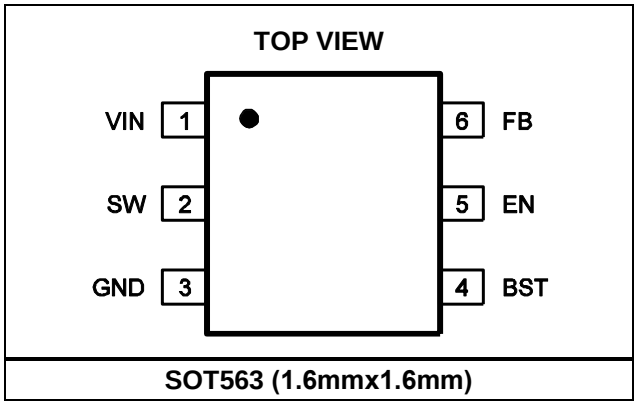
* For Tape & Reel, add suffix –Z (e.g. MP9459GTF–Z).

TOP MARKING

BPDY
LLL

BPD: Product code of MP9459GTF
Y: Year code
LLL: Lot number

PACKAGE REFERENCE



SOT563 (1.6mmx1.6mm)

PIN FUNCTIONS

Pin #	Name	Description
1	VIN	**Supply voltage.** The MP9459 operates from a 4.2V to 17V input rail. A capacitor (C1) is required to decouple the input rail. Connect VIN using a wide PCB trace.
2	SW	**Switch output.** Connect SW using a wide PCB trace.
3	GND	**System ground.** GND is the reference ground of the regulated output voltage. GND requires additional consideration while designing the PCB layout. Connect GND with copper traces and vias.
4	BST	**Bootstrap.** Connect a capacitor and a resistor between SW and BST to form a floating supply across the high-side switch driver. Use a 1µF bootstrap capacitor.
5	EN	**Enable.** Drive EN high to enable the MP9459. For automatic start-up, connect EN to VIN with a 100kΩ pull-up resistor.
6	FB	**Feedback.** To set the output voltage, connect FB to the tap of an external resistor divider from the output to GND. The frequency foldback comparator lowers the oscillator frequency when the FB voltage drops below 600mV. This prevents current-limit runaway during a short-circuit fault.

ABSOLUTE MAXIMUM RATINGS (1)

V_{IN} ..... -0.3V to +18V
V_{SW} ..... -0.6V (-6.5V for <10ns) to V_{IN} + 0.3V (19V for <10ns)
V_{BST} ..... V_{SW} + 5V
V_{EN} ..... -0.3V to +5V (2)
All other pins ..... -0.3V to +5V
Continuous power dissipation (T_A = 25°C) (3) (5) 2.2W
Junction temperature ..... 150°C
Lead temperature ..... 260°C
Storage temperature ..... -65°C to +150°C

ESD Rating

Human-body model (HBM) 2000V
Charged-device model (CDM) 1500V

Recommended Operating Conditions (4)

Supply voltage (V_{IN}) ..... 4.2V to 17V
Output voltage (V_{OUT}) ..... 0.8V to V_{IN} x D_{MAX} or 10V max
Operating junction temp (T_J) .... -40°C to +125°C

Thermal Resistance

SOT563	θ_{JA}	θ_{JC}	
EV9459-TF-00A (5)	55	21	°C/W
JESD51-7 (6)	130	60	°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) For details on EN's ABS max rating, see the Enable (EN) Control section on page 10.
3) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
4) The device is not guaranteed to function outside of its operating conditions.
5) Measured on EV9459-TF-00A, 2-layer PCB.
6) The value of θ_{JA} given in this table is only valid for comparison with other packages, and cannot be used for design purposes. These values were calculated in accordance with JESD51-7, and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application.

ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, T_J = -40°C to +125°C [7], typical value is tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Supply current (shutdown)	I_{IN}	V_{EN} = 0V			10	μA
Supply current (quiescent)	I_Q	V_{EN} = 2V, V_{FB} = 0.85V	170	200	250	μA
HS switch on resistance	$HS_{RDS(ON)}$	V_{BST-SW} = 3.3V		60		mΩ
LS switch on resistance	$LS_{RDS(ON)}$			30		mΩ
Switch leakage	SW_{LKG}	V_{EN} = 0V, V_{SW} = 12V			10	μA
Valley current limit	I_{LIMIT}	V_{OUT} = 0V		5		A
Zero-current detection (ZCD)	I_{ZCD}	V_{OUT} = 3.3V, L_O = 2.2μH, I_{OUT} = 0A	-250	20	+250	mA
Oscillator frequency	f_{SW}	V_{FB} = 0.75V	420	600	780	kHz
Minimum on time [8]	t_{ON_MIN}			45		ns
Minimum off time [8]	t_{OFF_MIN}			180		ns
Feedback voltage	V_{REF}	T_J = 25°C	793	805	817	mV
Feedback current	I_{FB}			10	100	nA
Feedback under-voltage threshold (H to L)	V_{UV_th}	Hiccup entry		75%		V_{REF}
Hiccup duty cycle [8]	D_{Hiccup}			25		%
EN rising threshold	V_{EN_RISING}		1.14	1.2	1.26	V
EN hysteresis	V_{EN_HYS}			100		mV
EN input current	I_{EN}	V_{EN} = 2V		2		μA
VIN under-voltage lockout rising threshold	$INUV_{Vth}$		3.7	4	4.18	V
VIN under-voltage lockout hysteresis threshold	$INUV_{HYS}$			330		mV
Soft-start period	t_{SS}		1.6	2.5	3	ms
Thermal shutdown [8]	TSD			150		°C
Thermal hysteresis [8]	TSD_{HYS}			20		°C

Notes:

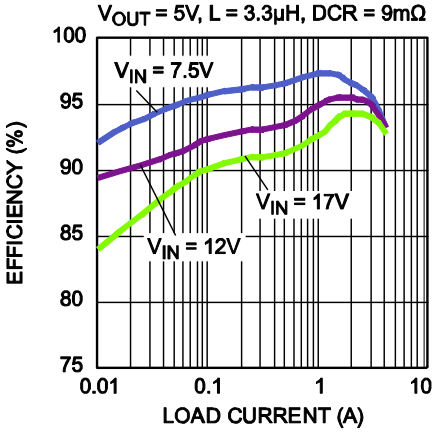
7) Guaranteed by over-temperature correlation. Not tested in production.
8) Guaranteed by design and engineering sample characterization.

TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 12V, V_{OUT} = 3.3V, L = 2.2µH, T_A = 25°C, unless otherwise noted.

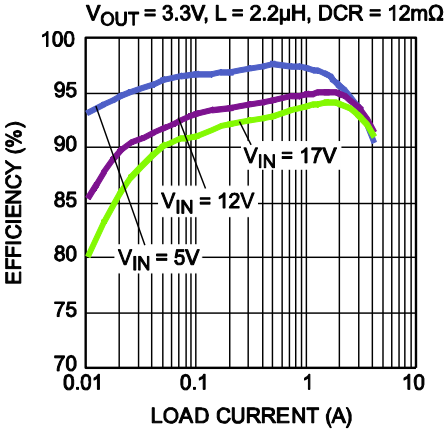
Efficiency

V_{OUT} = 5V, L = 3.3µH, DCR = 9mΩ



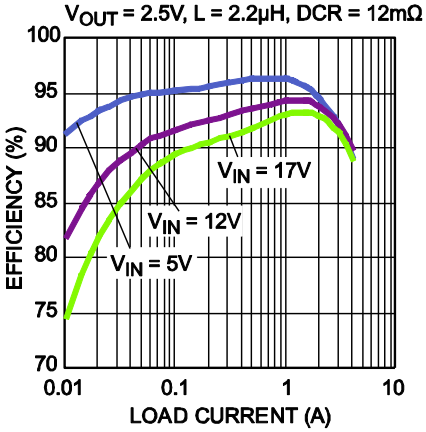
Efficiency

V_{OUT} = 3.3V, L = 2.2µH, DCR = 12mΩ



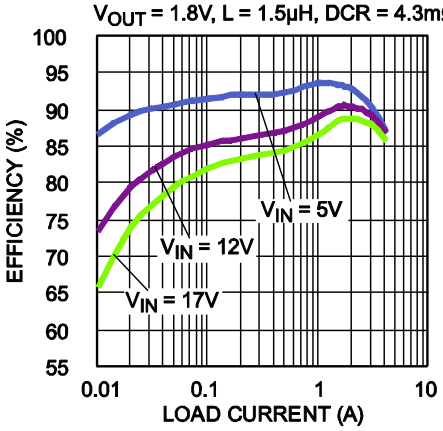
Efficiency

V_{OUT} = 2.5V, L = 2.2µH, DCR = 12mΩ



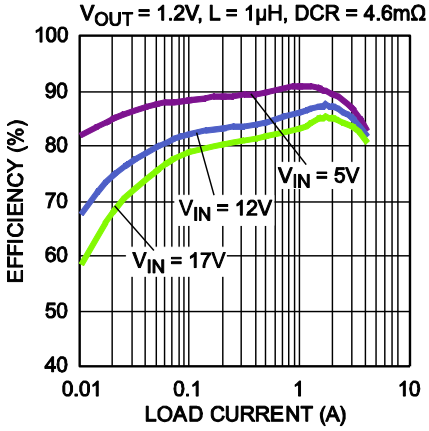
Efficiency

V_{OUT} = 1.8V, L = 1.5µH, DCR = 4.3mΩ



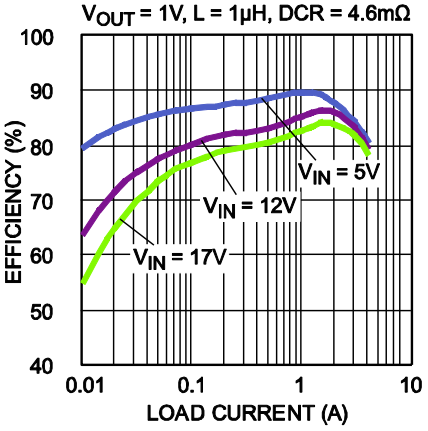
Efficiency

V_{OUT} = 1.2V, L = 1µH, DCR = 4.6mΩ

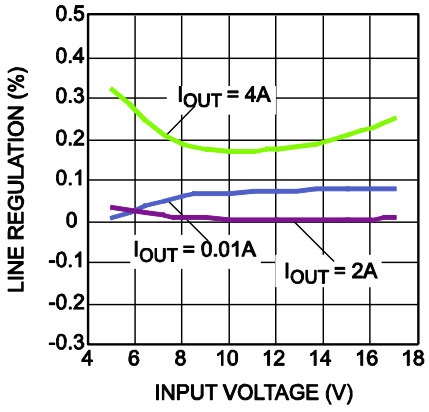


Efficiency

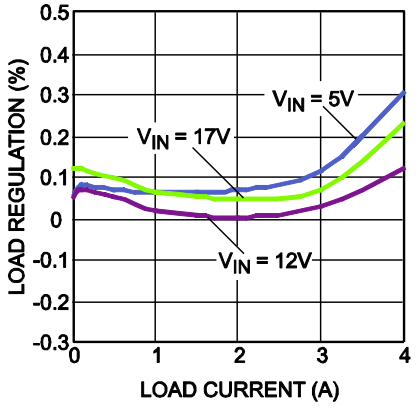
V_{OUT} = 1V, L = 1µH, DCR = 4.6mΩ



Line Regulation

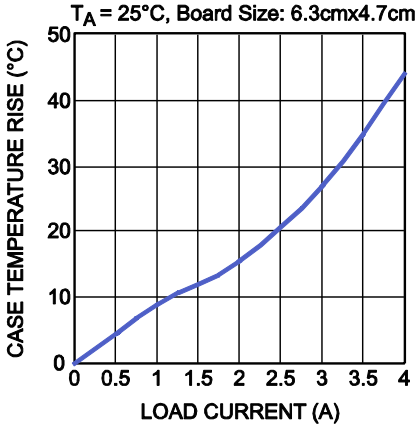


Load Regulation



Case Temperature Rise vs. Load Current

T_A = 25°C, Board Size: 6.3cmx4.7cm

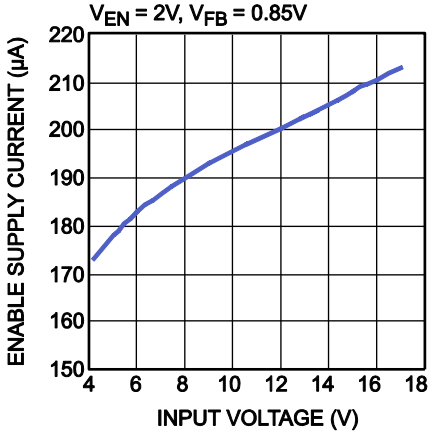


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 3.3V, L = 2.2µH, T_A = 25°C, unless otherwise noted.

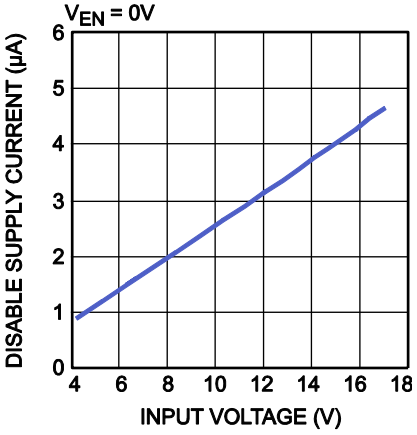
Enable Supply Current vs. Input Voltage

V_{EN} = 2V, V_{FB} = 0.85V



Disable Supply Current vs. Input Voltage

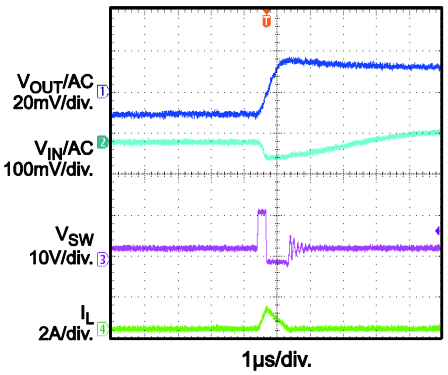
V_{EN} = 0V



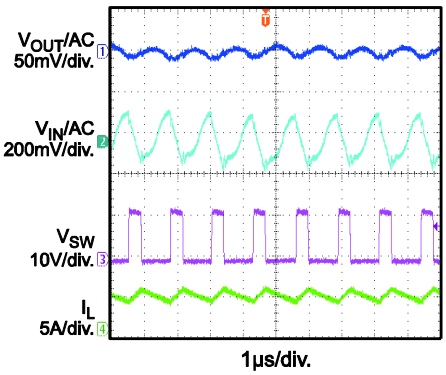
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 3.3V, L = 2.2µH, T_A = 25°C, unless otherwise noted.

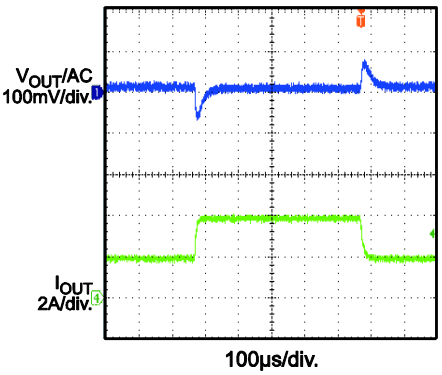
Input/Output Ripple
I_{OUT} = 0A



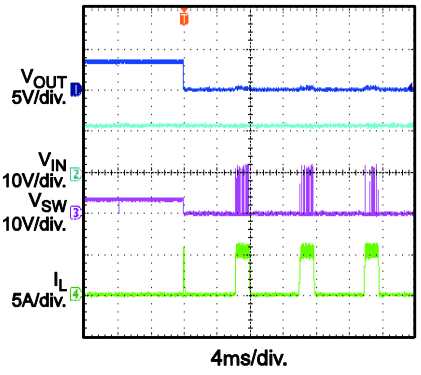
Input/Output Ripple
I_{OUT} = 4A



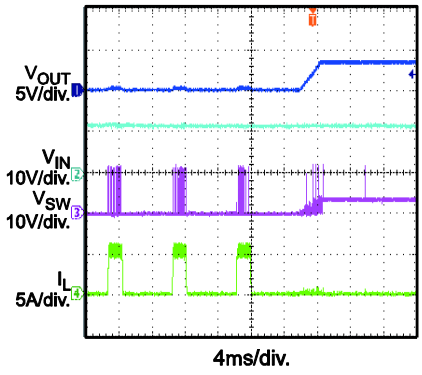
Transient Response
I_{OUT} = 2A to 4A, 2.5A/µs



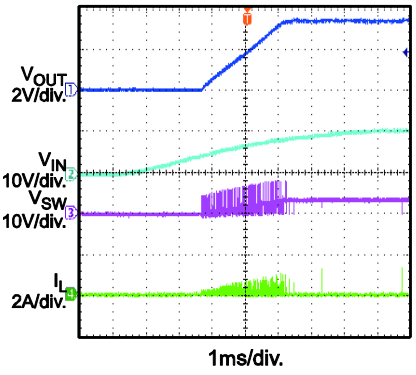
Short-Circuit Entry
I_{OUT} = 0A



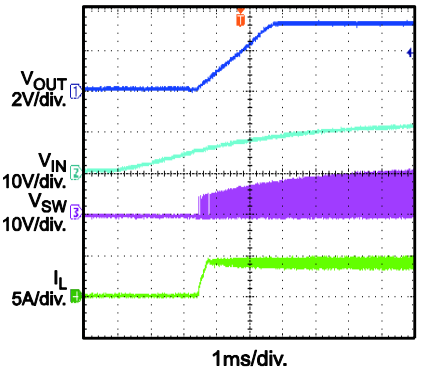
Short-Circuit Recovery
I_{OUT} = 0A



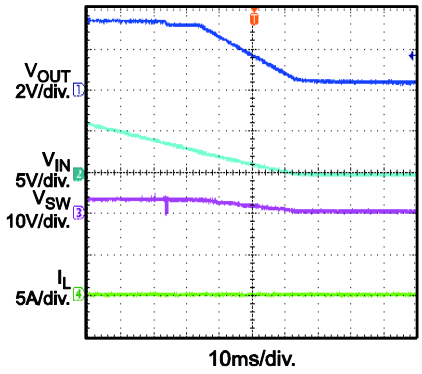
Start-Up through Input Voltage
I_{OUT} = 0A



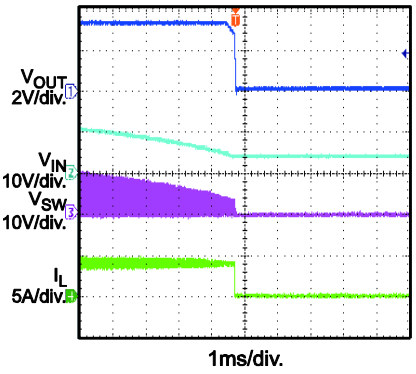
Start-Up through Input Voltage
I_{OUT} = 4A



Shutdown through Input Voltage
I_{OUT} = 0A



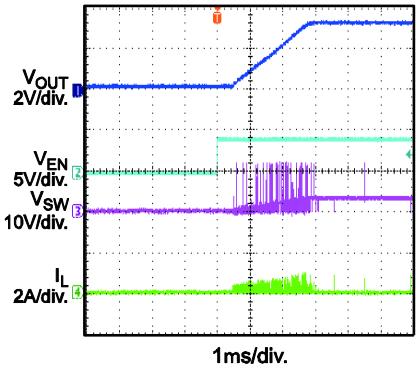
Shutdown through Input Voltage
I_{OUT} = 4A



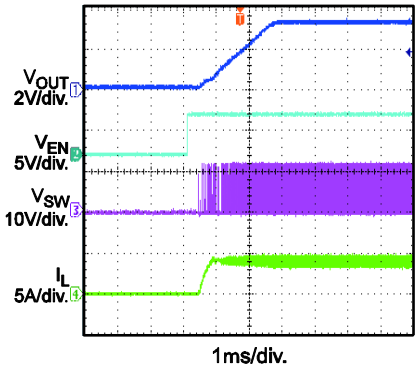
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 3.3V, L = 2.2µH, T_A = 25°C, unless otherwise noted.

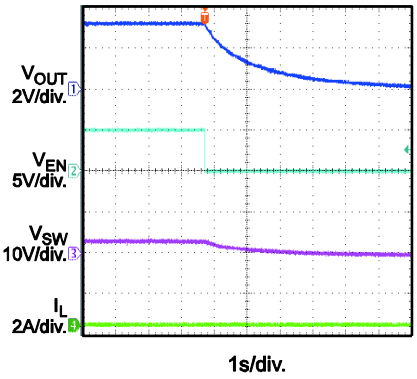
Start-Up through Enable
I_{OUT} = 0A



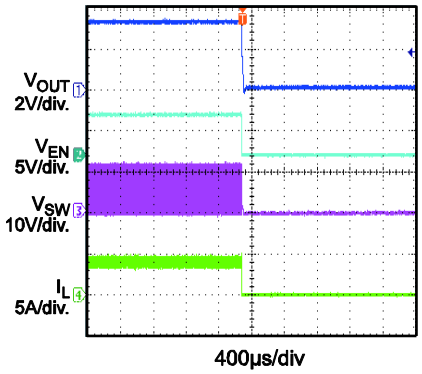
Start-Up through Enable
I_{OUT} = 4A



Shutdown through Enable
I_{OUT} = 0A



Shutdown through Enable
I_{OUT} = 4A



FUNCTIONAL BLOCK DIAGRAM

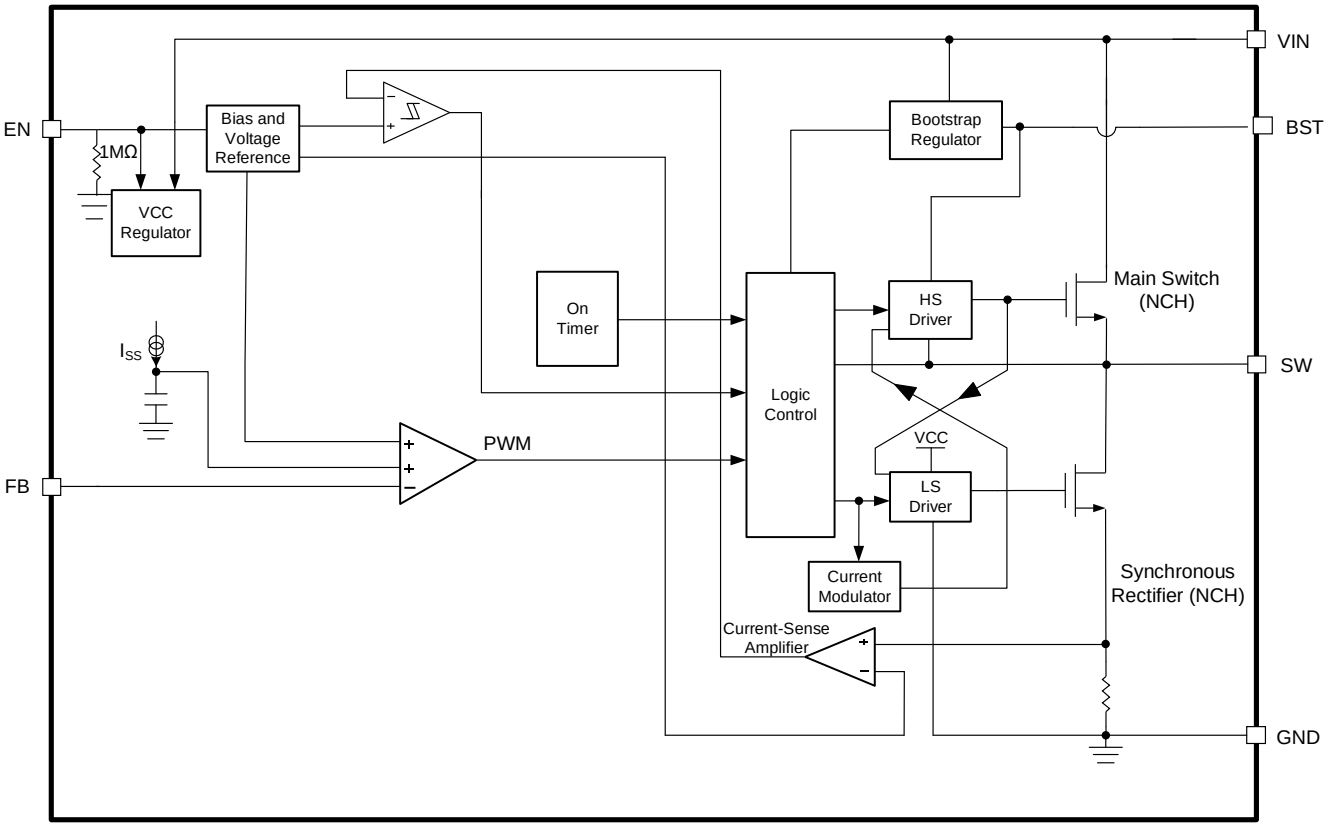


Figure 1: Functional Block Diagram

OPERATION

The MP9459 is a fully integrated, synchronous, rectified, step-down, switch-mode converter. Constant-on-time (COT) control provides fast transient response and eases loop stabilization.

At the beginning of each cycle, the high-side MOSFET (HS-FET) turns on when the feedback voltage (V_{FB}) drops below the reference voltage (V_{REF}). The HS-FET turns on for a fixed interval determined by the one-shot on timer. The on time is determined by both the output voltage and input voltage to maintain a constant switching frequency over the input voltage range.

After the on period elapses, the HS-FET turns off until the next period. By repeating this operation, the converter regulates the output voltage.

Continuous conduction mode (CCM) occurs when the output current is high and the inductor current is above 0A. The low-side MOSFET (LS-FET) turns on when the HS-FET is off to minimize conduction loss. If both the HS-FET and LS-FET are turned on at the same time, there is a dead short between the input and GND. This is called shoot-through. To avoid shoot-through, a dead time is generated internally between the HS-FET off and LS-FET on period, or vice versa.

When the MP9459 works in pulse-frequency modulation (PFM) mode during light-load operation, the device reduces the switching frequency automatically to maintain high efficiency, and the inductor current drops to almost 0A. When the inductor current reaches 0A, the low-side driver goes into tri-state (Hi-Z). Then the output capacitors discharge slowly to GND through resistors R1 and R2. When V_{FB} drops below V_{REF}, the HS-FET turns on. This operation greatly improves device efficiency when the output current is low.

Light-load operation is also called skip mode because the HS-FET does not turn on as frequently as it does during heavy-load conditions. The HS-FET turn-on frequency is a function of the output current. As the output current increases, the current modulator regulates over a shorter period, and the HS-FET turns on more frequently. The switching frequency also increases. The output current (I_{OUT}) reaches the critical level when the current modulator time is zero. I_{OUT} can be calculated with Equation (1):

$$I_{OUT} = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{2 \times L \times f_{SW} \times V_{IN}} \quad (1)$$

The device reverts to pulse-width modulation (PWM) mode once the output current exceeds the critical level. Afterward, the switching frequency remains fairly constant over the output current range.

Enable (EN) Control

EN is a digital control pin that turns the regulator on and off. Drive EN high to turn on the regulator; drive EN low to turn it off. An internal 1MΩ resistor from EN to GND allows EN to be floated to shut down the chip.

EN is clamped internally using a 2.8V series Zener diode (see Figure 2). Connect the EN input to VIN through a pull-up resistor to limit the EN input current below 100μA and prevent damage to the Zener diode.

For example, when connecting 12V to VIN, then $R_{PULLUP} \geq (12V - 2.8V) / (100k\Omega + 35k\Omega) = 68\mu A$.

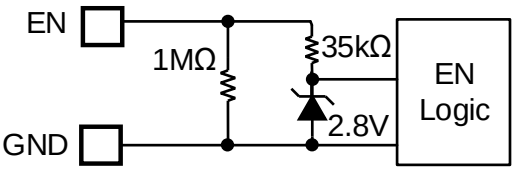


Figure 2: Zener Diode between EN and GND

Under-Voltage Lockout (UVLO)

Under-voltage lockout (UVLO) protects the chip from operating at an insufficient supply voltage. The MP9459's UVLO comparator monitors the output voltage of the internal regulator (VCC). The UVLO rising threshold is about 4V, and its falling threshold is 3.67V.

Internal Soft Start (SS)

Soft start (SS) prevents the converter output voltage from overshooting during start-up. When the chip starts up, the internal circuitry generates an SS voltage (V_{SS}) that ramps up from 0V to 1.2V. When V_{SS} drops below V_{REF},

V_{SS} overrides V_{REF}, so the error amplifier uses V_{SS} as the reference. When V_{SS} exceeds V_{REF}, the error amplifier uses V_{REF} as the reference. The SS time is set internally to 2.5ms.

Over-Current Protection (OCP) and Short-Circuit Protection (SCP)

The MP9459 has valley current limit control. The inductor current is monitored when the LS-FET is on. When the sensed inductor current reaches the valley current limit, the low-side limit comparator turns over, and the device enters over-current protection (OCP) mode. The HS-FET waits until the valley current limit is removed before turning on again. Meanwhile, the output voltage drops until V_{FB} falls below the under-voltage (UV) threshold (about 75% of V_{REF}). Once UV is triggered, the MP9459 enters hiccup mode to periodically restart the part.

During OCP, the device attempts to recover from the over-current fault with hiccup mode. In hiccup mode, the chip disables the output power stage, discharges the soft start, and then automatically attempts to soft start again. If the over-current condition still remains after soft start ends, the device repeats this operation cycle until the over-current condition is removed. Then the output rises back to the regulation level. OCP is a non-latch protection.

Pre-Biased Start-Up

The MP9459 is designed for monotonic start-up into pre-biased loads. If the output is pre-biased to a certain voltage during start-up, the bootstrap (BST) voltage is refreshed and charged, and the soft-start voltage is also charged. If the BST voltage exceeds its rising threshold voltage and the soft-start voltage exceeds the sensed output voltage at FB, the part begins working normally.

Floating Driver and Bootstrap Charging

An external bootstrap capacitor powers the floating power MOSFET driver. This floating driver has its own UVLO protection with a rising threshold of 2.2V and a hysteresis of 150mV. V_{IN} regulates the bootstrap capacitor voltage internally through D1, M1, C3, L1, and C2 (see Figure 3). If V_{IN} - V_{SW} exceeds 3.3V, U1 regulates M1 to maintain a 3.3V BST voltage across C3.

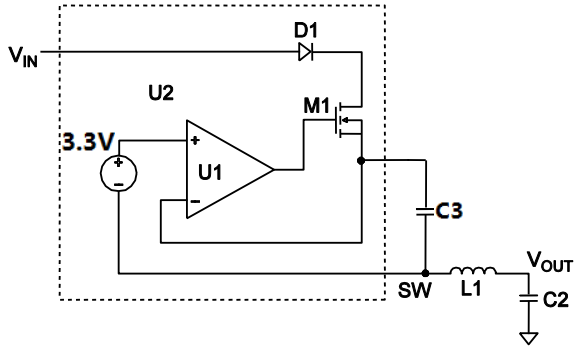


Figure 3: Internal Bootstrap Charger

Start-Up and Shutdown

If both V_{IN} and EN exceed their respective thresholds, the chip starts up. The reference block starts first, generating a stable reference voltage and current, and then the internal regulator is enabled. The regulator provides a stable supply for the remaining circuits.

Three events can shut down the chip: EN going low, V_{IN} going low, and thermal shutdown. The shutdown procedure starts by blocking the signaling path to avoid any fault triggering. The internal supply rail is then pulled down.

Thermal Shutdown

Thermal shutdown prevents the chip from operating at exceedingly high temperatures. When the silicon die temperature exceeds 150°C, the entire chip shuts down. When the temperature falls below its lower threshold (typically 130°C), the chip is enabled again.

APPLICATION INFORMATION

Setting the Output Voltage

The external resistor divider sets the output voltage. First, choose a value for R2. Choose a reasonable R2, since a small R2 leads to a considerable quiescent current loss, while a large R2 makes FB noise-sensitive. R1 can be determined with Equation (2):

$$R1 = \frac{V_{OUT} - V_{REF}}{V_{REF}} \times R2 \quad (2)$$

Figure 4 shows the feedback circuit.

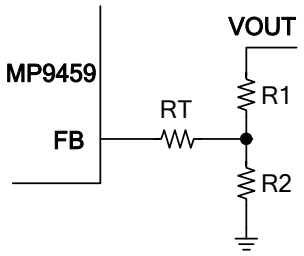


Figure 4: Feedback Network

Table 1 lists the recommended parameters for common output voltages.

Table 1: Parameters for Common Output Voltages (9)

V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)	RT (kΩ)	L (µH)
5	40.2	7.68	75	3.3
3.3	40.2	13	75	2.2
2.5	40.2	19.1	115	2.2
1.8	40.2	32.4	115	1.5
1.5	40.2	45.3	160	1.5
1.2	40.2	82	210	1
1	20.5	84.5	316	1

Note:

9) For a detailed design circuit, see the Typical Application Circuits on pages 15, 16, and 17.

Selecting the Inductor

An inductor is required to supply constant current to the output load while being driven by the switched input voltage. A larger-value inductance results in less ripple current and lower output ripple voltage. However, a larger inductance has a larger physical size, higher series resistance, and lower saturation current. A good rule to determine the inductance value is to design the peak-to-peak ripple current in the inductor to be between 30% and 60% of the maximum output current, and to keep the peak inductor current below the maximum switch current limit. The inductance value can be calculated with Equation (3):

$$L = \frac{V_{OUT}}{f_{SW} \times \Delta I_L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (3)$$

Where ΔI_L is the peak-to-peak inductor ripple current.

The inductor should not saturate under the maximum inductor peak current. The peak inductor current can be calculated with Equation (4):

$$I_{LP} = I_{OUT} + \frac{V_{OUT}}{2f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (4)$$

Selecting the Input Capacitor

The step-down converter has a discontinuous input current, and requires a capacitor to supply AC current to the converter while maintaining the DC input voltage. For the best performance, use ceramic capacitors placed as close to VIN as possible. Capacitors with X5R and X7R ceramic dielectrics are recommended because they are fairly stable amid temperature fluctuations.

The capacitors must also have a ripple current rating that exceeds the converter's maximum input ripple current. The input ripple current can be estimated with Equation (5):

$$I_{CIN} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}})} \quad (5)$$

The worst-case condition occurs at V_{IN} = 2 x V_{OUT}, estimated with Equation (6):

$$I_{CIN} = \frac{I_{OUT}}{2} \quad (6)$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

The input capacitance value determines the input voltage ripple of the converter. If there is an input voltage ripple requirement in the system, choose an input capacitor that meets the specification.

The input voltage ripple can be estimated with Equation (7):

$$\Delta V_{IN} = \frac{I_{OUT}}{f_{SW} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (7)$$

The worst-case condition occurs at V_{IN} = 2 x V_{OUT}, calculated with Equation (8):

$$\Delta V_{IN} = \frac{1}{4} \times \frac{I_{OUT}}{f_{SW} \times C_{IN}} \quad (8)$$

Selecting the Output Capacitor

An output capacitor is required to maintain the DC output voltage. Ceramic or POSCAP capacitors are recommended. The output voltage ripple can be estimated with Equation (9):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times (R_{ESR} + \frac{1}{8 \times f_{SW} \times C_{OUT}}) \quad (9)$$

In the case of ceramic capacitors, the capacitance dominates the impedance at the switching frequency and causes most of the output voltage ripple. For simplification, the output voltage ripple can be calculated with Equation (10):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_{SW}^{2} \times L \times C_{OUT}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (10)$$

The output voltage ripple caused by the ESR is very small.

In the case of POSCAP capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be estimated with Equation (11):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times R_{ESR} \quad (11)$$

A larger output capacitor can improve load transient response, but the maximum output capacitor limitation should also be considered in the design application. If the output capacitance is too high, the output voltage cannot reach the design value during the soft-start time, and the device fails to regulate.

The maximum output capacitor value (C_{O_MAX}) can be estimated with Equation (12):

$$C_{O\_MAX} = (I_{LIM\_AVG} - I_{OUT}) \times t_{ss} / V_{OUT} \quad (12)$$

Where I_{LIM_AVG} is the average start-up current during the soft-start period, and t_{ss} is the soft-start time.

Design Example

Table 2 shows a design example with ceramic capacitors.

Table 2: Design Example

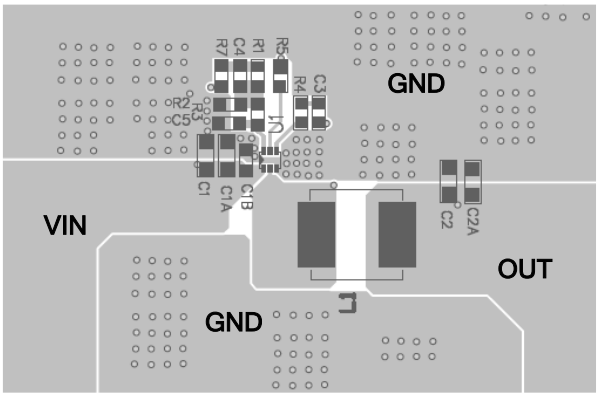
V_{IN}	12V
V_{OUT}	3.3V
I_{OUT}	4A

For detailed application schematics, see the Typical Applications Circuits section on page 15. For typical performance and waveforms, see the Typical Performance Characteristics section on page 5. For more device applications, refer to the related evaluation board datasheet.

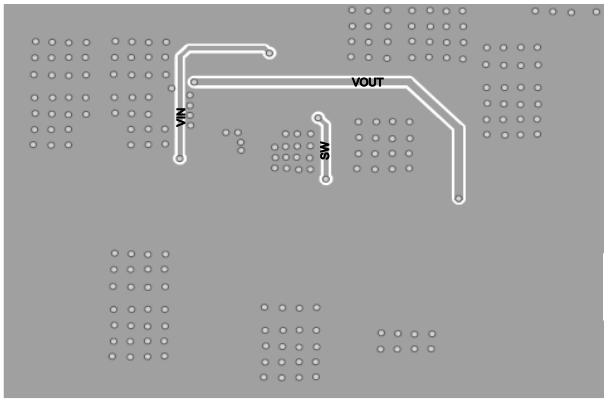
PCB Layout Guidelines

Efficient layout of the switching power supplies is critical for stable operation.Poor layout design can result in poor line or load regulation and stability issues. For the best results, refer to Figure 5 and follow the guidelines below:

1. Place the high current paths (GND, VIN, and SW) very close to the device with short, direct, and wide traces.
2. Place the input capacitor as close to VIN and GND as possible (within 1mm).
3. Place the external feedback resistors next to FB.
4. Keep the switching node (SW) short, and route it away from the feedback network.



Top Layer



Bottom Layer

Figure 5: Recommended PCB Layout

TYPICAL APPLICATION CIRCUITS

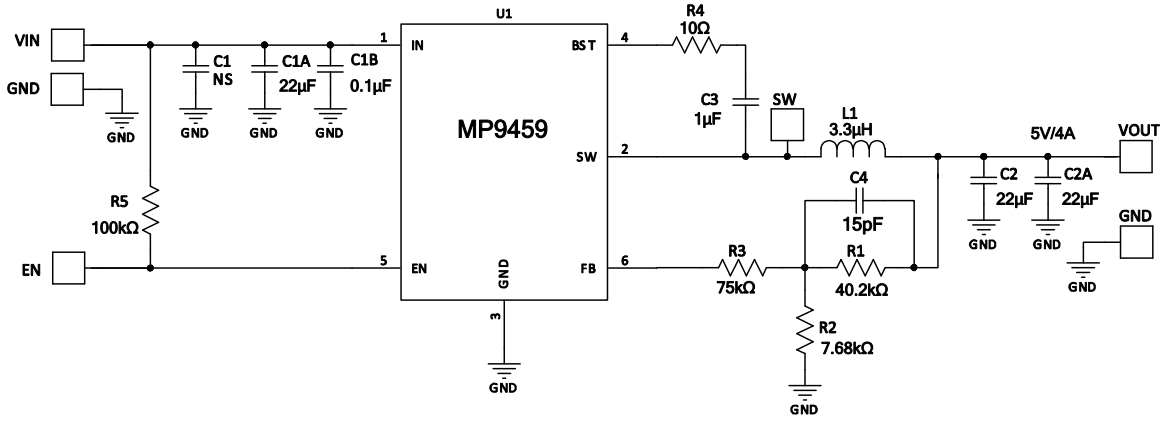


Figure 6: V_{IN} = 12V, V_{OUT} = 5V/4A

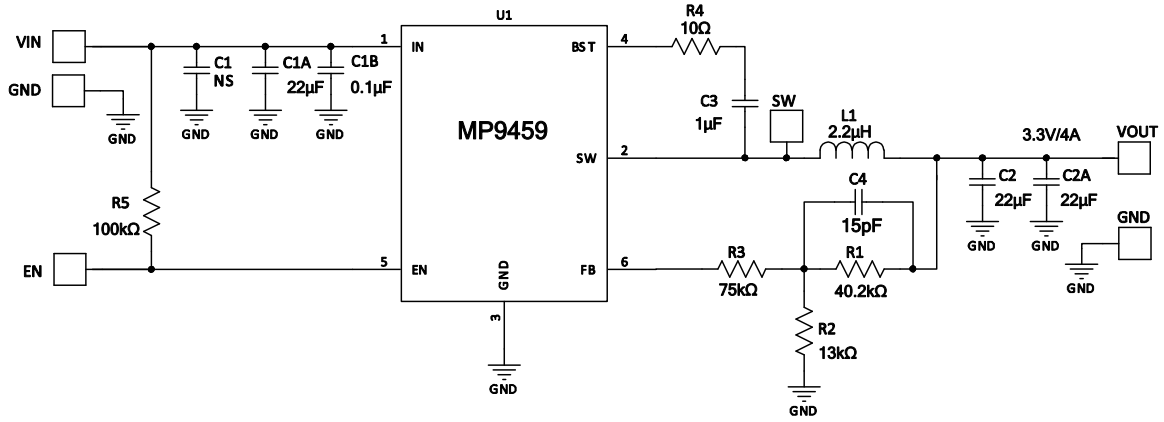


Figure 7: V_{IN} = 12V, V_{OUT} = 3.3V/4A

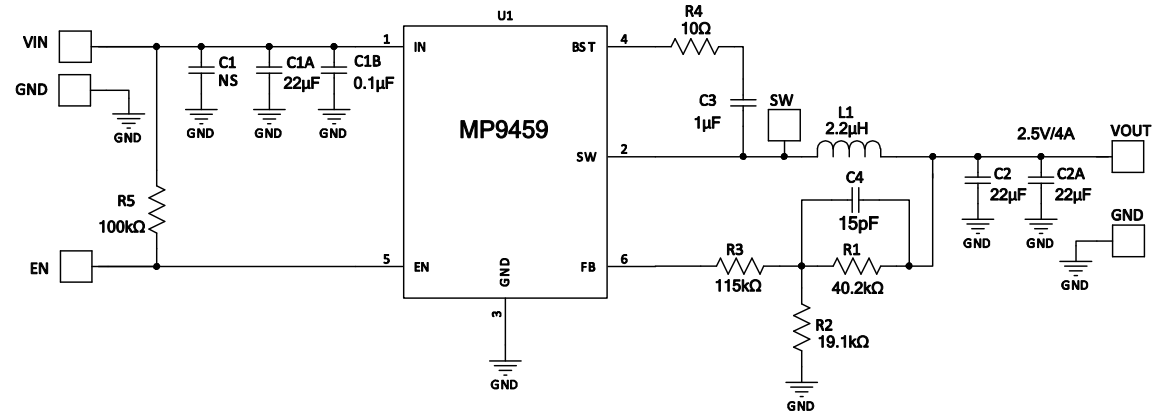


Figure 8: V_{IN} = 12V, V_{OUT} = 2.5V/4A

TYPICAL APPLICATION CIRCUITS *(continued)*

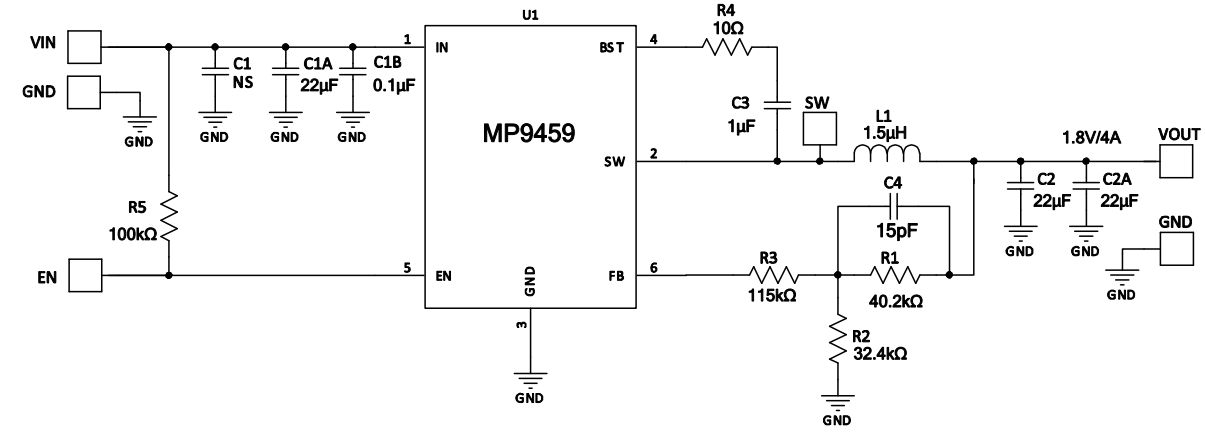


Figure 9: V_{IN} = 12V, V_{OUT} = 1.8V/4A

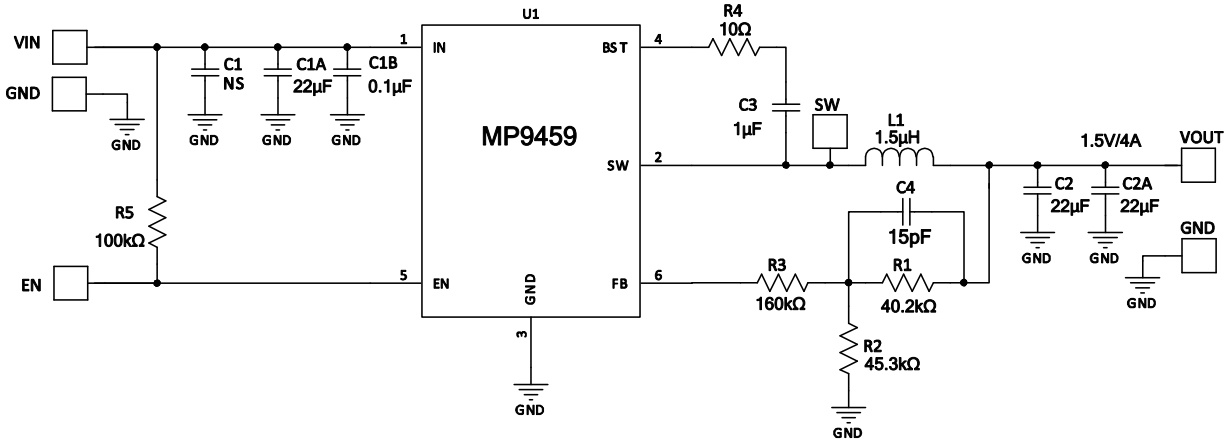


Figure 10: V_{IN} = 12V, V_{OUT} = 1.5V/4A

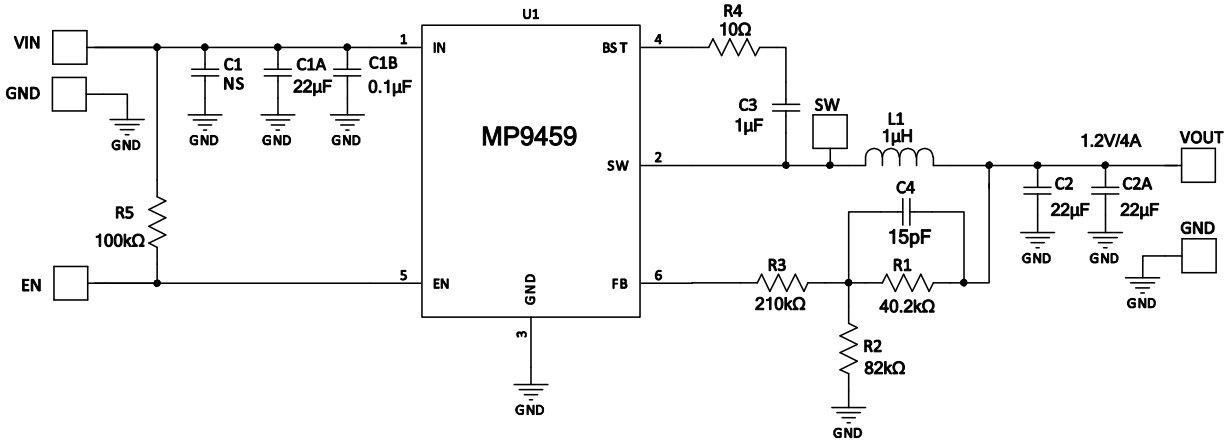


Figure 11: V_{IN} = 12V, V_{OUT} = 1.2V/4A

TYPICAL APPLICATION CIRCUITS *(continued)*

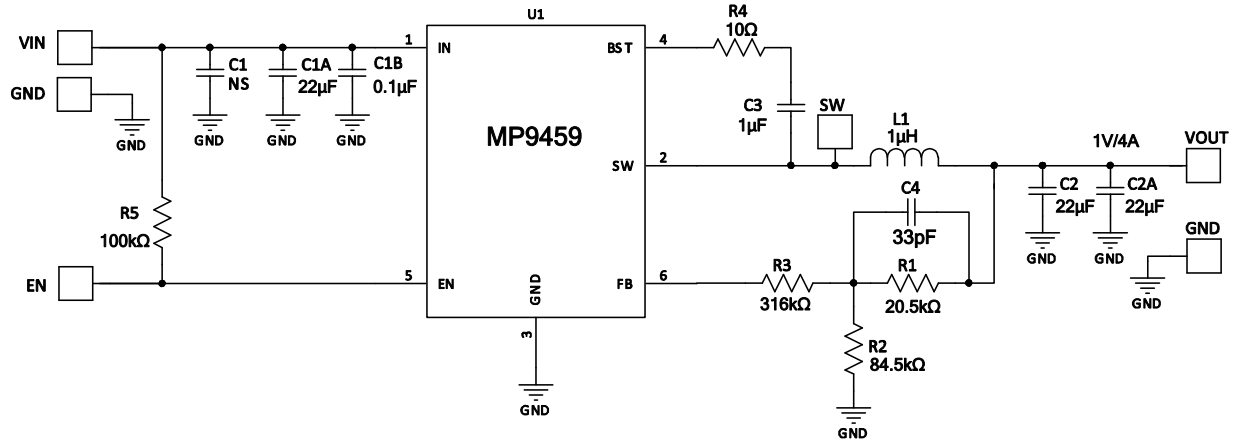
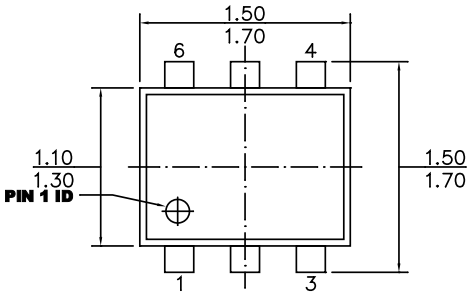


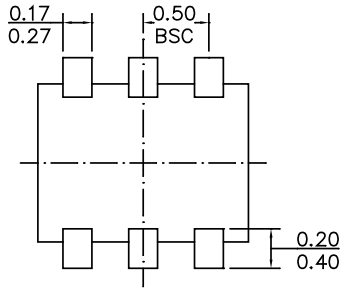
Figure 12: V_{IN} = 12V, V_{OUT} = 1V/4A

PACKAGE INFORMATION

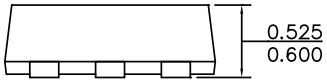
SOT563 (1.6mmx1.6mm)



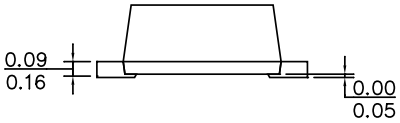
TOP VIEW



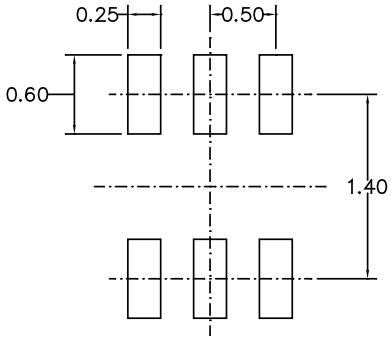
BOTTOM VIEW



FRONT VIEW



SIDE VIEW

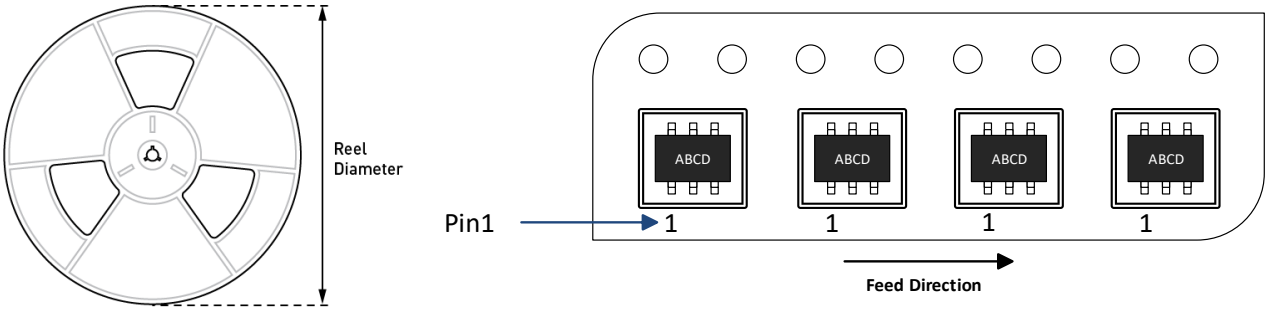


RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION, OR GATE BURR.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
5) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION



Part Number	Package Description	Quantity/Reel	Quantity/Tube	Quantity/Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP9459GTF	SOT563 (1.6mmx1.6mm)	5000	N/A	N/A	7in	8mm	4mm