LM74703-Q1, LM74704-Q1 Ideal Diode Controller with External FET Health Indication

1 Features

- AEC-Q100 qualified with the following results
  - Device temperature grade 1: –40°C to +125°C ambient operating temperature range
- 3.2-V to 65-V input range (3.9-V start up)
- –65-V reverse voltage rating
- Charge pump for external N-Channel MOSFET
- 20-mV ANODE to CATHODE forward voltage drop regulation
- Enable pin feature
- 1-µA shutdown current (EN=Low)
- 80-µA operating quiescent current (EN=High)
- 2.3-A peak gate turnoff current
- FETGOOD output to indicate external MOSFET health status
- Fast response to reverse current blocking: < 0.75 µs
- Meets automotive ISO7637 transient requirements with a suitable TVS Diode
- 8-pin SOT-23 Package 2.90 mm × 1.60 mm

2 Applications

- Automotive ADAS systems - camera
- Automotive infotainment systems - digital cluster, head unit
- Body electronics and lighting
- Active ORing for redundant power

3 Description

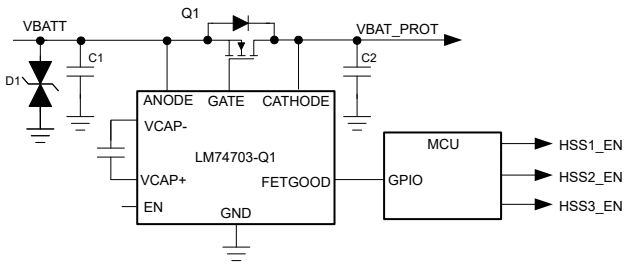
The LM74703-Q1, LM74704-Q1 is an automotive AEC Q100 qualified ideal diode controller which operates in conjunction with an external N-channel MOSFET as an ideal diode rectifier for low loss reverse polarity protection with a 20-mV forward voltage drop. The wide supply input range of 3.2 V to 65 V allows control of many popular DC bus voltages such as 12-V, 24-V, and 48-V automotive battery systems. The 3.2-V input voltage support is particularly well suited for severe cold crank requirements in automotive systems. The device can withstand and protect the loads from negative supply voltages down to –65 V.

The device controls the GATE of the MOSFET to regulate the forward voltage drop at 20 mV. The regulation scheme enables graceful turn off of the MOSFET during a reverse current event and ensures zero DC reverse current flow. Fast response (< 0.75 µs) to reverse current blocking makes the device suitable for systems with output voltage holdup requirements during ISO7637 pulse testing as well as power fail and input micro-short conditions. LM74703-Q1, LM74704-Q1 has FETGOOD output to indicate external MOSFET drain to source short or open condition. The device features enable pin (EN). With the enable pin low, the controller is off and draws approximately 1 µA of current.

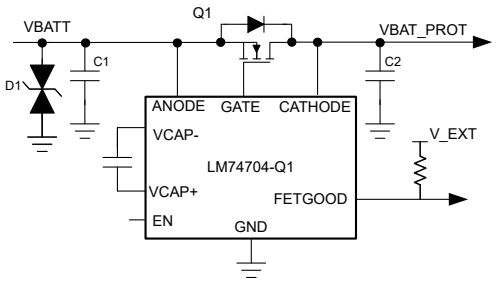
Package Information

PART NUMBER	PACKAGE(1)	BODY SIZE (NOM)
LM74703-Q1	DDF (SOT-23, 8)	2.90 mm × 1.60 mm
LM74704-Q1		

(1) For all available packages, see the orderable addendum at the end of the data sheet.



LM74703-Q1 Typical Application Schematic



LM74704-Q1 Typical Application Schematic

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
May 2023	*	Initial Release

5 Device Comparison Table

	LM74703-Q1	LM74704-Q1
FETGOOD Output Type	Push-Pull Output	Open-Drain Output

6 Pin Configuration and Functions

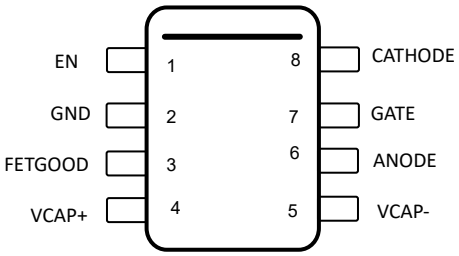

Figure 6-1. DDF Package, 8-Pin SOT-23 (Top View)

Table 6-1. Pin Functions

PIN		I/O(1)	DESCRIPTION
NO.	NAME		
1	EN	I	Enable pin. Can be connected to ANODE for always ON operation.
2	GND	G	Ground pin.
3	FET_GOOD	O	External MOSFET status indicator. LM74703-Q1 has push-pull while LM74704-Q1 has open drain FET_GOOD output.
4	VCAP+	O	Charge pump output. Connect to external charge pump capacitor between VCAP+ and VCAP-.
5	VCAP-	I	Charge pump capacitor reference input.
6	ANODE	I	Anode of the diode and input power. Connect to the source of the external N-channel MOSFET.
7	GATE	O	Gate drive output. Connect to gate of the external N-channel MOSFET.
8	CATHODE	I	Cathode of the diode. Connect to the drain of the external N-channel MOSFET.

(1) I = Input, O = Output, G = GND

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7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Input Pins	ANODE, VCAP– to GND	–65	65	V
	EN to GND, $V_{(ANODE)}$ > 0 V	–0.3	65	V
	EN to GND, $V_{(ANODE)}$ ≤ 0 V	$V_{(ANODE)}$	(65 + $V_{(ANODE)}$)	V
Output Pins	FET_GOOD to GND	–0.3	80	V
Output Pins	I_{FET_GOOD}		1	mA
Output Pins	GATE to ANODE	–0.3	15	V
	VCAP+ to VCAP–, ANODE	–0.3	15	V
Output to Input Pins	CATHODE to ANODE	–5	75	V
Operating junction temperature(2)		–40	150	°C
Storage temperature, T_{stg}		–40	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) High junction temperatures degrade operating lifetimes. Operating lifetime is de-rated for junction temperatures greater than 125°C.

7.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1)		±2000	V
		Charged device model (CDM), per AEC Q100-011	Corner pins (EN, VCAP+, VCAP- CATHODE)	±750	
			Other pins	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	NOM	MAX	UNIT
Input Pins	ANODE, VCAP– to GND	–60		60	V
	CATHODE to GND			60	
	EN to GND	–60		60	
Input to Output pins	ANODE to CATHODE	–70			V
External capacitance	ANODE	22			nF
	CATHODE to GND, VCAP+ to VCAP–	0.1			µF
External MOSFET max V_{GS} rating	GATE to ANODE	15			V
T_J	Operating junction temperature range(2)	–40		150	°C

(1) Recommended Operating Conditions are conditions under which the device is intended to be functional. For specifications and test conditions, see *Electrical Characteristics*.
(2) High junction temperatures degrade operating lifetimes. Operating lifetime is de-rated for junction temperatures greater than 125°C.

7.4 Thermal Information

THERMAL METRIC[1]		LM74703-Q1, LM74704-Q1 DDF (SOT) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	133.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	72.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	54.5	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	4.6	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	54.2	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report, SPRA953.

7.5 Electrical Characteristics

T_J = –40°C to +125°C; typical values at T_J = 25°C, $V_{(ANODE)}$ = 12 V, $C_{(VCAP+)}$ = 0.1 µF, $V_{(EN)}$ = 3.3 V, over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{ANODE} SUPPLY VOLTAGE						
$V_{(ANODE)}$	Operating input voltage		4		60	V
$V_{(ANODE\ POR)}$	VANODE POR Rising threshold			3.9		V
	VANODE POR Falling threshold			2.8		V
$I_{(SHDN)}$	Shutdown Supply Current	$V_{(EN)}$ = 0 V		1		µA
$I_{(Q)}$	Operating Quiescent Current			80		µA
ENABLE INPUT						
$V_{(EN\_IL)}$	Enable input low threshold			0.9		V
$V_{(EN\_IH)}$	Enable input high threshold			2		
$I_{(EN)}$	Enable sink current	$V_{(EN)}$ = 12 V		3		µA
FET GOOD						
FET_GOOD High	FET GOOD voltage for Logic High	VCAP> VCAP_UVLO, V_{ANODE} – $V_{CATHODE}$ < 200 mV, LM74703-Q1		5.2		V
$R_{FET\_GOOD(Pull-Up)}$	FET_GOOD pull up resistor	VCAP> VCAP_UVLO & V_{ANODE} – $V_{CATHODE}$ < 200 mV, LM74703-Q1		50		kΩ
$R_{FET\_GOOD(Pull-Down)}$	FET_GOOD pull down resistor	VCAP < VCAP_UVLO || V_{ANODE} – $V_{CATHODE}$ > 200 mV, LM74703-Q1		50		kΩ
$R_{FET\_GOOD(Pull-Down)}$	FET_GOOD pull down resistor	VCAP < VCAP_UVLO || V_{ANODE} – $V_{CATHODE}$ > 200mV, LM74704-Q1		1		kΩ
FET_GOOD Comparator	V_{AC} comparator rising threshold for FETGOOD going low	EN=High, VA=12V		200		mV
FET_GOOD Comparator	V_{AC} comparator falling threshold for FETGOOD going high	EN=High, VA=12V		185		mV
FET_GOOD Comparator Hyst				15		mV
V_{ANODE} to $V_{CATHODE}$						
$V_{(AK\ REG)}$	Regulated Forward $V_{(AC)}$ Threshold			20		mV
$V_{(AK)}$	$V_{(AC)}$ threshold for full conduction mode			50		mV
$V_{(AK\ REV)}$	$V_{(AC)}$ threshold for reverse current blocking			–11		mV
GATE DRIVE						

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T_J = –40°C to +125°C; typical values at T_J = 25°C, $V_{(ANODE)}$ = 12 V, $C_{(VCAP+)}$ = 0.1 µF, $V_{(EN)}$ = 3.3 V, over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{(GATE)}$	Peak source current	$V_{(ANODE)} - V_{(CATHODE)}$ = 100 mV, $V_{(GATE)} - V_{(ANODE)}$ = 5 V		11		mA
	Peak sink current	$V_{(ANODE)} - V_{(CATHODE)}$ = –20 mV, $V_{(GATE)} - V_{(ANODE)}$ = 5 V		2370		mA
	Regulation max sink current	$V_{(ANODE)} - V_{(CATHODE)}$ = 0 V, $V_{(GATE)} - V_{(ANODE)}$ = 5 V		26		µA
RDS_{ON}	discharge switch RDS_{ON}	$V_{(ANODE)} - V_{(CATHODE)}$ = –20 mV, $V_{(GATE)} - V_{(ANODE)}$ = 100 mV		2		Ω
CHARGE PUMP						
$I_{(VCAP)}$	Charge Pump source current (Charge pump on)	$V_{(VCAP+)} - V_{(VCAP–)}$ = 7 V		300		µA
	Charge Pump sink current (Charge pump off)	$V_{(VCAP+)} - V_{(VCAP–)}$ = 14 V		5		µA
$V_{(VCAP+)} - V_{(VCAP–)}$	Charge pump voltage at $V_{(ANODE)}$ = 3.2 V	$I_{(VCAP)}$ ≤ 30 µA		8		V
	Charge pump turn on voltage			12.1		V
	Charge pump turn off voltage			13		V
	Charge Pump Enable comparator Hysteresis			0.9		V
$V_{(VCAP\ UVLO)}$	$V_{(VCAP)} - V_{(ANODE)}$ UV release at rising edge	$V_{(ANODE)} - V_{(CATHODE)}$ = 100 mV		6.6		V
	$V_{(VCAP)} - V_{(ANODE)}$ UV threshold at falling edge	$V_{(ANODE)} - V_{(CATHODE)}$ = 100 mV		5.68		V
CATHODE						
$I_{(CATHODE)}$	CATHODE sink current	$V_{(ANODE)}$ = 12 V, $V_{(ANODE)} - V_{(CATHODE)}$ = –100 mV		1.7		µA
		$V_{(ANODE)} - V_{(CATHODE)}$ = –100 mV		1.2		µA
		$V_{(ANODE)}$ = –12 V, $V_{(CATHODE)}$ = 12 V		1.25		µA

7.6 Switching Characteristics

T_J = –40°C to +125°C; typical values at T_J = 25°C, $V_{(ANODE)}$ = 12 V, $C_{(VCAP+)}$ = 0.1 µF, $V_{(EN)}$ = 3.3 V, over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
EN_{TDLY}	Enable (low to high) to Gate Turn On delay	$V_{(VCAP)} > V_{(VCAP\ UVLOR)}$		100		µs
$t_{Reverse\ delay}$	Reverse voltage detection to Gate Turn Off delay	$V_{(ANODE)} - V_{(CATHODE)}$ = 100 mV to –100 mV		0.5		µs
$t_{Forward\ recovery}$	Forward voltage detection to Gate Turn On delay	$V_{(ANODE)} - V_{(CATHODE)}$ = –100 mV to 700 mV		1.4		µs
$t_{FET\_GOOD\_ASSERT(DLY)}$	FET GOOD assert delay	$V_{ANODE} - V_{CATHODE}$ > 200 mV or VCAP < VCAP_UVLO to FET_GOOD going low		40		us
$t_{FET\_GOOD\_DEASSERT(DLY)}$	FET GOOD de-assert delay	$V_{ANODE} - V_{CATHODE}$ < 200 mV & VCAP > VCAP_UVLO to FET_GOOD going High		5		us

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8 Detailed Description

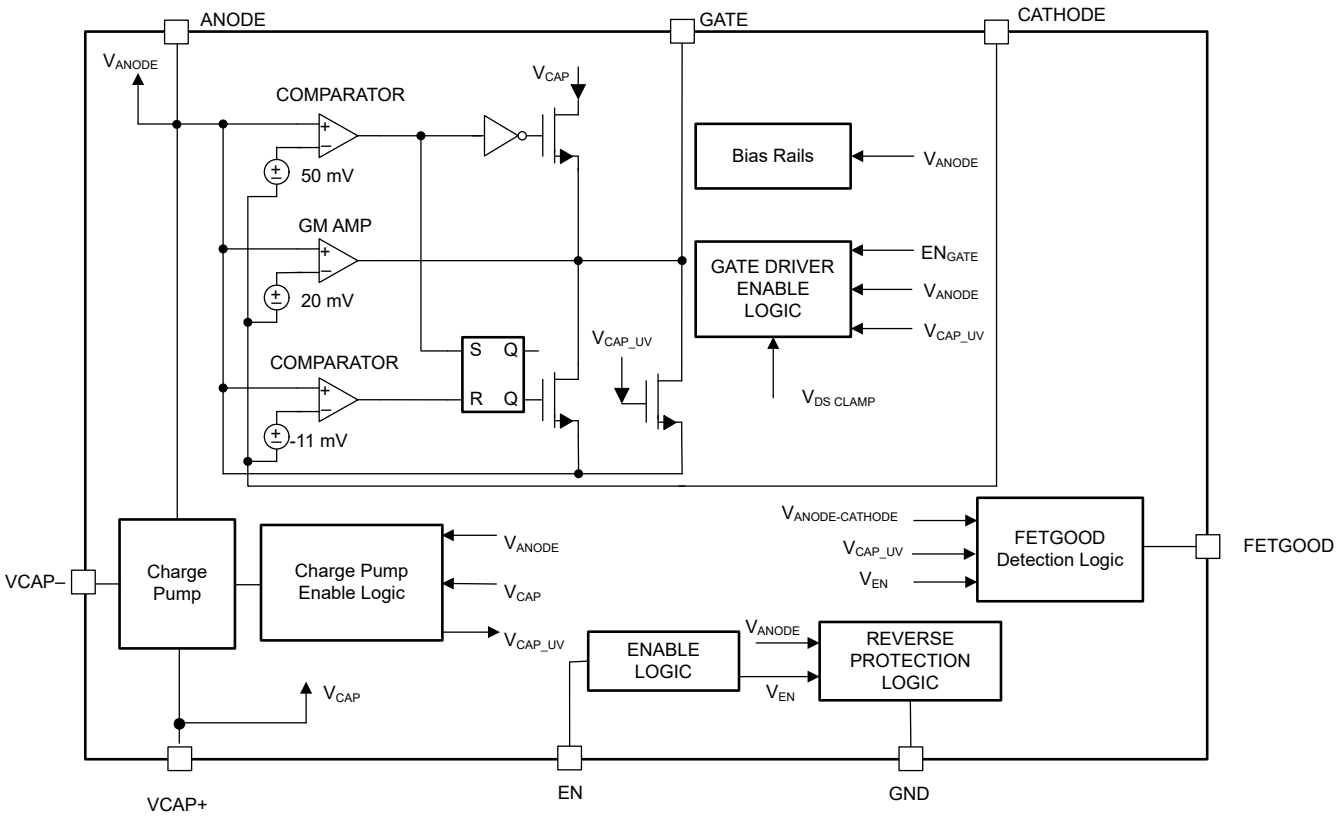
8.1 Overview

The LM74703-Q1, LM74704-Q1 ideal diode controller has all the features necessary to implement an efficient and fast reverse polarity protection circuit or be used in an ORing configuration while minimizing the number of external components. This easy to use ideal diode controller is paired with an external N-channel MOSFET to replace other reverse polarity schemes such as a P-channel MOSFET or a Schottky diode. An internal charge pump is used to drive the external N-Channel MOSFET to a maximum gate to source drive voltage of approximately 12 V. The voltage drop across the MOSFET is continuously monitored between the ANODE and CATHODE pins, and the GATE to ANODE voltage is adjusted as needed to regulate the forward voltage drop at 20 mV. This closed loop regulation scheme enables graceful turn off of the MOSFET during a reverse current event and ensures zero DC reverse current flow. A fast reverse current condition is detected when the voltage across ANODE and CATHODE pins reduces below –11 mV , resulting in the GATE pin being internally connected to the ANODE pin turning off the external N-channel MOSFET, and using the body diode to block any of the reverse current. An enable pin, EN is available to place the LM74703-Q1 in shutdown mode disabling the N-Channel MOSFET and minimizing the quiescent current.

LM74703-Q1, LM74704-Q1 offers external FET health monitoring feature with FETGOOD pin. Device monitors for external FET drain to source short or open condition during power-up and pulls the FETGOOD pin low in case external FET fault condition is diagnosed.

For automotive applications such as automotive lighting, Camera modules which are exterior facing usually require low conducted and radiated emissions in the frequency band ranging up to 1-GHz. LM74703-Q1, LM74704-Q1 offers extremely lower emissions in high frequency band (108 MHz to 1 GHz) making it an attractive candidate for applications where high frequency emissions is a key care about.

8.2 Functional Block Diagram



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8.3 Feature Description

8.3.1 Input Voltage

The ANODE pin is used to power the LM74703-Q1's internal circuitry, typically drawing 80 µA when enabled and 1 µA when disabled. If the ANODE pin voltage is greater than the POR Rising threshold, then LM74703-Q1 operates in either shutdown mode or conduction mode in accordance with the EN pin voltage. The voltage from ANODE to GND is designed to vary from 65 V to –65 V, allowing the LM74703-Q1 to withstand negative voltage transients.

8.3.2 Charge Pump

The charge pump supplies the voltage necessary to drive the external N-channel MOSFET. An external charge pump capacitor is placed between VCAP+ and VCAP– pins to provide energy to turn on the external MOSFET. In order for the charge pump to supply current to the external capacitor the EN pin voltage must be above the specified input high threshold, $V_{(EN\_IH)}$. When enabled the charge pump sources a charging current of 300-µA typical. If EN pins is pulled low, then the charge pump remains disabled. To ensure that the external MOSFET can be driven above its specified threshold voltage, the VCAP+ to VCAP–voltage must be above the undervoltage lockout threshold, typically 6.6 V, before the internal gate driver is enabled. Use Equation 1 to calculate the initial gate driver enable delay.

$$T_{(DRV\_EN)} = 75\mu s + C_{(VCAP)} x \frac{V_{(VCAP\_UVLOR)}}{300\mu A} \quad (1)$$

where

- $C_{(VCAP)}$ is the charge pump capacitance connected across ANODE and VCAP pins
- $V_{(VCAP\_UVLOR)}$ = 6.6 V (typical)

To remove any chatter on the gate drive approximately 900 mV of hysteresis is added to the VCAP undervoltage lockout. The charge pump remains enabled until the VCAP+ to VCAP–voltage reaches 13 V, typically, at which point the charge pump is disabled decreasing the current drawn on the ANODE pin. The charge pump remains disabled until the VCAP+ to VCAP–voltage is below to 12.1 V typically at which point the charge pump is enabled. The voltage between VCAP+ to VCAP– continue to charge and discharge between 12.1 V and 13 V as shown in Figure 8-1. By enabling and disabling the charge pump, the operating quiescent current of the LM74703-Q1 is reduced. When the charge pump is disabled it sinks 5-µA typical.

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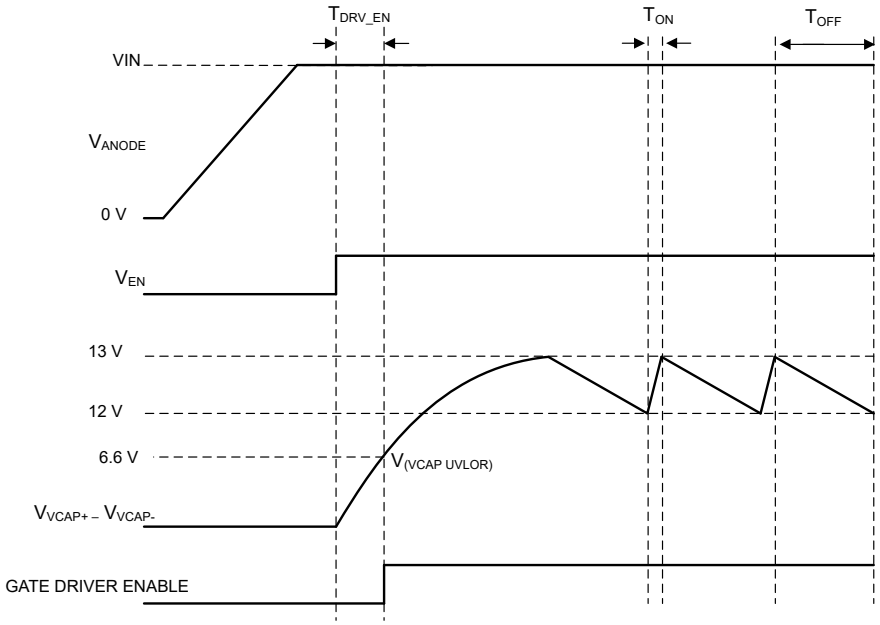

Figure 8-1. Charge Pump Operation

8.3.3 Gate Driver

The gate driver is used to control the external N-Channel MOSFET by setting the GATE to ANODE voltage to the corresponding mode of operation. There are three defined modes of operation that the gate driver operates under forward regulation, full conduction mode and reverse current protection, according to the ANODE to CATHODE voltage. Forward regulation mode, full conduction mode and reverse current protection mode are described in more detail in the *Regulated conduction Mode*, *Full Conduction Mode* and *Reverse Current Production Mode* sections. Figure 8-2 depicts how the modes of operation vary according to the ANODE to CATHODE voltage of the LM74703-Q1. The threshold between forward regulation mode and conduction mode is when the ANODE to CATHODE voltage is 50 mV. The threshold between forward regulation mode and reverse current protection mode is when the ANODE to CATHODE voltage is –11 mV.

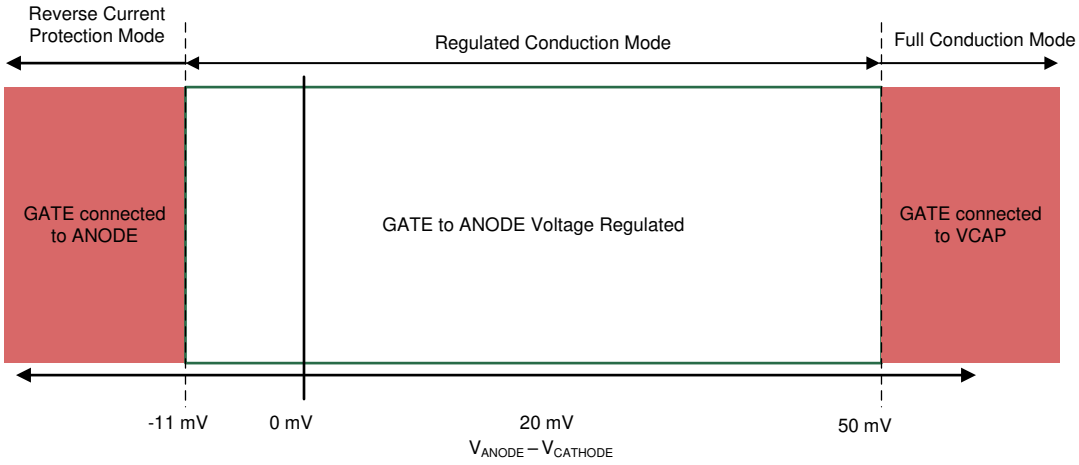

Figure 8-2. Gate Driver Mode Transitions

Before the gate driver is enabled following three conditions must be achieved:

- The EN pin voltage must be greater than the specified input high voltage.
- The VCAP+ to VCAP– voltage must be greater than the undervoltage lockout voltage.
- The ANODE voltage must be greater than VANODE POR Rising threshold.

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If the above conditions are not achieved, then the GATE pin is internally connected to the ANODE pin, assuring that the external MOSFET is disabled. Once these conditions are achieved the gate driver operates in the correct mode depending on the ANODE to CATHODE voltage.

8.3.4 Enable

The LM74703-Q1 has an enable pin, EN. The enable pin allows for the gate driver to be either enabled or disabled by an external signal. If the EN pin voltage is greater than the rising threshold, the gate driver and charge pump operates as described in *Gate Driver* and *Charge Pump* sections. If the enable pin voltage is less than the input low threshold, the charge pump and gate driver are disabled placing the LM74703-Q1 in shutdown mode. The EN pin can withstand a voltage as large as 65 V and as low as –65 V. This allows for the EN pin to be connected directly to the ANODE pin if enable functionality is not needed. In conditions where EN is left floating, the internal sink current of 3 uA pulls EN pin low and disables the device.

8.3.5 FET Status Indication (FETGOOD)

LM74703-Q1, LM74704-Q1 has FETGOOD pin which can be used to detect external MOSFET health such as MOSFET is VDS short or VDS open. External MOSFET health status is indicated over FETGOOD pin. Device monitors external MOSFET V_{SD} drop to decide MOSFET status as FET open or FET short condition. FETGOOD pin is pulled low whenever MOSFET fault condition is detected.

MOSFET VDS short detection can be indicated at each start-up event (ANODE ramp-up or EN pin going from low to high). For MOSFET VDS short detection to work correctly, device Anode pin voltage has to be 200mV higher than cathode pin voltage before performing external MOSFET VDS short diagnosis. MOSFET open detection is available during device start-up and well as during normal operation.

For ideal diode configuration, when controller is off output loads are always powered through body diode of the external MOSFET. It is important to detect if external MOSFET is completely turned on or not before turning on downstream loads to avoid large current flowing through the body diode of MOSFET which can potentially damage the MOSFET. This condition could arise due to gate voltage not getting applied to MOSFET gate pin under specific fault condition such as MOSFET gate pin open due to PCB manufacturing defect. LM74703-Q1, LM74704-Q1 monitors external MOSFET source to drain drop and pulls the FETGOOD pin low if this drop is higher than 200mV, even when gate voltage is applied to the MOSFET. This helps systems to monitor MOSFET off condition during start-up (even when ideal diode controller is enabled) and indicate the same using FETGOOD pin so that a decision on system level can be taken to turn off downstream loads to avoid large load current flow through body diode of the MOSFET.

FETGOOD pin is also pulled low if charge pump voltage is lower than charge pump UVLO threshold of 6.6-V to indicate gate drive voltage is not enough to fully enhance the MOSFET.

LM74703-Q1 has push-pull FETGOOD output to support systems where there is no external pull up or bias voltage available when system starts-up.

LM74704-Q1 has open-drain FETGOOD output. FETGOOD pin should be pulled to external bias voltage through pull-up resistor. External pull-up resistor should be selected such that current through FETGOOD pull down switch is less than 1-mA to stay within the recommonded operating conditions.

8.4 Device Functional Modes

8.4.1 Shutdown Mode

The LM74703-Q1 enters shutdown mode when the EN pin voltage is below the specified input low threshold $V_{(EN\_IL)}$. Both the gate driver and the charge pump are disabled in shutdown mode. During shutdown mode the LM74703-Q1 enters low I_Q operation with the ANODE pin only sinking 1 µA. When the LM74703-Q1 is in shutdown mode, forward current flow through the external MOSFET is not interrupted but is conducted through the MOSFET's body diode.

8.4.2 Conduction Mode

Conduction mode occurs when the gate driver is enabled. There are three regions of operating during conduction mode based on the ANODE to CATHODE voltage of the LM74703-Q1. Each of the three modes

is described in the *Regulated Condution Mode*, *Full Conduction Mode* and *Reverse Current Protection Mode* sections.

8.4.2.1 Regulated Conduction Mode

For the LM74703-Q1 to operate in regulated conduction mode, the gate driver must be enabled as described in the *Gate Driver* section and the current from source to drain of the external MOSFET must be within the range to result in an ANODE to CATHODE voltage drop of –11 mV to 50 mV. During forward regulation mode the ANODE to CATHODE voltage is regulated to 20 mV by adjusting the GATE to ANODE voltage. This closed loop regulation scheme enables graceful turn off of the MOSFET at very light loads and ensures zero DC reverse current flow.

8.4.2.2 Full Conduction Mode

For the LM74703-Q1 to operate in full conduction mode the gate driver must be enabled as described in the *Gate Driver* section and the current from source to drain of the external MOSFET must be large enough to result in an ANODE to CATHODE voltage drop of greater than 50-mV typical. If these conditions are achieved the GATE pin is internally connected to the VCAP pin resulting in the GATE to ANODE voltage being approximately the same as the VCAP to ANODE voltage. By connecting VCAP to GATE the external MOSFET's $R_{DS(ON)}$ is minimized reducing the power loss of the external MOSFET when forward currents are large.

8.4.2.3 Reverse Current Protection Mode

For the LM74703-Q1 to operate in reverse current protection mode, the gate driver must be enabled as described in the *Gate Driver* section and the current of the external MOSFET must be flowing from the drain to the source. When the ANODE to CATHODE voltage is typically less than –11 mV, reverse current protection mode is entered and the GATE pin is internally connected to the ANODE pin. The connection of the GATE to ANODE pin disables the external MOSFET. The body diode of the MOSFET blocks any reverse current from flowing from the drain to source.

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9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The LM74703-Q1, LM74704-Q1 is used with N-Channel MOSFET controller in a typical reverse polarity protection application. The schematic for the 12-V battery protection application is shown in Figure 9-1 where the LM74703-Q1, LM74704-Q1 is used in series with a battery to drive the MOSFET Q1. The TVS is not required for the LM74703-Q1, LM74704-Q1 to operate, but they are used to clamp the positive and negative voltage surges. The output capacitor C_{OUT} is recommended to protect the immediate output voltage collapse as a result of line disturbance.

9.2 Typical Application

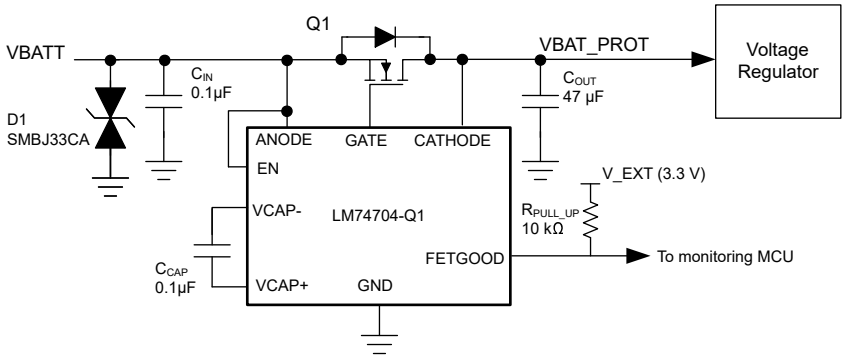

Figure 9-1. Typical Application Circuit

9.2.1 Design Requirements

A design example, with system design parameters listed in Table 9-1 is presented.

Table 9-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	12-V Battery, 12-V Nominal with 3.2-V Cold Crank and 35-V Load Dump
Output voltage	3.2 V during Cold Crank to 35-V Load Dump
Output current range	3-A nominal, 6-A Maximum
Output capacitance	1-µF Minimum, optional 47-µF Hold Up Capacitance
Automotive EMC Compliance	ISO 7637-2 and ISO 16750-2

9.2.2 Detailed Design Procedure

9.2.2.1 Design Considerations

- Input operating voltage range, including cold crank and load dump conditions
- Nominal load current and maximum load current

9.2.2.2 MOSFET Selection

The important MOSFET electrical parameters are the maximum continuous drain current I_D, the maximum drain-to-source voltage $V_{DS(MAX)}$, the maximum source current through body diode and the drain-to-source On resistance R_{DSON}.

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The maximum continuous drain current, I_D, rating must exceed the maximum continuous load current. The maximum drain-to-source voltage, $V_{DS(MAX)}$, must be high enough to withstand the highest differential voltage seen in the application. This would include any anticipated fault conditions. It is recommended to use MOSFETs with voltage rating up to 60-V maximum with the LM74704-Q1 because anode-cathode maximum voltage is 65 V. The maximum V_{GS} LM74704-Q1 can drive is 13 V, so a MOSFET with 15-V minimum V_{GS} should be selected. If a MOSFET with < 15-V V_{GS} rating is selected, a zener diode can be used to clamp V_{GS} to safe level. During startup, inrush current flows through the body diode to charge the bulk hold-up capacitors at the output. The maximum source current through the body diode must be higher than the inrush current that can be seen in the application.

To reduce the MOSFET conduction losses, lowest possible $R_{DS(ON)}$ is preferred, but selecting a MOSFET based on low $R_{DS(ON)}$ may not be beneficial always. Higher $R_{DS(ON)}$ will provide increased voltage information to LM74704-Q1's reverse comparator at a lower reverse current. Reverse current detection is better with increased $R_{DS(ON)}$. It is recommended to operate the MOSFET in regulated conduction mode during nominal load conditions and select $R_{DS(ON)}$ such that at nominal operating current, forward voltage drop V_{DS} is close to 20-mV regulation point and not more than 50 mV.

As a guideline, it is suggested to choose (20 mV / $I_{Load(Nominal)}$) ≤ $R_{DS(ON)}$ ≤ (50 mV / $I_{Load(Nominal)}$).

MOSFET manufacturers usually specify $R_{DS(ON)}$ at 4.5-V V_{GS} and 10-V V_{GS}. $R_{DS(ON)}$ increases drastically below 4.5-V V_{GS} and $R_{DS(ON)}$ is highest when V_{GS} is close to MOSFET V_{th}. For stable regulation at light load conditions, it is recommended to operate the MOSFET close to 4.5-V V_{GS}, that is, much higher than MOSFET gate threshold voltage. It is recommended to choose MOSFET with typical gate threshold voltage V_{th} of 2-V to 2.5-V. Choosing a lower V_{th} MOSFET also reduces the turn ON time.

Based on the design requirements, preferred MOSFET ratings are:

- 60-V $V_{DS(MAX)}$ and ±20-V $V_{GS(MAX)}$
- $R_{DS(ON)}$ at 3-A nominal current: (20 mV / 3A) ≤ $R_{DS(ON)}$ ≤ (50 mV / 3A) = 6.67 mΩ ≤ $R_{DS(ON)}$ ≤ 16.67 mΩ
- MOSFET gate threshold voltage V_{th}: 2V typical

Thermal resistance of the MOSFET should be considered against the expected maximum power dissipation in the MOSFET to ensure that the junction temperature (T_J) is well controlled.

9.2.2.3 Charge Pump VCAP, input and output capacitance

Minimum required capacitance for charge pump VCAP and input/output capacitance are:

- VCAP: Minimum 0.1 µF is required; recommended value of VCAP (µF) ≥ 10 x $C_{ISS(MOSFET)}$(µF)
- C_{IN}: minimum 22 nF of input capacitance
- C_{OUT}: minimum 100 nF of output capacitance

9.2.2.4 Selection of TVS Diodes for 12-V Battery Protection Applications

TVS diodes are used in automotive systems for protection against transients. In the 12-V battery protection application circuit shown in Figure 9-2, a bi-directional TVS diode is used to protect from positive and negative transient voltages that occur during normal operation of the car and these transient voltage levels and pulses are specified in ISO 7637-2 and ISO 16750-2 standards.

There are two important specifications are breakdown voltage and clamping voltage of the TVS. Breakdown voltage is the voltage at which the TVS diode goes into avalanche similar to a zener diode and is specified at a low current value typical 1 mA and the breakdown voltage should be higher than worst case steady state voltages seen in the system. The breakdown voltage of the TVS+ should be higher than 24-V jump start voltage and 35-V suppressed load dump voltage and less than the maximum ratings of LM74703-Q1, LM74704-Q1 (65 V). The breakdown voltage of TVS- should be beyond than maximum reverse battery voltage –16 V, so that the TVS- is not damaged due to long time exposure to reverse connected battery.

Clamping voltage is the voltage the TVS diode clamps in high current pulse situations and this voltage is much higher than the breakdown voltage. TVS diodes are meant to clamp transient pulses and should not interfere with steady state operation. In the case of an ISO 7637-2 pulse 1, the input voltage goes up to –150 V with a generator impedance of 10 Ω. This translates to 15 A flowing through the TVS - and the voltage across the TVS would be close to its clamping voltage.

ADVANCE INFORMATION

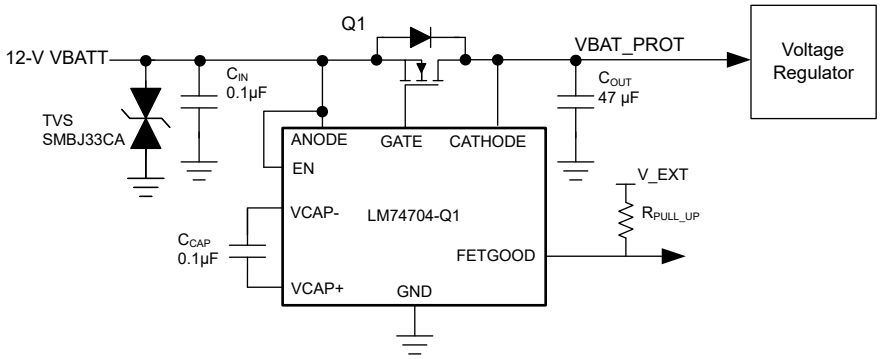


Figure 9-2. Typical 12-V Battery Protection with Single Bi-Directional TVS

The next criterion is that the absolute maximum rating of Anode to Cathode reverse voltage of the LM74703-Q1, LM74704-Q1 (–75 V) and the maximum V_{DS} rating MOSFET are not exceeded. In the design example, 60-V rated MOSFET is chosen and maximum limit on the cathode to anode voltage is 60 V.

In case of ISO 7637-2 pulse 1, the anode of LM74703-Q1, LM74704-Q1 is pulled down by the ISO pulse and clamped by TVS-. The MOSFET is turned off quickly to prevent reverse current from discharging the bulk output capacitors. When the MOSFET turns off, the cathode to anode voltage seen is equal to (TVS Clamping voltage + Output capacitor voltage). If the maximum voltage on output capacitor is 16 V (maximum battery voltage), then the clamping voltage of the TVS- should not exceed, (60 V – 16) V = –44 V.

The SMBJ33CA TVS diode can be used for 12-V battery protection application. The breakdown voltage of 36.7 V meets the jump start, load dump requirements on the positive side and 16-V reverse battery connection on the negative side. During ISO 7637-2 pulse 1 test, the SMBJ33CA clamps at –42 V with 15 A of peak surge current as shown in Figure 9-5 and it meets the clamping voltage ≤ 44 V.

SMBJ series of TVS' are rated up to 600-W peak pulse power levels. This is sufficient for ISO 7637-2 pulses and suppressed load dump (ISO-16750-2 pulse B).

9.2.2.5 Selection of TVS Diodes and MOSFET for 24-V Battery Protection Applications

Typical 24-V battery protection application circuit shown in Figure 9-3 uses two uni-directional TVS diodes to protect from positive and negative transient voltages.

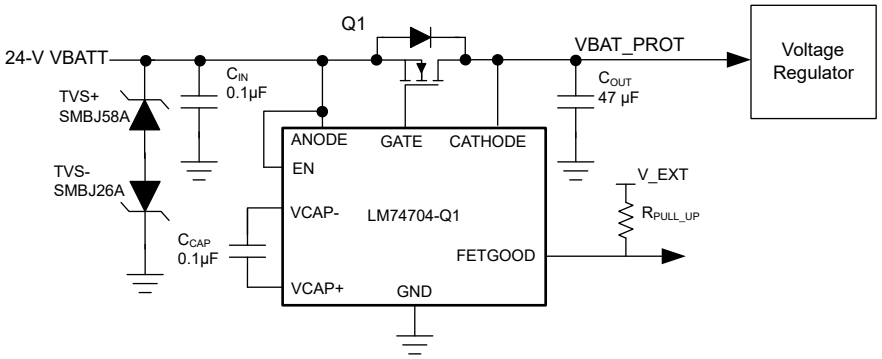


Figure 9-3. Typical 24-V Battery Protection with Two Uni-Directional TVS

The breakdown voltage of the TVS+ should be higher than 48-V jump start voltage, less than the absolute maximum ratings of anode and enable pin of LM74703-Q1, LM74704-Q1 (65 V) and should withstand 65-V suppressed load dump. The breakdown voltage of TVS- should be lower than maximum reverse battery voltage –32 V, so that the TVS- is not damaged due to long time exposure to reverse connected battery.

During ISO 7637-2 pulse 1, the input voltage goes up to –600 V with a generator impedance of 50 Ω. This translates to 12 A flowing through the TVS-. The clamping voltage of the TVS- cannot be same as that of 12-V battery protection circuit. Because during the ISO 7637-2 pulse, the Anode to Cathode voltage seen is equal

to (-TVS Clamping voltage + Output capacitor voltage). For a 24-V battery application, the maximum battery voltage is 32 V, then the clamping voltage of the TVS- should not exceed, 75 V – 32 V = 43 V.

Single bi-directional TVS cannot be used for 24-V battery protection because breakdown voltage for TVS+ ≥ 65 V, maximum clamping voltage is ≤ 43 V and the clamping voltage cannot be less than the breakdown voltage. Two un-directional TVS connected back-back needs to be used at the input. For positive side TVS+, SMBJ58A with the breakdown voltage of 64.4 V (minimum), 67.8 (typical) is recommended. For the negative side TVS-, SMBJ26A with breakdown voltage close to 32 V (to withstand maximum reverse battery voltage –32 V) and maximum clamping voltage of 42.1 V is recommended.

For 24-V battery protection, a 75-V rated MOSFET is recommended to be used along with SMBJ26A and SMBJ58A connected back-back at the input.

9.2.3 Application Curves

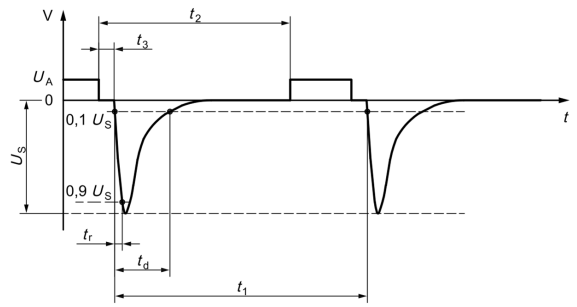
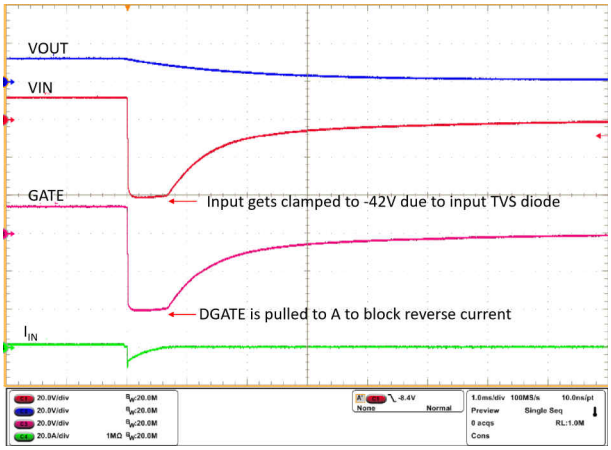
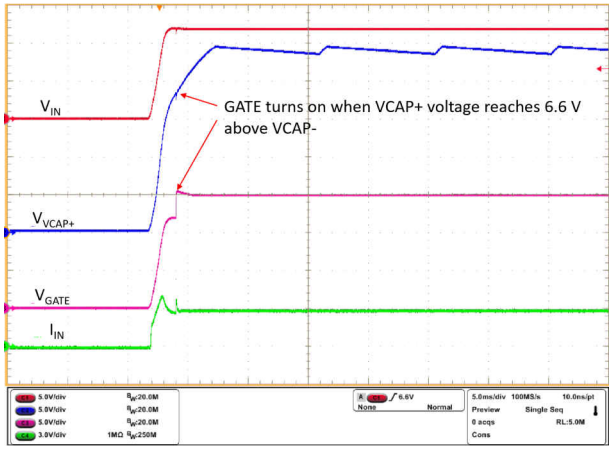


Figure 9-4. ISO 7637-2 Pulse 1



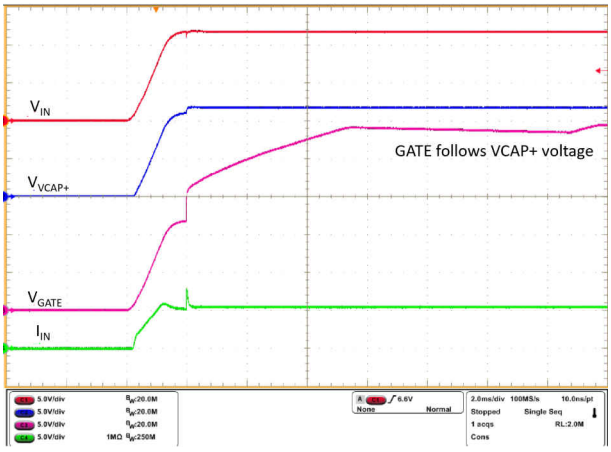
Time (1 ms/DIV)

Figure 9-5. Response to ISO 7637-2 Pulse 1



Time (5 ms/DIV)

Figure 9-6. Startup with 3-A Load



Time (2 ms/DIV)

Figure 9-7. Startup with 5.8-A Load

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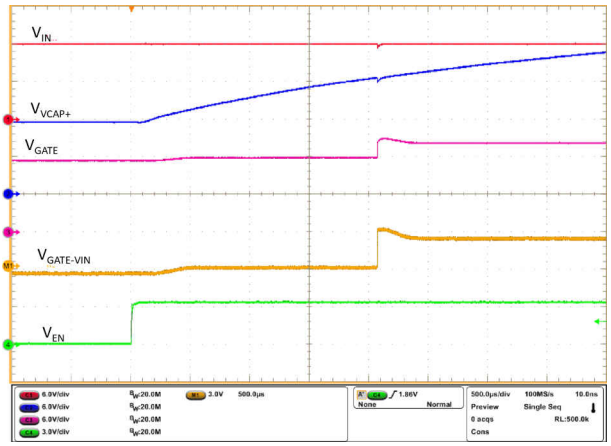
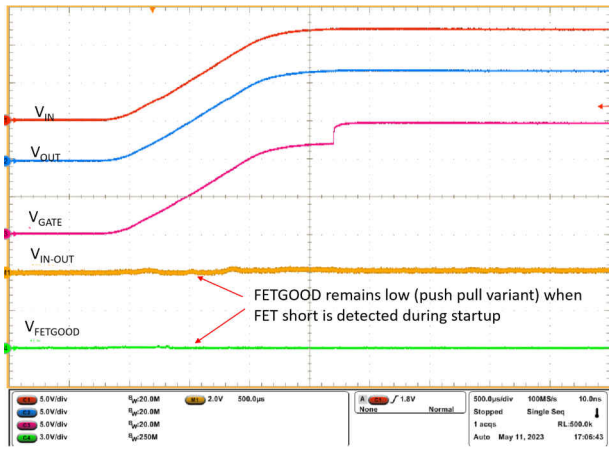


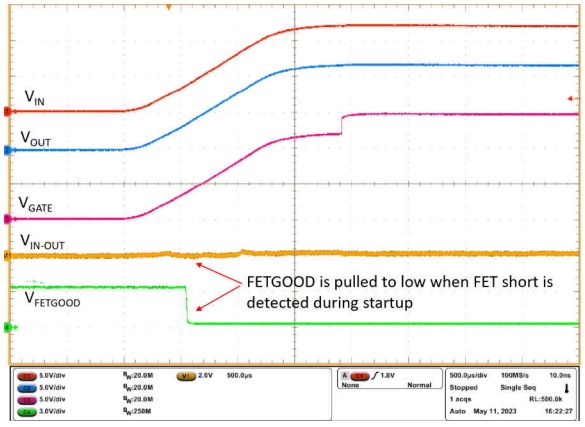
Time (0.5 ms/DIV)

Figure 9-8. Device Start-Up with EN Toggle



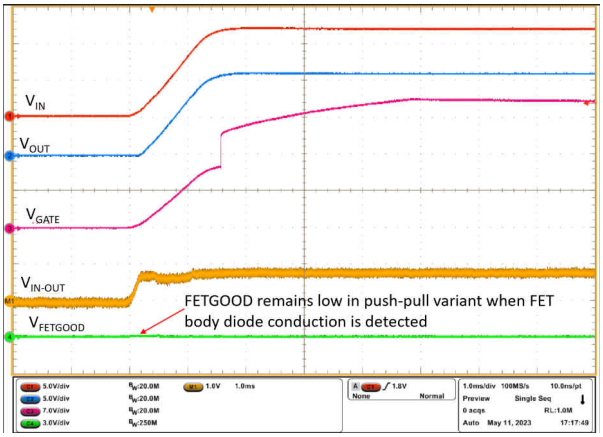
Time (0.5 ms/DIV)

Figure 9-9. FETGOOD During Startup with FET Short (LM74703-Q1)



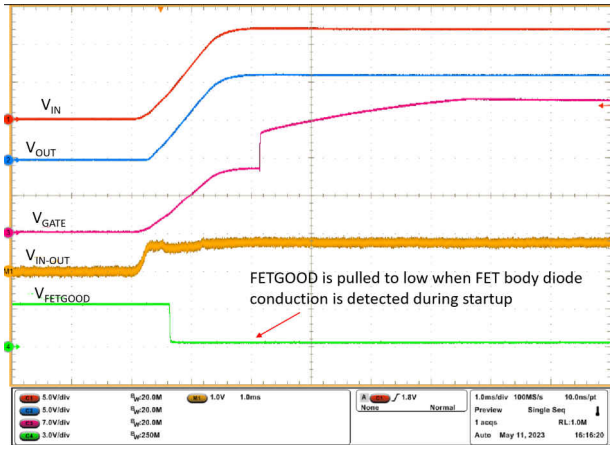
Time (0.5 ms/DIV)

Figure 9-10. FETGOOD During Startup with FET Short (LM74704-Q1)



Time (1 ms/DIV)

Figure 9-11. FETGOOD During Startup with FET Off / GATE pin open (LM74703-Q1)



Time (1 ms/DIV)

Figure 9-12. FETGOOD During Startup with FET Off / GATE pin open (LM74704-Q1)

9.3 Power Supply Recommendations

The LM74703-Q1, LM74704-Q1 Ideal Diode Controller designed for the supply voltage range of 3.2 V ≤ V_{ANODE} ≤ 65 V. If the input supply is located more than a few inches from the device, an input ceramic bypass capacitor higher than 100 nF is recommended. To prevent LM74703-Q1 and surrounding components from damage under the conditions of a direct output short circuit, it is necessary to use a power supply having over load and short circuit protection.

9.4 Layout

9.4.1 Layout Guidelines

- Connect ANODE, GATE and CATHODE pins of LM74703-Q1, LM74704-Q1 close to the MOSFET's SOURCE, GATE and DRAIN pins.
- The high current path of for this solution is through the MOSFET, therefore it is important to use thick traces for source and drain of the MOSFET to minimize resistive losses.
- The charge pump capacitor across VCAP and ANODE pins must be kept away from the MOSFET to lower the thermal effects on the capacitance value.
- The Gate pin of the LM74703-Q1, LM74704-Q1 must be connected to the MOSFET gate with short trace. Avoid excessively thin and long trace to the Gate Drive.
- Keep the GATE pin close to the MOSFET to avoid increase in MOSFET turn-off delay due to trace resistance.
- Obtaining acceptable performance with alternate layout schemes is possible, however the layout shown in the *Layout Example* is intended as a guideline and to produce good results.

9.4.2 Layout Example

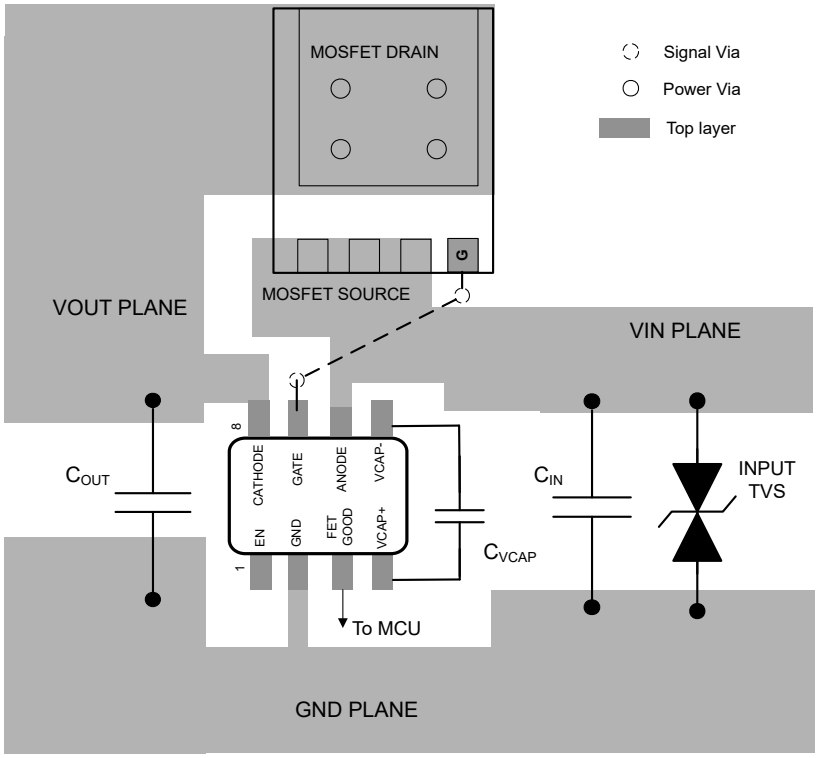


Figure 9-13. LM74703-Q1 DDF Package Example Layout

ADVANCE INFORMATION

10 Device and Documentation Support

10.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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10.3 Trademarks

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10.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

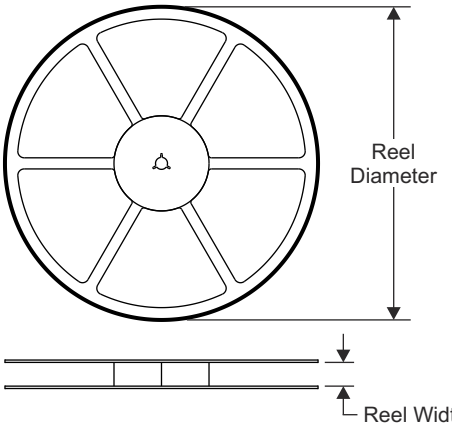
11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

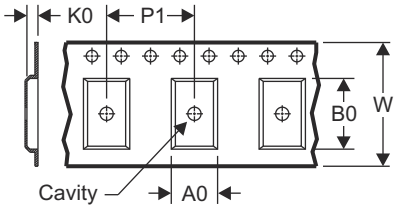
ADVANCE INFORMATION

11.1 Tape and Reel Information

REEL DIMENSIONS

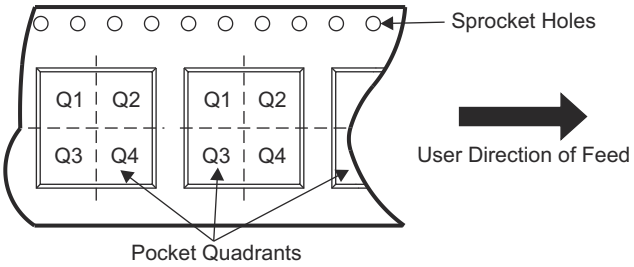


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

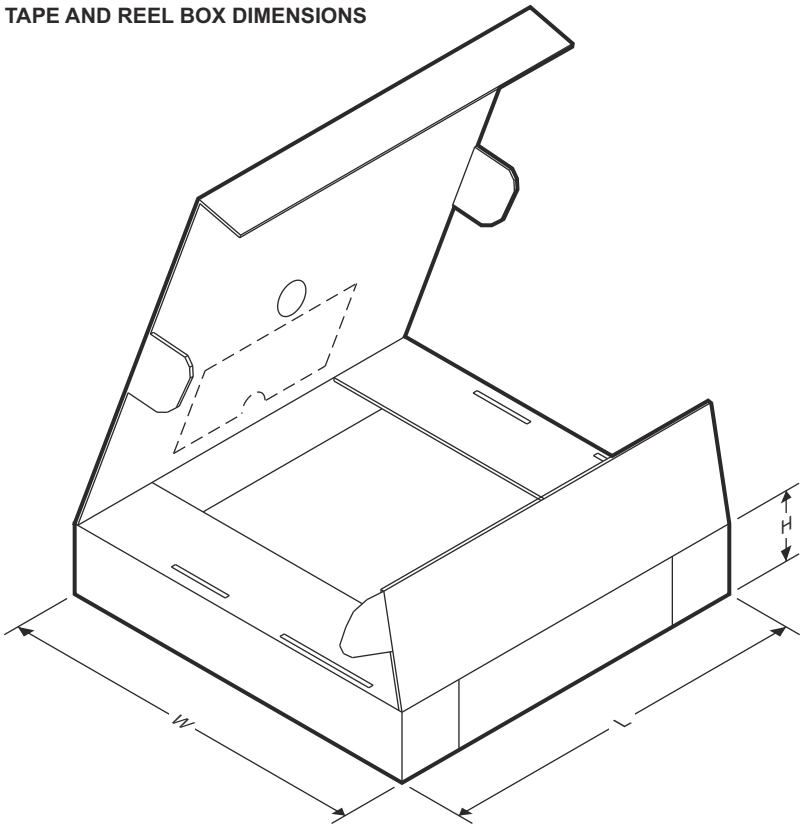


Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM74703QDDFRQ1	SOT-23	DDF	8	3000	180.0	8.4	3.2	3.1	1.25	4	8	3
LM74704QDDFRQ1	SOT-23	DDF	8	3000	180.0	8.4	3.2	3.1	1.25	4	8	3

ADVANCE INFORMATION

ADVANCE INFORMATION

TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM74703QDDFRQ1	SOT-23	DDF	8	3000	210	185	35
LM74704QDDFRQ1	SOT-23	DDF	8	3000	210	185	35

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PLM74703QDDFRQ1	ACTIVE	SOT-23-THIN	DDF	8	3000	TBD	Call TI	Call TI	-40 to 125		Samples
PLM74704QDDFRQ1	ACTIVE	SOT-23-THIN	DDF	8	3000	TBD	Call TI	Call TI	-40 to 125		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

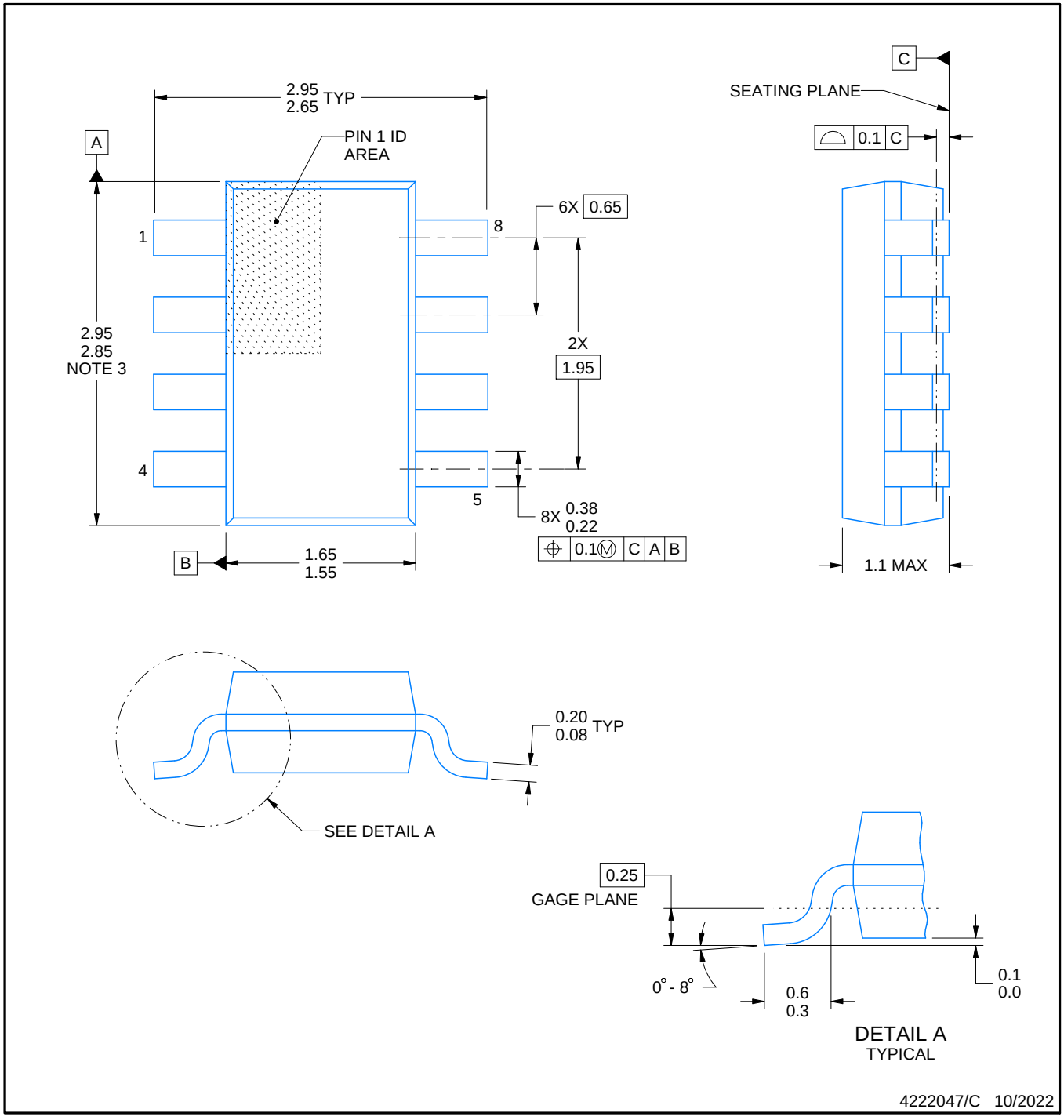
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

PACKAGE OUTLINE

DDF0008A

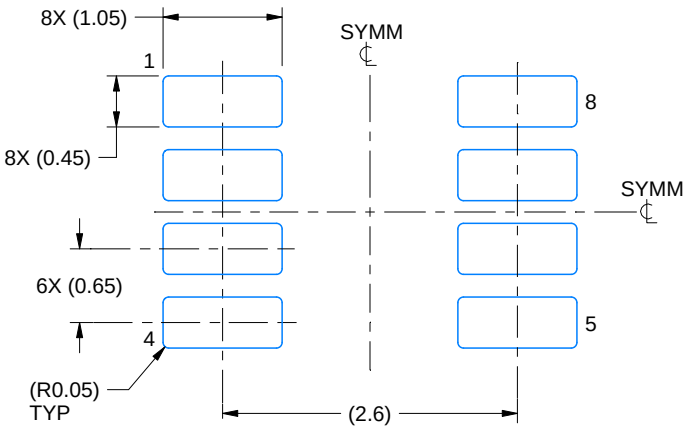
SOT-23 - 1.1 mm max height

PLASTIC SMALL OUTLINE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.



LAND PATTERN EXAMPLE
SCALE:15X

NON SOLDER MASK
DEFINED

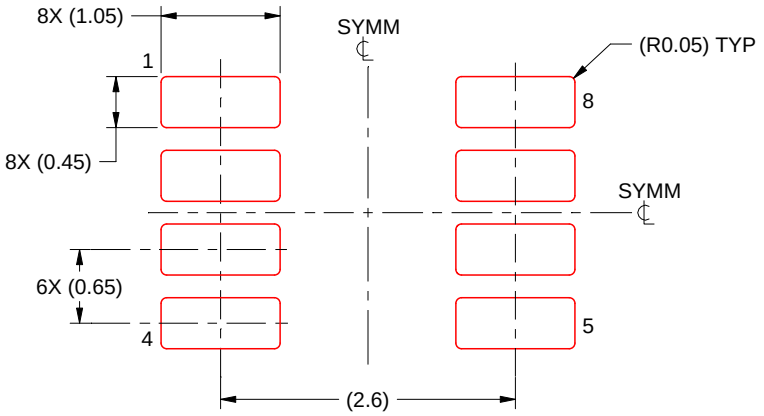
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4222047/C 10/2022

NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4222047/C 10/2022

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

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