MSM74017

MODULATOR/DEMODULATOR FOR MODEM FUNCTION IN THE CELLULAR MOBILE PHONE

GENERAL DESCRIPTION

The MSM74017 performs the modulator/demodulator functions in the modem part of the cellular mobile phone.

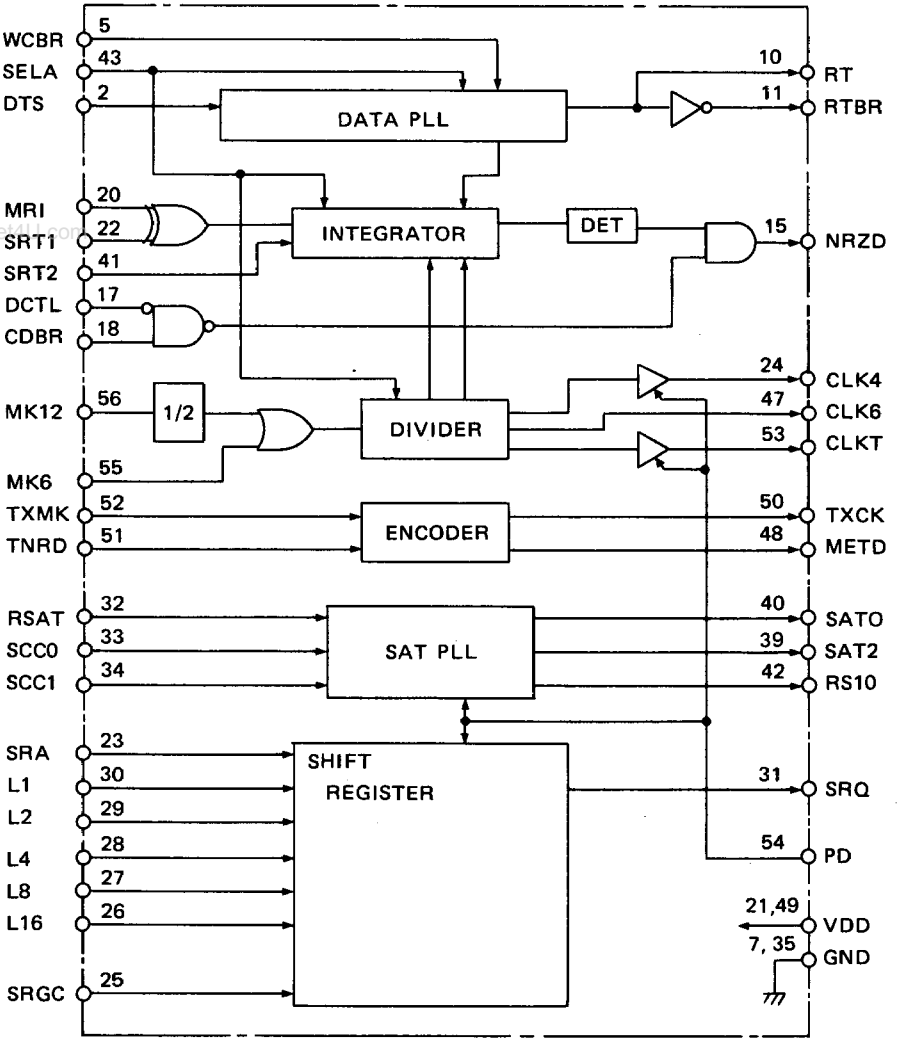
The MSM74017 consists of digital PLL for Data Timing Signal (DTS), Received Audio Tone (RSAT) and shift register and is fabricated by OKI's low power consumption CMOS silicon gate technology.

The MSM74017 can configurate a 10K bps SPL modem for AMPS system in combination with MSM6808. A 8K bps SPL modem for TACS system can be configurated in combination with MSM6818.

FEATURES

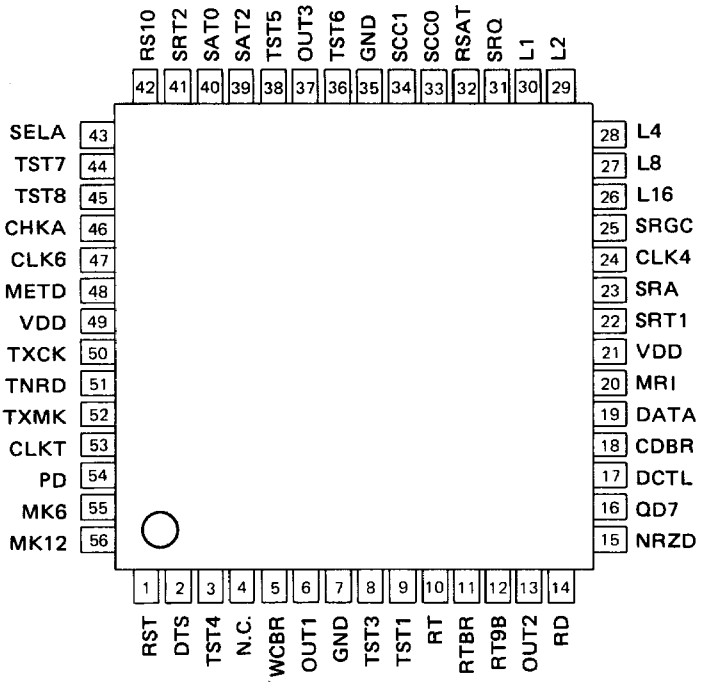
- Built-in DATA PLL to derive a phase from DTS.
- Built-in SAT PLL to derive a phase from RSAT.
- Built-in Detector for MRI demodulation.
- Built-in Manchester Encoder.
- TTL compatible digital interface.
- Low power consumption: 20 mW (typ).
- 56-pin plastic package.

BLOCK DIAGRAM



PIN CONFIGURATION

MSM74017GS-VK



56 pin FLAT package

PIN DESCRIPTION

Pin Name	Pin No.	I/O	Function
RST	1	I	Power on reset. "1" = reset "0" = normal operation
DTS	2	I	This is a Data Timing Signal input from MSM6808/6818. The input signal is output as the Received Timing (RT), after the S/N has been improved by a built-in Digital PLL.
WCBR	5	I	This input controls the bandwidth of the Digital PLL for Received Timing. WCBR = "1": narrow band width WCBR = "0": wide band width
RT	10	O	Received Timing Signal. When DTS is nearly equal to 10 kHz (AMPS) or 8 kHz (TACS), RT harmonizes with DTS. Refer to the description of DTS.
RTBR	11	O	This pin is the inverting output of RT, and is connected to SRT1 and SRT2 for demodulation clock.
NRZD	15	O	Manchester Received Input Signal (MRI) is demodulated by RTBR and is output as Non Return Zero Data (NRZD). See Figure 1.
DCTL	17	I	This pin controls the output of NRZD. Refer to the description about CDBR.
CDBR	18	I	This signal is Carrier Detection Data which is detected in MSM6808/6818. CDBR controls the output of NRZD with DCTL.
MRI	20	I	Manchester Received Input Signal. See Figure 1.
SRT1	22	I	This pin should be connected to RTBR. RTBR is used for Demodulation Clock.
SRA	23	I	Shift Register Data input. This shift register is a static clock serial shift register whose length may be programmed to be any number of bits between 1 and 32.

DCTL	CDBR	NRZD
0	0	NRZD
0	1	0
1	0	NRZD
1	1	NRZD

Pin Name	Pin No.	I/O	Function
CLK4	24	O	This is a clock output, the frequency of which, is 1.5 MHz devided from MK6 or MK12. This may be used for Shift Register Clock.
SRGC	25	I	Shift Register Clock input.
L16	26	I	Length Control inputs. The number of selected bit is equal to the sum of the subscripts of these enabled inputs plus one.
L8	27	I	
L4	28	I	
L2	29	I	
L1	30	I	
SRQ	31	O	Shift Register Output.
RSAT	32	I	Received Supervisory Audio Tone. This pin should be connected to RSAT of MSM6808/6818. The signal is input into a buld-in Digital PLL for SAT so that the S/N is improved, and is output as SATO, SAT2, RS10.
SCC0	33	I	SCC0 and SCC1 are SAT Color Code. These signals determine the center frequency of the Digital PLL for SAT.
SCC1	34	I	
SAT2	39	I	The double frequency of SAT Signal is output. This may be used for discrimination of SAT frequencies. Refer to the description about RSAT.
SATO	40	I	This is an output for transmitting SAT signal. Before this signal is input into DSAT of MSM6808/6818, the phase of the signal may be delayed by build-in Shift Register.
SRT2	41	I	This pin should be tied to RTBR. SRT1 is used for the Demodulation Clock, same as SRT2.
RS10	42	O	The output is ten times of the frequency of RSAT signal. When this signal is input to MSM6808/6818, it controls the center frequency of SAT and BPF to fit to RSAT signal.

SCC1	SCC0	Center Frequency
0	0	5970 Hz
0	1	6000 Hz
1	0	6030 Hz
1	1	–

Pin Name	Pin No.	I/O	Function
SELA	43	I	This pin is used for selecting the center frequency of built-in Digital PLL for DTS and used for selecting Transmitting Data Rate. SELA = "1": 10 kHz (AMPS) SELA = "0": 8 kHz (TACS)
METD	48	O	Manchester Encoded Data output. See Figure 2.
TXCK	50	O	This is a clock output using for Transmitting Data. Refer to the description of SELA and Figure 2.
TNRD	51	I	Transmit NRZ Data. This input signale is modulated by an internal TXCK and is output as METD. See Figure 2.
TXMK	52	I	This pin should be connected to CLKT.
CLKT	53	O	The double frequency of TXCK is output. CLKT should be connected with TXMK.
PD	54	I	Power down function enable pin. Logical "0" enables the power down mode.
MK6	55	I	Main Clock Input. One of MK6 and MK12 should be input. When this pin is not used, it should be set to digital "0".
MK12	56	I	Main Clock Input. See the description of MK6. When this pin is not used, it should be set at digital "0".
GND	7		Ground level: 0 V
	35		
VDD	21		Power Supply: +5V
	49		
TST4	3	I	These pins are used for various tests. These pins should be usually connected to GND.
TST3	8	I	
TST1	9	I	
TST6	36	I	
TST5	38	I	

Pin Name	Pin No.	I/O	Function
TST7	44	I	These pins are used for various tests. These pins should be usually connected to GND.
TST8	45	I	
OUT1	6	O	These pins are output pins for test.
RT9B	12	O	
OUT2	13	O	
RD	14	O	
QD7	16	O	
DATA	19	O	
OUT3	37	O	
CHKA	46	O	

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATING

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Power Supply Voltage	V_{DD}	T_a = 25°C	-0.5	–	+7	V
Input/Output Voltage	V_I, V_O	with reset to GND	-0.5	–	V_{DD}+0.5	V
Input/Output Current	I_I, I_O	T_a = 25°C	-10	–	+10	mA
Storage Temperature	T_{st}	–	-55	–	+150	°C
Power Dissipation	Pd	–	–	1	–	W

OPERATING RANGE

Parameter	Symbol	Min	Typ	Max	Unit
Power Supply Voltage	V_{DD}	3	–	6	V
Operating Temperature	T_{opr}	-40	–	85	°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Condition			Unit
		Min	Typ	Max	
Power Supply Voltage	V_{DD}	4.25	5	5.25	V
Operating Temperature	T_{opr}	-40	25	85	°C
"1" Input Voltage	V_{IH}	2.2	–	V_{DD}+0.3	V
"0" Input Voltage	V_{IL}	-0.3	–	0.8	V

MASTER CLOCK

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Frequency	Fi	MK6 = 6 MHz or MK12 = 12 MHz	-0.01	0	+0.01	%
Duty Ratio	Fd	MK6 = 6 MHz	45	50	55	%
		MK12 = 12 MHz	20	50	80	

DC CHARACTERISTICS

(V_{DD} = 5V + 5%, T_a = -40 +85°C)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
"1" Input Current	I_{IH}	$V_i = V_{DD}$ V_{DD} = 5.25 V	–	–	10	μA
"0" Input Current	I_{IL}	V_i = GND	-10	–	–	
"1" Output Voltage	V_{OH}	I_o = -40 μA V_{DD} = 4.75 V I_o = -400 μA	4.2 2.4	– –	– –	V
"0" Output Voltage	V_{OL}	I_o = 2 mA (*1) I_o = 5 mA	– –	– –	0.4 0.5	V
Standby Current	I_{CCS}	$V_i = V_{DD}$/GND V_{DD} = 5.25 V	–	1	0.5	mA
Operation Power Supply Current	I_{CCO}	$V_i = V_{DD}$/GND Output pin open	–	4	6	mA

(*1) V_{OH}: upper/CMOS4000
lower/TTL74, 74LS

V_{OL}: upper/CMOS4000, TTL74LS
lower/TTL74

AC CHARACTERISTICS

(V_{DD} = 5V +5%, T_a = −40 +85°C)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Output Frequency	RT	f RT1 DTS = 10 kHz, SELA = "1" f RT0 DTS = 8 kHz, SELA = "0"	– –	10 8	– –	kHz
	RTBR	f RTBR1 DTS = 10 kHz, SELA = "1" f RTBR0 DTS = 8 kHz, SELA = "0"	– –	10 8	– –	kHz
	RS10	f RS10 RSAT = 6 kHz	–	60	–	kHz
	SAT2 SATO	f SAT2 f SATO SCC0 = "1", SCC1 = "0"	– –	12 6	– –	kHz
	CLK4 CLK6	f CLK4 f CLK6	– –	1.5 1	– –	MHz
	CLKT	f CLKT1 SELA = "1" SELA = "0"	– –	20 16	– –	kHz
	TXCK	f TXCK TXMK = 20 kHz TXMK = 16 kHz	– –	10 8	– –	kHz
PLL Capture Range	DTS-RT	f LDN1 f HDN1 SELA = "1", WCBR = "1"	9.993	–	10.007	kHz
		f LDW1 f HDW1 SELA = "1", WCBR = "0"	9.939	–	10.061	kHz
		f LDN0 f HDN0 SELA = "0", WCBR = "1"	7.993	–	8.007	kHz
		f LDW0 f HDW0 SELA = "0", WCBR = "0"	7.961	–	8.040	kHz
		f LS0 f HS0 SCC0= SCC1 = "0"	5952.4	–	5988.0	Hz
	RSAT-STO	f LS1 f HS1 SCC0 = "1", SCC1 = "0"	5982.1	–	6018.1	Hz
		f LS2 f HS2 SCC0 = "0", SCC1 = "1"	6012.0	–	6048.4	Hz

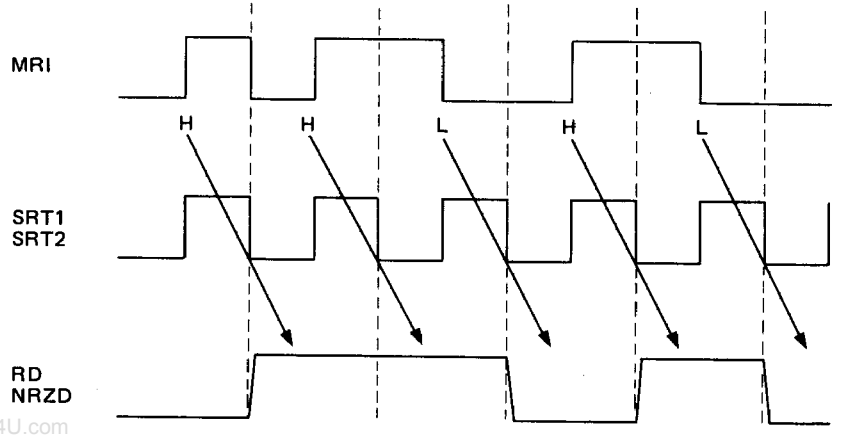


Figure 1 MRI – NRZD Timing Chart

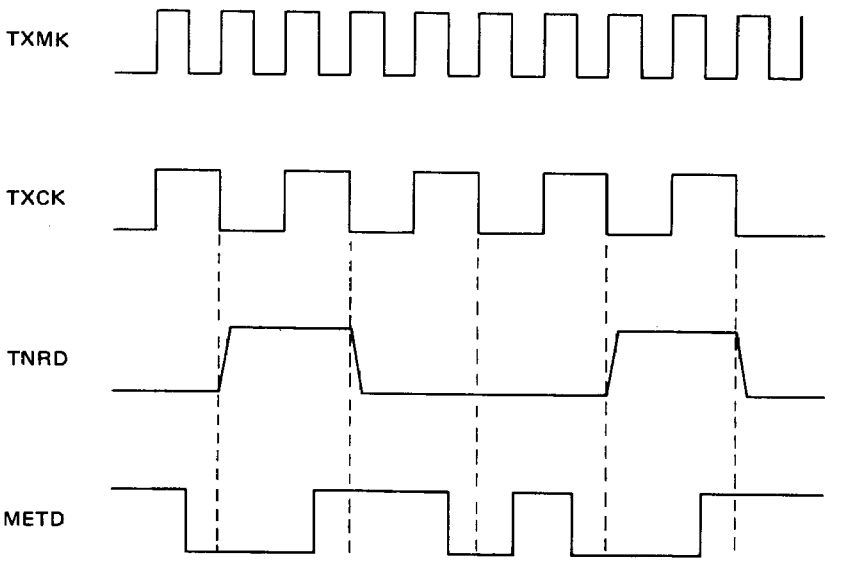


Figure 2 METD Timing Chart

APPLICATION CIRCUIT