

## AND8001/D

# Odd Number Divide By Counters With 50% Outputs and Synchronous Clocks

Prepared by: Cleon Petty and Paul Shockman  
Product Applications  
ON Semiconductor



**ON Semiconductor**  
Formerly a Division of Motorola  
<http://onsemi.com>

## APPLICATION NOTE

The application inquiries handled by the Product Applications gives opportunities to solve customer needs with new ideas and learn of ways the customer has used our devices in new applications. A couple of these calls lead to techniques of designing odd number counters with synchronous clocks and 50% outputs.

The first technique requires a differential clock, that has a 50% duty cycle, a extra Flip Flop, and a gate to allow Odd integers, such as 3, 5, 7, 9, to have 50% duty cycle outputs and a synchronous clock. The frequency of operations is limited by Tpd of the driving FF, Setup, and Hold of the extra FF, and the times cannot exceed one half on the incoming clock cycle time.

The design begins with producing a odd number counter (Divide By 3 for this discussion) by any means one wishes

and add a flip flop, and a couple of gates to produce the desired function. Karnaugh maps usually produce counters that are lockup immune.

### Example:

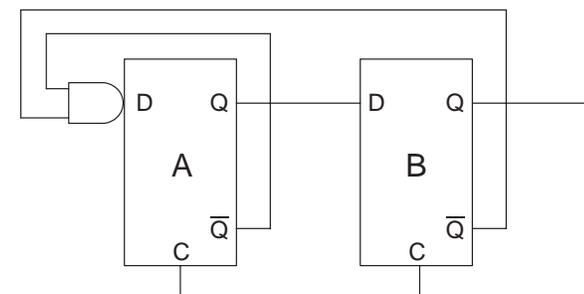
Specify, Divide By 3,  
50% duty cycle on the output  
Synchronous clocking  
50% duty cycle clock in

Using D type Flop flips and karnaugh maps we find;

$A_d = A * B^*$  and  $B_d = A$

(Note: \* indicates BAR function)

Figure 1 shows schematic and timing of such a design.



Divide By 3

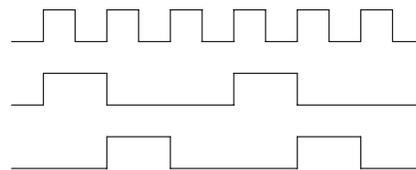
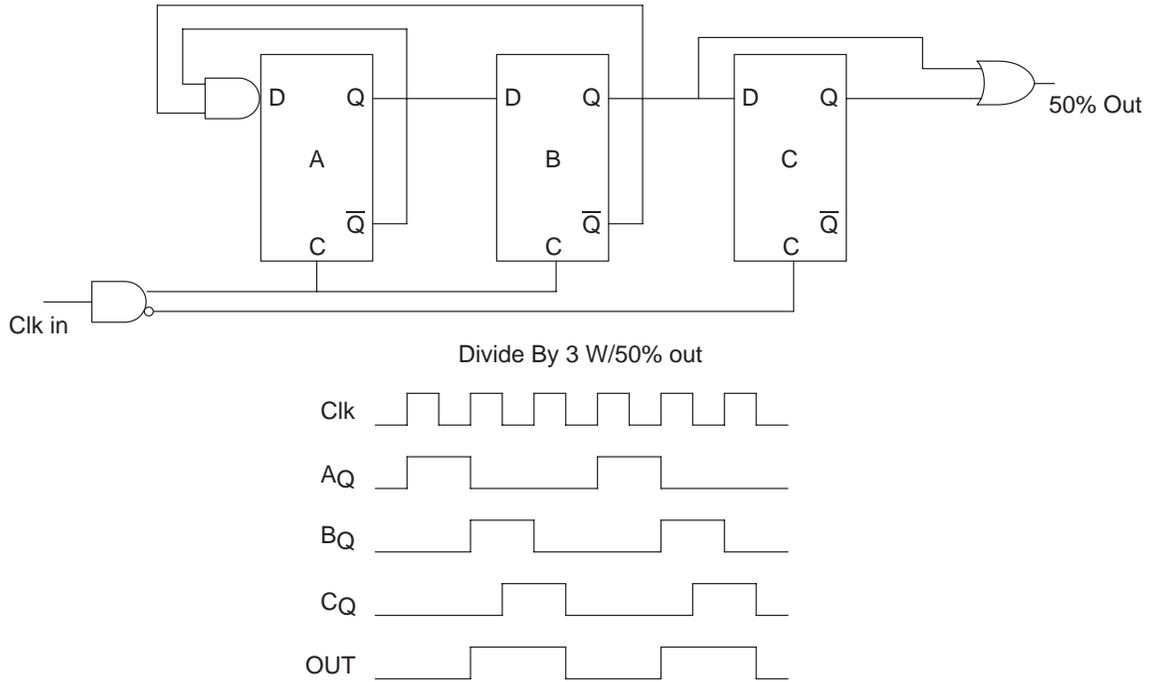


Figure 1.

## AND8001/D

Using the technique, we add a gate on the clock to get differential Clock and Clock bar, a flip flop that triggers on the Clock Bar rising edge (Clock Neg.) to shift the output of

"B" by 90 degrees and a gate to AND/OR two FF output to produce the 50% output. We get Figure 2, a Divide By 3 that clocks synchronously with 50% output duty cycle.



**Figure 2.**

The Max frequency of the configuration (figure 2) is calculated as Clock input freq./2 = Tpd of FF "B" + Setup of "C" + Hold of "C".

**Example:**

Tpd = 1Ns, Setup = 1NS and Hold time = 0Ns.

with these numbers the Max Frequency the configuration can expect is; Cycle time = 2\*(1 + 1)Ns or 4 Ns that converts to 250MHZ.

The Method is usable on other divide by "N" counters as well by using the same methodology. The use of different types of Flip Flops (J,K, S,R, Toggle, ETC.) may produce fewer components. The type logic used may also dictate configuration. The configuration should always be checked for lockup conditions before the design is committed to a production.

**Example:**

A Divide By 3 design has all possible states shown in chart 1 but uses only the states shown in chart 2 leaving the states 2,3,4,5, & 7 for possible lockup.

	Chart 1			Chart 2			
	A	B	C		A	B	C
0	0	0	0	0	0	0	0
1	1	0	0	1	1	0	0
2	0	1	0	6	0	1	1
3	1	1	0				
4	0	0	1				
5	1	0	1				
6	0	1	1				
7	1	1	1				

## AND8001/D

We need to know that the counter will go into the flow, shown in chart 2, if it happens to come up in one of the unused states at powerup or for any other reason. Figure 3 shows the resulting flow chart of the analysis of the Divide

By 3 counter of Figure 2. There is no state that the counter can begin in that doesn't lead to the desired flow after one clock cycle.

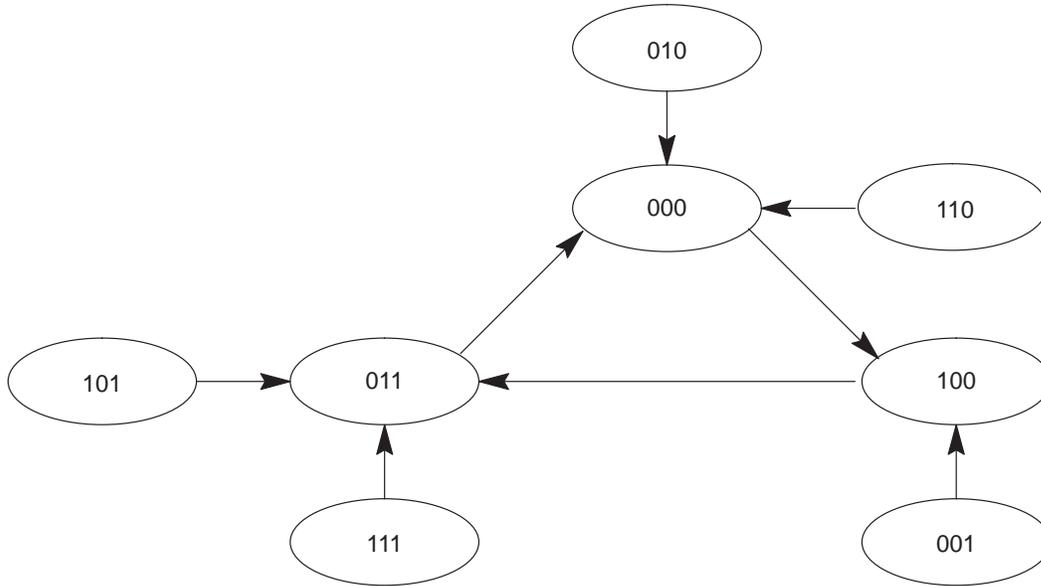


Figure 3.

Observation shows that FF "C" follows FF "B" by a half a clock cycle and will never be able to lockup making the analysis of the Divide By 3 sufficient to assure the whole configuration will have no lockup flow. So; only the 1 1 state of the divide by three needed to be confirmed.

The method is extendible to other odd larger divide by "N" numbers by following the same design flow.

- Design a stable UP or Down divide by "N" counter
- Make the Clock input a 50% duty cycle differential signal
- Add a FF to follow one of the FF's in the counter by 1/2 clock cycle
- OR/AND the shifted FF with the one that is driving it to obtain the desired 50% output

### Example:

Design a 50% Divide By 9

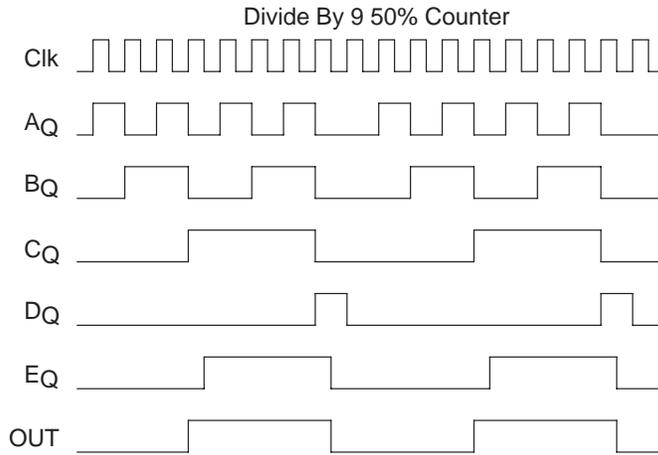
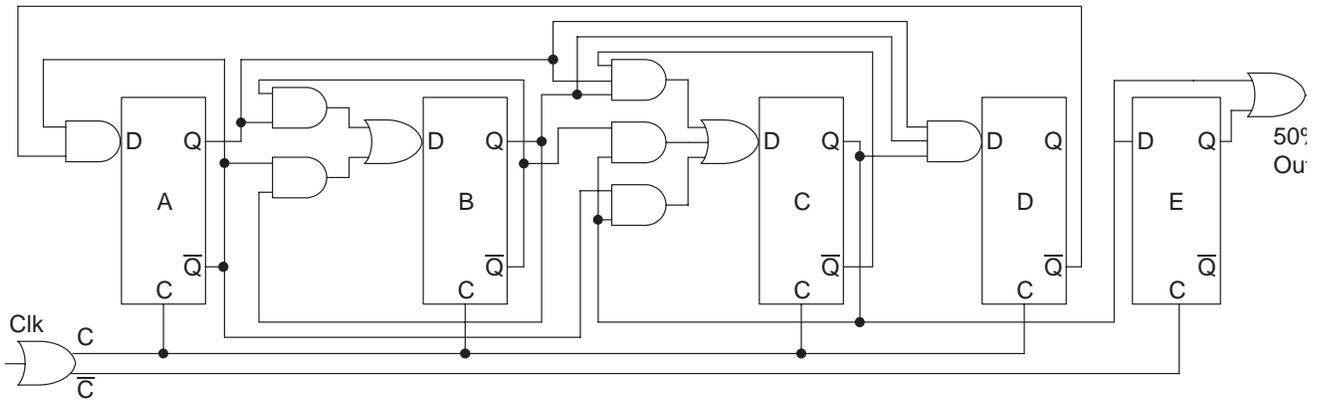
Use "D" type FF's, other types may give smaller component count

Karnaugh maps yield:

$$Ad = A*B* \quad Bd = A*B + AB*$$

$$Cd = ABC* + CB* + A*C \quad Dd = ABC$$

# AND8001/D



**Figure 4.**

Choosing to use "C" as the flip flop to delay by a 1/2 clock cycle is necessary to accomplish the 50% output required when "ANDed" with "E".

Another Synchronous 50% counter for Divide By 6, 10, 12, 14, 18, etc. can be realized by the additions of a J K FF and some gates. Other types of FF's may be used.

# AND8001/D

Take the before mentioned Divide By 3 add a J K and a divide by 6, 50% duty cycle, synchronous counter is realized as shown in Figure 5.

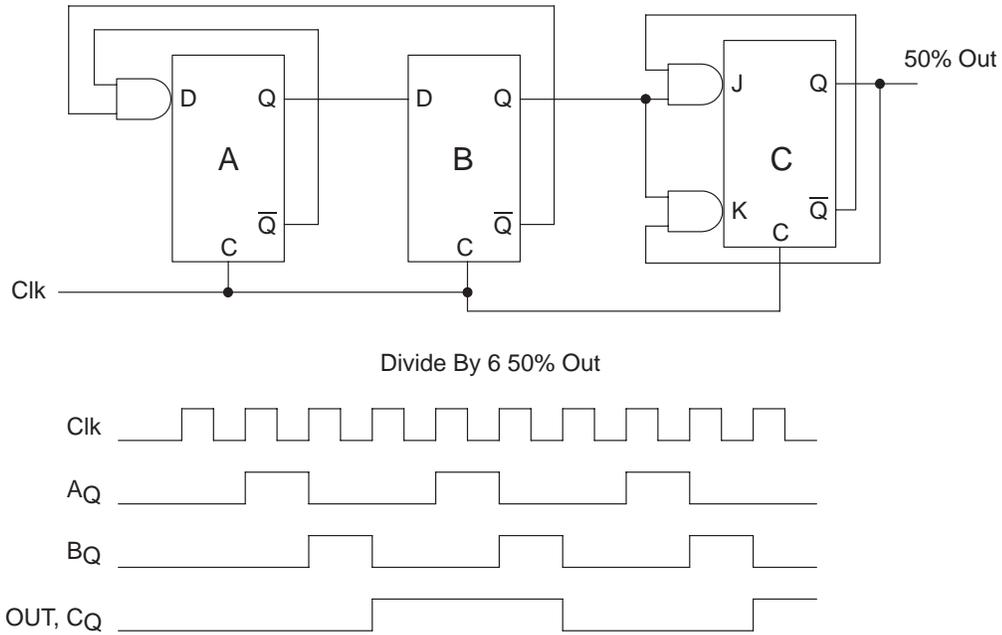
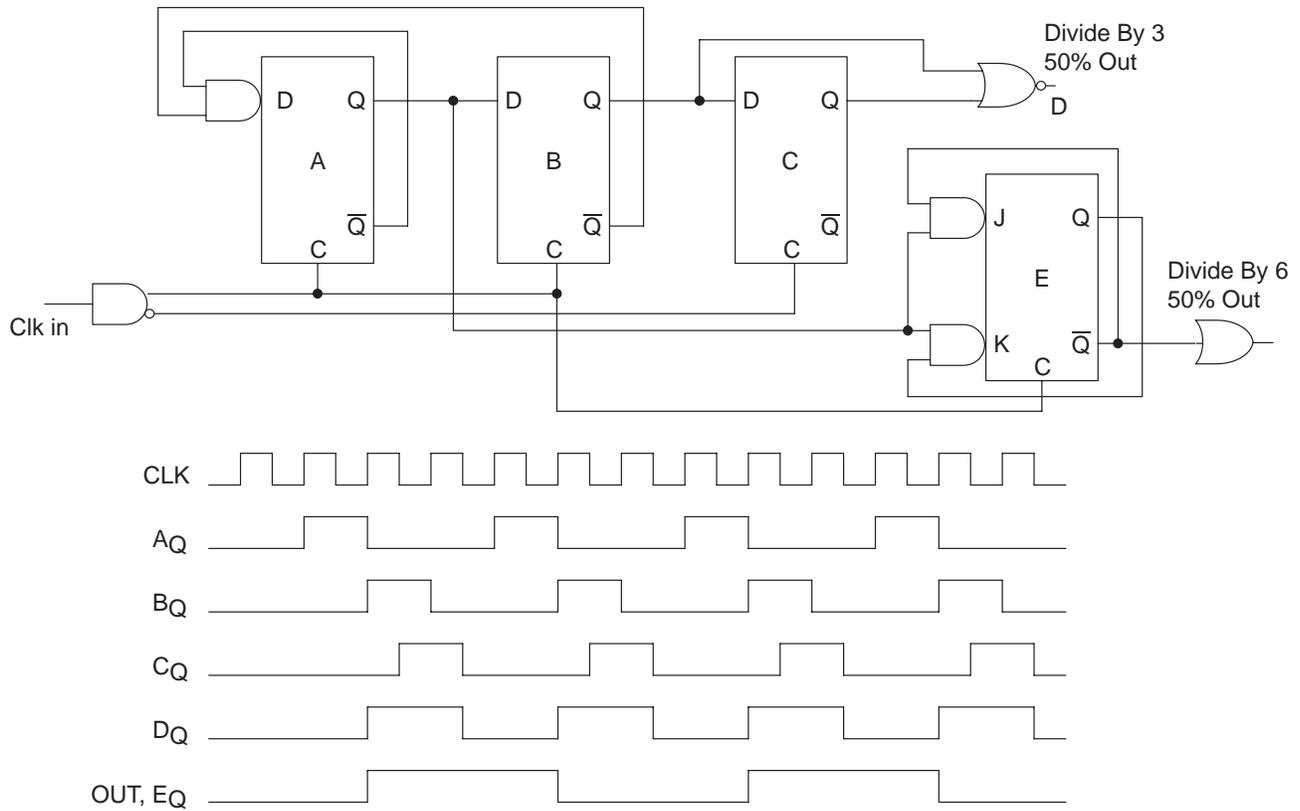


Figure 5.

Of course, there are better ways to realize a Divide By 6 but it does demonstrate how the method works. Note this configuration does not require a 50% input clock duty cycle and it is synchronous. This type of configuration could be

useful in a clock generating PLL chip where a Divide By 3 and Divide By 6 are needed to synchronize two signals as shown in figure 6.

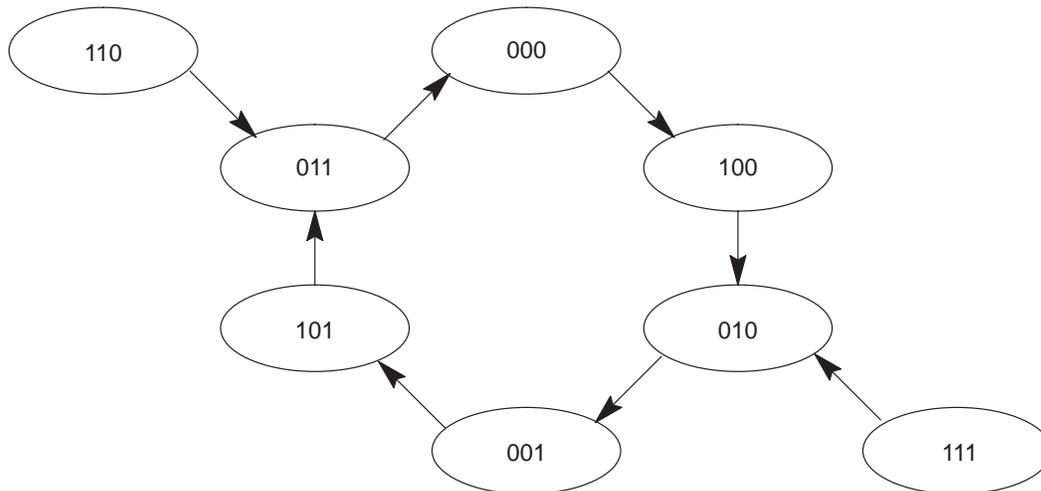
## AND8001/D



**Figure 6.**

Notice FF "A" was chosen as the FF to drive FF "E" in order to align the positive edges of the clock, Divide By 3, and divide by 6. The overall skew of the output could be better matched if all the same type of FF and gates are used.

We already know the Divide By 3 is lockup immune, following flow chart Figure 7 shows that the addition of the J K does not change that situation for the Divide By 6.



**Figure 7. Divide by 6 Flow Chart**

The flow shows no lockup, but if one observes that the J K is a sort of toggle device it is obvious that it can't lock up the counter.

The J K may need bigger input AND gates to accomplish larger divide numbers. As an example, pick a Divide By 12 and use J K type FF's to do the function.

# AND8001/D

Maps show:

Ja = 1      JB = AC\*  
Ka = 1      Kb = A

Jc = AB  
Kc = A

Figure 8 shows the implementation.

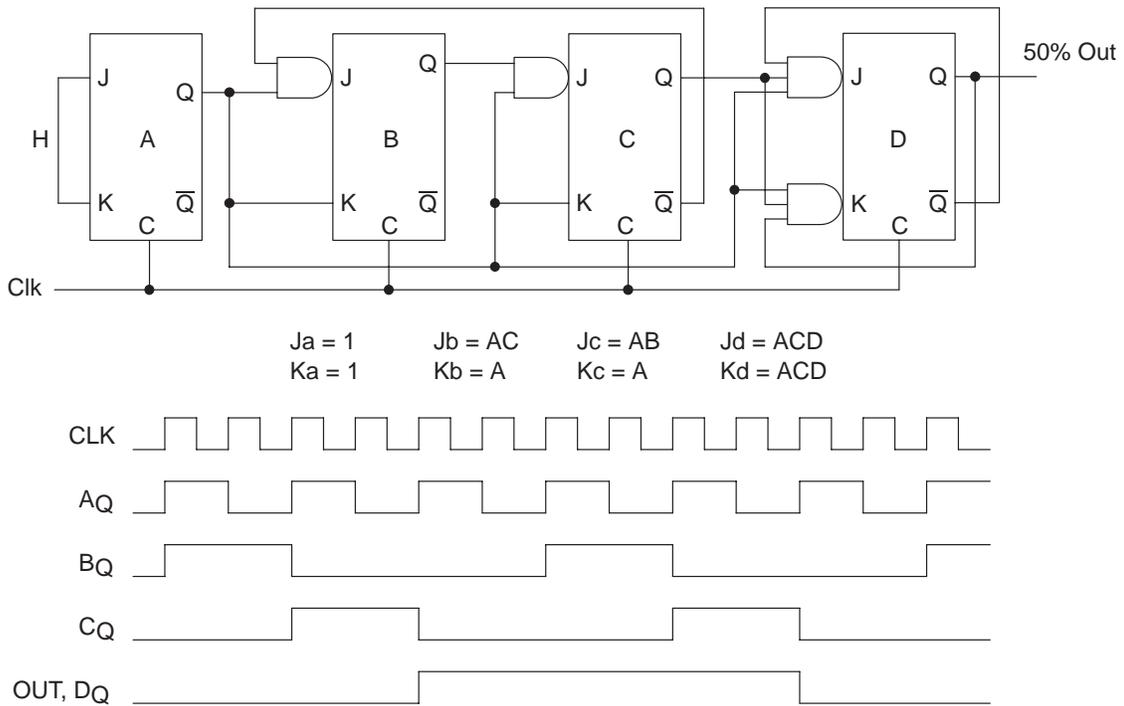


Figure 8. Synchronous Divide By 12

	A	B	C	D
0	0	0	0	0
1	1	0	0	0
2	0	1	0	0
3	1	1	0	0
4	0	0	1	0
5	1	0	1	0*
6	0	0	0	1
7	1	0	0	1
8	0	1	0	1
9	1	1	0	1
10	0	0	1	1
11	1	0	1	1*

The truth table shows that the FF "D" must change state at 5 and 13

Examination of the truth table shows that the FF "D" must decode a 5 and a 13 in order to make the desired 50% function.

The inputs to the "D" FF are  $J = ACD^*$  and  $K = ACD$  and requires 3 input AND gates. For larger counters the inputs on the AND gates will need to increase to reach the desired configuration; However for the single digit integers such as 3, 5, 7, & 9 to realize 6, 10, 14, & 18 a fan in of three is max.

The methods are expandable. A little observation, thinking, and logic typing will allow the designer to minimize the component count and skew on this type of counter.

**ON Semiconductor** and  are trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer.

**PUBLICATION ORDERING INFORMATION**

**USA/EUROPE Literature Fulfillment:**  
Literature Distribution Center for ON Semiconductor  
P.O. Box 5163, Denver, Colorado 80217 USA  
**Phone:** 303-675-2175 or 800-344-3860 Toll Free USA/Canada  
**Fax:** 303-675-2176 or 800-344-3867 Toll Free USA/Canada  
**Email:** ONlit@hibbertco.com

**Fax Response Line\*:** 303-675-2167  
800-344-3810 Toll Free USA/Canada  
\*To receive a Fax of our publications

**N. America Technical Support:** 800-282-9855 Toll Free USA/Canada

**ASIA/PACIFIC:** LDC for ON Semiconductor – Asia Support  
**Phone:** 303-675-2121 (Tue-Fri 9:00am to 1:00pm, Hong Kong Time)  
**Email:** ONlit-asia@hibbertco.com

**JAPAN:** ON Semiconductor, Japan Customer Focus Center  
4-32-1 Nishi-Gotanda, Shinagawa-ku, Tokyo, Japan 141-8549  
**Phone:** 81-3-5487-8345  
**Email:** r14153@onsemi.com

**ON Semiconductor Website:** <http://onsemi.com>

For additional information, please contact your local Sales Representative.