DATA SHEET

NEC

# MOS FIELD EFFECT TRANSISTOR
# 2SK4145

## SWITCHING
## N-CHANNEL POWER MOS FET

### DESCRIPTION

The 2SK4145 is N-channel MOS Field Effect Transistor designed for high current switching applications.

### FEATURES

- Low on-state resistance

  $R_{DS(on)}$ = 10 mΩ MAX. ($V_{GS}$ = 10 V, $I_D$ = 42 A)

- Low input capacitance

  $C_{iss}$ = 5300 pF TYP.

### ORDERING INFORMATION

| PART NUMBER | LEAD PLATING | PACKING | PACKAGE |
|---|---|---|---|
| 2SK4145-S19-AY Note | Pure Sn (Tin) | Tube 50 p/tube | TO-220 typ. 1.9 g |

**Note** Pb-free (This product does not contain Pb in the external electrode).

### ABSOLUTE MAXIMUM RATINGS ($T_A$ = 25°C)

| | | | |
|---|---|---|---|
| Drain to Source Voltage ($V_{GS}$ = 0 V) | $V_{DSS}$ | 60 | V |
| Gate to Source Voltage ($V_{DS}$ = 0 V) | $V_{GSS}$ | ±20 | V |
| Drain Current (DC) ($T_C$ = 25°C) | $I_{D(DC)}$ | ±84 | A |
| Drain Current (pulse) Note1 | $I_{D(pulse)}$ | ±215 | A |
| Total Power Dissipation ($T_C$ = 25°C) | $P_{T1}$ | 84 | W |
| Total Power Dissipation ($T_A$ = 25°C) | $P_{T2}$ | 1.5 | W |
| Channel Temperature | $T_{ch}$ | 150 | °C |
| Storage Temperature | $T_{stg}$ | −55 to +150 | °C |
| Single Avalanche Current Note2 | $I_{AS}$ | 32 | A |
| Single Avalanche Energy Note2 | $E_{AS}$ | 102 | mJ |



**Notes 1.** PW ≤ 10 μs, Duty Cycle ≤ 1%

**2.** Starting $T_{ch}$ = 25°C, $V_{DD}$ = 30 V, $R_G$ = 25 Ω, $V_{GS}$ = 20 → 0 V, L = 100 μH

### THERMAL RESISTANCE

| | | | |
|---|---|---|---|
| Channel to Case Thermal Resistance | $R_{th(ch-C)}$ | 1.49 | °C/W |
| Channel to Ambient Thermal Resistance | $R_{th(ch-A)}$ | 83.3 | °C/W |



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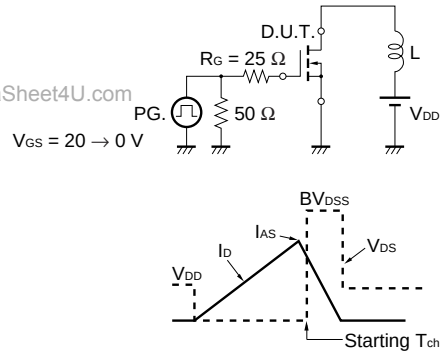
**The mark <R> shows major revised points.**
**The revised points can be easily searched by copying an "<R>" in the PDF file and specifying it in the "Find what:" field.**

## ELECTRICAL CHARACTERISTICS ($T_A$ = 25°C)

| CHARACTERISTICS | SYMBOL | TEST CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| Zero Gate Voltage Drain Current | $I_{DSS}$ | $V_{DS}$ = 60 V, $V_{GS}$ = 0 V | | | 10 | μA |
| Gate Leakage Current | $I_{GSS}$ | $V_{GS}$ = ±20 V, $V_{DS}$ = 0 V | | | ±100 | nA |
| Gate to Source Cut-off Voltage | $V_{GS(off)}$ | $V_{DS}$ = 10 V, $I_D$ = 1 mA | 2.0 | 3.0 | 4.0 | V |
| Forward Transfer Admittance Note | $\|y_{fs}\|$ | $V_{DS}$ = 10 V, $I_D$ = 30 A | 16 | 31 | | S |
| Drain to Source On-state Resistance Note | $R_{DS(on)}$ | $V_{GS}$ = 10 V, $I_D$ = 42 A | | 7 | 10 | mΩ |
| Input Capacitance | $C_{iss}$ | $V_{DS}$ = 10 V, | | 5300 | | pF |
| Output Capacitance | $C_{oss}$ | $V_{GS}$ = 0 V, | | 540 | | pF |
| Reverse Transfer Capacitance | $C_{rss}$ | f = 1 MHz | | 330 | | pF |
| Turn-on Delay Time | $t_{d(on)}$ | $V_{DD}$ = 30 V, $I_D$ = 42 A, | | 25 | | ns |
| Rise Time | $t_r$ | $V_{GS}$ = 10 V, | | 17 | | ns |
| Turn-off Delay Time | $t_{d(off)}$ | $R_G$ = 0 Ω | | 66 | | ns |
| Fall Time | $t_f$ | | | 9 | | ns |
| Total Gate Charge | $Q_G$ | $V_{DD}$ = 48 V, | | 90 | | nC |
| Gate to Source Charge | $Q_{GS}$ | $V_{GS}$ = 10 V, | | 21 | | nC |
| Gate to Drain Charge | $Q_{GD}$ | $I_D$ = 84 A | | 30 | | nC |
| Body Diode Forward Voltage Note | $V_{F(S-D)}$ | $I_F$ = 84 A, $V_{GS}$ = 0 V | | 1.0 | 1.5 | V |
| Reverse Recovery Time | $t_{rr}$ | $I_F$ = 84 A, $V_{GS}$ = 0 V, | | 43 | | ns |
| Reverse Recovery Charge | $Q_{rr}$ | di/dt = 100 A/μs | | 62 | | nC |

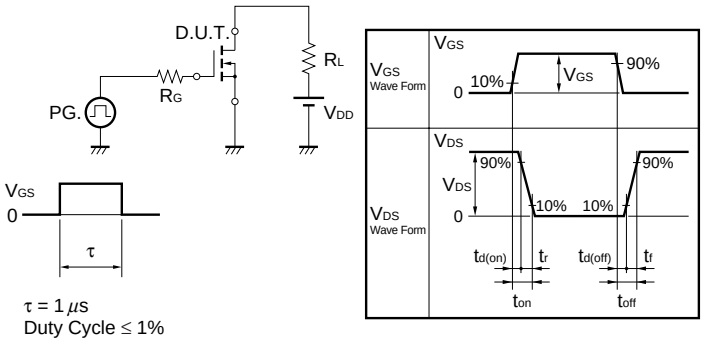
**Note** Pulsed

### TEST CIRCUIT 1 AVALANCHE CAPABILITY

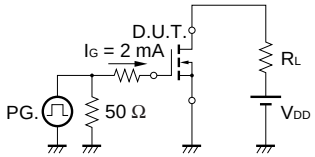





### TEST CIRCUIT 2 SWITCHING TIME

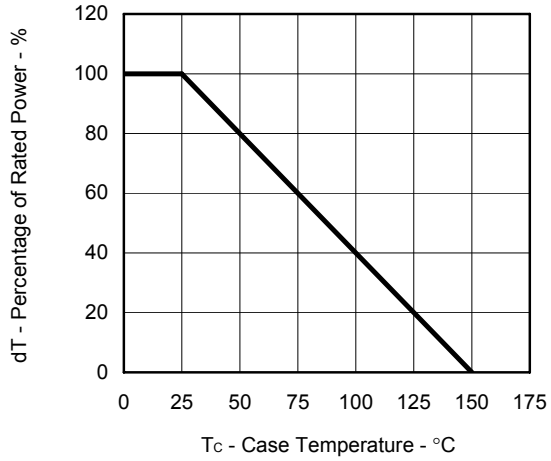



### TEST CIRCUIT 3 GATE CHARGE

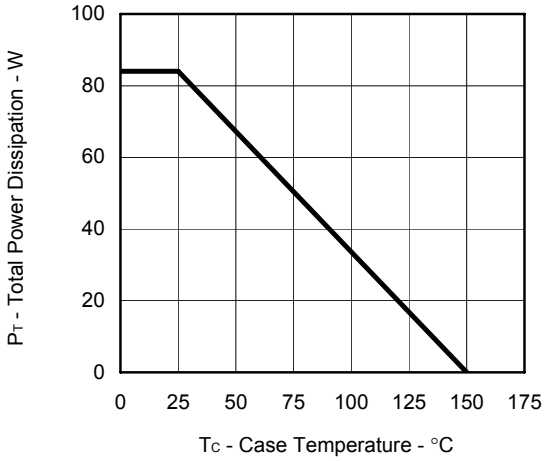


## TYPICAL CHARACTERISTICS ($T_A$ = 25°C)

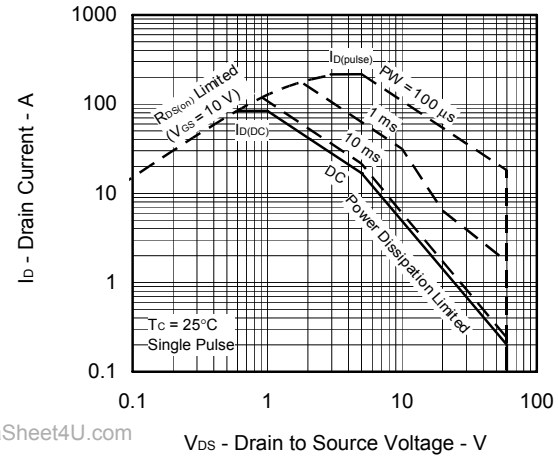
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA




TOTAL POWER DISSIPATION vs. CASE TEMPERATURE

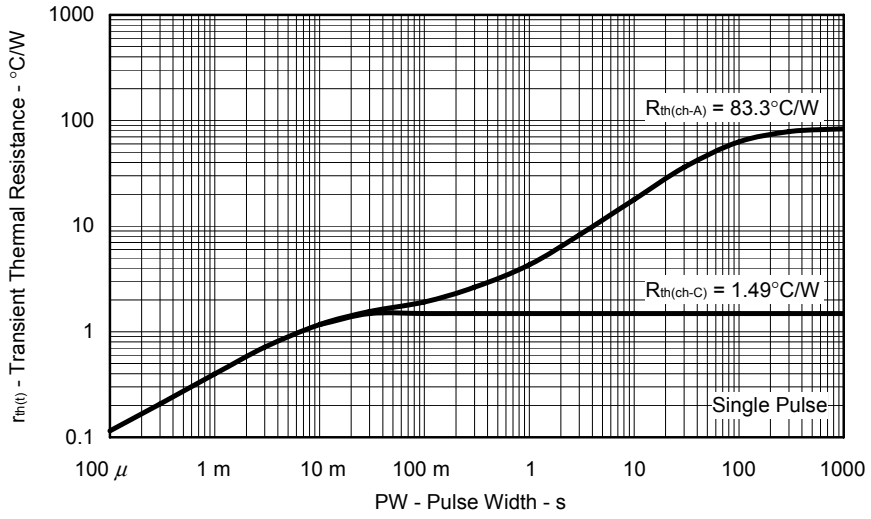



<R> FORWARD BIAS SAFE OPERATING AREA

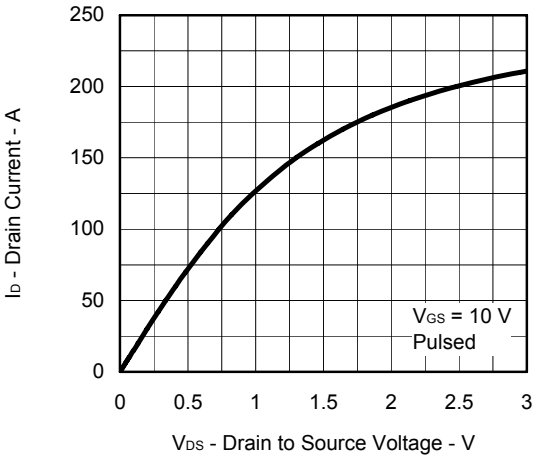




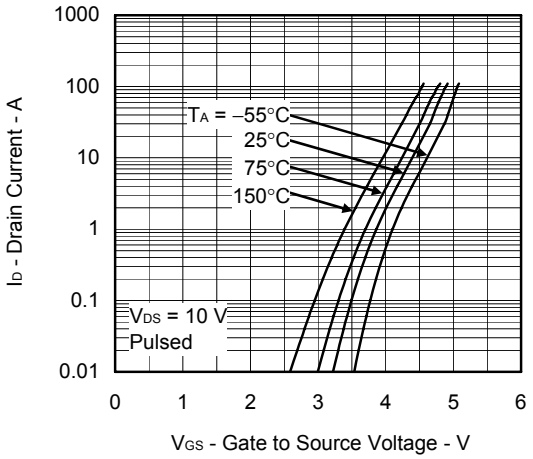

<R> TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



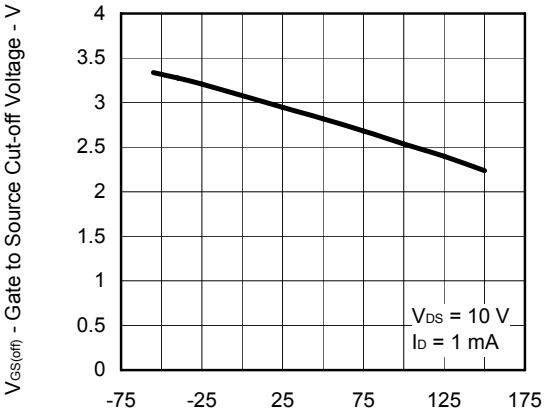
DRAIN CURRENT vs.
DRAIN TO SOURCE VOLTAGE




FORWARD TRANSFER CHARACTERISTICS

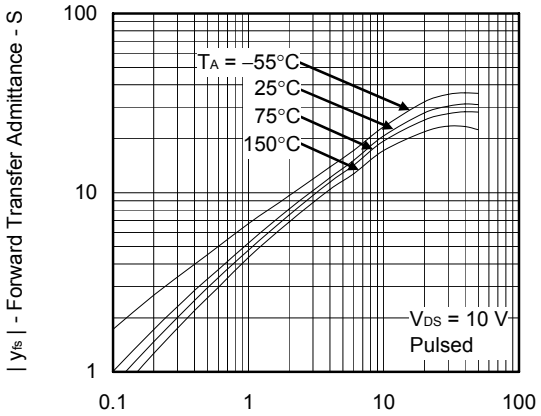



GATE TO SOURCE CUT-OFF VOLTAGE vs.
CHANNEL TEMPERATURE

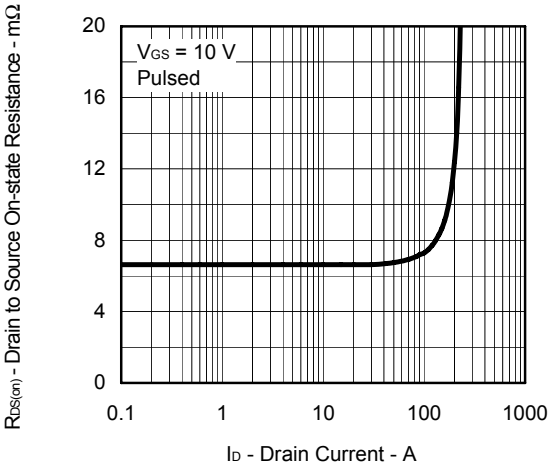




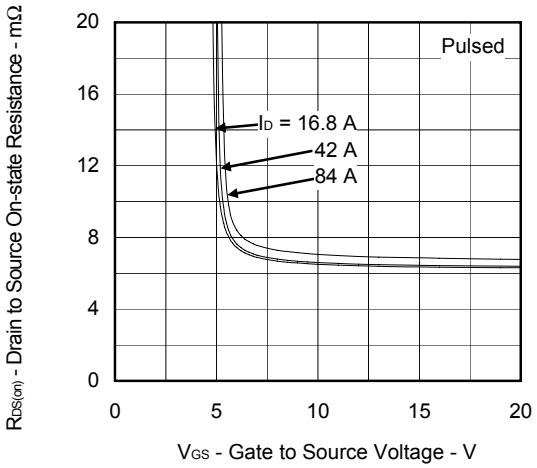

FORWARD TRANSFER ADMITTANCE vs.
DRAIN CURRENT



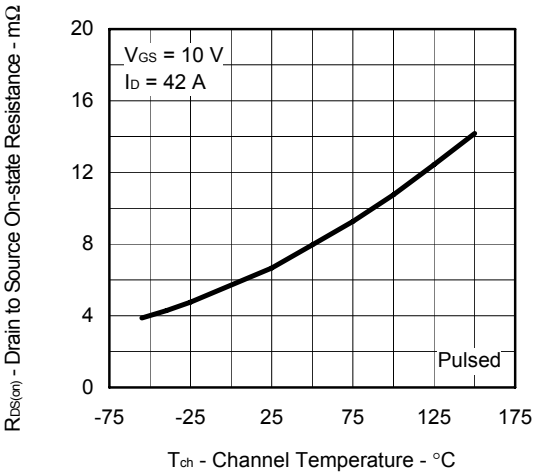

DRAIN TO SOURCE ON-STATE RESISTANCE vs.
DRAIN CURRENT



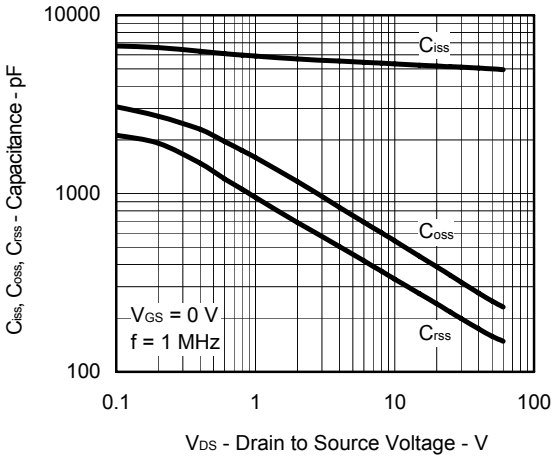

DRAIN TO SOURCE ON-STATE RESISTANCE vs.
GATE TO SOURCE VOLTAGE



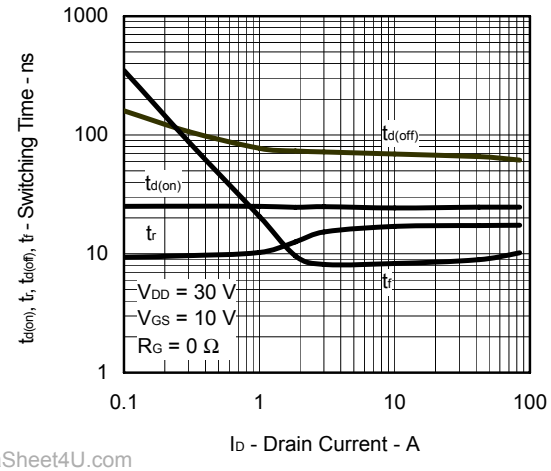
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



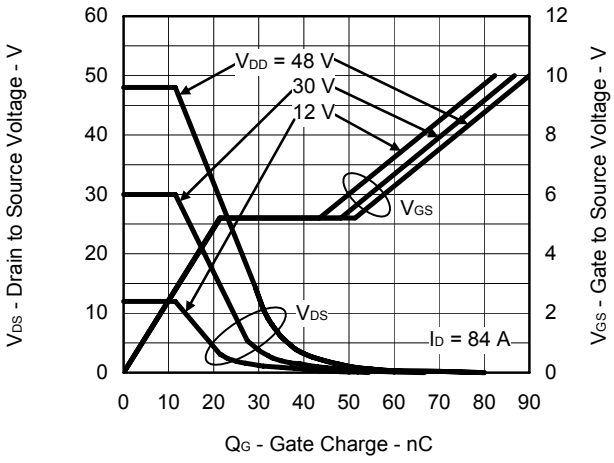

CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE




SWITCHING CHARACTERISTICS

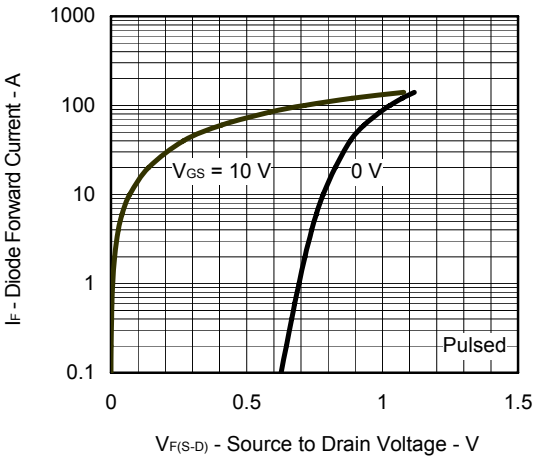



DYNAMIC INPUT/OUTPUT CHARACTERISTICS

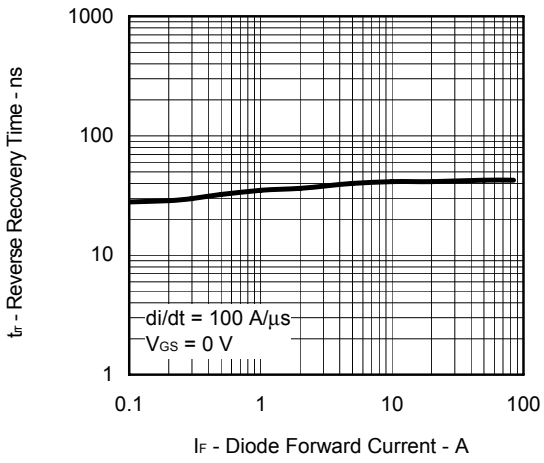





SOURCE TO DRAIN DIODE FORWARD VOLTAGE

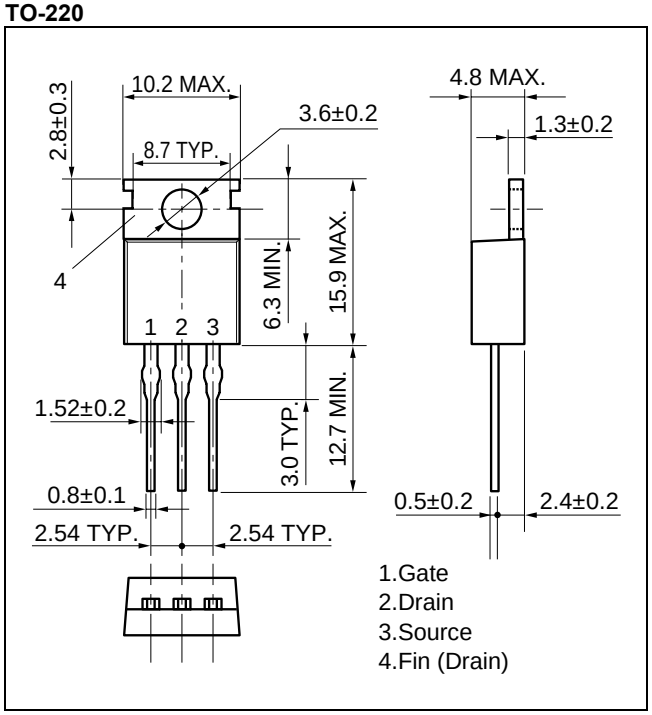



REVERSE RECOVERY TIME vs. DIODE FORWARD CURRENT

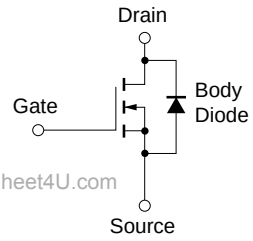


## PACKAGE DRAWING (Unit: mm)

**TO-220**



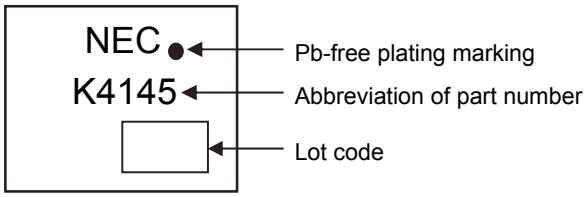

## EQUIVALENT CIRCUIT






**Remark** Strong electric field, when exposed to this device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred.

## MARKING INFORMATION




## RECOMMENDED SOLDERING CONDITIONS

The 2SK4145 should be soldered and mounted under the following recommended conditions.

For soldering methods and conditions other than those recommended below, please contact an NEC Electronics sales representative.

For technical information, see the following website.

Semiconductor Device Mount Manual (http://www.necel.com/pkg/en/mount/index.html)

| Soldering Method | Soldering Conditions | Recommended Condition Symbol |
|---|---|---|
| Wave soldering | Maximum temperature (Solder temperature): 260°C or below<br>Time: 10 seconds or less<br>Maximum chlorine content of rosin flux: 0.2% (wt.) or less | THDWS |
| Partial heating | Maximum temperature (Pin temperature): 350°C or below<br>Time (per side of the device): 3 seconds or less<br>Maximum chlorine content of rosin flux: 0.2% (wt.) or less | P350 |

**Caution Do not use different soldering methods together (except for partial heating).**

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