AK4140

Digital BTSC Decoder

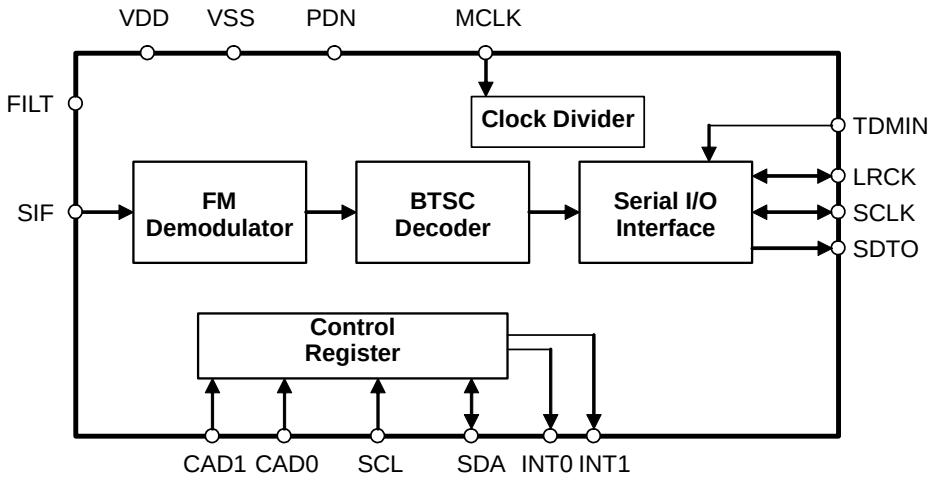
GENERAL DESCRIPTION

The AK4140 is a BTSC decoder, which is optimized for Digital STB/TV application. The AK4140 achieves high audio performance using original demodulation techniques for 4.5MHz inter-carrier sound, and the digital BTSC decoding architecture using digital dbx-TV® technology licensed from THAT Corporation requires no alignment of external parts. The AK4140 supports major audio data formats (MSB justified, I^2S, TDM) to interface with usual DSP. Therefore, the AK4140 is suitable for the systems such as Digital STB/TV, AV recorder etc.

The dbx-TV® brand identifies a range of technology solutions for digital TV-audio decoding developed and licensed by THAT Corporation. The dbx-TV provides high performance solutions with high quality sound.

FEATURES

- ☐ **Capable of receiving 4.5MHz intercarrier sound and FM demodulation**
- ☐ **Alignment Free Digital BTSC decoding (Mono/Stereo/SAP)**
- ☐ **Programmable pilot/SAP/noise detection threshold**
- ☐ **Automatic return to mono dependant on pilot/noise level**
- ☐ **Mono/Stereo/SAP selectable output**
- ☐ **Digital volume control**
- ☐ **Soft Mute function**
- ☐ **Digital HPF for DC-Offset cancel**
- ☐ **Sampling Rate (fs): 32k/44.1k/48kHz**
- ☐ **Master Clock: 256fs/384fs/512fs/768fs**
- ☐ **Audio Interface: Master or Slave Mode**
- ☐ **Output format: 16bit MSB justified / I^2S or TDM**
- ☐ **S/(N+D): 0.13%**
- ☐ **S/N: 73dB**
- ☐ **Power Supply: 2.7 ~ 3.6V**
- ☐ **Ta: -20 ~ 85°C**



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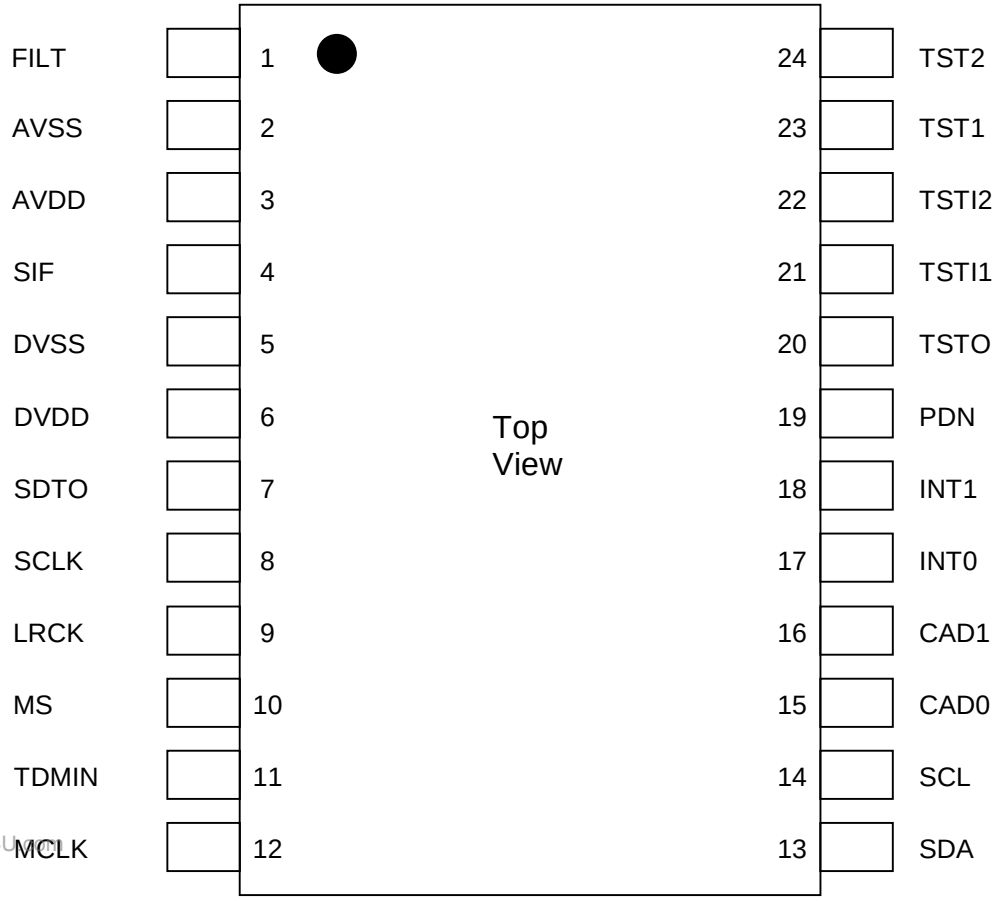
■ Ordering Guide

AK4140VF	-20 ~ +85°C	24pin VSOP
AKD4140	Evaluation Board	

■ Pin Layout



PIN/FUNCTION

No.	Pin Name	I/O	Function
1	FILT	-	Filter Pin 2.2nF should be connected between FILT pin and VSS pin.
2	AVSS	-	Analog Ground Pin
3	AVDD	-	Analog Power Supply Pin, 2.7 ~ 3.3V
4	SIF	I	4.5MHz SIF Input Pin. Should be AC-coupled with 68nF.
5	DVSS	-	Digital Ground Pin
6	DVDD	-	Digital Power Supply Pin, 2.7 ~ 3.3V
7	SDTO	O	Audio Serial Data Output Pin "L" Output at Power-down mode.
8	SCLK	I/O	Audio Serial Data Clock Pin "L" Output in Master Mode at Power-down mode.
9	LRCK	I/O	Output Channel Clock Pin "L" Output in Master Mode at Power-down mode.
10	MS	I	Master/Slave Control Pin "H": Master Mode, "L": Slave Mode
11	TDMIN	I	TDM Serial Data Input Pin Should be connected to "L" in normal mode.
12	MCLK	I	Master Clock Input Pin
13	SDA	I/O	Control Data Pin.
14	SCL	I	Control Data Clock Pin.
15	CAD0	I	Chip Address Pin 0
16	CAD1	I	Chip Address Pin 1
17	INT0	O	Interrupt Pin 0
18	INT1	O	Interrupt Pin 1
19	PDN	I	Power Down Mode Pin "H": Power up, "L": Power down and reset. The AK4140 must be reset once upon power-up.
20	TSTO	O	Test Output Pin Should be open.
21	TSTI1	I	Test Input Pin 1 (pull-down pin. typ: 150k ohm.) Should be connected to DVSS.
22	TSTI2	I	Test Input Pin 2 Should be connected to DVSS.
23	TST1	I	Test Mode Pin 1 (pull-down pin. typ: 150k ohm.) Should be connected to DVSS.
24	TST2	I	Test Mode Pin 2 (pull-down pin. typ: 150k ohm.) Should be connected to DVSS.

ABSOLUTE MAXIMUM RATINGS

(AVSS=DVSS=0V; Note 1)

Parameter		Symbol	min	max	Units
Power Supplies (Note 2)	Analog	AVDD	-0.3	4.6	V
	Digital	DVDD	-0.3	4.6	V
Input Current, Any Pin Except Supply		IIN	-	±10	mA
Analog Input Voltage		VINA	–0.3	AVDD+0.3	V
Digital Input Voltage		VIND	–0.3	DVDD+0.3	V
Ambient Temperature (powered applied)		Ta	–20	85	°C
Storage Temperature		Tstg	–65	150	°C

Note 1. All voltages with respect to ground.
Note 2. AVSS and DVSS must be connected to the same analog ground plane.

WARNING: Operation at or beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS

(AVSS=DVSS=0V;Note 1)

Parameter		Symbol	min	typ	max	Units
Power Supplies	AVDD	AVDD	2.7	3.3	3.6	V
	DVDD	DVDD	2.7	3.3	3.6	V

WARNING: AKM assumes no responsibility for the usage beyond the conditions in this datasheet.

AUDIO CHARACTERISTICS

(Ta=25°C; AVDD=DVDD=3.3V; AVSS=DVSS=0V; fs=48kHz; SCLK=64fs; Signal Frequency=1kHz; 16bit Data; Measurement frequency=50Hz ~ 13kHz; unless otherwise specified)

Parameter		Min	typ	max	Units
Resolution				16	Bits
Input Voltage		100			mVrms
S/(N+D)	(1kHz, 100% modulation) mono		0.13		%
	(1kHz, 66% modulation L or R) Stereo		0.13		%
	(1kHz, 100% modulation) SAP		0.86		%
S/N (A-weighted)	(input off) mono		73		dB
	(input off) Stereo		73		dB
	(input off) SAP		80		dB
Interchannel Isolation		20	35		dB
Frequency response	(50~12kHz) mono	-1		1	dB
	(50~12kHz) Stereo	-1		1	dB
	(50~9kHz) SAP	-1		1	dB
Power Supplies					
Power Supply Current					
Normal Operation (PDN pin = "H"): VDD			50	80	mA
Power down mode (PDN pin = "L"): VDD (Note 3)			10	100	μA

Note 3. All digital input pins are held to VSS.

FILTER CHARACTERISTICS (MONO/STEREO)

(Ta=-20~ 85°C; AVDD=DVDD=2.7~3.6V, fs=48kHz)

Parameter		Symbol	min	typ	max	Units
Digital Filter (LPF):						
Passband	±1dB	PB			12	kHz
Group Delay	(Note 4)	GD		13		1/fs
Digital Filter (HPF):						
Frequency Response	–3dB	FR		1.0		Hz
	–0.1dB			6.5		Hz

FILTER CHARACTERISTICS (SAP)

(Ta=-20~ 85°C; AVDD=DVDD=2.7~3.6V, fs=48kHz)

Parameter		Symbol	min	typ	max	Units
Digital Filter (LPF):						
Passband (Note 9)	±1dB	PB			9	kHz
Group Delay	(Note 4)	GD		24		1/fs
Digital Filter (HPF):						
Frequency Response	–3dB	FR		1.0		Hz
	–0.1dB			6.5		Hz

Note 4. The calculated delay time induced by digital filtering. This time is from the input of an analog signal to the setting of 16bit data both channels to the output register for the device.

DC CHARACTERISTICS

(Ta=-20~ 85°C; AVDD=DVDD=2.7~3.6V)

Parameter	Symbol	min	typ	Max	Units
High-Level Input Voltage	VIH	70%VDD	-	-	V
Low-Level Input Voltage	VIL	-	-	30%VDD	V
High-Level Output Voltage (Iout=-400μA)	VOH	VDD-0.4	-	-	V
Low-Level Output Voltage					
(Except SDA pin: Iout= 400μA)	VOL	-	-	0.4	V
(SDA pin: Iout= 3mA)	VOL	-	-	0.4	V
Input Leakage Current	Iin	-	-	± 10	μA

SWITCHING CHARACTERISTICS

(Ta=-20~ 85°C; AVDD=DVDD=2.7~3.6V; C_L=20pF)

Parameter	Symbol	min	typ	max	Units
Master Clock Timing					
Master Clock 256fs:	fCLK	8.192		12.288	MHz
Pulse Width Low	tCLKL	27			ns
Pulse Width High	tCLKH	27			ns
384fs:	fCLK	12.288		18.432	MHz
Pulse Width Low	tCLKL	20			ns
Pulse Width High	tCLKH	20			ns
512fs:	fCLK	16.384		24.576	MHz
Pulse Width Low	tCLKL	16			ns
Pulse Width High	tCLKH	16			ns
768fs:	fCLK	24.576		36.864	MHz
Pulse Width Low	tCLKL	11			ns
Pulse Width High	tCLKH	11			ns
LRCK Timing (Slave Mode)					
Normal mode (TDM1="L", TDM0="L")					
LRCK Frequency	fs	32		48	kHz
Duty Cycle	Duty	45		55	%
TDM256 MODE (TDM1="L", TDM0="H")					
LRCK Frequency	fs	32		48	kHz
"H" time	tLRH	1/256fs			ns
"L" time	tLRL	1/256fs			ns
TDM128 MODE (TDM1="H", TDM0="H")					
LRCK Frequency	fs	32		48	kHz
"H" time	tLRH	1/128fs			ns
"L" time	tLRL	1/128fs			ns
LRCK Timing (Master Mode)					
Normal mode (TDM1="L", TDM0="L")					
LRCK Frequency	fs	32		48	kHz
Duty Cycle	Duty		50		%
TDM256 MODE (TDM1="L", TDM0="H")					
LRCK Frequency	fs	32		48	kHz
"H" time (Note 5)	tLRH		1/8fs		ns
TDM128 MODE (TDM1="H", TDM0="H")					
LRCK Frequency	fs	32		48	kHz
"H" time (Note 5)	tLRH		1/4fs		ns

Note 5. "L" time at I^2S format.

Parameter		Symbol	min	typ	max	Units
Audio Interface Timing (Slave mode)						
Normal mode (TDM1="L", TDM0="L")						
SCLK Period		tBCK	160			ns
SCLK Pulse Width Low		tBCKL	65			ns
Pulse Width High		tBCKH	65			ns
LRCK Edge to SCLK "↑"	(Note 6)	tLRB	30			ns
SCLK "↑" to LRCK Edge	(Note 6)	tBLR	30			ns
LRCK to SDTO(MSB) (Except I^2S mode)		tLRS			35	ns
SCLK "↓" to SDTO		tBSD			35	ns
TDM256 mode (TDM1="L", TDM0="H")						
SCLK Period		tBCK	81			ns
SCLK Pulse Width Low		tBCKL	32			ns
Pulse Width High		tBCKH	32			ns
LRCK Edge to SCLK "↑"	(Note 6)	tLRB	20			ns
SCLK "↑" to LRCK Edge	(Note 6)	tBLR	20			ns
SCLK "↓" to SDTO		tBSD			20	ns
TDMIN Hold Time		tSDH	10			ns
TDMIN Setup Time		tSDS	10			ns
TDM128 mode (TDM1="H", TDM0="H")						
SCLK Period		tBCK	81			ns
SCLK Pulse Width Low		tBCKL	32			ns
Pulse Width High		tBCKH	32			ns
LRCK Edge to SCLK "↑"	(Note 6)	tLRB	20			ns
SCLK "↑" to LRCK Edge	(Note 6)	tBLR	20			ns
SCLK "↓" to SDTO		tBSD			20	ns
TDMIN Hold Time		tSDH	10			ns
TDMIN Setup Time		tSDS	10			ns

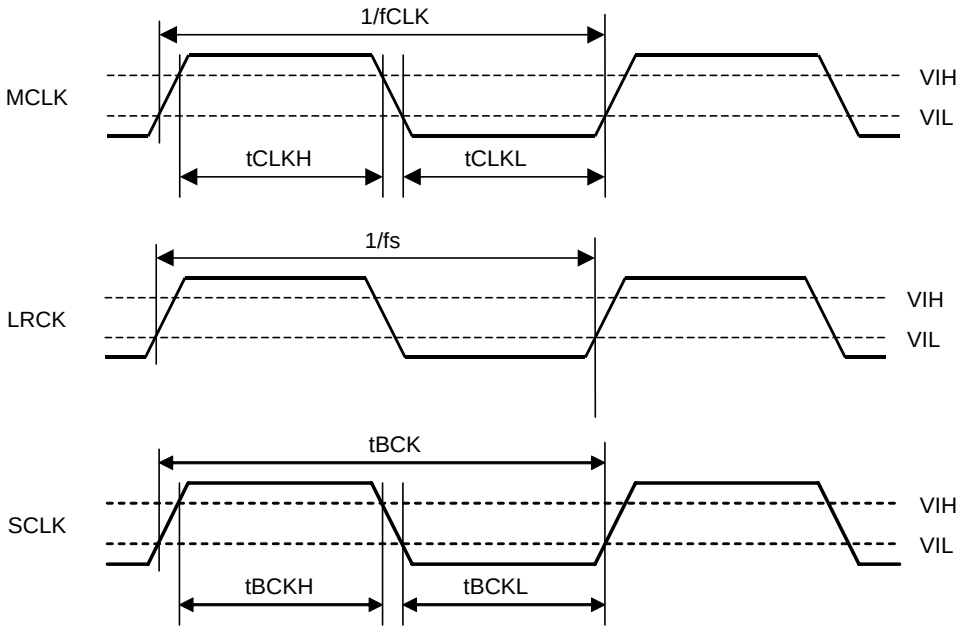
Parameter		Symbol	min	typ	max	Units
Audio Interface Timing (Master mode)						
Normal mode (TDM1="L", TDM0="L")						
SCLK Frequency		fBCK		64fs		Hz
SCLK Duty		dBCK		50		%
SCLK "↓" to LRCK		tMBLR	–20		20	ns
SCLK "↓" to SDTO		tBSD	–40		40	ns
TDM256 mode (TDM1="L", TDM0="H")						
SCLK Frequency		fBCK		256fs		Hz
SCLK Duty	(Note 7)	dBCK		50		%
SCLK "↓" to LRCK		tMBLR	–12		12	ns
SCLK "↓" to SDTO		tBSD	–20		20	ns
TDMIN Hold Time		tSDH	10			ns
TDMIN Setup Time		tSDS	10			ns
TDM128 mode (TDM1="H", TDM0="H")						
SCLK Frequency		fBCK		128fs		Hz
SCLK Duty		dBCK		50		%
SCLK "↓" to LRCK		tMBLR	–12		12	ns
SCLK "↓" to SDTO		tBSD	–20		20	ns
TDMIN Hold Time		tSDH	10			ns
TDMIN Setup Time		tSDS	10			ns
Power-Down & Reset Timing						
PDN Pulse Width	(Note 8)	tPD	150			ns
PDN "↑" to SDTO valid	(Note 9)	tPDV		516		1/fs

Note 6. SCLK rising edge must not occur at the same time as LRCK edge.
Note 7. This value is MCLK=512fs. Duty cycle is not guaranteed when MCLK=256fs/384fs.
Note 8. The AK4140 can be reset by bringing the PDN pin = "L".
Note 9. This cycle is the number of LRCK rising edges from the PDN pin = "H".

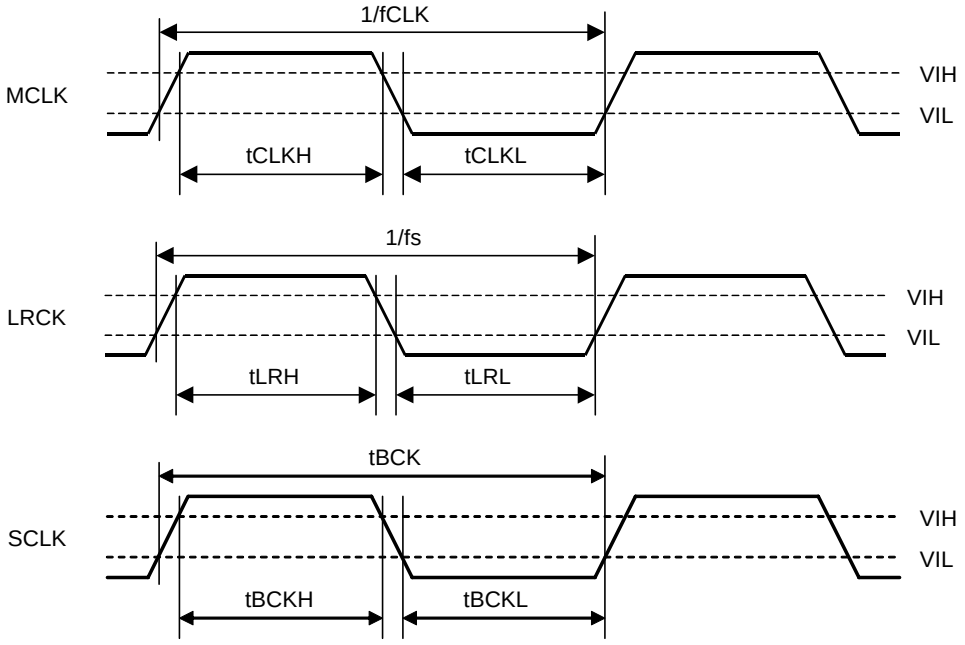
Parameter	Symbol	Min	typ	max	Units
Control Interface Timing (I^2C Bus):					
SCL Clock Frequency	fSCL	-		400	kHz
Bus Free Time Between Transmissions	tBUF	1.3		-	µs
Start Condition Hold Time (prior to first clock pulse)	tHD:STA	0.6		-	µs
Clock Low Time	tLOW	1.3		-	µs
Clock High Time	tHIGH	0.6		-	µs
Setup Time for Repeated Start Condition	tSU:STA	0.6		-	µs
SDA Hold Time from SCL Falling (Note 10)	tHD:DAT	0		-	µs
SDA Setup Time from SCL Rising	tSU:DAT	0.1		-	µs
Rise Time of Both SDA and SCL Lines	tR	-		0.3	µs
Fall Time of Both SDA and SCL Lines	tF	-		0.3	µs
Setup Time for Stop Condition	tSU:STO	0.6		-	µs
Pulse Width of Spike Noise Suppressed by Input Filter	tSP	0		50	ns
Capacitive load on bus	Cb	0		400	pF

Note 10. Data must be held for sufficient time to bridge the 300 ns transition time of SCL.

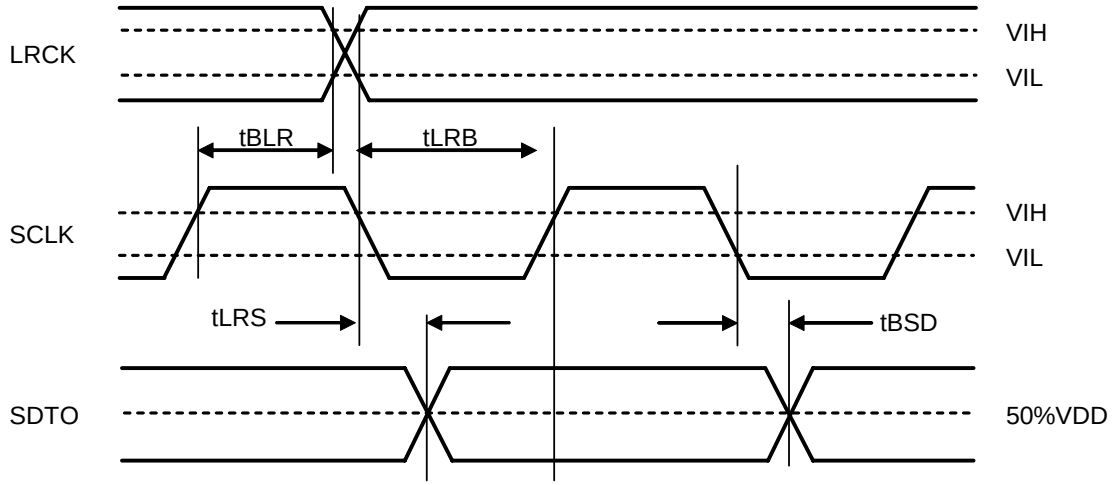
■ Timing Diagram



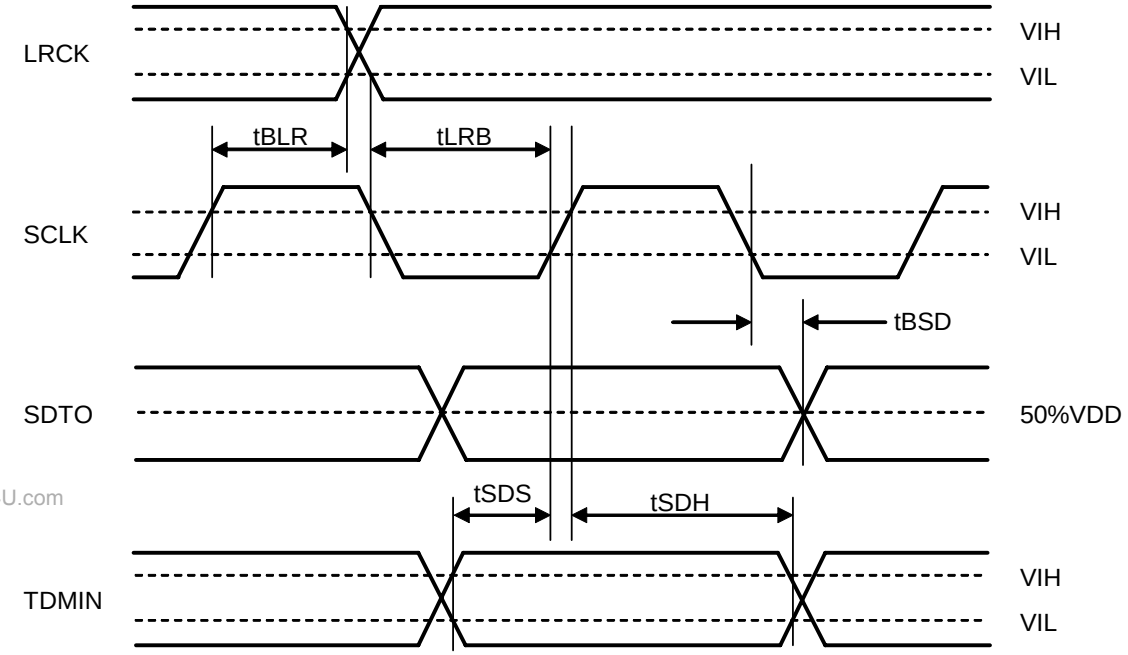
Clock Timing (Normal mode)



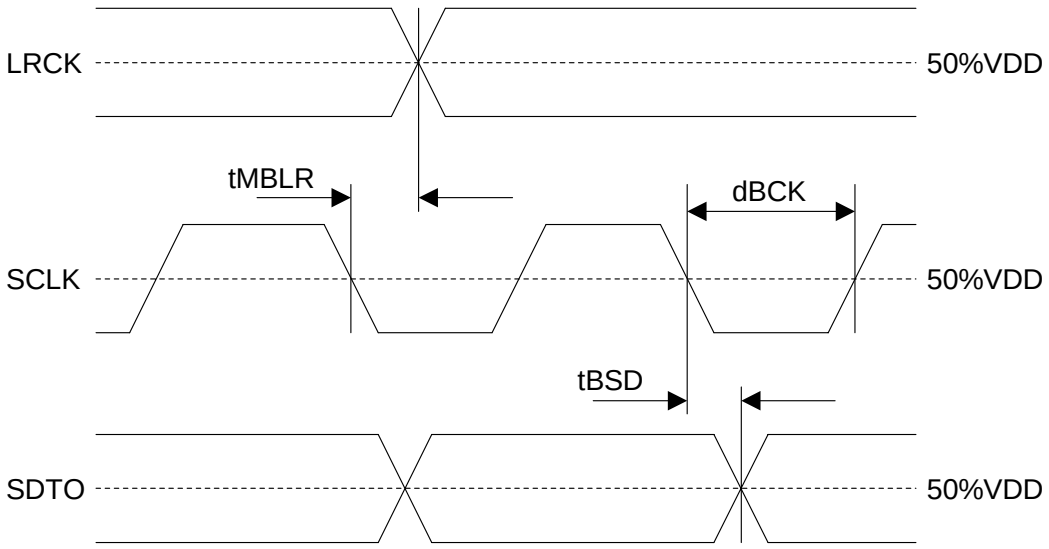
Clock Timing (TDM256/TDM128A/B mode)



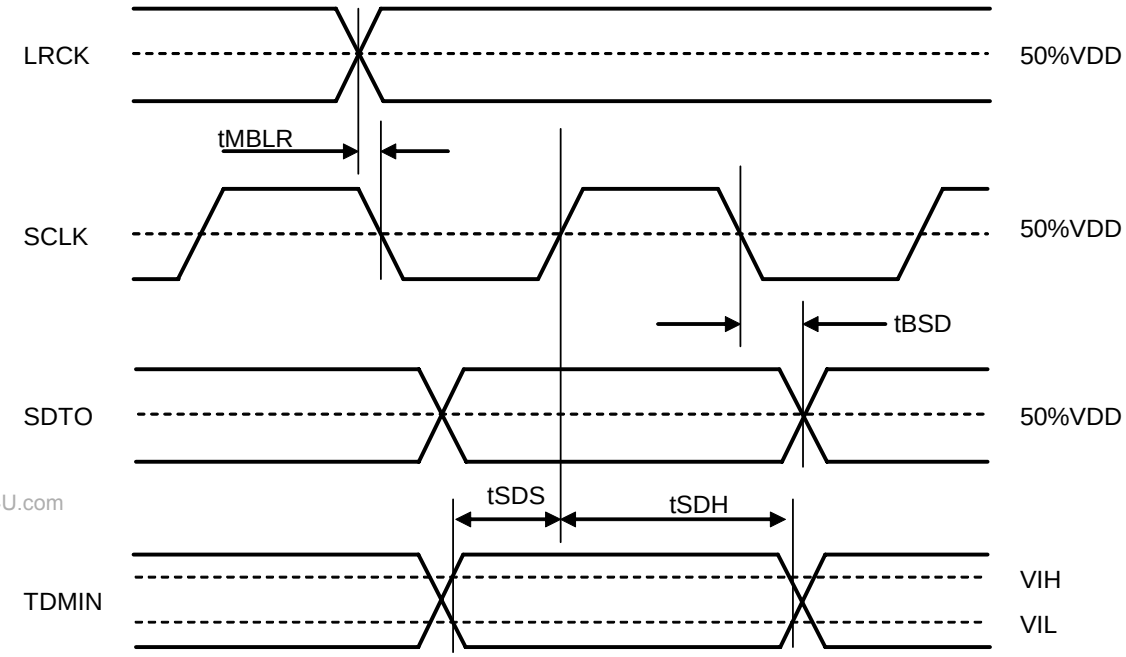
Audio Interface Timing (Slave mode, Normal Mode)



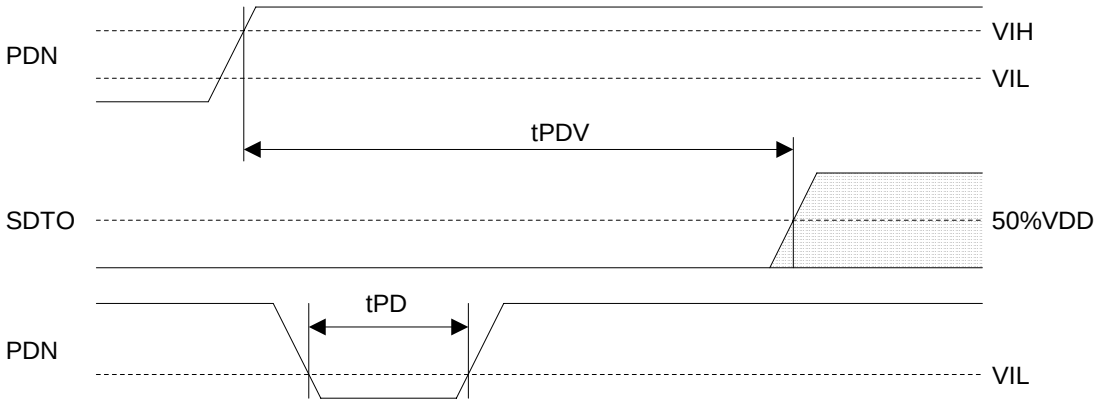
Audio Interface Timing (Slave mode, TDM256/TDM128A/B Mode)



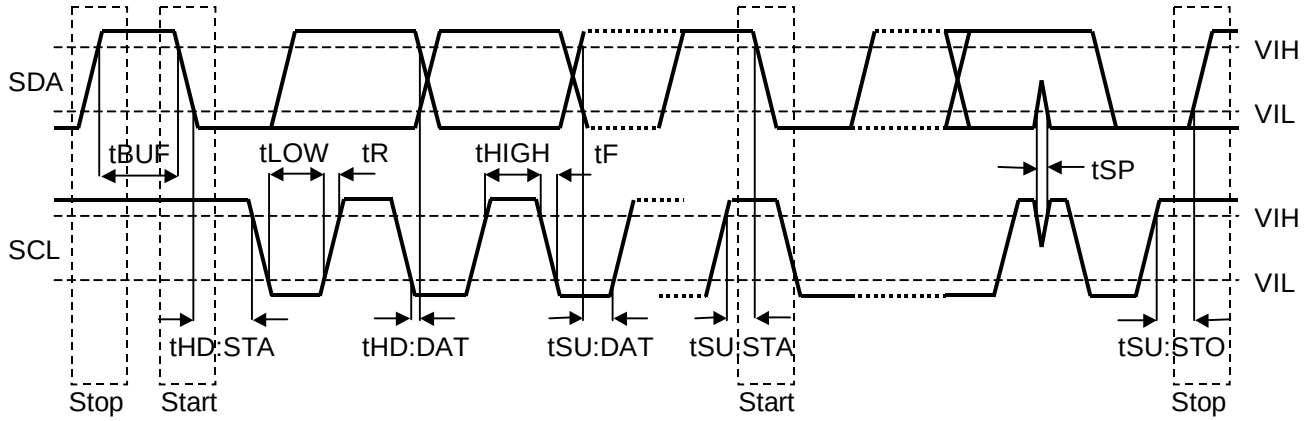
Audio Interface Timing (Master mode, Normal Mode)



Audio Interface Timing (Master mode, TDM256/TDM128A/B Mode)



Power Down & Reset Timing



I^2C Bus mode Timing

OPERATION OVERVIEW

■ System reset and Power-down Mode

The AK4140 should be reset once by bringing PDN PIN = "L" upon power-up.

PDN pin: Power down pin
"H": Normal operation
"L": Device power down & reset.

■ System Clock

The external clocks required to operate the AK4140 are MCLK, LRCK and SCLK. The AK4140 supports 256fs, 384fs, 512fs and 768fs as master clock (MCLK). The CKS1/0 bits select MCLK frequency. The AK4140 should be reset by PDN pin= "L" after these clocks are provided. If the external clocks are not present, place the AK4140 in power-down mode. After exiting reset at power-up etc., the AK4140 remains in power-down mode until MCLK and LRCK are input.

fs	MCLK				SCLK	
	256fs	384fs	512fs	768fs	64fs	128fs
32.0kHz	8.1920MHz	12.2880MHz	16.3840MHz	24.576MHz	2.0480MHz	4.0960MHz
44.1kHz	11.2896MHz	16.9344MHz	22.5792MHz	33.8688MHz	2.8224MHz	5.6448MHz
48.0kHz	12.2880MHz	18.4320MHz	24.5760MHz	36.8640MHz	3.0720MHz	6.1440MHz

Table 1. System clock example (Slave mode)

CKS1 bit	CKS0 bit	MCLK	
0	0	256fs	(default)
0	1	384fs	
1	0	512fs	
1	1	768fs	

Table 2. Master clock frequency select

■ Audio Interface Format

The AK4140 supports 16 types of audio data interface selected by the TDM1-0, DIF bits and M/S pin as shown in Table 3. In all formats the serial data is MSB-first, 2's compliment format. The SDTO is clocked out on the falling edge of SCLK.

In normal mode, Mode 0-1 are the slave mode, and SCLK is available up to 128fs. SCLK outputs 64fs clock in Mode 2-3.

In TDM256 mode, SCLK should be fixed to 256fs. In the slave mode, "H" time and "L" time of LRCK should be 1/256fs at least. In the master mode, "H" time ("L" time at I^2S mode) of LRCK is 1/8fs typically.

In TDM128A mode, SCLK should be fixed to 128fs. In the slave mode, "H" time and "L" time of LRCK should be 1/128fs at least. In the master mode, "H" time ("L" time at I^2S mode) of LRCK is 1/4fs typically.

In TDM128B mode, SCLK should be fixed to 128fs. In the slave mode, "H" time and "L" time of LRCK should be 1/128fs at least. In the master mode, "H" time ("L" time at I^2S mode) of LRCK is 1/8fs typically.

Mode		TDM1 bit	TDM0 bit	M/S pin	DIF bit	SDTO	LRCK		SCLK	
								I/O		I/O
0	Normal (2ch)	0	0	0	0	16bit, MSB justified	H/L	I	32-128fs	I
1					1	16bit, I^{2}S Compatible	L/H	I	32-128fs	I
2				1	0	16bit, MSB justified	H/L	O	64fs	O
3					1	16bit, I^{2}S Compatible	L/H	O	64fs	O
4	TDM256 (max: 8ch)	0	1	0	0	16bit, MSB justified	↑	I	256fs	I
5					1	16bit, I^{2}S Compatible	↓	I	256fs	I
6				1	0	16bit, MSB justified	↑	O	256fs	O
7					1	16bit, I^{2}S Compatible	↓	O	256fs	O
8	TDM128A (max: 4ch)	1	0	0	0	16bit, MSB justified	↑	I	128fs	I
9					1	16bit, I^{2}S Compatible	↓	I	128fs	I
10				1	0	16bit, MSB justified	↑	O	128fs	O
11					1	16bit, I^{2}S Compatible	↓	O	128fs	O
12	TDM128B (max: 8ch)	1	1	0	0	16bit, MSB justified	↑	I	128fs	I
13					1	16bit, I^{2}S Compatible	↓	I	128fs	I
14				1	0	16bit, MSB justified	↑	O	128fs	O
15					1	16bit, I^{2}S Compatible	↓	O	128fs	O

Table 3 Audio Interface Formats (default : Mode 0)

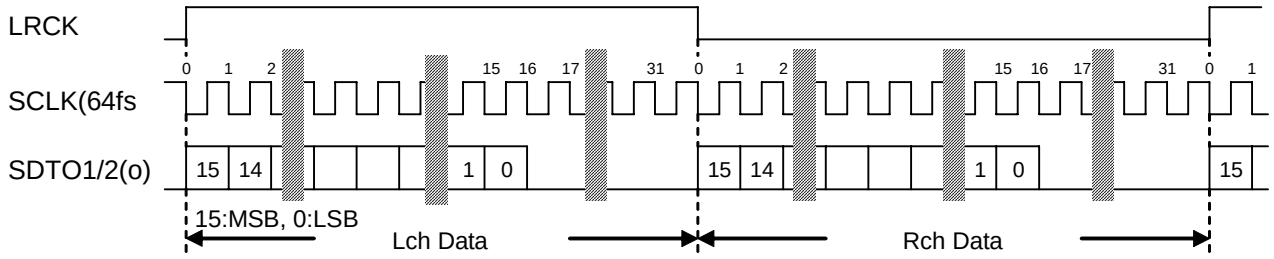


Figure 1. Mode 0, 2 Timing (Normal mode, MSB justified)

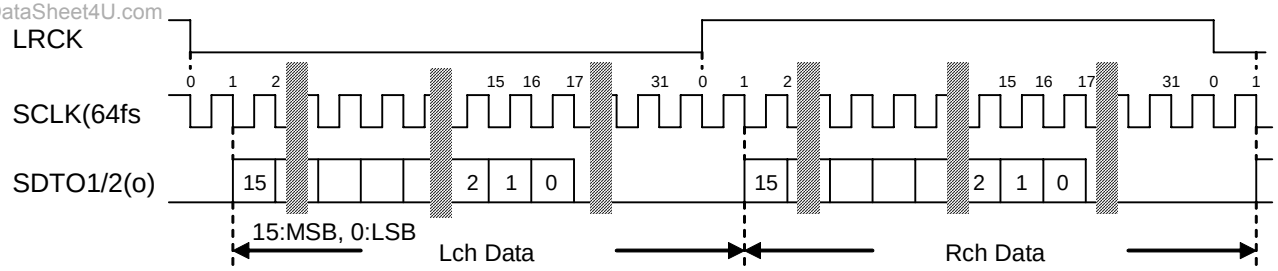


Figure 2. Mode 1, 3 Timing (Normal mode, I^{2}S Compatible)

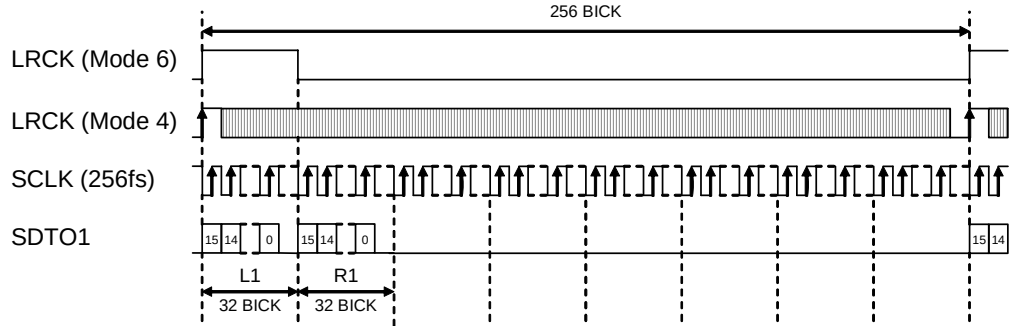


Figure 3. Mode 4, 6 Timing (TDM256 mode, MSB justified)

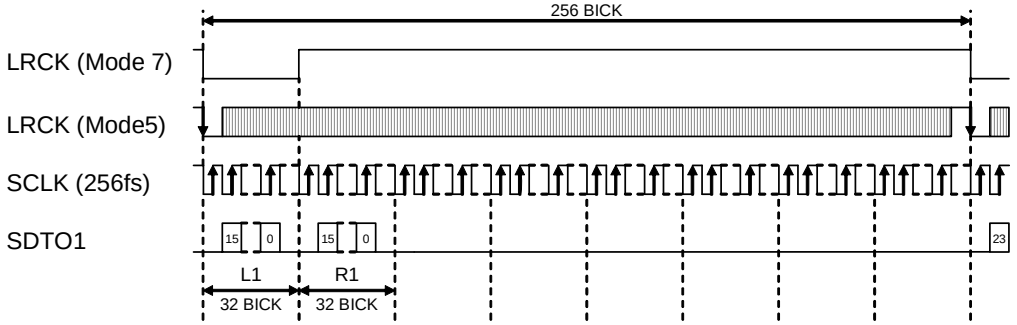


Figure 4. Mode 5, 7 Timing (TDM256 mode, I^{2}S Compatible)

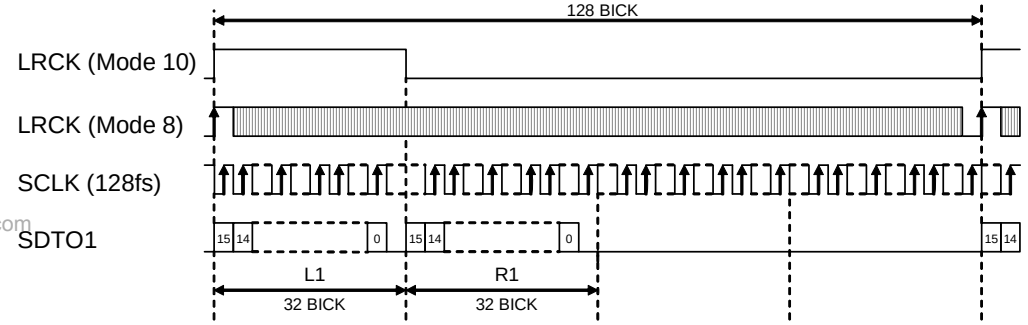


Figure 5. Mode 8, 10 Timing (TDM128A mode, MSB justified)

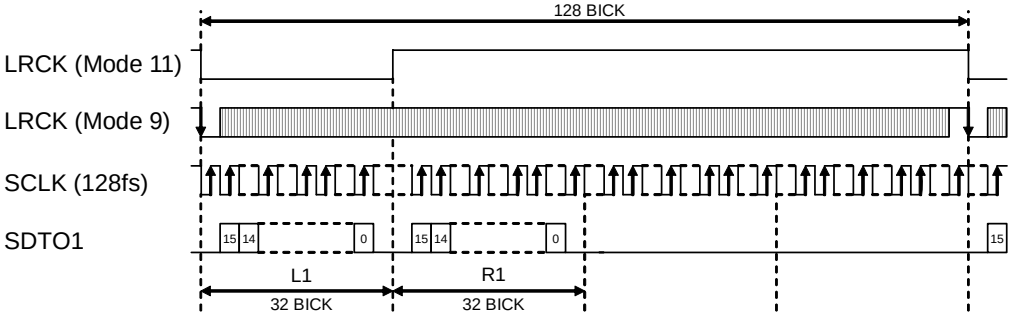


Figure 6. Mode 9, 11 Timing (TDM128A mode, I^{2}S Compatible)

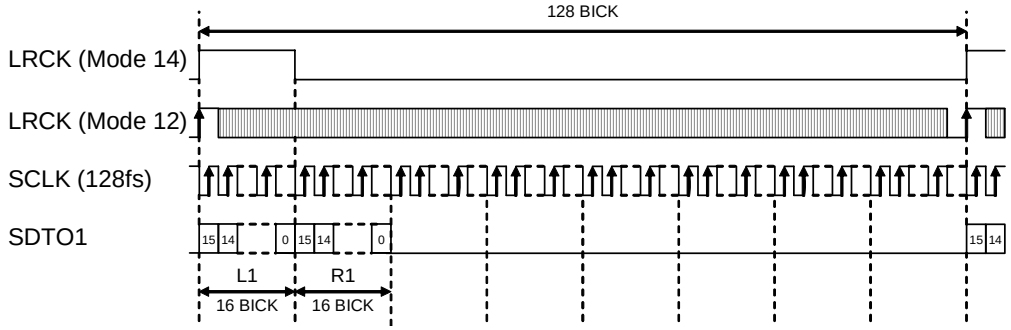


Figure 7. Mode 12, 14 Timing (TDM128B mode, MSB justified)

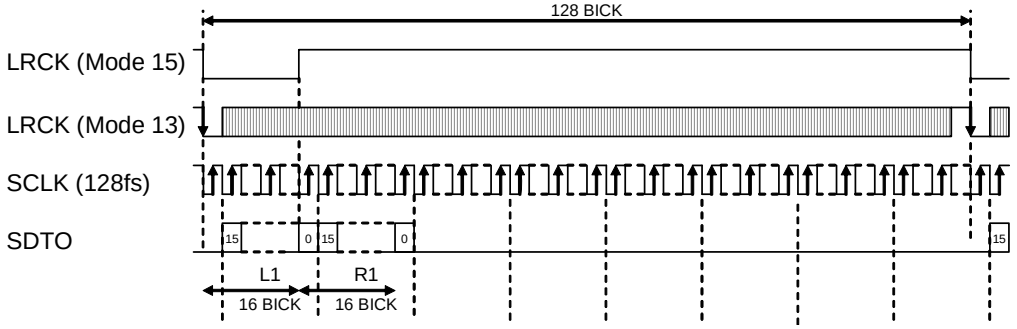


Figure 8. Mode 13, 15 Timing (TDM128B mode, I^2S Compatible)

■ Cascade TDM Mode

The AK4140 supports cascading connection of up to four devices in a daisy chain configuration at TDM256 mode. In this mode, SDTO pin of device #N is connected to TDMIN pin of device #(N+1). The device can output up to 8ch TDM data multiplexed with TDMIN data. Figure 8 shows a connection example of a daisy chain.

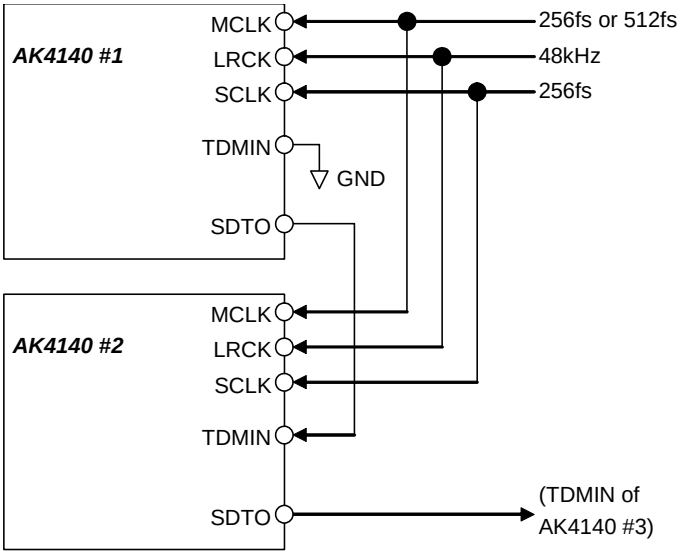


Figure 9. Cascade TDM Connection Diagram

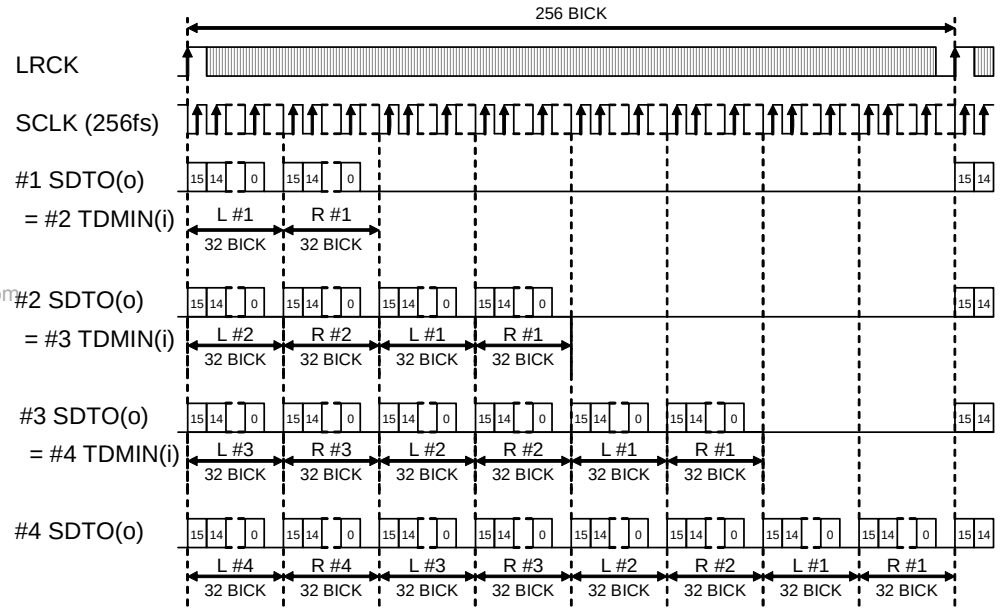


Figure 10. Cascade TDM Timing (4devices)

■ Audio Sampling Rate

The AK4140 supports 3 sampling rates as 32kHz, 44.1kHz and 48kHz.

FS1	FS0	Sampling rate	
0	0	32kHz	
0	1	44.1kHz	
1	0	48kHz	(default)
1	1	(Reserved)	

Table 4. Sampling rate select

■ Digital High Pass Filter

The AK4140 has a digital high pass filter for DC offset cancellation. The cut-off frequency of the HPF is 1Hz (@fs=48kHz) and scales with sampling rate (fs).

■ Pilot/SAP/Noise Detection (read)

PILOT bit: Pilot Signal Detection

Pilot signal	PILOT bit	
Detected	1	
Not detected	0	(default)

Table 5. Pilot Signal Detection

0 → 1 :
Pilot Signal Level ≥ Pilot Threshold Level (PTHR1,0 bit)
+ Pilot Hysteresis Level (PHYS1,0 bit) / 2 (in dB)

1 → 0 :
Pilot Signal Level < Pilot Threshold Level (PTHR1,0 bit)
- Pilot Hysteresis Level (PHYS1,0 bit) / 2 (in dB)

SAP bit: SAP Signal Detection

SAP signal	SAP bit	
Detected	1	
Not detected	0	(default)

Table 6. SAP Signal Detection

0 → 1 :
SAP Signal Level ≥ SAP Threshold Level (STHR1,0 bit)
+ SAP Hysteresis Level (SHYS1,0 bit) / 2 (in dB)

1 → 0 :
SAP Signal Level <SAP Threshold Level (STHR1,0 bit)
- SAP Hysteresis Level (SHYS1,0 bit) / 2 (in dB)

NOISE bit: Noise Detection

noise signal	NOISE bit
Detected	1
Not detected	0

Table 7. Noise Detection

0 → 1 :
Noise Level ≥ Noise Threshold Level (NTHR1,0 bit)
+ Noise Hysteresis Level (NHYS1,0 bit) / 2 (in dB)

1 → 0 :
Noise Level < Noise Threshold Level (NTHR1,0 bit)
- Noise Hysteresis Level (NHYS1,0 bit) / 2 (in dB)

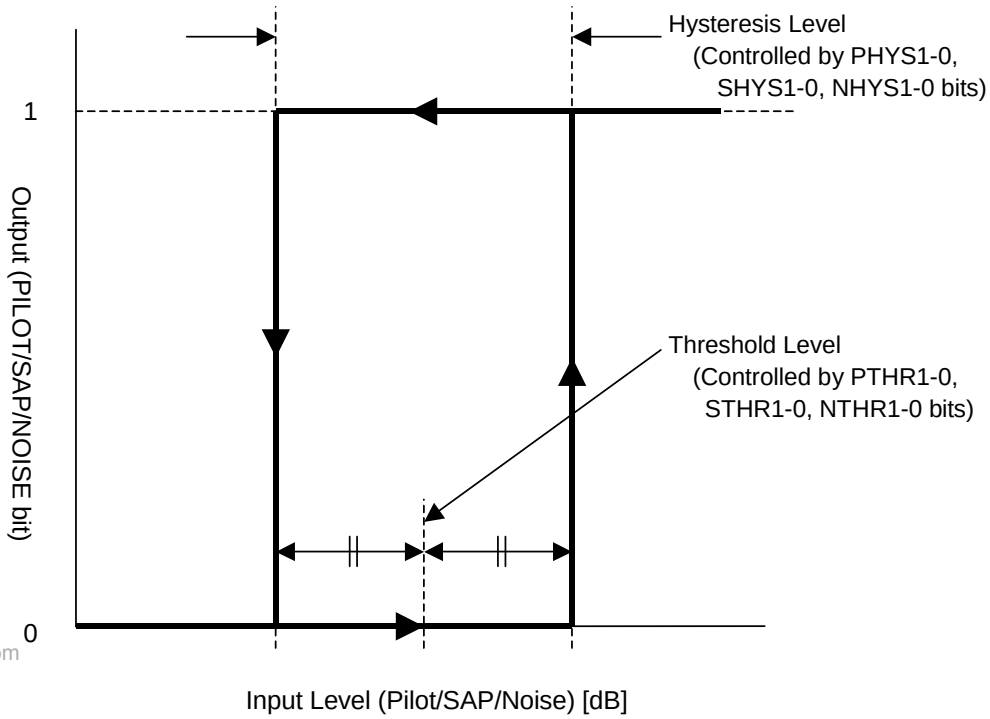


Figure 11. Pilot, SAP, Noise Detection Function

■ Pilot/SAP/Noise Detection Threshold Control

PTHR1 bit	PTHR0 bit	Threshold Level (typ)
0	0	-1.5dB
0	1	-3dB
1	0	-6dB (default)
1	1	-9dB

0dB= full scale of 1fH Pilot tone

Table 8. Pilot(fH) Threshold Level Control

STHR1 bit	STHR0 bit	Threshold Level (typ)
0	0	-1dB
0	1	-4.5dB
1	0	-9dB (default)
1	1	-13.5dB

0dB= full scale of 5fH SAP carrier

Table 9. SAP(5fH) Threshold Level Control

NTHR1 bit	NTHR0 bit	Threshold Level (typ)
0	0	-2dB
0	1	-7dB
1	0	-13dB (default)
1	1	-20dB

0dB= full scale of 5fH SAP carrier, BW=5fH+/-10kHz

Table 10. Noise(5fH) Threshold Level Control

■ Pilot/SAP/Noise Detection On/Off Hysteresis Range

PHYS1 bit	PHYS0 bit	Hysteresis Level (typ)
0	0	3dB
0	1	6dB (default)
1	0	9dB
1	1	12dB

0dB= full scale of 1fH Pilot tone

Table 11. Pilot(fH) Hysteresis Level Control

SHYS1 bit	SHYS0 bit	Hysteresis Level (typ)
0	0	2dB
0	1	4dB (default)
1	0	6dB
1	1	8dB

0dB= full scale of 5fH SAP carrier

Table 12. SAP(5fH) Hysteresis Level Control

NHYS1 bit	NHYS0 bit	Hysteresis Level (typ)
0	0	1dB
0	1	2.5dB (default)
1	0	4dB
1	1	6.5dB

0dB= full scale of 5fH SAP carrier, BW=5fH+/-10kHz

Table 13. Noise(5fH) Hysteresis Level Control

■ Output control

The OUT4-0 bits and the status bits (PILOT, SAP, NOISE bits) control the Output Mode.

Mode	Control bit					Operation
	OUT4	OUT3	OUT2	OUT1	OUT0	
0	0	0	0	0	0	Fix to Mono
1	0	0	0	0	1	Fix to Stereo
2	0	0	0	1	0	Fix to Mono/ SAP
3	0	0	0	1	1	Fix to Mono/ SAP*
4	0	0	1	0	0	Fix to SAP
5	0	0	1	0	1	Fix to SAP*
6	0	0	1	1	0	(Reserved)
7	0	0	1	1	1	(Reserved)
8	0	1	0	0	0	(Reserved)
9	0	1	0	0	1	(Reserved)
10	0	1	0	1	0	(Reserved)
11	0	1	0	1	1	(Reserved)
12	0	1	1	0	0	(Reserved)
13	0	1	1	0	1	(Reserved)
14	0	1	1	1	0	(Reserved)
15	0	1	1	1	1	(Reserved)
16	1	0	0	0	0	Mono ⇔ Stereo Auto
17	1	0	0	0	1	Mono ⇔ Stereo ⇔ Mono/ SAP Auto 1(NOISE ignored)
18	1	0	0	1	0	Mono ⇔ Stereo ⇔ Mono/ SAP Auto 2
19	1	0	0	1	1	Mono ⇔ Stereo ⇔ Mono/ SAP ⇔ Mono/ SAP* Auto
20	1	0	1	0	0	Mono ⇔ Stereo ⇔ SAP Auto 1(NOISE ignored)
21	1	0	1	0	1	Mono ⇔ Stereo ⇔ SAP Auto 2
22	1	0	1	1	0	Mono ⇔ Stereo ⇔ SAP ⇔ SAP* Auto (default)
23	1	0	1	1	1	MONO ⇔ Mono/ SAP Auto 1(NOISE ignored)
24	1	1	0	0	0	MONO ⇔ Mono/ SAP Auto 2
25	1	1	0	0	1	MONO ⇔ Mono/ SAP ⇔ Mono/ SAP* Auto
26	1	1	0	1	0	MONO ⇔ SAP Auto 1(NOISE ignored)
27	1	1	0	1	1	MONO ⇔ SAP Auto 2
28	1	1	1	0	0	MONO ⇔ SAP ⇔ SAP* Auto
29	1	1	1	0	1	SAP ⇔ SAP* Auto
30	1	1	1	1	0	Mono/ SAP ⇔ Mono/ SAP* Auto
31	1	1	1	1	1	

Table 14. Output Control (OUT4-0)

Mode in Table 14	Operation	Status			Output	
		PILOT	SAP	NOISE	Lch	Rch
0	Fix Mono	0	0	0	L+R	L+R
		0	0	1	L+R	L+R
		0	1	0	L+R	L+R
		0	1	1	L+R	L+R
		1	0	0	L+R	L+R
		1	0	1	L+R	L+R
		1	1	0	L+R	L+R
		1	1	1	L+R	L+R
1	Fix Stereo	0	0	0	L	R
		0	0	1	L	R
		0	1	0	L	R
		0	1	1	L	R
		1	0	0	L	R
		1	0	1	L	R
		1	1	0	L	R
		1	1	1	L	R
2	Fix Mono/SAP	0	0	0	L+R	SAP
		0	0	1	L+R	SAP
		0	1	0	L+R	SAP
		0	1	1	L+R	SAP
		1	0	0	L+R	SAP
		1	0	1	L+R	SAP
		1	1	0	L+R	SAP
		1	1	1	L+R	SAP
3	Fix Mono/SAP*	0	0	0	L+R	SAP*
		0	0	1	L+R	SAP*
		0	1	0	L+R	SAP*
		0	1	1	L+R	SAP*
		1	0	0	L+R	SAP*
		1	0	1	L+R	SAP*
		1	1	0	L+R	SAP*
		1	1	1	L+R	SAP*
4	Fix SAP	0	0	0	SAP	SAP
		0	0	1	SAP	SAP
		0	1	0	SAP	SAP
		0	1	1	SAP	SAP
		1	0	0	SAP	SAP
		1	0	1	SAP	SAP
		1	1	0	SAP	SAP
		1	1	1	SAP	SAP
5	Fix SAP*	0	0	0	SAP*	SAP*
		0	0	1	SAP*	SAP*
		0	1	0	SAP*	SAP*
		0	1	1	SAP*	SAP*
		1	0	0	SAP*	SAP*
		1	0	1	SAP*	SAP*
		1	1	0	SAP*	SAP*
		1	1	1	SAP*	SAP*

Mode in Table 14	Operation	Status			Output	
		PILOT	SAP	NOISE	Lch	Rch
16	Mono ⇔ Stereo Auto	0	0	0	L+R	L+R
		0	0	1	L+R	L+R
		0	1	0	L+R	L+R
		0	1	1	L+R	L+R
		1	0	0	L	R
		1	0	1	L	R
		1	1	0	L	R
		1	1	1	L	R
17	Mono ⇔ Stereo ⇔ MONO/SAP Auto 1	0	0	0	L+R	L+R
		0	0	1	L+R	L+R
		0	1	0	L+R	SAP
		0	1	1	L+R	SAP
		1	0	0	L	R
		1	0	1	L	R
		1	1	0	L+R	SAP
		1	1	1	L+R	SAP
18	Mono ⇔ Stereo ⇔ MONO/SAP Auto 2	0	0	0	L+R	L+R
		0	0	1	L+R	L+R
		0	1	0	L+R	SAP
		0	1	1	L+R	L+R
		1	0	0	L	R
		1	0	1	L	R
		1	1	0	L+R	SAP
		1	1	1	L	R
19	Mono ⇔ Stereo ⇔ MONO/SAP ⇔ MONO/SAP* Auto	0	0	0	L+R	L+R
		0	0	1	L+R	L+R
		0	1	0	L+R	SAP
		0	1	1	L+R	SAP*
		1	0	0	L	R
		1	0	1	L	R
		1	1	0	L+R	SAP
		1	1	1	L+R	SAP*
20	Mono ⇔ Stereo ⇔ SAP Auto 1	0	0	0	L+R	L+R
		0	0	1	L+R	L+R
		0	1	0	SAP	SAP
		0	1	1	SAP	SAP
		1	0	0	L	R
		1	0	1	L	R
		1	1	0	SAP	SAP
		1	1	1	SAP	SAP
21	Mono ⇔ Stereo ⇔ SAP Auto 2	0	0	0	L+R	L+R
		0	0	1	L+R	L+R
		0	1	0	SAP	SAP
		0	1	1	L+R	L+R
		1	0	0	L	R
		1	0	1	L	R
		1	1	0	SAP	SAP
		1	1	1	L	R

Mode in Table 14	Operation	Status			Output	
		PILOT	SAP	NOISE	Lch	Rch
22	Mono ⇔ Stereo ⇔ SAP ⇔ SAP* Auto	0	0	0	L+R	L+R
		0	0	1	L+R	L+R
		0	1	0	SAP	SAP
		0	1	1	SAP*	SAP*
		1	0	0	L	R
		1	0	1	L	R
		1	1	0	SAP	SAP
		1	1	1	SAP*	SAP*
23	Mono ⇔ Mono/SAP Auto 1	0	0	0	L+R	L+R
		0	0	1	L+R	L+R
		0	1	0	L+R	SAP
		0	1	1	L+R	SAP
		1	0	0	L+R	L+R
		1	0	1	L+R	L+R
		1	1	0	L+R	SAP
		1	1	1	L+R	SAP
24	Mono ⇔ Mono/SAP Auto 2	0	0	0	L+R	L+R
		0	0	1	L+R	L+R
		0	1	0	L+R	SAP
		0	1	1	L+R	L+R
		1	0	0	L+R	L+R
		1	0	1	L+R	L+R
		1	1	0	L+R	SAP
		1	1	1	L+R	L+R
25	Mono ⇔ Mono/SAP ⇔ Mono/SAP* Auto	0	0	0	L+R	L+R
		0	0	1	L+R	L+R
		0	1	0	L+R	SAP
		0	1	1	L+R	SAP*
		1	0	0	L+R	L+R
		1	0	1	L+R	L+R
		1	1	0	L+R	SAP
		1	1	1	L+R	SAP*
26	Mono ⇔ SAP Auto 1	0	0	0	L+R	L+R
		0	0	1	L+R	L+R
		0	1	0	SAP	SAP
		0	1	1	SAP	SAP
		1	0	0	L+R	L+R
		1	0	1	L+R	L+R
		1	1	0	SAP	SAP
		1	1	1	SAP	SAP
27	Mono ⇔ SAP Auto 2	0	0	0	L+R	L+R
		0	0	1	L+R	L+R
		0	1	0	SAP	SAP
		0	1	1	L+R	L+R
		1	0	0	L+R	L+R
		1	0	1	L+R	L+R
		1	1	0	SAP	SAP
		1	1	1	L+R	L+R

Mode in Table 14	Operation	Status			Output	
		PILOT	SAP	NOISE	Lch	Rch
28	Mono ⇔ SAP ⇔ SAP* Auto	0	0	0	L+R	L+R
		0	0	1	L+R	L+R
		0	1	0	SAP	SAP
		0	1	1	SAP*	SAP*
		1	0	0	L+R	L+R
		1	0	1	L+R	L+R
		1	1	0	SAP	SAP
		1	1	1	SAP*	SAP*
29	SAP ⇔ SAP* Auto	0	0	0	SAP	SAP
		0	0	1	SAP*	SAP*
		0	1	0	SAP	SAP
		0	1	1	SAP*	SAP*
		1	0	0	SAP	SAP
		1	0	1	SAP*	SAP*
		1	1	0	SAP	SAP
		1	1	1	SAP*	SAP*
30	Mono/SAP ⇔ Mono/SAP* Auto	0	0	0	L+R	SAP
		0	0	1	L+R	SAP*
		0	1	0	L+R	SAP
		0	1	1	L+R	SAP*
		1	0	0	L+R	SAP
		1	0	1	L+R	SAP*
		1	1	0	L+R	SAP
		1	1	1	L+R	SAP*

: These status bits are not reflected to the output data.
SAP*: -7dB attenuated.

Table 15 Output Control

■ Output Lch/Rch Swapping Operation

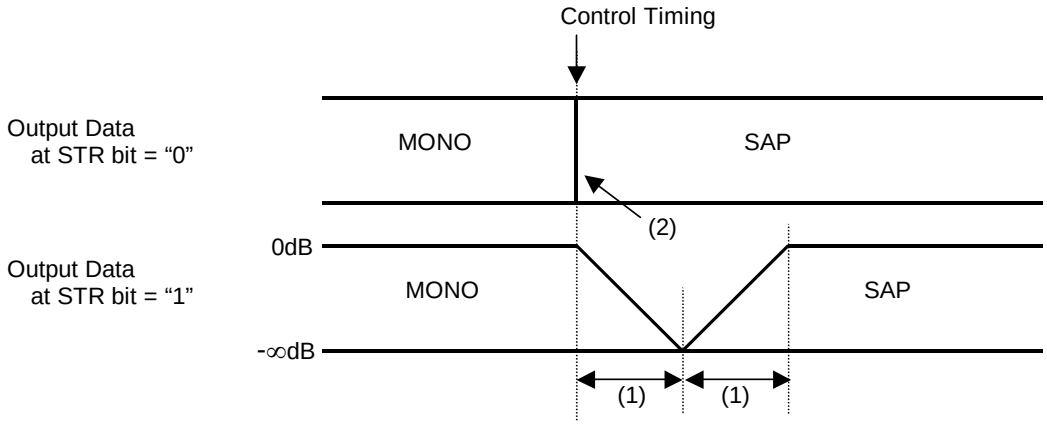
When the LRR bit is “1”, the output data is swapped between Lch and Rch. When the LR bit is “0”, the output data is as Table 15.

LR bit	Mode	Operation
0	Normal	Output Lch/Rch data as Table 15
1	Swap	Swap Lch/Rch data as Table 15

Table 16. Output Channel Control

■ Soft Transition Operation

When the STR bit is “1”, the transition among MONO, Stereo and SAP is operated using soft muting function. When the STR bit is “0”, the transition among MONO, Stereo and SAP is operated immediately.



Notes:
(1) Transition time. 768 LRCK cycles (768/fs) for both muting and unmuting.
(2) When the STR bit = “0”, a noise may occur at transition.

Figure 12. Soft Transition Control (ex. MONO to SAP)

■ Stereo Volume Control

The AK4140 has a digital output volume (25 levels, 1dB step, Mute). The L4-0 and R4-0 bits can set the volume. The volume is placed in front of a stereo matrix block. The input data of the digital volume is changed from +12 to –12dB or MUTE. When the VOLC bit = "1" (default), the L4-0 bits control both Lch and Rch attenuation levels. When the VOLC bit = "0", the L4-0 bits control Lch level and R4-0 bits control Rch level. This volume has a soft transition function. When changing levels, transitions are executed with soft changes; thus no switching noise occurs during these transitions. The transition time of 1 level and all levels are shown in Table 17.

Transition Time	
1 Level	+12 to -12
8LRCK	192LRCK

Table 17. ATT Transition Time

L4	L3	L2	L1	L0	Gain
1	1	0	0	1	+12dB
1	1	0	0	0	+11dB
…	…	…	…	…	…
0	1	1	1	0	+1dB
0	1	1	0	1	0dB
0	1	1	0	0	-1dB
…	…	…	…	…	…
0	0	0	1	0	-11dB
0	0	0	0	1	-12dB
0	0	0	0	0	Mute (default)

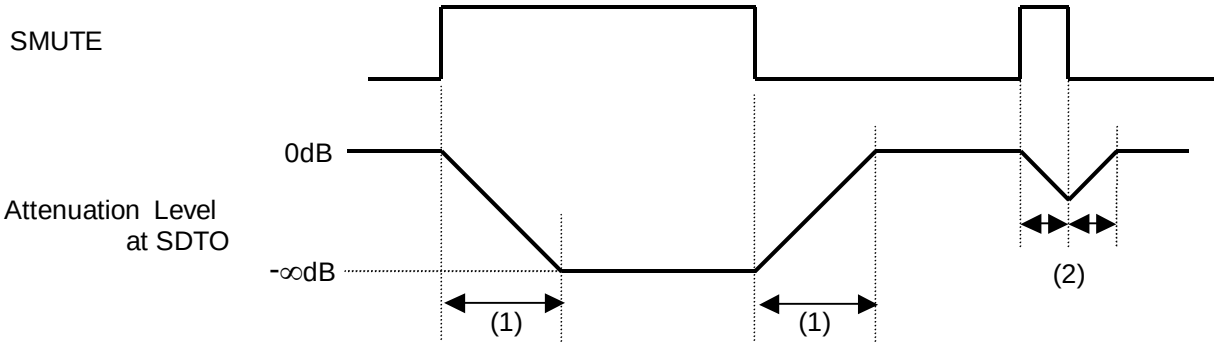
Table 18. Volume (Lch)

R4	R3	R2	R1	R0	Gain
1	1	0	0	1	+12dB
1	1	0	0	0	+11dB
…	…	…	…	…	…
0	1	1	1	0	+1dB
0	1	1	0	1	0dB
0	1	1	0	0	-1dB
…	…	…	…	…	…
0	0	0	1	0	-11dB
0	0	0	0	1	-12dB
0	0	0	0	0	Mute (default)

Table 19. Volume (Rch)

■ Soft Mute Operation (default = Mute)

When the SMUTE bit goes to "1", the output signal is attenuated from 0dB to -∞dB during 768 LRCK cycles. When the SMUTE bit returns to "0", the mute is cancelled and the attenuation gradually changes to 0dB during 768 LRCK cycles. If the soft mute is cancelled before attenuating to -∞, the attenuation is discontinued and returns to 0dB. This return takes the same number of clock cycles as the point at which the soft mute cancel was initiated, i.e. if 500 clock cycles passed and then a soft mute cancel was issued, it will take 500 clock cycles to return to 0dB. The soft mute is used primarily when changing the signal source.



Notes:
(1) Transition time. 768 LRCK cycles (768/fs).
(2) If the soft mute is cancelled before attenuating to -∞ after starting the operation, the attenuation is discontinued and returned to 0dB by the same number of clock cycles.

Figure 13. Soft Mute

■ Status Change Handling

The INT1/0 pin goes "H" when one of following three statuses changes without masking. Each change of status can be masked by MPLT bit, MSP bit and MNS bit. When masked, the interrupt event does not affect the operation of the INT1/0 pin (the masks do not affect the status registers). When the PDN pin= "L" or RSTN= "0", the INT pin goes to "L".

1. PILOT bit : PILOT detection
   Goes "1" when the Pilot signal is detected.

2. SAP bit : SAP detection
   Goes "1" when the SAP signal is detected.

3. NOISE bit : Noise detection
   Goes "1" when the noise is detected.

Once INT1/0 pin goes to "H", it remains "H" for the hold time controlled by the INT11-10, INT01-00 bits.

INT01 bit	INT00 bit	INT0 pin Hold time
0	0	1LRCK cycle
0	1	1024 LRCK cycle
1	0	4096 LRCK cycle
1	1	Holds "H" until the status register is read.

Table 20. INT0 pin Hold Time Control

INT11 bit	INT10 bit	INT1 pin Hold time
0	0	1LRCK cycle
0	1	1024 LRCK cycle
1	0	4096 LRCK cycle
1	1	Holds "H" until the status register is read.

Table 21. INT1 pin Hold Time Control

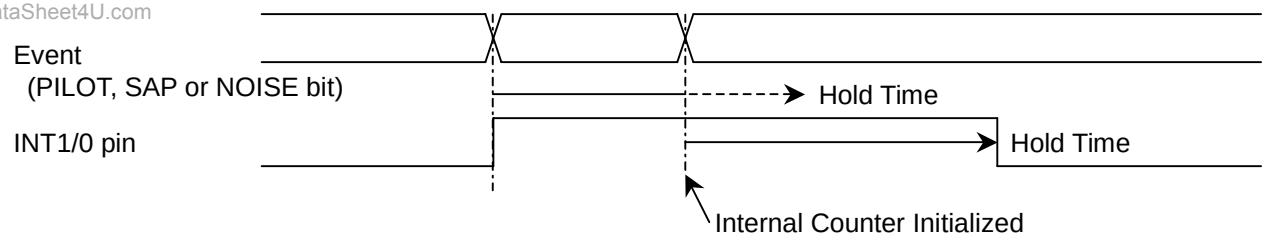


Figure 14. INT pin Timing

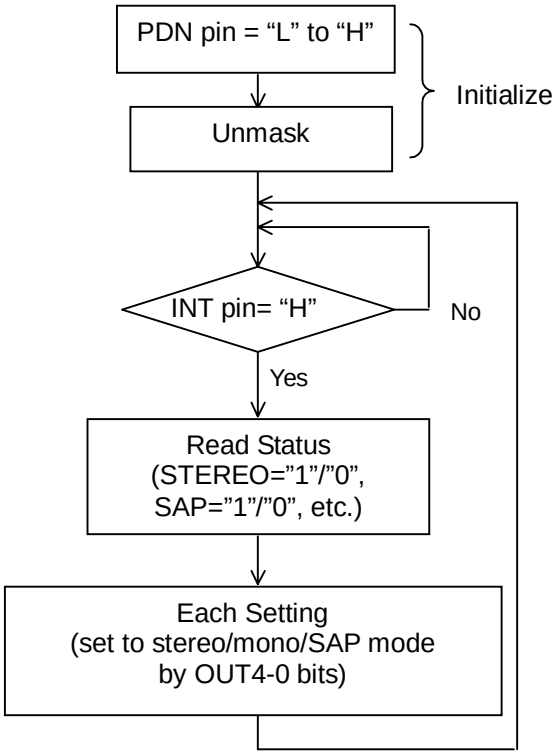


Figure 15. Status Change Handling Sequence Example

■ Control Interface (I^2C-bus)

AK4140 supports a fast-mode I^2C-bus system (max : 400kHz).

1. Data transfer

All commands are preceded by a START condition. After the START condition, a slave address is sent. After the AK4140 recognizes the START condition, the device interfaced to the bus waits for the slave address to be transmitted over the SDA line. If the transmitted slave address matches an address for one of the devices, the designated slave device pulls the SDA line to LOW (ACKNOWLEDGE). The data transfer is always terminated by a STOP condition generated by the master device.

1-1. Data validity

The data on the SDA line must be stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW except for the START and the STOP condition.

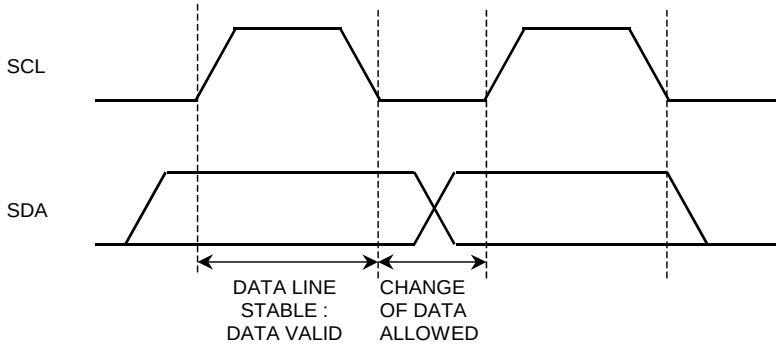


Figure 16. Data transfer

1-2. START and STOP condition

A HIGH to LOW transition on the SDA line while SCL is HIGH indicates a START condition. All sequences start from the START condition.
A LOW to HIGH transition on the SDA line while SCL is HIGH defines a STOP condition. All sequences end by the STOP condition.

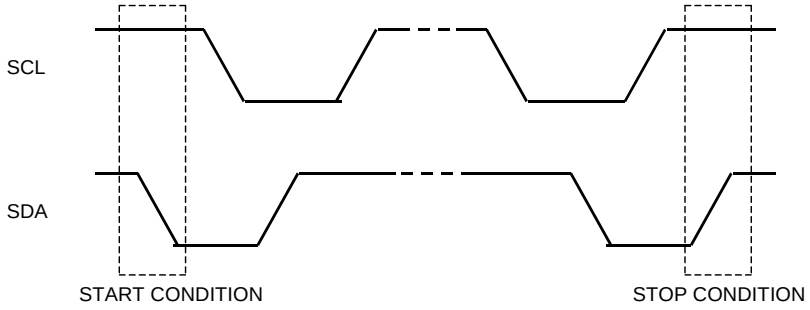


Figure 17. START and STOP conditions

1-3. ACKNOWLEDGE

ACKNOWLEDGE is a software convention used to indicate successful data transfers. The transmitting device will release the SDA line (HIGH) after transmitting eight bits. The receiver must pull down the SDA line during the acknowledge clock pulse so that that it remains stable “L” during “H” period of this clock pulse. The AK4140 will generates an acknowledge after each byte has been received.
In the read mode, the slave, the AK4140 will transmit eight bits of data, release the SDA line and monitor the line for an acknowledge. If an acknowledge is detected and no STOP condition is generated by the master, the slave will continue to transmit data. If an acknowledge is not detected, the slave will terminate further data transmissions and await the STOP condition.

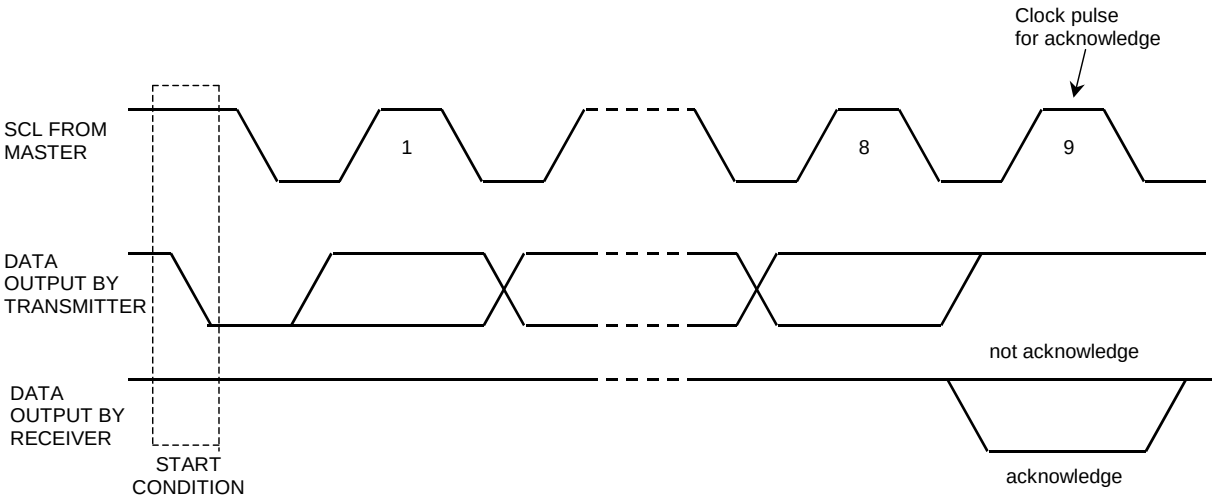


Figure 18. Acknowledge on the I^2C-bus

1-4. FIRST BYTE

The first byte, which includes seven bits of slave address and one bit of R/W bit, is sent after the START condition. If the transmitted slave address matches an address for one of the device, the receiver who has been addressed pulls down the SDA line.
The most significant five bits of the slave address are fixed as “10000”. The next two bits are CAD1 and CAD0 (device address bits). These two bits identify the specific device on the bus. The hard-wired input pins (CAD1 pin and CAD0 pin) set them. The eighth bit (LSB) of the first byte (R/W bit) defines whether the master requests a write or read condition. A “1” indicates that the read operation is to be executed. A “0” indicates that the write operation is to be executed.

1	0	0	0	0	CAD1	CAD0	R/W

(Those CAD1/0 should match with CAD1/0 pins.)

Figure 19. The First Byte

2. WRITE Operations

Set R/W bit = "0" for the WRITE operation of the AK4140.
After receipt the start condition and the first byte, the AK4140 generates an acknowledge, and awaits the second byte (register address). The second byte consists of the address for control registers of AK4140. The format is MSB first, and those most significant 3-bits are "Don't care".

*	*	*	A4	A3	A2	A1	A0

(*: Don't care)

Figure 20. The Second Byte

After receipt the second byte, the AK4140 generates an acknowledge, and awaits the third byte. Those data after the second byte contain control data. The format is MSB first, 8bits.

D7	D6	D5	D4	D3	D2	D1	D0

Figure 21. Byte structure after the second byte

The AK4140 is capable of more than one byte write operation by one sequence.
After receipt of the third byte, the AK4140 generates an acknowledge, and awaits the next data again. The master can transmit more than one words instead of terminating the write cycle after the first data word is transferred. After the receipt of each data, the internal 5bits address counter is incremented by one, and the next data is taken into next address automatically. If the address exceed 08H prior to generating the stop condition, the address counter will "roll over" to 00H and the previous data will be overwritten.

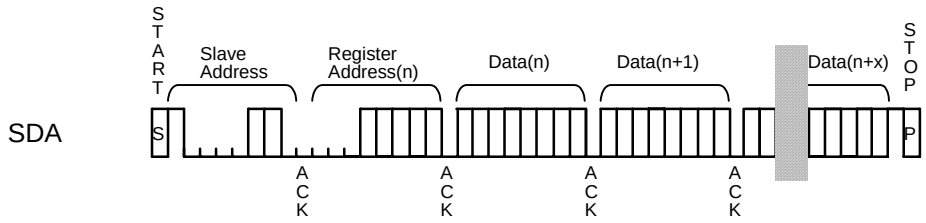


Figure 22. WRITE Operation

3. READ Operations

Set R/W bit = "1" for the READ operation of the AK4140.
After transmission of a data, the master can read next address's data by generating the acknowledge instead of terminating the write cycle after the receipt the first data word. After the receipt of each data, the internal 5bits address counter is incremented by one, and the next data is taken into next address automatically. If the address exceed 08H prior to generating the stop condition, the address counter will "roll over" to 00H and the previous data will be overwritten.
The AK4140 supports two basic read operations: CURRENT ADDRESS READ and RANDOM READ.

3-1. CURRENT ADDRESS READ

The AK4140 contains an internal address counter that maintains the address of the last word accessed, incremented by one. Therefore, if the last access (either a read or write) was to address n, the next CURRENT READ operation would access data from the address n+1.
After receipt of the slave address with R/W bit set to "1", the AK4140 generates an acknowledge, transmits 1byte data which address is set by the internal address counter and increments the internal address counter by 1. If the master does not generate an acknowledge to the data but generate the stop condition, the AK4140 discontinues transmission

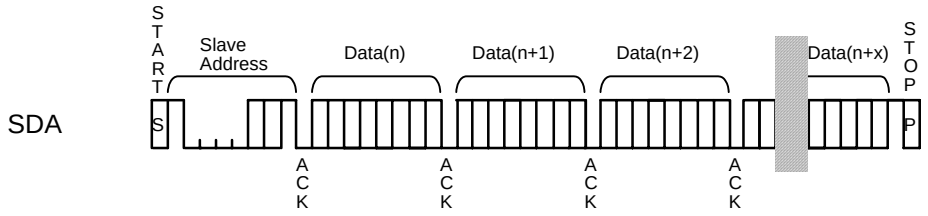


Figure 23. CURRENT ADDRESS READ

3-2. RANDOM READ

Random read operation allows the master to access any memory location at random. Prior to issuing the slave address with the R/W bit set to "1", the master must first perform a "dummy" write operation.
The master issues the start condition, slave address(R/W="0") and then the register address to read. After the register address's acknowledge, the master immediately reissues the start condition and the slave address with the R/W bit set to "1". Then the AK4140 generates an acknowledge, 1byte data and increments the internal address counter by 1. If the master does not generate an acknowledge to the data but generate the stop condition, the AK4140 discontinues transmission.

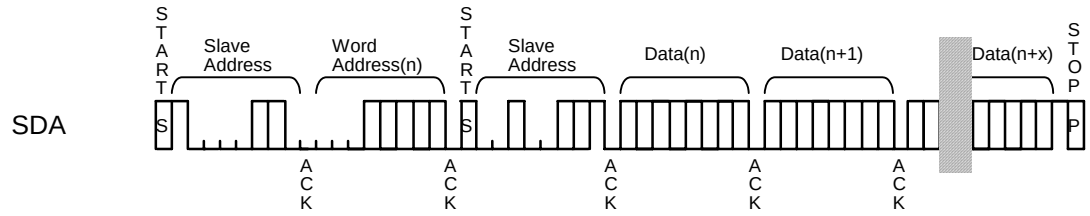


Figure 24. RANDOM READ

■ Register Map

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	CLK & Power Down Control	CKS1	CKS0	TDM1	TDM0	DIF	0	SMUTE	RSTN
01H	Output Control	FS1	FS0	LR	OUT4	OUT3	OUT2	OUT1	OUT0
02H	Threshold Control	STR	0	NTHR1	NTHR0	STHR1	STHR0	PTHR1	PTHR0
03H	Hysteresis Control	ATTR	ATTL	NHYS1	NHYS0	SHYS1	SHYS0	PHYS1	PHYS0
04H	Lch ATT	VOLC	0	0	L4	L3	L2	L1	L0
05H	Rch ATT	0	0	0	R4	R3	R2	R1	R0
06H	Signal Status	0	0	0	0	0	NOISE	SAP	PILOT
07H	INT0 Mask	0	0	0	INT01	INT00	MNS0	MSP0	MPLT0
08H	INT1 Mask	0	0	0	INT11	INT10	MNS1	MSP1	MPLT1

When the PDN pin goes “L”, the registers are initialized to their default values.

While the PDN pin =“H”, all registers can be accessed.

Do not write any data to the register over 08H.

When RSTN bit goes “0”, the internal timing is reset and registers are not initialized to their default values.

Reset & Initialize

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	CLK & Power Down Control	CKS1	CKS0	TDM1	TDM0	DIF	0	SMUTE	RSTN
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	1	1

RSTN: Timing Reset & Register Initialize
0: Reset & Initialize
1: Normal Operation (Default)

SMUTE: Soft Mute Enable
0: Normal Operation
1: Soft-muted (Default)

DIF, TDM1-0: Data Interface Control
Default: 16bit, MSB justified. Please refer Table 3.

CKS1-0: Master Clock Frequency Select
Default: 256fs

Output Control

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
01H	Output Control	FS1	FS0	LR	OUT4	OUT3	OUT2	OUT1	OUT0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		1	0	0	1	0	1	1	0

OUT4-0: Output Control
Please refer Table 14.

LR: Output Channel Control
Please refer Table 16.

FS1-0: Sampling Rate Select
Default: 48kHz

Threshold Control

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
02H	Threshold Control	STR	0	NTHR1	NTHR0	STHR1	STHR0	PTHR1	PTHR0
R/W		R/W	RD	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	1	0	1	0	1	0

PTHR1-0: Pilot Detection Threshold Level Control

STHR1-0: SAP Detection Threshold Level Control

NTHR1-0: Noise Detection Threshold Level Control

STR: Switching Sequence Control

Hysteresis Control

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
03H	Hysteresis Control	ATTR	ATTL	NHYS1	NHYS0	SHYS1	SHYS0	PHYS1	PHYS0
R/W		RD	RD	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	1	0	1	0	1

ATTR: Rch Attenuation Control
0: 0dB
1: -6dB (Default)

ATTL: Lch Attenuation Control
0: 0dB
1: -6dB (Default)

PHYS1-0: Pilot Detection Hysteresis Level Control

SHYS1-0: SAP Detection Hysteresis Level Control

NHYS1-0: Noise Detection Hysteresis Level Control

Lch Volume control

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
04H	Lch ATT	VOLC	0	0	L4	L3	L2	L1	L0
R/W		R/W	RD	RD	R/W	R/W	R/W	R/W	R/W
Default		1	0	0	0	0	0	0	0

L4-0: Lch Volume Control

VOLC: Lch/Rch Volume Common Control Enable
0: Independent Control. L4-0 and R4-0 bits control Lch and Rch independently.
1: Common Control (default). L4-0 bits control both Lch and Rch. R4-0 bits are ignored.

Rch Volume control

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
05H	Rch ATT	0	0	0	R4	R3	R2	R1	R0
R/W		RD	RD	RD	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

R4-0: Rch Volume Control when VOLC bit = "0". Don't care when VOLC bit = "1".

Signal Status

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
06H	Signal Status	0	0	0	0	0	NOISE	SAP	PILOT
R/W		RD	RD	RD	RD	RD	RD	RD	RD
Default		0	0	0	0	0	0	0	0

PILOT: Pilot signal status
0: Pilot signal.
1: Pilot signal is detected.

SAP: SAP signal status
0: No SAP signal.
1: SAP signal is detected.

NOISE: NOISE status
0: No noise.
1: Noise is detected.

INT Mask

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
07H	INT0 Mask	0	0	0	INT01	INT00	MNS0	MSP0	MPLT0
R/W		RD	RD	RD	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	1	1	1

MPLT0: Mask enable for PILOT bit
0: Mask disable
1: Mask enable (Default)

MSP0: Mask enable for SAP bit
0: Mask disable
1: Mask enable (Default)

MNS0: Mask enable for NOISE bit
0: Mask disable
1: Mask enable (Default)

When mask is set to "1", corresponding event does not affect INT0 pin operation.

INT01-00: INT0 Hold Time Control

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
08H	INT1 Mask	0	0	0	INT11	INT10	MNS1	MSP1	MPLT1
R/W		RD	RD	RD	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	1	1	1

MPLT1: Mask enable for PILOT bit
0: Mask disable
1: Mask enable (Default)

MSP1: Mask enable for SAP bit
0: Mask disable
1: Mask enable (Default)

MNS1: Mask enable for NOISE bit
0: Mask disable
1: Mask enable (Default)

When each mask bit is set to "1", corresponding event does not affect INT1 pin operation.

INT11-10: INT1 Hold Time Control

SYSTEM DESIGN

Figure 25 shows the system connection diagram. An evaluation board is available which demonstrates application circuits, the optimum layout, power supply arrangements and measurement results.

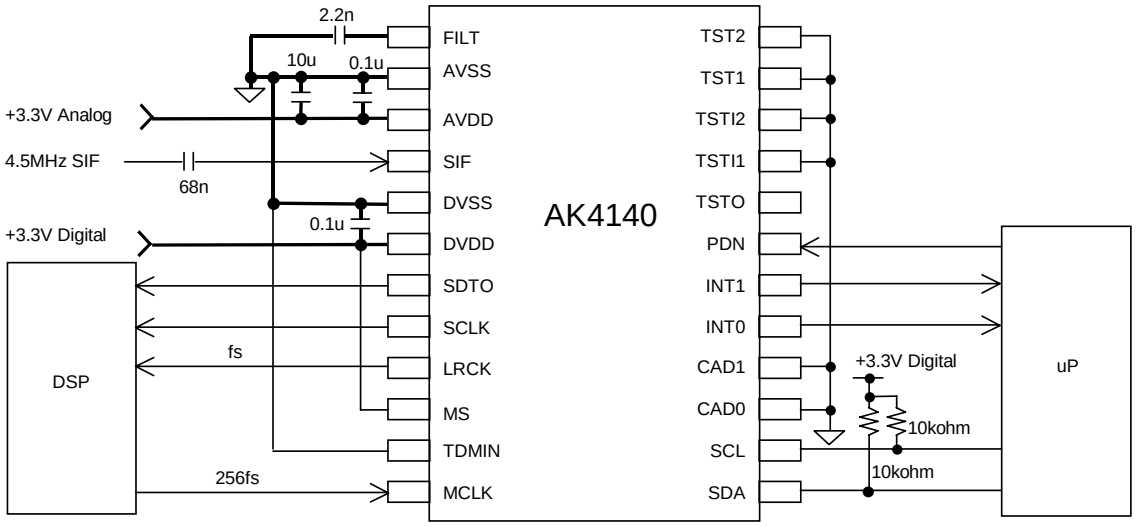
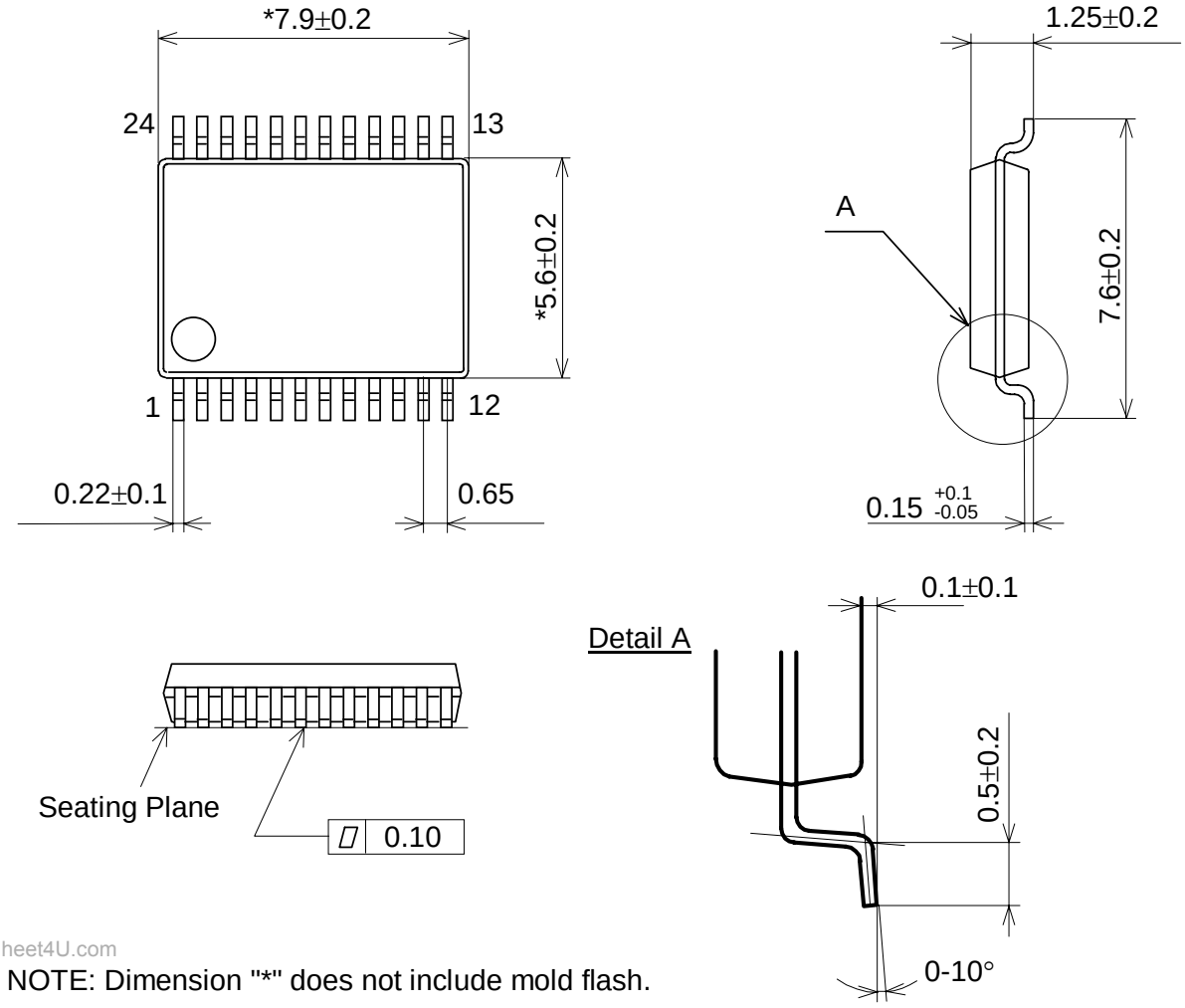


Figure 25. System Connection Example (CAD1/0 bit = “00”, Master Mode, Normal (Non-TDM) Mode.

PACKAGE

24pin VSOP (Unit: mm)

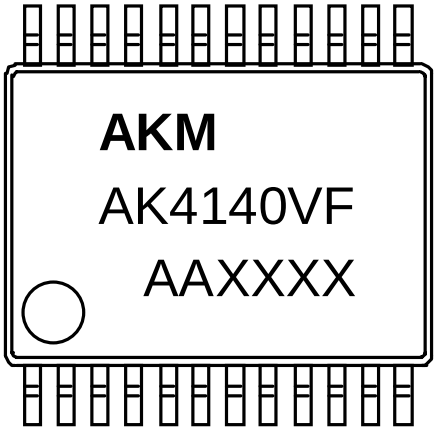


NOTE: Dimension "*" does not include mold flash.

■ Material & Lead finish

Package molding compound:	Epoxy
Lead frame material:	Cu
Lead frame surface treatment:	Solder plate (Pb Free)

MARKING



Contents of AAXXXX
AA: Lot#
XXXX: Date Code

Revision History

Date (YY/MM/DD)	Revision	Reason	Page	Contents
06/10/11	00	First Edition		
07/03/14	01	Error Correction	4	Absolute Maximum Ratings AVDD, DVDD 6.0V → 4.6V
		Error Correction	8	I2C Bus Timing tHD:DAT(max): 0.9 → -
		Error Correction	13	BICK → SCLK

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