Features

General

- High-performance, Low-power secureAVR™ Enhanced RISC Architecture
  - 135 Powerful Instructions (Most Executed in a Single Clock Cycle)
- Low Power Idle and Power-down Modes
- Bond Pad Locations Conforming to ISO 7816-2
- ESD Protection to ± 6000V
- Operating Ranges: 2.7 to 5.5V
- Compliant with GSM, 3GPP and EMV 2000 Specifications; PC Industry Compatible
- Available in Wafers, Modules, and Industry-standard Packages

Memory

- 64K Bytes of ROM Program Memory
- 4K Bytes of EEPROM, Including 64 OTP Bytes and 192-byte Bit-addressable Area
  - 1 to 64-byte Program / Erase
  - 1 ms Program / 1 ms Erase
  - Typically More than 500,000 Write/Erase Cycles at a Temperature of 25°C
  - 10 Years Data Retention
- 2K Bytes of RAM

Peripherals

- One ISO 7816 Controller
  - Up to 625 kbps at 5 MHz
  - Compliant with T=0 and T=1 Protocols
- One I/O Port
- Programmable Internal Oscillator (Up to 16 MHz on ROM)
- Two 16-bit Timers
- Random Number Generator (RNG)
- 2-level, 7-vector Interrupt Controller
- Hardware DES and Triple DES DPA Resistant
- Checksum Accelerator
- CRC 16 Engine (Compliant with ISO/IEC 3309)

Security

- Dedicated Hardware for Protection Against SPA/DPA Attacks
- Advanced Protection Against Physical Attack, Including Active Shield
- Environmental Protection Systems
- Voltage Monitor
- Frequency Monitor
- Temperature Monitor
- Light Protection
- Secure Memory Management/Access Protection (Supervisor Mode)

Development Tools

- Voyager Emulation Platform (ATV2 Advanced) to Support Software Development
- IAR Embedded Workbench® V3.20 Debugger or Atmel's AVR Studio® Version 4.07 or Above
- Software Libraries and Application Notes

Secure Microcontroller for Smart Cards

AT90SC6404RT Summary

6511AS–SMIC–28Feb05

Note: This is a summary document. A complete document will be available under NDA. For more information, please contact your local Atmel sales office.

Description

The AT90SC6404RT is a low-power, high-performance, 8/16-bit microcontroller with ROM program memory, EEPROM data memory, based on the secureAVR enhanced RISC architecture. By executing powerful instructions in a single clock cycle, the AT90SC6404RT achieves throughputs close to 1 MIPS per MHz. Its Harvard architecture includes 32 general-purpose working registers directly connected to the ALU, allowing two independent registers to be accessed in one single instruction executed in one clock cycle.

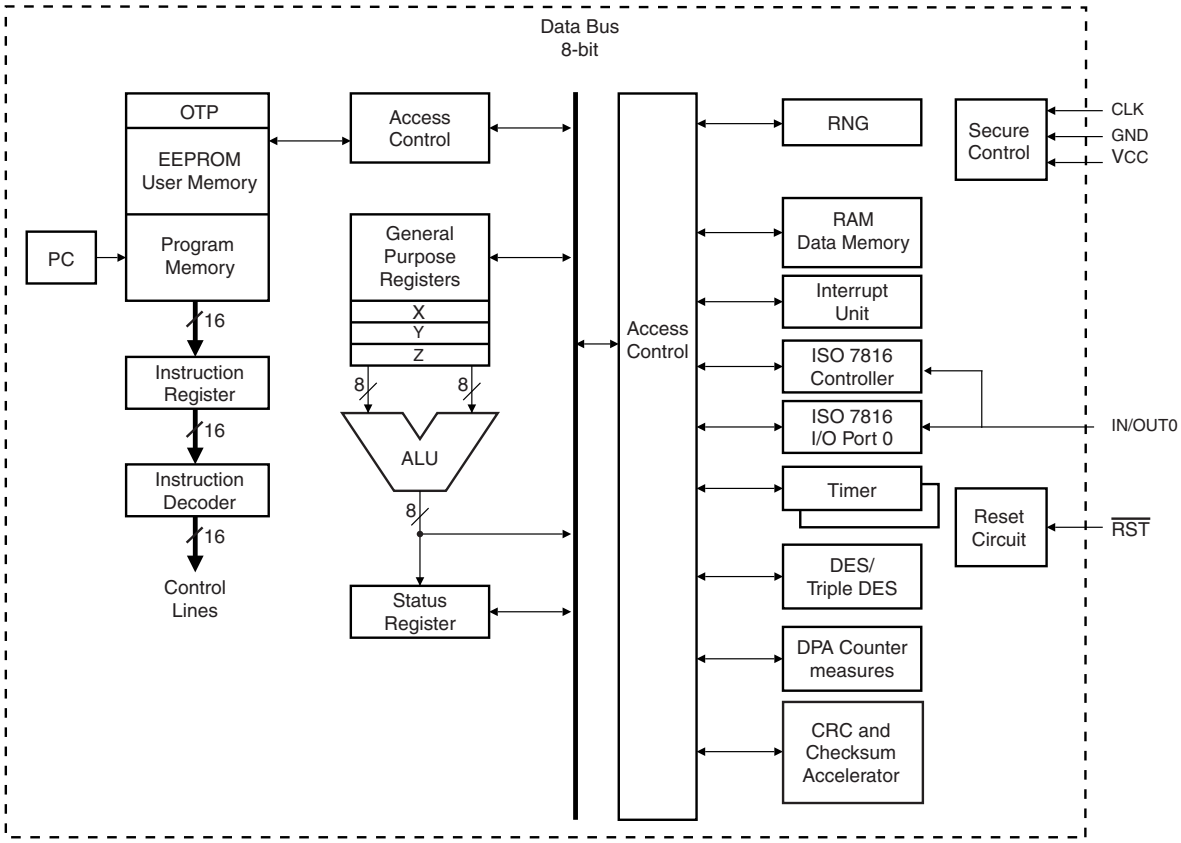
The AT90SC6404RT uses the secureAVR that allows the linear addressing of up to 8M bytes of code and up to 16M bytes of data as well as a number of new functional and security features.

The ability to map the EEPROM in the code space allows parts of the program memory to be reprogrammed in-system. This technology combined with the versatile 8/16-bit CPU on a monolithic chip provides a highly flexible and cost-effective solution to many smart card applications.

Additional security features include power, frequency and temperature protection logic, logical scrambling on program data and addresses, Power Analysis countermeasures and memory accesses controlled by a supervisor mode.

Figure 1 shows the AT90SC6404RT block diagram.

Figure 1. AT90SC6404RT secureAVR Enhanced RISC Architecture



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Literature Requests
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