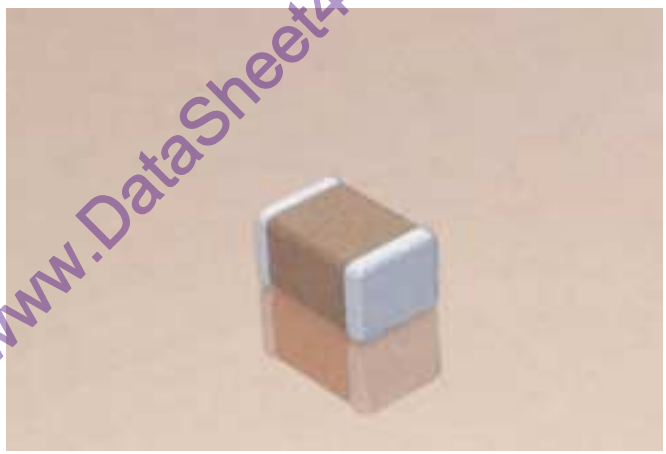
X7R Dielectric

General Specifications



X7R formulations are called “temperature stable” ceramics and fall into EIA Class II materials. X7R is the most popular of these intermediate dielectric constant materials. Its temperature variation of capacitance is within ±15% from -55°C to +125°C. This capacitance change is non-linear.

Capacitance for X7R varies under the influence of electrical operating conditions such as voltage and frequency.

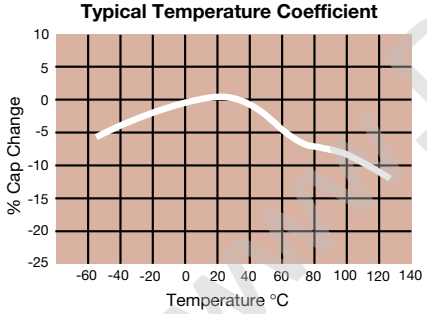
X7R dielectric chip usage covers the broad spectrum of industrial applications where known changes in capacitance due to applied voltages are acceptable.

PART NUMBER (see page 2 for complete part number explanation)

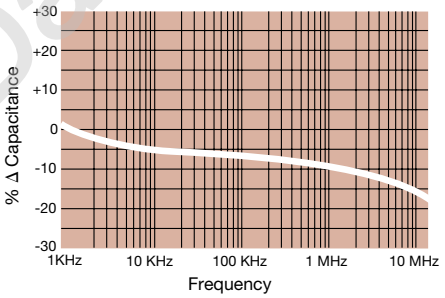
0805	5	C	103	M	A	T	2	A
Size (L" x W")	**Voltage** 6.3V = 6, 10V = Z, 16V = Y, 25V = 3, 50V = 5, 100V = 1, 200V = 2	**Dielectric** X7R = C	**Capacitance Code (In pF)** 2 Sig. Digits + Number of Zeros	**Capacitance Tolerance** Preferred J = ± 5%, K = ±10%, M = ± 20%	**Failure Rate** A = Not Applicable	**Terminations** T = Plated Ni and Sn, 7 = Gold Plated	**Packaging** 2 = 7" Reel, 4 = 13" Reel, 7 = Bulk Cass., 9 = Bulk	**Special Code** A = Std. Product

Contact Factory For Multiples

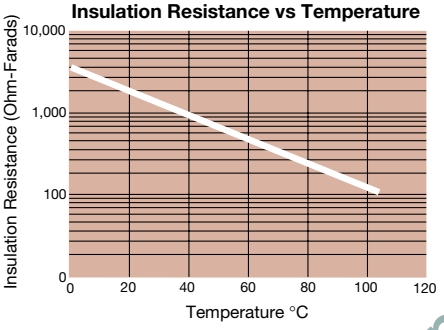
X7R Dielectric Typical Temperature Coefficient



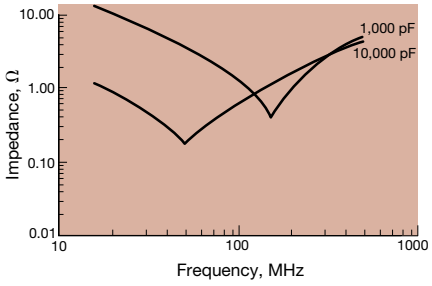
Δ Capacitance vs. Frequency



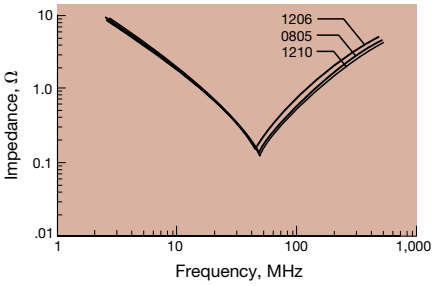
Insulation Resistance vs Temperature



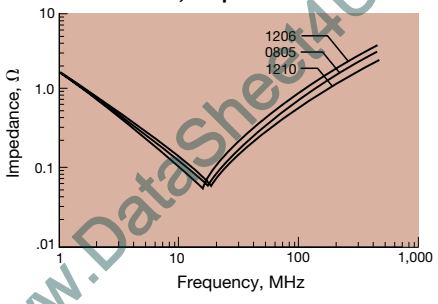
Variation of Impedance with Cap Value Impedance vs. Frequency 1,000 pF vs. 10,000 pF - X7R 0805



Variation of Impedance with Chip Size Impedance vs. Frequency 10,000 pF - X7R



Variation of Impedance with Chip Size Impedance vs. Frequency 100,000 pF - X7R



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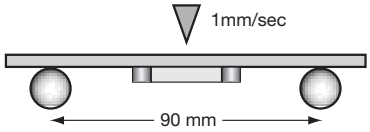
X7R Dielectric

Specifications and Test Methods

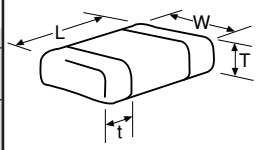
Parameter/Test		X7R Specification Limits	Measuring Conditions	
Operating Temperature Range		-55ºC to +125ºC	Temperature Cycle Chamber	
Capacitance		Within specified tolerance	Freq.: 1.0 kHz ± 10% Voltage: 1.0Vrms ± .2V For Cap > 10 µF, 0.5Vrms @ 120Hz	
Dissipation Factor		≤ 2.5% for ≥ 50V DC rating ≤ 3.0% for 25V DC rating ≤ 3.5% for 16V DC rating ≤ 5.0% for ≤ 10V DC rating		
Insulation Resistance		100,000MΩ or 1000MΩ - µF, whichever is less	Charge device with rated voltage for 60 ± 5 secs @ room temp/humidity	
Dielectric Strength		No breakdown or visual defects	Charge device with 300% of rated voltage for 1-5 seconds, w/charge and discharge current limited to 50 mA (max)	
Resistance to Flexure Stresses	Appearance	No defects	Deflection: 2mm Test Time: 30 seconds 	
	Capacitance Variation	≤ ±12%		
	Dissipation Factor	Meets Initial Values (As Above)		
	Insulation Resistance	≥ Initial Value x 0.3		
Solderability		≥ 95% of each terminal should be covered with fresh solder	Dip device in eutectic solder at 230 ± 5ºC for 5.0 ± 0.5 seconds	
Resistance to Solder Heat	Appearance	No defects, <25% leaching of either end terminal	Dip device in eutectic solder at 260ºC for 60 seconds. Store at room temperature for 24 ± 2 hours before measuring electrical properties.	
	Capacitance Variation	≤ ±7.5%		
	Dissipation Factor	Meets Initial Values (As Above)		
	Insulation Resistance	Meets Initial Values (As Above)		
	Dielectric Strength	Meets Initial Values (As Above)		
Thermal Shock	Appearance	No visual defects	Step 1: -55ºC ± 2º	30 ± 3 minutes
	Capacitance Variation	≤ ±7.5%	Step 2: Room Temp	≤ 3 minutes
	Dissipation Factor	Meets Initial Values (As Above)	Step 3: +125ºC ± 2º	30 ± 3 minutes
	Insulation Resistance	Meets Initial Values (As Above)	Step 4: Room Temp	≤ 3 minutes
	Dielectric Strength	Meets Initial Values (As Above)	Repeat for 5 cycles and measure after 24 ± 2 hours at room temperature	
Load Life	Appearance	No visual defects	Charge device with twice rated voltage in test chamber set at 125ºC ± 2ºC for 1000 hours (+48, -0) Remove from test chamber and stabilize at room temperature for 24 ± 2 hours before measuring.	
	Capacitance Variation	≤ ±12.5%		
	Dissipation Factor	≤ Initial Value x 2.0 (See Above)		
	Insulation Resistance	≥ Initial Value x 0.3 (See Above)		
	Dielectric Strength	Meets Initial Values (As Above)		
Load Humidity	Appearance	No visual defects	Store in a test chamber set at 85ºC ± 2ºC/ 85% ± 5% relative humidity for 1000 hours (+48, -0) with rated voltage applied. Remove from chamber and stabilize at room temperature and humidity for 24 ± 2 hours before measuring.	
	Capacitance Variation	≤ ±12.5%		
	Dissipation Factor	≤ Initial Value x 2.0 (See Above)		
	Insulation Resistance	≥ Initial Value x 0.3 (See Above)		
	Dielectric Strength	Meets Initial Values (As Above)		

X7R Dielectric

Capacitance Range

PREFERRED SIZES ARE SHADED

SIZE	0201		0402					0603							0805						1206					
Soldering	Reflow Only		Reflow Only					Reflow/Wave							Reflow/Wave						Reflow/Wave					
Packaging	All Paper		All Paper					All Paper							Paper/Embossed						Paper/Embossed					
(L) Length MM (in.)	0.60 ± 0.03 (0.024 ± 0.001)		1.00 ± 0.10 (0.040 ± 0.004)					1.60 ± 0.15 (0.063 ± 0.006)							2.01 ± 0.20 (0.079 ± 0.008)						3.20 ± 0.20 (0.126 ± 0.008)					
(W) Width MM (in.)	0.30 ± 0.03 (0.011 ± 0.001)		0.50 ± 0.10 (0.020 ± 0.004)					0.81 ± 0.15 (0.032 ± 0.006)							1.25 ± 0.20 (0.049 ± 0.008)						1.60 ± 0.20 (0.063 ± 0.008)					
(t) Terminal MM (in.)	0.15 ± 0.05 (0.006 ± 0.002)		0.25 ± 0.15 (0.010 ± 0.006)					0.35 ± 0.15 (0.014 ± 0.006)							0.50 ± 0.25 (0.020 ± 0.010)						0.50 ± 0.25 (0.020 ± 0.010)					
WVDC	10	16	6.3	10	16	25	50	6.3	10	16	25	50	100	200	10	16	25	50	100	200	10	16	25	50	100	200
Cap (pF) 100	A	A	C	C	C	C	C																			
120	A	A	C	C	C	C	C																			
150	A	A	C	C	C	C	C																			
180	A	A	C	C	C	C	C	G	G	G	G	G	G	G												
220	A	A	C	C	C	C	C	G	G	G	G	G	G	G												
270	A	A	C	C	C	C	C	G	G	G	G	G	G	G	E	E	E	E	E	E						
330	A	A	C	C	C	C	C	G	G	G	G	G	G	G	E	E	E	E	E	E						
390	A	A	C	C	C	C	C	G	G	G	G	G	G	G	E	E	E	E	E	E						
470	A	A	C	C	C	C	C	G	G	G	G	G	G	G	E	E	E	E	E	E						
560	A	A	C	C	C	C	C	G	G	G	G	G	G	G	E	E	E	E	E	E						
680	A	A	C	C	C	C	C	G	G	G	G	G	G	G	E	E	E	E	E	E						
820	A	A	C	C	C	C	C	G	G	G	G	G	G	G	E	E	E	E	E	E						
1000	A	A	C	C	C	C	C	G	G	G	G	G	G	G	E	E	E	E	E	E	J	J	J	J	J	J
1200			C	C	C	C	C	G	G	G	G	G	G		E	E	E	E	E	J	J	J	J	J	J	J
1500			C	C	C	C	C	G	G	G	G	G	G		E	E	E	E	E	J	J	J	J	J	J	J
1800			C	C	C	C	C	G	G	G	G	G	G		E	E	E	E	E	J	J	J	J	J	J	J
2200			C	C	C	C	C	G	G	G	G	G	G		E	E	E	E	E	J	J	J	J	J	J	J
2700			C	C	C	C	C	G	G	G	G	G	G		E	E	E	E	E	J	J	J	J	J	J	J
3300			C	C	C	C	C	G	G	G	G	G	G		E	E	E	E	E	J	J	J	J	J	J	J
3900			C	C	C	C	C	G	G	G	G	G	G		E	E	E	E	E	J	J	J	J	J	J	J
4700			C	C	C	C	C	G	G	G	G	G	G		E	E	E	E	J	J	J	J	J	J	J	J
5600			C	C	C	C	C	G	G	G	G	G	G		E	E	E	E	J	J	J	J	J	J	J	J
6800			C	C	C	C		G	G	G	G	G	G		E	E	E	E	J	J	J	J	J	J	J	J
8200			C	C	C	C		G	G	G	G	G	G		E	E	E	E	J	J	J	J	J	J	J	J
Cap. (µF) 0.010			C	C	C			G	G	G	G	G	G		E	E	E	E	J	J	J	J	J	J	J	J
0.012			C	C	C			G	G	G	G	G	G		J	J	J	J	J	J	J	J	J	J	J	M
0.015			C	C	C			G	G	G	G	G			J	J	J	J	J	J	J	J	J	J	J	M
0.018			C	C	C			G	G	G	G	G			J	J	J	J	J	M	J	J	J	J	J	M
0.022			C	C	C			G	G	G	G	G			J	J	J	J	J	M	J	J	J	J	J	M
0.027			C	C				G	G	G	G	G			J	J	J	J	J		J	J	J	J	J	M
0.033			C	C				G	G	G	G	G			J	J	J	J	M		J	J	J	J	J	M
0.039			C	C				G	G	G	G	G			J	J	J	J	M		J	J	J	J	J	M
0.047								G	G	G	G				J	J	J	J	M		J	J	J	J	J	M
0.056								G	G	G					J	J	J	J			J	J	J	J	J	P
0.068								G	G	G					J	J	J	J			J	J	J	J	J	P
0.082								G	G	G					J	J	J	J			J	J	J	J	M	
0.10								G	G	G					J	J	J	J			J	J	J	J	M	
0.12								G	G	G					J	J	J	J	M		J	J	J	J		
0.15								G	G	G					J	J	J	J			J	J	J	J		
0.18								G	G						J	J	M				J	J	J	J		
0.22								G	G						J	J	M				J	J	J	J		
0.27															M	M					J	J	J	M		
0.33															M	M					J	J	M	M		
0.47															N	M					M	M	M	M		
0.56															N						M	M	Q			
0.68															N						M	M	Q			
0.82															N						M	M	Q			
1.0															N						M	M	Q			
1.2																					P					
1.5																					P					
1.8																					P					
2.2																					Q					
3.3																										
4.7																										
10																										
22																										
47																										
100																										
WVDC	10	16	6.3	10	16	25	50	6.3	10	16	25	50	100	200	10	16	25	50	100	200	10	16	25	50	100	200
SIZE	0201		0402					0603							0805						1206					



Letter	A	C	E	G	J	K	M	N	P	Q	X	Y	Z	BB	CC
Max. Thickness	0.33 (0.013)	0.56 (0.022)	0.71 (0.028)	0.86 (0.034)	0.94 (0.037)	1.02 (0.040)	1.27 (0.050)	1.40 (0.055)	1.52 (0.060)	1.78 (0.070)	2.29 (0.090)	2.54 (0.100)	2.79 (0.110)	3.05 (0.120)	3.175 (0.125)
	PAPER					EMBOSSED									

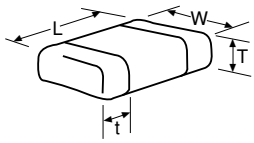
Contact Factory for Multiples

X7R Dielectric

Capacitance Range

PREFERRED SIZES ARE SHADED

SIZE	1210					1812				1825		2220			2225	
Soldering	Reflow/Wave					Reflow Only				Reflow Only		Reflow Only			Reflow Only	
Packaging	Paper/Embossed					All Embossed				All Embossed		All Embossed			All Embossed	
(L) Length MM (in.)	3.20 ± 0.20 (0.126 ± 0.008)					4.50 ± 0.30 (0.177 ± 0.012)				4.50 ± 0.30 (0.177 ± 0.012)		5.7 ± 0.40 (0.224 ± 0.016)			5.72 ± 0.25 (0.225 ± 0.010)	
(W) Width MM (in.)	2.50 ± 0.20 (0.098 ± 0.008)					3.20 ± 0.20 (0.126 ± 0.008)				6.40 ± 0.40 (0.252 ± 0.016)		5.0 ± 0.40 (0.197 ± 0.016)			6.35 ± 0.25 (0.250 ± 0.010)	
(t) Terminal MM (in.)	0.50 ± 0.25 (0.020 ± 0.010)					0.61 ± 0.36 (0.024 ± 0.014)				0.61 ± 0.36 (0.024 ± 0.014)		0.64 ± 0.39 (0.025 ± 0.015)			0.64 ± 0.39 (0.025 ± 0.015)	
WVDC	10	16	25	50	100	16	25	50	100	50	100	50	100	200	50	100
Cap (pF) 100																
120																
150																
180																
220																
270																
330																
390																
470																
560																
680																
820																
1000	J	J	J	J	J											
1200	J	J	J	J	J											
1500	J	J	J	J	J											
1800	J	J	J	J	J											
2200	J	J	J	J	J											
2700	J	J	J	J	J											
3300	J	J	J	J	J											
3900	J	J	J	J	J											
4700	J	J	J	J	J											
5600	J	J	J	J	J											
6800	J	J	J	J	J											
8200	J	J	J	J	J											
Cap. (µF) 0.010	J	J	J	J	J			K	K	M	M	X	X	X	M	M
0.012	J	J	J	J	J			K	K	M	M	X	X	X	M	M
0.015	J	J	J	J	J			K	K	M	M	X	X	X	M	M
0.018	J	J	J	J	J			K	K	M	M	X	X	X	M	M
0.022	J	J	J	J	J			K	K	M	M	X	X	X	M	M
0.027	J	J	J	J	J			K	K	M	M	X	X	X	M	M
0.033	J	J	J	J	J			K	K	M	M	X	X	X	M	M
0.039	J	J	J	J	J			K	K	M	M	X	X	X	M	M
0.047	J	J	J	J	J			K	K	M	M	X	X	X	M	M
0.056	J	J	J	J	J			K	K	M	M	X	X	X	M	M
0.068	J	J	J	J	J			K	K	M	M	X	X	X	M	M
0.082	J	J	J	J	J			K	K	M	M	X	X	X	M	M
0.10	J	J	J	J	J			K	K	M	M	X	X	X	M	M
0.12	J	J	J	J	M			K	K	M	M	X	X	X	M	M
0.15	J	J	J	J	M			K	K	M	M	X	X	X	M	M
0.18	J	J	J	J	P			K	K	M	M	X	X	X	M	M
0.22	J	J	J	J	P			K	K	M	M	X	X	X	M	M
0.27	J	J	J	J	Z			K	M	M	M	X	X		M	M
0.33	J	J	J	J	Z			K	M	M	M	X	X		M	M
0.47	M	M	M	M	Z			K	P	M	M	X	X		M	M
0.56	M	M	M		Z			M	Q	M	M	X	X		M	M
0.68	M	M	P		Z			M	X	M	Q	X	X		M	M
0.82	M	M	P					M	X	M	Q	X			M	M
1.0	N	N	P	X	Z			M	X	M	Q	X			M	M
1.2	N	N					M			M		X			M	P
1.5	N	N								M					M	P
1.8	N	P													M	
2.2			X										Z		M	
3.3																
4.7	Q	Z														
10						Z										
22																
47																
100																
WVDC	10	16	25	50	100	16	25	50	100	50	100	50	100	200	50	100
SIZE	1210					1812				1825		2220			2225	

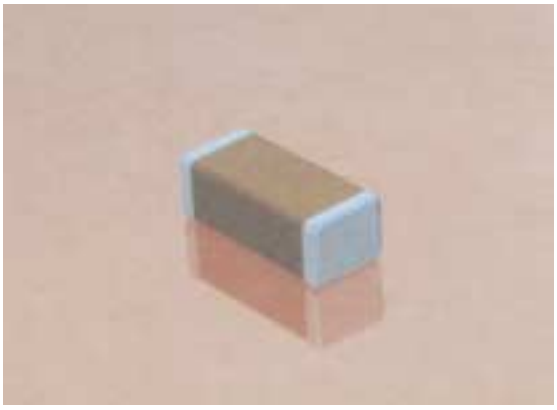


Letter	A	C	E	G	J	K	M	N	P	Q	X	Y	Z	BB	CC
Max. Thickness	0.33 (0.013)	0.56 (0.022)	0.71 (0.028)	0.86 (0.034)	0.94 (0.037)	1.02 (0.040)	1.27 (0.050)	1.40 (0.055)	1.52 (0.060)	1.78 (0.070)	2.29 (0.090)	2.54 (0.100)	2.79 (0.110)	3.05 (0.120)	3.175 (0.125)
	PAPER					EMBOSSED									

Contact Factory for Multiples

High Voltage Chips

For 500V to 5000V Applications



High value, low leakage and small size are difficult parameters to obtain in capacitors for high voltage systems. AVX special high voltage MLC chips capacitors meet these performance characteristics and are designed for applications such as snubbers in high frequency power converters, resonators in SMPS, and high voltage coupling/DC blocking. These high voltage chip designs exhibit low ESRs at high frequencies.

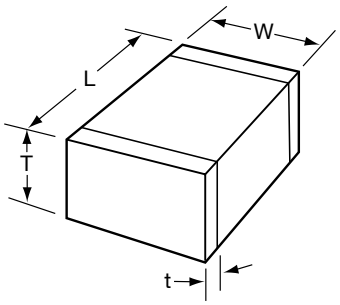
Larger physical sizes than normally encountered chips are used to make high voltage chips. These larger sizes require that special precautions be taken in applying these chips in surface mount assemblies. This is due to differences in the coefficient of thermal expansion (CTE) between the substrate materials and chip capacitors. Apply heat at less than 4°C per second during the preheat. Maximum preheat temperature must be within 50°C of the soldering temperature. The solder temperature should not exceed 230°C. Chips 1808 and larger to use reflow soldering only.

Capacitors with X7R Dielectrics are not intended for AC line filtering applications.

Contact plant for recommendations. Capacitors may require protective surface coating to prevent external arcing.

PART NUMBER (see page 2 for complete information and options)

1808	A	A	271	K	A	1	1A
AVX Style	**Voltage**	**Temperature Coefficient**	**Capacitance Code**	**Capacitance Tolerance**	**Failure Rate**	**Termination**	**Packaging/Marking**
1206	7 = 500V	A = C0G	(2 significant digits + no. of zeros)	C0G: J = ±5%	A=Not Applicable	1= Pd/Ag	1A = 7" Reel Unmarked
1210	C = 600V	C = X7R	Examples:	K = ±10%		T = Plated Ni and Solder	3A = 13" Reel Unmarked
1808	A = 1000V		10 pF = 100	M = ±20%			9A = Bulk/Unmarked
1812	S = 1500V		100 pF = 101	X7R: K = ±10%			
1825	G = 2000V		1,000 pF = 102	M = ±20%			
2220	W = 2500V		22,000 pF = 223	Z = +80%, -20%			
2225	H = 3000V		220,000 pF = 224				
3640	J = 4000V		1 µF = 105				
	K = 5000V						



DIMENSIONS

millimeters (inches)

SIZE	1206	1210	1808*	1812*	1825*	2220*	2225*	3640*
(L) Length	3.20 ± 0.2 (0.126 ± 0.008)	3.20 ± 0.2 (0.126 ± 0.008)	4.57 ± 0.25 (0.180 ± 0.010)	4.50 ± 0.3 (0.177 ± 0.012)	4.50 ± 0.3 (0.177 ± 0.012)	5.7 ± 0.4 (0.224 ± 0.016)	5.72 ± 0.25 (0.225 ± 0.010)	9.14 ± 0.25 (0.360 ± 0.010)
(W) Width	1.60 ± 0.2 (0.063 ± 0.008)	2.50 ± 0.2 (0.098 ± 0.008)	2.03 ± 0.25 (0.080 ± 0.010)	3.20 ± 0.2 (0.126 ± 0.008)	6.40 ± 0.3 (0.252 ± 0.012)	5.0 ± 0.4 (0.197 ± 0.016)	6.35 ± 0.25 (0.250 ± 0.010)	10.2 ± 0.25 (0.400 ± 0.010)
(T) Thickness Max.	1.52 (0.060)	1.70 (0.067)	2.03 (0.080)	2.54 (0.100)	2.54 (0.100)	3.3 (0.130)	2.54 (0.100)	2.54 (0.100)
(t) terminal min.	0.25 (0.010)	0.25 (0.010)	0.25 (0.010)	0.25 (0.010)	0.25 (0.010)	0.25 (0.010)	0.25 (0.010)	0.76 (0.030)
max.	0.75 (0.030)	0.75 (0.030)	1.02 (0.040)	1.02 (0.040)	1.02 (0.040)	1.02 (0.040)	1.02 (0.040)	1.52 (0.060)

*Reflow Soldering Only

High Voltage Chips

For 500V to 5000V Applications

C0G Dielectric

PERFORMANCE CHARACTERISTICS

Capacitance Range	10 pF to 0.047 µF (25°C, 1.0 ±0.2 Vrms at 1kHz, for ≤ 1000 pF use 1 MHz)
Capacitance Tolerances	±5%, ±10%, ±20%
Dissipation Factor	0.1% max. (+25°C, 1.0 ±0.2 Vrms, 1kHz, for ≤ 1000 pF use 1 MHz)
Operating Temperature Range	-55°C to +125°C
Temperature Characteristic	0 ±30 ppm/°C (0 VDC)
Voltage Ratings	500, 600, 1000, 1500, 2000, 2500, 3000, 4000 & 5000 VDC (+125°C)
Insulation Resistance (+25°C, at 500 VDC)	100K MΩ min. or 1000 MΩ - µF min., whichever is less
Insulation Resistance (+125°C, at 500 VDC)	10K MΩ min. or 100 MΩ - µF min., whichever is less
Dielectric Strength	500V, 150% rated voltage for 5 seconds at 50 mA max. current ≥ 600V, 120% rated voltage for 5 seconds at 50 mA max. current

HIGH VOLTAGE C0G CAPACITANCE VALUES

VOLTAGE		1206	1210	1808	1812	1825	2220	2225	3640
500	min.	—	—	—	—	—	—	—	—
	max.	680 pF	1500 pF	3300 pF	5600 pF	0.012 µF	—	0.018 µF	—
600	min.	100 pF	100 pF	100 pF	100 pF	1000 pF	1000 pF	1000 pF	1000 pF
	max.	680 pF	1500 pF	2700 pF	5600 pF	0.012 µF	0.012 µF	0.015 µF	0.047 µF
1000	min.	10 pF	100 pF	100 pF	100 pF	100 pF	1000 pF	1000 pF	1000 pF
	max.	470 pF	820 pF	1500 pF	2700 pF	6800 pF	0.010 µF	0.010 µF	0.018 µF
1500	min.	10 pF	100 pF	10 pF	10 pF	100 pF	1000 pF	1000 pF	100 pF
	max.	150 pF	330 pF	470 pF	1000 pF	2700 pF	2700 pF	3300 pF	8200 pF
2000	min.	10 pF	10 pF	10 pF	10 pF	100 pF	1000 pF	1000 pF	100 pF
	max.	68 pF	150 pF	270 pF	680 pF	1800 pF	2200 pF	2200 pF	5600 pF
2500	min.	—	—	10 pF	10 pF	10 pF	100 pF	100 pF	100 pF
	max.	—	—	150 pF	390 pF	1000 pF	1000 pF	1200 pF	3900 pF
3000	min.	—	—	10 pF	10 pF	10 pF	10 pF	10 pF	100 pF
	max.	—	—	100 pF	330 pF	680 pF	680 pF	820 pF	2200 pF
4000	min.	—	—	10 pF	10 pF	10 pF	10 pF	10 pF	100 pF
	max.	—	—	39 pF	100 pF	220 pF	220 pF	330 pF	1000 pF
5000	min.	—	—	—	—	—	—	—	10 pF
	max.	—	—	—	—	—	—	—	680 pF

X7R Dielectric

PERFORMANCE CHARACTERISTICS

Capacitance Range	10 pF to 0.56 µF (25°C, 1.0 ±0.2 Vrms at 1kHz)
Capacitance Tolerances	±10%; ±20%; +80%, -20%
Dissipation Factor	2.5% max. (+25°C, 1.0 ±0.2 Vrms, 1kHz)
Operating Temperature Range	-55°C to +125°C
Temperature Characteristic	±15% (0 VDC)
Voltage Ratings	500,600, 1000, 1500, 2000, 2500, 3000, 4000 & 5000 VDC (+125°C)
Insulation Resistance (+25°C, at 500 VDC)	100K MΩ min. or 1000 MΩ - µF min., whichever is less
Insulation Resistance (+125°C, at 500 VDC)	10K MΩ min. or 100 MΩ - µF min., whichever is less
Dielectric Strength	500V, 150% rated voltage for 5 seconds at 50 mA max. current ≥ 600V, 120% rated voltage for 5 seconds at 50 mA max. current

HIGH VOLTAGE X7R MAXIMUM CAPACITANCE VALUES

VOLTAGE		1206	1210	1808	1812	1825	2220	2225	3640
500	min.	—	—	—	—	—	—	—	—
	max.	0.015 µF	0.027 µF	—	0.056 µF	—	—	—	—
600	min.	1000 pF	1000 pF	.01 µF	.01 µF	.01 µF	.01 µF	.01 µF	.01 µF
	max.	0.015 µF	0.027 µF	0.033 µF	0.068 µF	0.15 µF	0.15 µF	0.22 µF	0.56 µF
1000	min.	1000 pF	1000 pF	1000 pF	1000 pF	1000 pF	.01 µF	.01 µF	.01 µF
	max.	4700 pF	0.010 µF	0.015 µF	0.027 µF	0.068 µF	0.068 µF	0.082 µF	0.22 µF
1500	min.	100 pF	100 pF	100 pF	100 pF	1000 pF	1000 pF	1000 pF	.01 µF
	max.	1200 pF	2700 pF	3900 pF	8200 pF	0.018 µF	0.022 µF	0.027 µF	0.068 µF
2000	min.	10 pF	100 pF	100 pF	100 pF	100 pF	1000 pF	1000 pF	1000 pF
	max.	470 pF	1000 pF	1800 pF	4700 pF	8200 pF	0.010 µF	0.012 µF	0.027 µF
2500	min.	—	—	10 pF	10 pF	100 pF	1000 pF	1000 pF	1000 pF
	max.	—	—	1200 pF	2200 pF	5600 pF	6800 pF	8200 pF	0.022 µF
3000	min.	—	—	10 pF	10 pF	100 pF	1000 pF	1000 pF	1000 pF
	max.	—	—	560 pF	1200 pF	2700 pF	3300pF	4700 pF	0.018 µF
4000	min.	—	—	—	—	—	—	—	100 pF
	max.	—	—	—	—	—	—	—	6800 pF
5000	min.	—	—	—	—	—	—	—	100 pF
	max.	—	—	—	—	—	—	—	3300 pF

Packaging of Chip Components

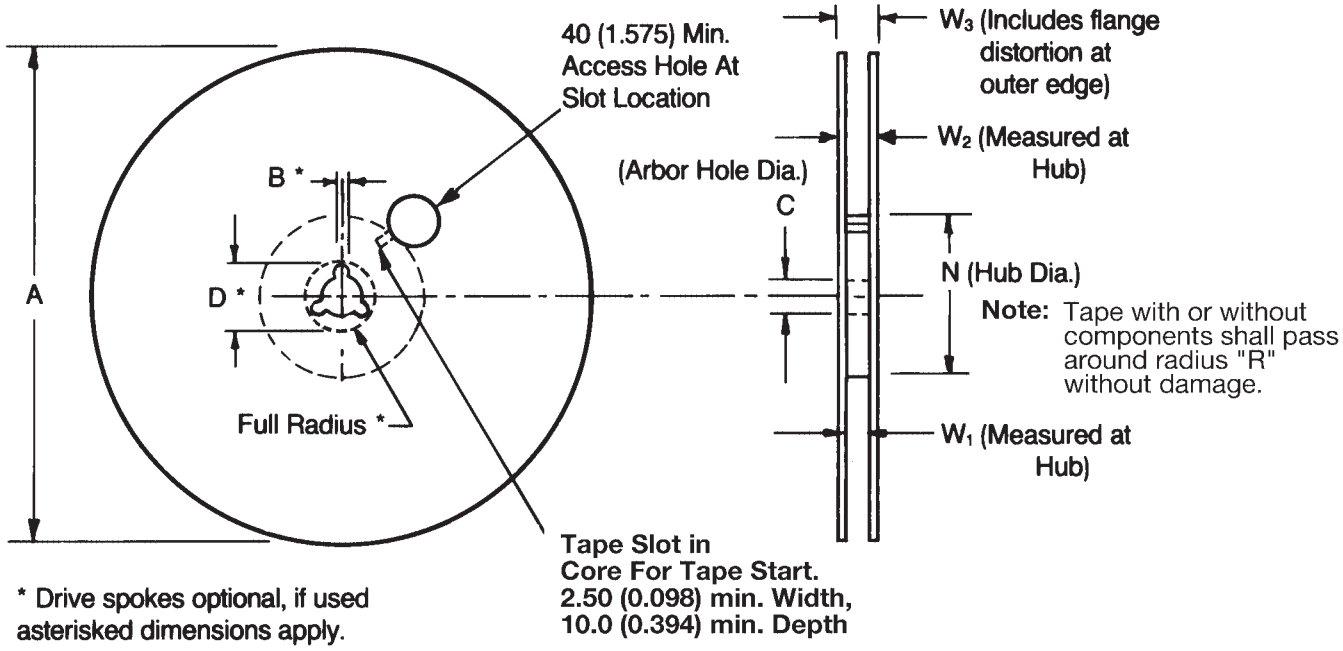
Automatic Insertion Packaging

TAPE & REEL QUANTITIES

All tape and reel specifications are in compliance with RS481.

	8mm	12mm	
Paper or Embossed Carrier	0612, 0508, 0805, 1206, 1210		
Embossed Only	0306	1808	1812, 1825 2220, 2225
Paper Only	0201, 0402, 0603		
Qty. per Reel/7" Reel	2,000, 3,000 or 4,000, 10,000, 15,000 Contact factory for exact quantity	3,000	500, 1,000 Contact factory for exact quantity
Qty. per Reel/13" Reel	5,000, 10,000, 50,000 Contact factory for exact quantity	10,000	4,000

REEL DIMENSIONS

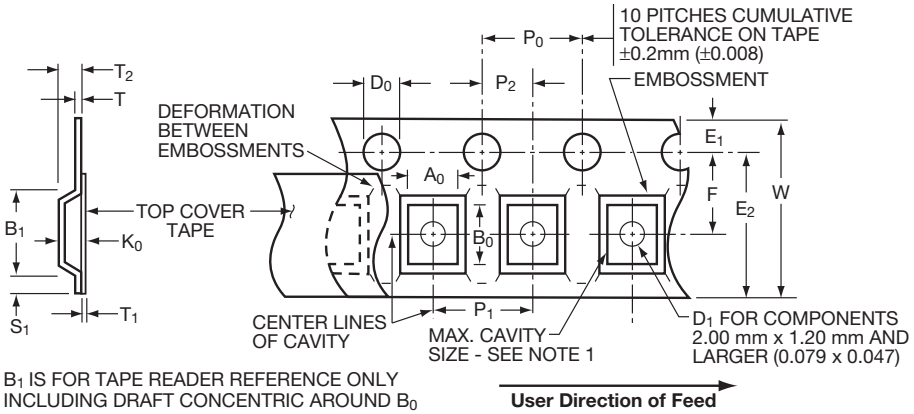


Tape Size(1)	A Max.	B* Min.	C	D* Min.	N Min.	W_1	W_2 Max.	W_3
8mm	330 (12.992)	1.5 (0.059)	$13.0^{+0.50}_{-0.20}$ ($0.512^{+0.020}_{-0.008}$)	20.2 (0.795)	50.0 (1.969)	$8.40^{+1.5}_{-0.0}$ ($0.331^{+0.059}_{-0.0}$)	14.4 (0.567)	7.90 Min. (0.311) 10.9 Max. (0.429)
12mm						$12.4^{+2.0}_{-0.0}$ ($0.488^{+0.079}_{-0.0}$)	18.4 (0.724)	11.9 Min. (0.469) 15.4 Max. (0.607)

Metric dimensions will govern.
English measurements rounded and for reference only.
(1) For tape sizes 16mm and 24mm (used with chip size 3640) consult EIA RS-481 latest revision.

Embossed Carrier Configuration

8 & 12mm Tape Only



8 & 12mm Embossed Tape Metric Dimensions Will Govern

CONSTANT DIMENSIONS

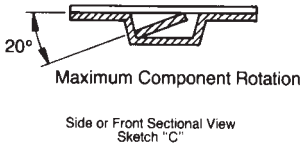
Tape Size	D_0	E	P_0	P_2	S_1 Min.	T Max.	T_1
8mm and 12mm	$1.50^{+0.10}_{-0.0}$ ($0.059^{+0.004}_{-0.0}$)	1.75 ± 0.10 (0.069 ± 0.004)	4.0 ± 0.10 (0.157 ± 0.004)	2.0 ± 0.05 (0.079 ± 0.002)	0.60 (0.024)	0.60 (0.024)	0.10 (0.004) Max.

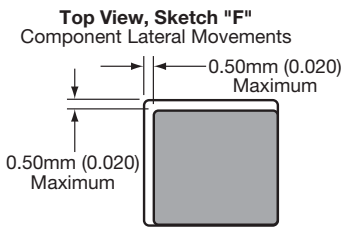
VARIABLE DIMENSIONS

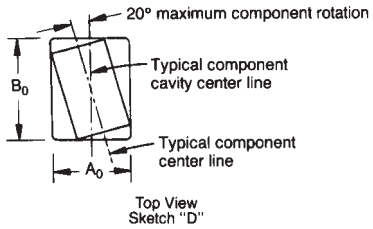
Tape Size	B_1 Max.	D_1 Min.	E_2 Min.	F	P_1 See Note 5	R Min. See Note 2	T_2	W Max.	A_0 B_0 K_0
8mm	4.35 (0.171)	1.00 (0.039)	6.25 (0.246)	3.50 ± 0.05 (0.138 ± 0.002)	4.00 ± 0.10 (0.157 ± 0.004)	25.0 (0.984)	2.50 Max. (0.098)	8.30 (0.327)	See Note 1
12mm	8.20 (0.323)	1.50 (0.059)	10.25 (0.404)	5.50 ± 0.05 (0.217 ± 0.002)	4.00 ± 0.10 (0.157 ± 0.004)	30.0 (1.181)	6.50 Max. (0.256)	12.3 (0.484)	See Note 1
8mm 1/2 Pitch	4.35 (0.171)	1.00 (0.039)	6.25 (0.246)	3.50 ± 0.05 (0.138 ± 0.002)	2.00 ± 0.10 (0.079 ± 0.004)	25.0 (0.984)	2.50 Max. (0.098)	8.30 (0.327)	See Note 1
12mm Double Pitch	8.20 (0.323)	1.50 (0.059)	10.25 (0.404)	5.50 ± 0.05 (0.217 ± 0.002)	8.00 ± 0.10 (0.315 ± 0.004)	30.0 (1.181)	6.50 Max. (0.256)	12.3 (0.484)	See Note 1

NOTES:

1. The cavity defined by A_0, B_0, and K_0 shall be configured to provide the following:
   Surround the component with sufficient clearance such that:
   a) the component does not protrude beyond the sealing plane of the cover tape.
   b) the component can be removed from the cavity in a vertical direction without mechanical restriction, after the cover tape has been removed.
   c) rotation of the component is limited to 20° maximum (see Sketches D & E).
   d) lateral movement of the component is restricted to 0.5mm maximum (see Sketch F).
2. Tape with or without components shall pass around radius "R" without damage.
3. Bar code labeling (if required) shall be on the side of the reel opposite the round sprocket holes. Refer to EIA-556.
4. B_1 dimension is a reference dimension for tape feeder clearance only.
5. If P_1 = 2.0mm, the tape may not properly index in all tape feeders.

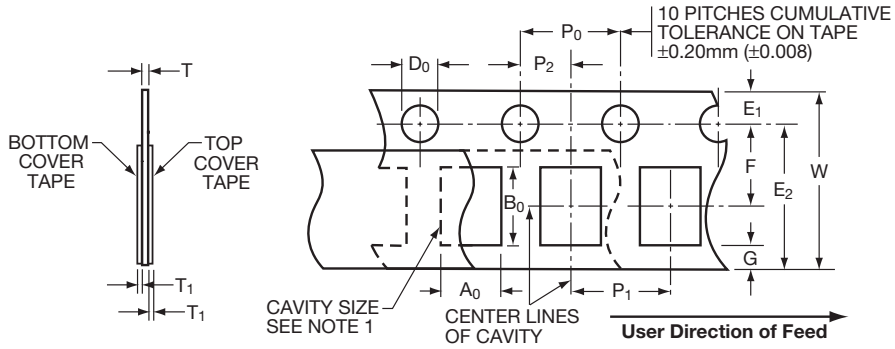






Paper Carrier Configuration

8 & 12mm Tape Only



8 & 12mm Paper Tape Metric Dimensions Will Govern

CONSTANT DIMENSIONS

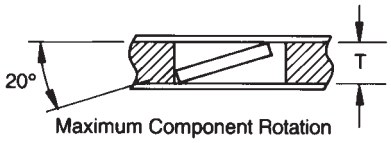
Tape Size	D_0	E	P_0	P_2	T_1	G. Min.	R Min.
8mm and 12mm	$1.50^{+0.10}_{-0.0}$ ($0.059^{+0.004}_{-0.0}$)	1.75 ± 0.10 (0.069 ± 0.004)	4.00 ± 0.10 (0.157 ± 0.004)	2.00 ± 0.05 (0.079 ± 0.002)	0.10 (0.004) Max.	0.75 (0.030) Min.	25.0 (0.984) See Note 2 Min.

VARIABLE DIMENSIONS

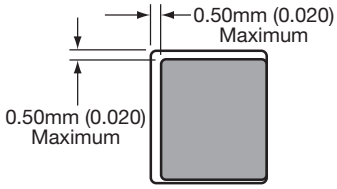
Tape Size	P_1 See Note 4	E_2 Min.	F	W	A_0 B_0	T
8mm	4.00 ± 0.10 (0.157 ± 0.004)	6.25 (0.246)	3.50 ± 0.05 (0.138 ± 0.002)	$8.00^{+0.30}_{-0.10}$ ($0.315^{+0.012}_{-0.004}$)	See Note 1	1.10mm (0.043) Max. for Paper Base Tape and 1.60mm (0.063) Max. for Non-Paper Base Compositions
12mm	4.00 ± 0.010 (0.157 ± 0.004)	10.25 (0.404)	5.50 ± 0.05 (0.217 ± 0.002)	12.0 ± 0.30 (0.472 ± 0.012)		
8mm 1/2 Pitch	2.00 ± 0.05 (0.079 ± 0.002)	6.25 (0.246)	3.50 ± 0.05 (0.138 ± 0.002)	$8.00^{+0.30}_{-0.10}$ ($0.315^{+0.012}_{-0.004}$)		
12mm Double Pitch	8.00 ± 0.10 (0.315 ± 0.004)	10.25 (0.404)	5.50 ± 0.05 (0.217 ± 0.002)	12.0 ± 0.30 (0.472 ± 0.012)		

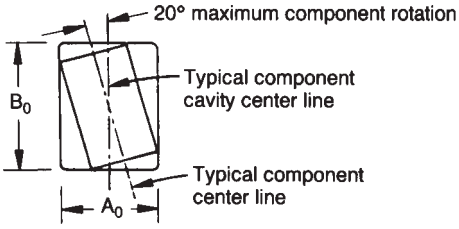
NOTES:

1. The cavity defined by A_0, B_0, and T shall be configured to provide sufficient clearance surrounding the component so that:
   a) the component does not protrude beyond either surface of the carrier tape;
   b) the component can be removed from the cavity in a vertical direction without mechanical restriction after the top cover tape has been removed;
   c) rotation of the component is limited to 20° maximum (see Sketches A & B);
   d) lateral movement of the component is restricted to 0.5mm maximum (see Sketch C).
2. Tape with or without components shall pass around radius "R" without damage.
3. Bar code labeling (if required) shall be on the side of the reel opposite the sprocket holes. Refer to EIA-556.
4. If P_1 = 2.0mm, the tape may not properly index in all tape feeders.



Side or Front Sectional View
Sketch "A"





Top View
Sketch "B"

Bar Code Labeling Standard

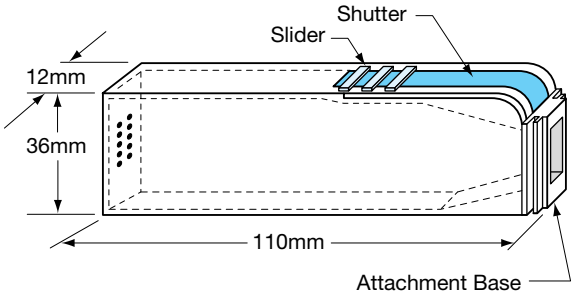
AVX bar code labeling is available and follows latest version of EIA-556

Bulk Case Packaging

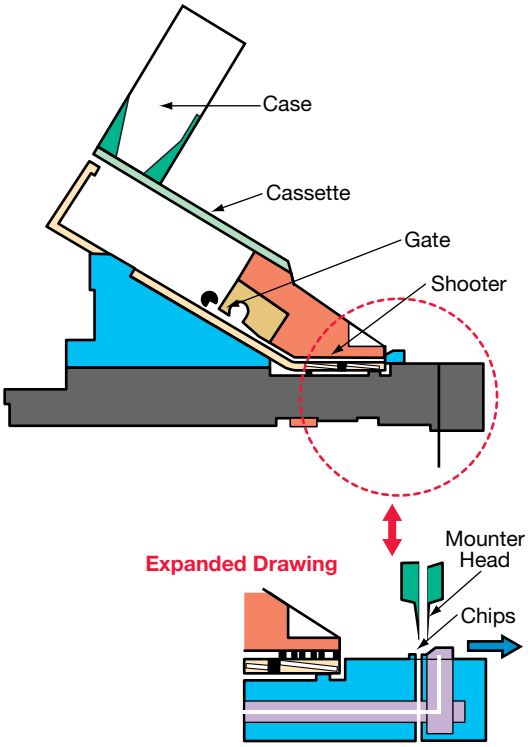
BENEFITS

- Easier handling
- Smaller packaging volume
  (1/20 of T/R packaging)
- Easier inventory control
- Flexibility
- Recyclable

CASE DIMENSIONS



BULK FEEDER



CASE QUANTITIES

Part Size	0402	0603	0805	1206
Qty. (pcs / cassette)	80,000	15,000	10,000 (T=.023") 8,000 (T=.031") 6,000 (T=.043")	5,000 (T=.023") 4,000 (T=.032") 3,000 (T=.044")

Basic Capacitor Formulas

I. Capacitance (farads)

English: $C = \frac{.224\ K\ A}{T_D}$

Metric: $C = \frac{.0884\ K\ A}{T_D}$

II. Energy stored in capacitors (Joules, watt - sec)

$E = \frac{1}{2} CV^2$

III. Linear charge of a capacitor (Amperes)

$I = C \frac{dV}{dt}$

IV. Total Impedance of a capacitor (ohms)

$Z = \sqrt{R_S^2 + (X_C - X_L)^2}$

V. Capacitive Reactance (ohms)

$x_C = \frac{1}{2 \pi fC}$

VI. Inductive Reactance (ohms)

$x_L = 2 \pi fL$

VII. Phase Angles:

Ideal Capacitors: Current leads voltage 90°
Ideal Inductors: Current lags voltage 90°
Ideal Resistors: Current in phase with voltage

VIII. Dissipation Factor (%)

$D.F. = \tan \delta \text{ (loss angle)} = \frac{E.S.R.}{X_C} = (2 \pi fC)(E.S.R.)$

IX. Power Factor (%)

P.F. = Sine δ (loss angle) = Cos ϕ (phase angle)
P.F. = (when less than 10%) = DF

X. Quality Factor (dimensionless)

$Q = \text{Cotan } \delta \text{ (loss angle)} = \frac{1}{D.F.}$

XI. Equivalent Series Resistance (ohms)

$E.S.R. = (D.F.)(Xc) = (D.F.) / (2 \pi fC)$

XII. Power Loss (watts)

Power Loss $= (2 \pi fCV^2)(D.F.)$

XIII. KVA (Kilowatts)

$KVA = 2 \pi fCV^2 \times 10^{-3}$

XIV. Temperature Characteristic (ppm/°C)

$T.C. = \frac{Ct - C_{25}}{C_{25}(T_t - 25)} \times 10^6$

XV. Cap Drift (%)

$C.D. = \frac{C_1 - C_2}{C_1} \times 100$

XVI. Reliability of Ceramic Capacitors

$\frac{L_0}{L_t} = \left(\frac{V_t}{V_o}\right)^X \left(\frac{T_t}{T_o}\right)^Y$

XVII. Capacitors in Series (current the same)

Any Number: $\frac{1}{C_T} = \frac{1}{C_1} + \frac{1}{C_2} --- \frac{1}{C_N}$

Two: $C_T = \frac{C_1 C_2}{C_1 + C_2}$

XVIII. Capacitors in Parallel (voltage the same)

$C_T = C_1 + C_2 --- + C_N$

XIX. Aging Rate

A.R. = %Δ C/decade of time

XX. Decibels

$db = 20 \log \frac{V_1}{V_2}$

METRIC PREFIXES

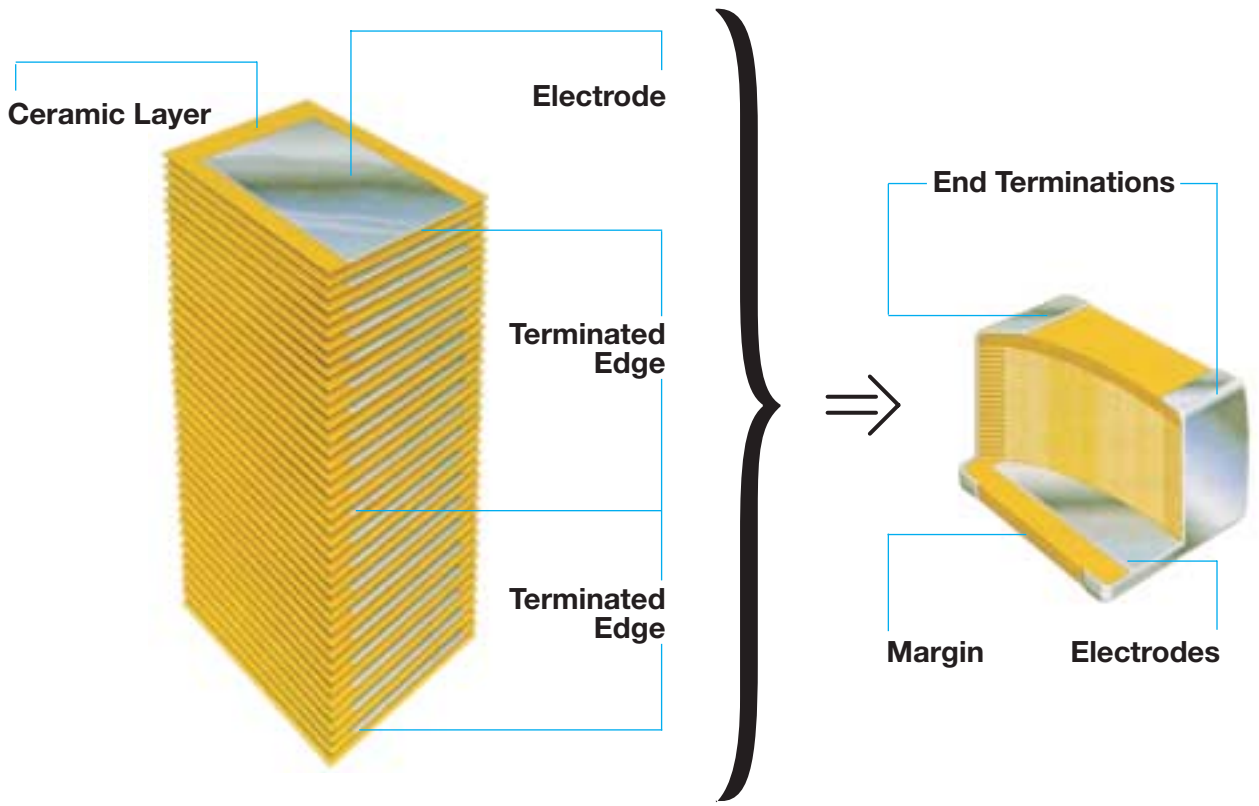
Pico	$X\ 10^{-12}$
Nano	$X\ 10^{-9}$
Micro	$X\ 10^{-6}$
Milli	$X\ 10^{-3}$
Deci	$X\ 10^{-1}$
Deca	$X\ 10^{+1}$
Kilo	$X\ 10^{+3}$
Mega	$X\ 10^{+6}$
Giga	$X\ 10^{+9}$
Tera	$X\ 10^{+12}$

SYMBOLS

K	= Dielectric Constant	f	= frequency	L_t	= Test life
A	= Area	L	= Inductance	V_t	= Test voltage
T_D	= Dielectric thickness	δ	= Loss angle	V_o	= Operating voltage
V	= Voltage	ϕ	= Phase angle	T_t	= Test temperature
t	= time	X & Y	= exponent effect of voltage and temp.	T_o	= Operating temperature
R_S	= Series Resistance	L_o	= Operating life		

General Description

Basic Construction – A multilayer ceramic (MLC) capacitor is a monolithic block of ceramic containing two sets of offset, interleaved planar electrodes that extend to two opposite surfaces of the ceramic dielectric. This simple structure requires a considerable amount of sophistication, both in material and manufacture, to produce it in the quality and quantities needed in today's electronic equipment.



Multilayer Ceramic Capacitor

Figure 1

Formulations – Multilayer ceramic capacitors are available in both Class 1 and Class 2 formulations. Temperature compensating formulation are Class 1 and temperature stable and general application formulations are classified as Class 2.

Class 1 – Class 1 capacitors or temperature compensating capacitors are usually made from mixtures of titanates where barium titanate is normally not a major part of the mix. They have predictable temperature coefficients and in general, do not have an aging characteristic. Thus they are the most stable capacitor available. The most popular Class 1 multilayer ceramic capacitors are C0G (NP0) temperature compensating capacitors (negative-positive 0 ppm/°C).

Class 2 – EIA Class 2 capacitors typically are based on the chemistry of barium titanate and provide a wide range of capacitance values and temperature stability. The most commonly used Class 2 dielectrics are X7R and Y5V. The X7R provides intermediate capacitance values which vary only ±15% over the temperature range of -55°C to 125°C. It finds applications where stability over a wide temperature range is required.

The Y5V provides the highest capacitance values and is used in applications where limited temperature changes are expected. The capacitance value for Y5V can vary from 22% to -82% over the -30°C to 85°C temperature range. The Z5U dielectric is between X7R and Y5V in both stability and capacitance range.

All Class 2 capacitors vary in capacitance value under the influence of temperature, operating voltage (both AC and DC), and frequency. For additional information on performance changes with operating conditions, consult AVX's software, SpiCap.

Table 1: EIA and MIL Temperature Stable and General Application Codes

EIA CODE Percent Capacity Change Over Temperature Range	
RS198	**Temperature Range**
X7	-55°C to +125°C
X5	-55°C to +85°C
Y5	-30°C to +85°C
Z5	+10°C to +85°C
Code	**Percent Capacity Change**
D	±3.3%
E	±4.7%
F	±7.5%
P	±10%
R	±15%
S	±22%
T	+22%, -33%
U	+22%, - 56%
V	+22%, -82%
EXAMPLE – A capacitor is desired with the capacitance value at 25°C to increase no more than 7.5% or decrease no more than 7.5% from -30°C to +85°C. EIA Code will be Y5F.	

MIL CODE		
Symbol	**Temperature Range**	
A	-55°C to +85°C	
B	-55°C to +125°C	
C	-55°C to +150°C	
Symbol	**Cap. Change Zero Volts**	**Cap. Change Rated Volts**
R	+15%, -15%	+15%, -40%
W	+22%, -56%	+22%, -66%
X	+15%, -15%	+15%, -25%
Y	+30%, -70%	+30%, -80%
Z	+20%, -20%	+20%, -30%
Temperature characteristic is specified by combining range and change symbols, for example BR or AW. Specification slash sheets indicate the characteristic applicable to a given style of capacitor.		

In specifying capacitance change with temperature for Class 2 materials, EIA expresses the capacitance change over an operating temperature range by a 3 symbol code. The first symbol represents the cold temperature end of the temperature range, the second represents the upper limit of the operating temperature range and the third symbol represents the capacitance change allowed over the operating temperature range. Table 1 provides a detailed explanation of the EIA system.

Effects of Voltage – Variations in voltage have little effect on Class 1 dielectric but does affect the capacitance and dissipation factor of Class 2 dielectrics. The application of DC voltage reduces both the capacitance and dissipation factor while the application of an AC voltage within a reasonable range tends to increase both capacitance and dissipation factor readings. If a high enough AC voltage is applied, eventually it will reduce capacitance just as a DC voltage will. Figure 2 shows the effects of AC voltage.

Cap. Change vs. A.C. Volts
X7R

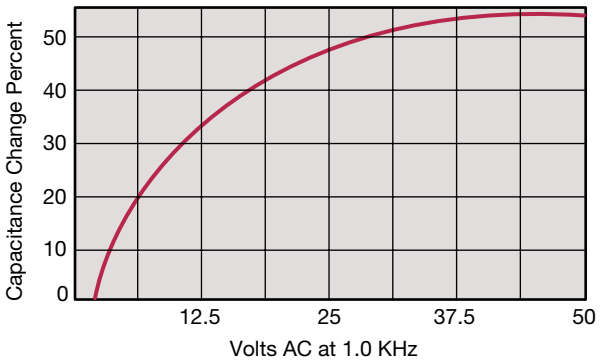


Figure 2

Capacitor specifications specify the AC voltage at which to measure (normally 0.5 or 1 VAC) and application of the wrong voltage can cause spurious readings. Figure 3 gives the voltage coefficient of dissipation factor for various AC voltages at 1 kilohertz. Applications of different frequencies will affect the percentage changes versus voltages.

D.F. vs. A.C. Measurement Volts
X7R

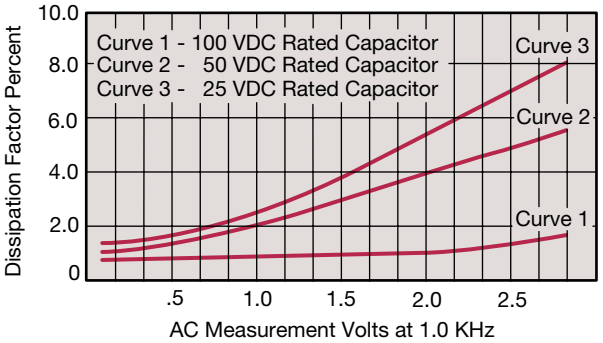


Figure 3

Typical effect of the application of DC voltage is shown in Figure 4. The voltage coefficient is more pronounced for higher K dielectrics. These figures are shown for room temperature conditions. The combination characteristic known as voltage temperature limits which shows the effects of rated voltage over the operating temperature range is shown in Figure 5 for the military BX characteristic.

Typical Cap. Change vs. D.C. Volts
X7R

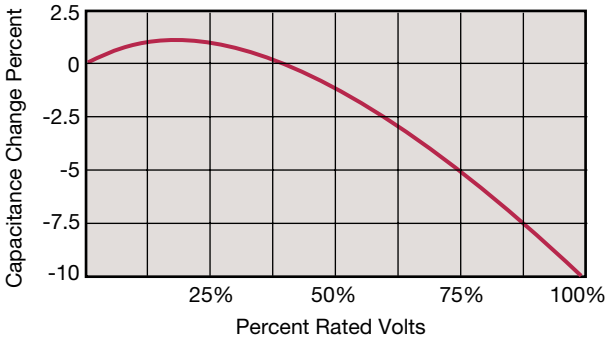


Figure 4

Typical Cap. Change vs. Temperature
X7R

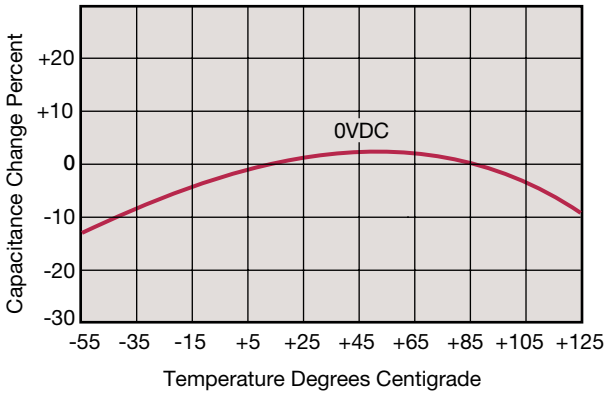
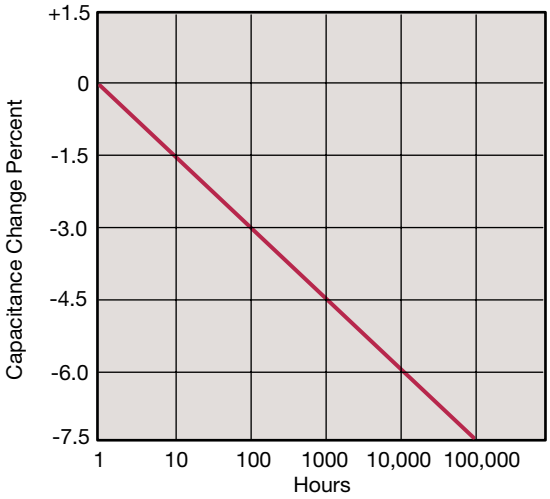


Figure 5

Effects of Time – Class 2 ceramic capacitors change capacitance and dissipation factor with time as well as temperature, voltage and frequency. This change with time is known as aging. Aging is caused by a gradual re-alignment of the crystalline structure of the ceramic and produces an exponential loss in capacitance and decrease in dissipation factor versus time. A typical curve of aging rate for semi-stable ceramics is shown in Figure 6.

If a Class 2 ceramic capacitor that has been sitting on the shelf for a period of time, is heated above its curie point, (125°C for 4 hours or 150°C for ½ hour will suffice) the part will de-age and return to its initial capacitance and dissipation factor readings. Because the capacitance changes rapidly, immediately after de-aging, the basic capacitance measurements are normally referred to a time period sometime after the de-aging process. Various manufacturers use different time bases but the most popular one is one day or twenty-four hours after "last heat." Change in the aging curve can be caused by the application of voltage and other stresses. The possible changes in capacitance due to de-aging by heating the unit explain why capacitance changes are allowed after test, such as temperature cycling, moisture resistance, etc., in MIL specs. The application of high voltages such as dielectric withstanding voltages also tends to de-age capacitors and is why re-reading of capacitance after 12 or 24 hours is allowed in military specifications after dielectric strength tests have been performed.

Typical Curve of Aging Rate
X7R



Characteristic	Max. Aging Rate %/Decade
C0G (NP0)	None
X7R, X5R	2
Y5V	7

Figure 6

Effects of Frequency – Frequency affects capacitance and impedance characteristics of capacitors. This effect is much more pronounced in high dielectric constant ceramic formulation that is low K formulations. AVX's SpiCap software generates impedance, ESR, series inductance, series resonant frequency and capacitance all as functions of frequency, temperature and DC bias for standard chip sizes and styles. It is available free from AVX and can be downloaded for free from AVX website: www.avxcorp.com.

Effects of Mechanical Stress – High "K" dielectric ceramic capacitors exhibit some low level piezoelectric reactions under mechanical stress. As a general statement, the piezoelectric output is higher, the higher the dielectric constant of the ceramic. It is desirable to investigate this effect before using high "K" dielectrics as coupling capacitors in extremely low level applications.

Reliability – Historically ceramic capacitors have been one of the most reliable types of capacitors in use today. The approximate formula for the reliability of a ceramic capacitor is:

$$\frac{L_o}{L_t} = \left(\frac{V_t}{V_o}\right)^X \left(\frac{T_t}{T_o}\right)^Y$$

where

L_o = operating life
L_t = test life
V_t = test voltage
V_o = operating voltage
T_t = test temperature and
T_o = operating temperature in °C
X,Y = see text

Historically for ceramic capacitors exponent X has been considered as 3. The exponent Y for temperature effects typically tends to run about 8.

A capacitor is a component which is capable of storing electrical energy. It consists of two conductive plates (electrodes) separated by insulating material which is called the dielectric. A typical formula for determining capacitance is:

$$C = \frac{.224\ KA}{t}$$

C = capacitance (picofarads)
K = dielectric constant (Vacuum = 1)
A = area in square inches
t = separation between the plates in inches (thickness of dielectric)
.224 = conversion constant (.0884 for metric system in cm)

Capacitance – The standard unit of capacitance is the farad. A capacitor has a capacitance of 1 farad when 1 coulomb charges it to 1 volt. One farad is a very large unit and most capacitors have values in the micro (10^{-6}), nano (10^{-9}) or pico (10^{-12}) farad level.

Dielectric Constant – In the formula for capacitance given above the dielectric constant of a vacuum is arbitrarily chosen as the number 1. Dielectric constants of other materials are then compared to the dielectric constant of a vacuum.

Dielectric Thickness – Capacitance is indirectly proportional to the separation between electrodes. Lower voltage requirements mean thinner dielectrics and greater capacitance per volume.

Area – Capacitance is directly proportional to the area of the electrodes. Since the other variables in the equation are usually set by the performance desired, area is the easiest parameter to modify to obtain a specific capacitance within a material group.

Energy Stored – The energy which can be stored in a capacitor is given by the formula:

$$E = \tfrac{1}{2}CV^2$$

E = energy in joules (watts-sec)
V = applied voltage
C = capacitance in farads

Potential Change – A capacitor is a reactive component which reacts against a change in potential across it. This is shown by the equation for the linear charge of a capacitor:

$$I_{ideal} = C\frac{dV}{dt}$$

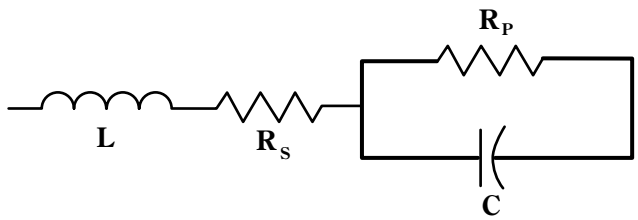
where

I = Current
C = Capacitance
dV/dt = Slope of voltage transition across capacitor

Thus an infinite current would be required to instantly change the potential across a capacitor. The amount of current a capacitor can "sink" is determined by the above equation.

Equivalent Circuit – A capacitor, as a practical device, exhibits not only capacitance but also resistance and inductance. A simplified schematic for the equivalent circuit is:

C = Capacitance
R_s = Series Resistance
L = Inductance
R_p = Parallel Resistance



Reactance – Since the insulation resistance (R_p) is normally very high, the total impedance of a capacitor is:

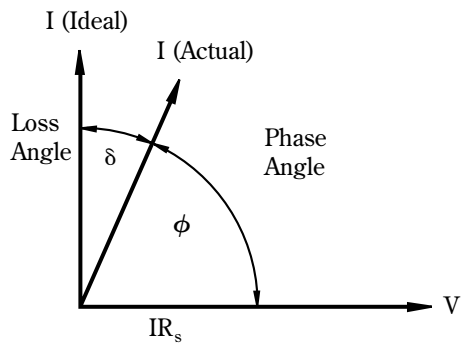
$$Z = \sqrt{R_S^2 + (X_C - X_L)^2}$$

where

Z = Total Impedance
R_s = Series Resistance
X_C = Capacitive Reactance $= \frac{1}{2\pi fC}$
X_L = Inductive Reactance $= 2\pi fL$

The variation of a capacitor's impedance with frequency determines its effectiveness in many applications.

Phase Angle – Power Factor and Dissipation Factor are often confused since they are both measures of the loss in a capacitor under AC application and are often almost identical in value. In a "perfect" capacitor the current in the capacitor will lead the voltage by 90°.

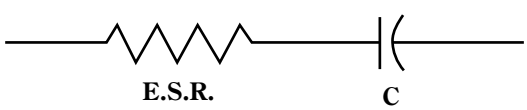


In practice the current leads the voltage by some other phase angle due to the series resistance R_S. The complement of this angle is called the loss angle and:

Power Factor (P.F.) = Cos ϕ or Sine δ
Dissipation Factor (D.F.) = tan δ

for small values of δ the tan and sine are essentially equal which has led to the common interchangeability of the two terms in the industry.

Equivalent Series Resistance – The term E.S.R. or Equivalent Series Resistance combines all losses both series and parallel in a capacitor at a given frequency so that the equivalent circuit is reduced to a simple R-C series connection.



Dissipation Factor – The DF/PF of a capacitor tells what percent of the apparent power input will turn to heat in the capacitor.

$$\textbf{Dissipation Factor} = \frac{\textbf{E.S.R.}}{\textbf{X}_c} = (2\,\pi\,\textbf{fC})\,(\textbf{E.S.R.})$$

The watts loss are:

$$\textbf{Watts loss} = (2\,\pi\,\textbf{fCV}^2)\,(\textbf{D.F.})$$

Very low values of dissipation factor are expressed as their reciprocal for convenience. These are called the "Q" or Quality factor of capacitors.

Parasitic Inductance – The parasitic inductance of capacitors is becoming more and more important in the decoupling of today's high speed digital systems. The relationship between the inductance and the ripple voltage induced on the DC voltage line can be seen from the simple inductance equation:

$$V = L\,\frac{di}{dt}$$

The $\frac{di}{dt}$ seen in current microprocessors can be as high as 0.3 A/ns, and up to 10A/ns. At 0.3 A/ns, 100pH of parasitic inductance can cause a voltage spike of 30mV. While this does not sound very drastic, with the Vcc for microprocessors decreasing at the current rate, this can be a fairly large percentage.

Another important, often overlooked, reason for knowing the parasitic inductance is the calculation of the resonant frequency. This can be important for high frequency, bypass capacitors, as the resonant point will give the most signal attenuation. The resonant frequency is calculated from the simple equation:

$$f_{res} = \frac{1}{2\pi\sqrt{LC}}$$

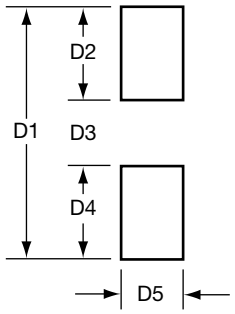
Insulation Resistance – Insulation Resistance is the resistance measured across the terminals of a capacitor and consists principally of the parallel resistance R_P shown in the equivalent circuit. As capacitance values and hence the area of dielectric increases, the I.R. decreases and hence the product (C x IR or RC) is often specified in ohm faradsor more commonly megohm-microfarads. Leakage current is determined by dividing the rated voltage by IR (Ohm's Law).

Dielectric Strength – Dielectric Strength is an expression of the ability of a material to withstand an electrical stress. Although dielectric strength is ordinarily expressed in volts, it is actually dependent on the thickness of the dielectric and thus is also more generically a function of volts/mil.

Dielectric Absorption – A capacitor does not discharge instantaneously upon application of a short circuit, but drains gradually after the capacitance proper has been discharged. It is common practice to measure the dielectric absorption by determining the "reappearing voltage" which appears across a capacitor at some point in time after it has been fully discharged under short circuit conditions.

Corona – Corona is the ionization of air or other vapors which causes them to conduct current. It is especially prevalent in high voltage units but can occur with low voltages as well where high voltage gradients occur. The energy discharged degrades the performance of the capacitor and can in time cause catastrophic failures.

REFLOW SOLDERING



Dimensions in millimeters (inches)

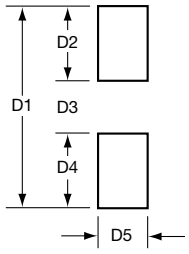
Case Size	D1	D2	D3	D4	D5
0402	1.70 (0.07)	0.60 (0.02)	0.50 (0.02)	0.60 (0.02)	0.50 (0.02)
0603	2.30 (0.09)	0.80 (0.03)	0.70 (0.03)	0.80 (0.03)	0.75 (0.03)
0805	3.00 (0.12)	1.00 (0.04)	1.00 (0.04)	1.00 (0.04)	1.25 (0.05)
1206	4.00 (0.16)	1.00 (0.04)	2.00 (0.09)	1.00 (0.04)	1.60 (0.06)
1210	4.00 (0.16)	1.00 (0.04)	2.00 (0.09)	1.00 (0.04)	2.50 (0.10)
1808	5.60 (0.22)	1.00 (0.04)	3.60 (0.14)	1.00 (0.04)	2.00 (0.08)
1812	5.60 (0.22)	1.00 (0.04))	3.60 (0.14)	1.00 (0.04)	3.00 (0.12)
1825	5.60 (0.22)	1.00 (0.04)	3.60 (0.14)	1.00 (0.04)	6.35 (0.25)
2220	6.60 (0.26)	1.00 (0.04)	4.60 (0.18)	1.00 (0.04)	5.00 (0.20)
2225	6.60 (0.26)	1.00 (0.04)	4.60 (0.18)	1.00 (0.04)	6.35 (0.25)

Component Pad Design

Component pads should be designed to achieve good solder filets and minimize component movement during reflow soldering. Pad designs are given below for the most common sizes of multilayer ceramic capacitors for both wave and reflow soldering. The basis of these designs is:

- Pad width equal to component width. It is permissible to decrease this to as low as 85% of component width but it is not advisable to go below this.
- Pad overlap 0.5mm beneath component.
- Pad extension 0.5mm beyond components for reflow and 1.0mm for wave soldering.

WAVE SOLDERING

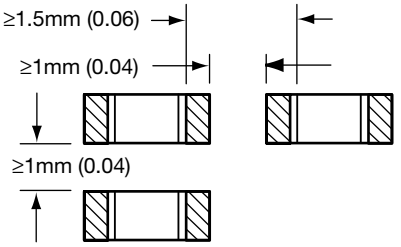


Case Size	D1	D2	D3	D4	D5
0603	3.10 (0.12)	1.20 (0.05)	0.70 (0.03)	1.20 (0.05)	0.75 (0.03)
0805	4.00 (0.15)	1.50 (0.06)	1.00 (0.04)	1.50 (0.06)	1.25 (0.05)
1206	5.00 (0.19)	1.50 (0.06)	2.00 (0.09)	1.50 (0.06)	1.60 (0.06)
1210	5.00 (0.19)	1.50 (0.06)	2.00 (0.09)	1.50 (0.06)	2.50 (0.10)

Dimensions in millimeters (inches)

Component Spacing

For wave soldering components, must be spaced sufficiently far apart to avoid bridging or shadowing (inability of solder to penetrate properly into small spaces). This is less important for reflow soldering but sufficient space must be allowed to enable rework should it be required.



Preheat & Soldering

The rate of preheat should not exceed 4°C/second to prevent thermal shock. A better maximum figure is about 2°C/second.

For capacitors size 1206 and below, with a maximum thickness of 1.25mm, it is generally permissible to allow a temperature differential from preheat to soldering of 150°C. In all other cases this differential should not exceed 100°C.

For further specific application or process advice, please consult AVX.

Cleaning

Care should be taken to ensure that the capacitors are thoroughly cleaned of flux residues especially the space beneath the capacitor. Such residues may otherwise become conductive and effectively offer a low resistance bypass to the capacitor.

Ultrasonic cleaning is permissible, the recommended conditions being 8 Watts/litre at 20-45 kHz, with a process cycle of 2 minutes vapor rinse, 2 minutes immersion in the ultrasonic solvent bath and finally 2 minutes vapor rinse.

APPLICATION NOTES

Storage
Good solderability is maintained for at least twelve months, provided the components are stored in their "as received" packaging at less than 40°C and 70% RH.

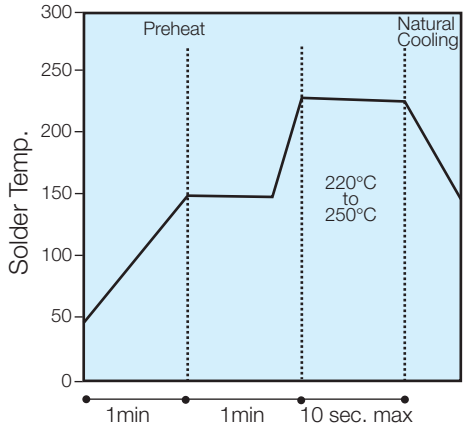
Solderability
Terminations to be well soldered after immersion in a 60/40 tin/lead solder bath at 235 ± 5°C for 2 ± 1 seconds.

Leaching
Terminations will resist leaching for at least the immersion times and conditions shown below.

Termination Type	Solder Tin/Lead/Silver	Solder Temp. °C	Immersion Time Seconds
Nickel Barrier	60/40/0	260 ± 5	30 ± 1

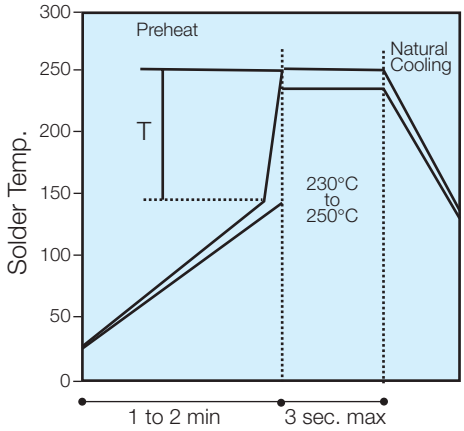
Recommended Soldering Profiles

Reflow



(Minimize soldering time)

Wave



(Preheat chips before soldering)
T/maximum 150°C

General
Surface mounting chip multilayer ceramic capacitors are designed for soldering to printed circuit boards or other substrates. The construction of the components is such that they will withstand the time/temperature profiles used in both wave and reflow soldering methods.

Handling
Chip multilayer ceramic capacitors should be handled with care to avoid damage or contamination from perspiration and skin oils. The use of tweezers or vacuum pick ups is strongly recommended for individual components. Bulk handling should ensure that abrasion and mechanical shock are minimized. Taped and reeled components provides the ideal medium for direct presentation to the placement machine. Any mechanical shock should be minimized during handling chip multilayer ceramic capacitors.

Preheat
It is important to avoid the possibility of thermal shock during soldering and carefully controlled preheat is therefore required. The rate of preheat should not exceed 4°C/second and a target figure 2°C/second is recommended. Although an 80°C to 120°C temperature differential is preferred, recent developments allow a temperature differential between the component surface and the soldering temperature of 150°C (Maximum) for capacitors of 1210 size and below with a maximum thickness of 1.25mm. The user is cautioned that the risk of thermal shock increases as chip size or temperature differential increases.

Soldering
Mildly activated rosin fluxes are preferred. The minimum amount of solder to give a good joint should be used. Excessive solder can lead to damage from the stresses caused by the difference in coefficients of expansion between solder, chip and substrate. AVX terminations are suitable for all wave and reflow soldering systems. If hand soldering cannot be avoided, the preferred technique is the utilization of hot air soldering tools.

Cooling
Natural cooling in air is preferred, as this minimizes stresses within the soldered joint. When forced air cooling is used, cooling rate should not exceed 4°C/second. Quenching is not recommended but if used, maximum temperature differentials should be observed according to the preheat conditions above.

Cleaning
Flux residues may be hygroscopic or acidic and must be removed. AVX MLC capacitors are acceptable for use with all of the solvents described in the specifications MIL-STD-202 and EIA-RS-198. Alcohol based solvents are acceptable and properly controlled water cleaning systems are also acceptable. Many other solvents have been proven successful, and most solvents that are acceptable to other components on circuit assemblies are equally acceptable for use with ceramic capacitors.

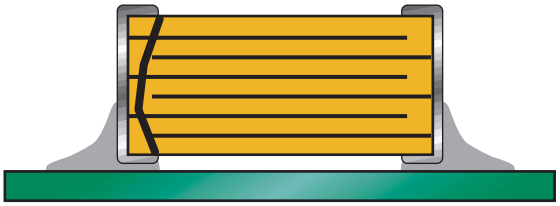
POST SOLDER HANDLING

Once SMP components are soldered to the board, any bending or flexure of the PCB applies stresses to the soldered joints of the components. For leaded devices, the stresses are absorbed by the compliancy of the metal leads and generally don't result in problems unless the stress is large enough to fracture the soldered connection.

Ceramic capacitors are more susceptible to such stress because they don't have compliant leads and are brittle in nature. The most frequent failure mode is low DC resistance or short circuit. The second failure mode is significant loss of capacitance due to severing of contact between sets of the internal electrodes.

Cracks caused by mechanical flexure are very easily identified and generally take one of the following two general forms:

Type A:
Angled crack between bottom of device to top of solder joint.



Type B:
Fracture from top of device to bottom of device.

Mechanical cracks are often hidden underneath the termination and are difficult to see externally. However, if one end termination falls off during the removal process from PCB, this is one indication that the cause of failure was excessive mechanical stress due to board warping.

COMMON CAUSES OF MECHANICAL CRACKING

The most common source for mechanical stress is board depanelization equipment, such as manual breakapart, v-cutters and shear presses. Improperly aligned or dull cutters may cause torqueing of the PCB resulting in flex stresses being transmitted to components near the board edge. Another common source of flexural stress is contact during parametric testing when test points are probed. If the PCB is allowed to flex during the test cycle, nearby ceramic capacitors may be broken.

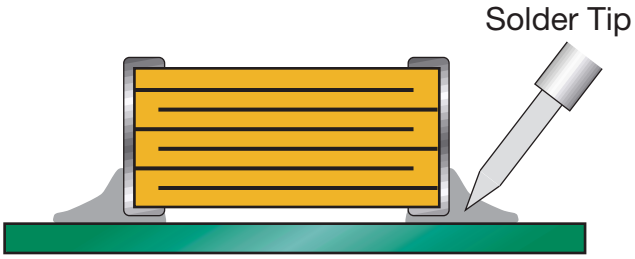
A third common source is board to board connections at vertical connectors where cables or other PCBs are connected to the PCB. If the board is not supported during the plug/unplug cycle, it may flex and cause damage to nearby components.

Special care should also be taken when handling large (>6" on a side) PCBs since they more easily flex or warp than smaller boards.

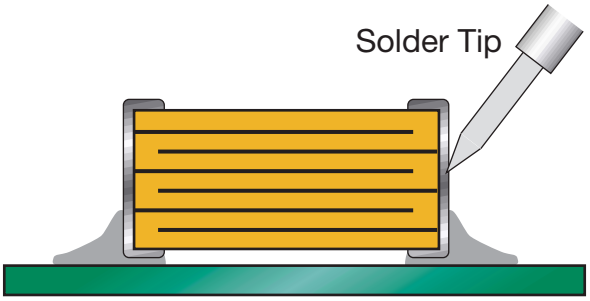
REWORKING OF MLCs

Thermal shock is common in MLCs that are manually attached or reworked with a soldering iron. *AVX strongly recommends that any reworking of MLCs be done with hot air reflow rather than soldering irons.* It is practically impossible to cause any thermal shock in ceramic capacitors when using hot air reflow.

However direct contact by the soldering iron tip often causes thermal cracks that may fail at a later date. If rework by soldering iron is absolutely necessary, it is recommended that the wattage of the iron be less than 30 watts and the tip temperature be <300ºC. *Rework should be performed by applying the solder iron tip to the pad and not directly contacting any part of the ceramic capacitor.*



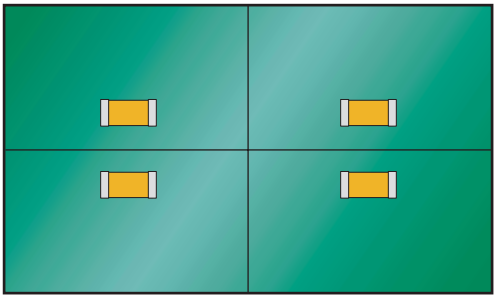
Preferred Method - No Direct Part Contact



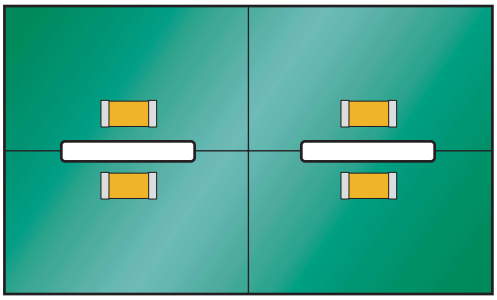
Poor Method - Direct Contact with Part

PCB BOARD DESIGN

To avoid many of the handling problems, AVX recommends that MLCs be located at least .2" away from nearest edge of board. However when this is not possible, AVX recommends that the panel be routed along the cut line, adjacent to where the MLC is located.



No Stress Relief for MLCs



Routed Cut Line Relieves Stress on MLC