USER'S MANUAL

NEC

μPD72103A

HDLC CONTROLLER

μPD72103A

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NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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- Standard: Computers, office equipment, communications equipment, test and measurement equipment, audio and visual equipment, home electronic appliances, machine tools, personal electronic equipment and industrial robots
- Special: Transportation equipment (automobiles, trains, ships, etc.), traffic control systems, anti-disaster systems, anti-crime systems, safety equipment and medical equipment (not specifically designed for life support)
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PREFACE

Target users

This manual describes the functions of the μPD72103A to engineers who will use the μPD72103A when designing application systems.

Objective

The objective of this manual is to describe the hardware functions of the μPD72103A, which includes the following components.

Composition

This manual can be broadly divided into the following sections.

- General
- Bus interface
- Communication operations
- Commands
- Status
- System configuration example
- Example of μPD72103A's operation sequence
- Connecting HDLC controller to a Motorola system
- Questions and answers about the μPD72103A
- Command list
- Status list

Use

This manual assumes that the reader has a general knowledge of electricity, logic circuits, and microcontrollers.

- Users who would like to check commands
  → Read "**CHAPTER 4 COMMAND LIST**".
- Users who would like to learn about the μPD72103A's functions
  → Read this manual in the order shown in the Table of Contents.
- Users who have questions about the μPD72103A's operations
  → Read "**APPENDIX C Q&A**".

Legend

Data representation weight	:	High-order digits are indicated at left and low-order digits at right.
Active low representation	:	$\overline{xxx}$ (pin or signal name is overlined) or xxxB (“B” is added after signal and pin names)
Memory map address	:	High order at low stage and low order at high stage (address 0H)
Note	:	Explanation of Note in the text
Caution	:	Item deserving extra attention
Remark	:	Supplementary explanation to the text
Number representation	:	Decimal number is xxxx Hexadecimal number is xxxxH

Appendix C uses the following abbreviations for reference documentation.

Data sheet	→ DS
User’s manual	→ UM
Application note	→ AN

Related Documentation

Document name	Data Sheet	User’s Manual	Application Note
μPD72103A	S10189J[Note]	This manual	—

The corresponding application note for this manual is the μPD72103 APPLICATION NOTE (IEA-713[Note]). In this application note, all references to the μPD72103 should be understood as referring to the μPD72103A.

Note This document number is that of the Japanese version.

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CHAPTER 1 GENERAL

The μPD72103A HDLCC (High-level Data Link Control procedure Controller) is a communication control LSI that supports the HDLC standard.

Because this HDLCC includes a DMA (Direct Memory Access) function, the host machine can use commands and data previously stored in memory to perform serial communication using HDLC frames.

1.1 Features

- HDLC frame control
- Address field recognition function: 1 byte/2 bytes
- Full-duplex communication via one channel
- Baud rate: 8 Mbps max. (2 Mbps max. when using DPLL)[Note]
- Maximum transmit/receive data length: 16 Kbytes
- Can be divided in external memory as level-two header and 1 field or level-two, level-three header and user
- Various statistical data
- DPLL (Digital Phase-Locked Loop) function
- On-chip DMA controller: 8/16-bit data, 24-bit address
- General-purpose input/output pins: Input pin x 2
  Output pin x 2
- On-chip transmission control function (LAP-D mode)
- Data format: NRZ and NRZI decoding/encoding
- Command chain function
- FCS (Frame Check Sequence) generation/detection: 16/32 bits
- System clock: 1 to 16 MHz
- CMOS
- 5-V single power supply

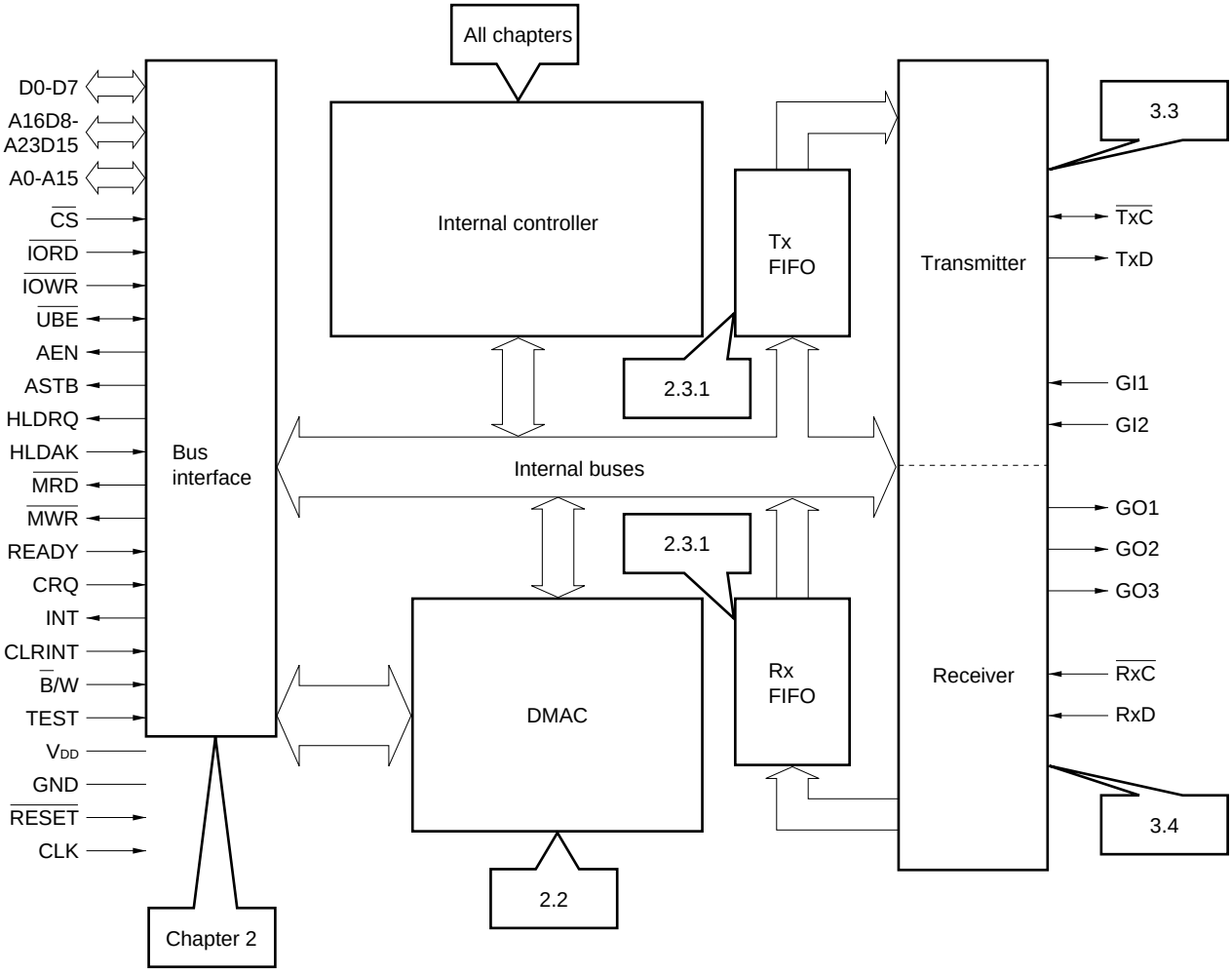
Note Transfer speed is restricted by the system clock's frequency and operation conditions. For details, see the caution points described in "**3.4.8 Cautions regarding overrun errors**".

ORDERING INFORMATION

Part No.	Package
μPD72103AGC-3B9	80-pin plastic QFP (14 x 14 mm)
μPD72103ALP	68-pin plastic QFJ (950 x 950 mil)

1.2 Block Diagram

Corresponding sections of this manual are indicated in the bubbles.



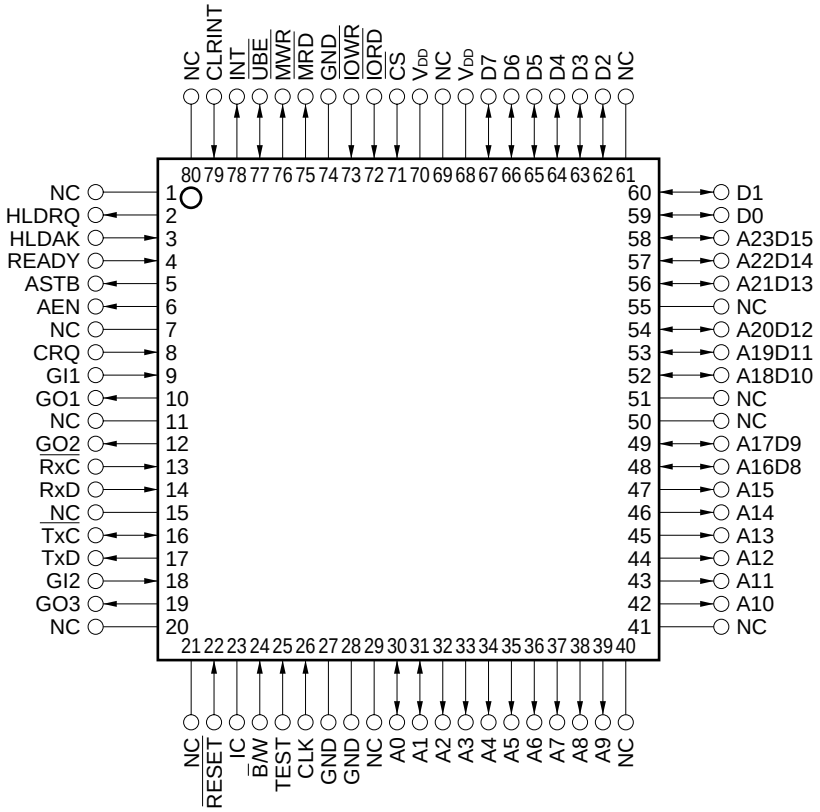
1.3 Internal Block Functions

Name	Function
Bus interface	Interface between the μPD72103A and external memory or external host processor
Internal controller	HDLC framing including the DMAC, transmitter, and receiver block control
DMAC (Direct Memory Access Controller)	Controls transfer of data in external memory to the internal controller or transmitter, or controls writing of data to external memory from the internal controller or receiver
Tx FIFO	A 32-byte buffer for transmitting transmit data from the DMAC to the transmitter
Rx FIFO	A 128-byte buffer for transmitting receive data from the receiver to the DMAC
Transmitter	Converts contents of TX FIFO to HDLC frames that are sent as serial data
Receiver	Writes data received in HDLC frames to RX FIFO
Internal buses	These buses, which include a 24-bit address bus and 8/16-bit data buses, connect the internal controller, DMAC, FIFOs, serial block, and bus interface block

1.4 Pin Configuration (Top View)

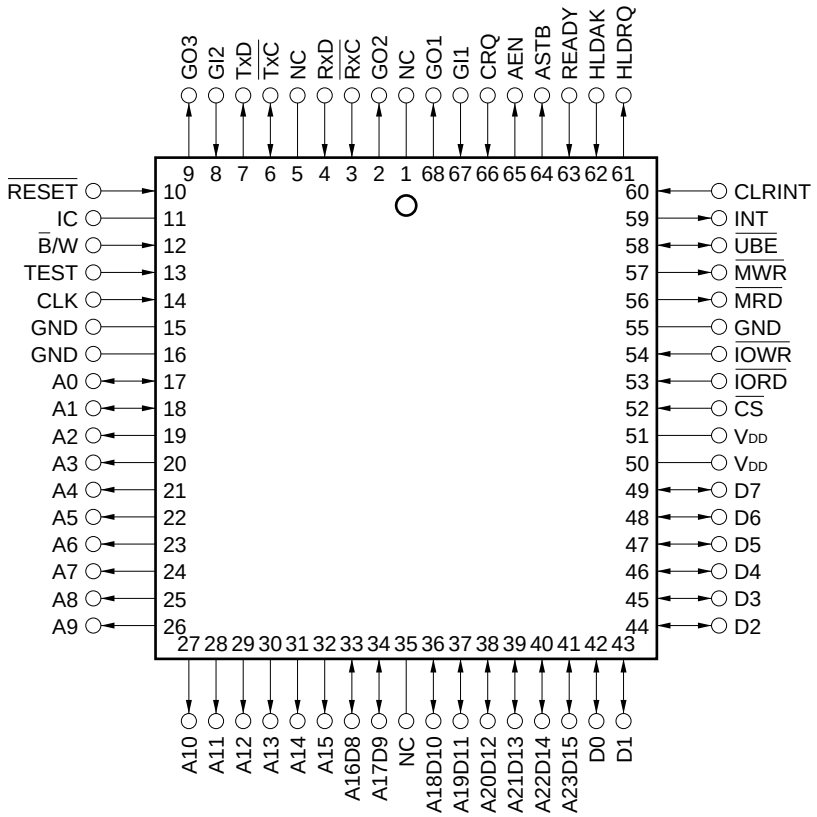
80-pin plastic QFP (14 x 14 mm)

μPD72103AGC-3B9



68-pin plastic QFJ (950 x 950 mil)

μPD72103ALP



1.5 Pin Functions

Pin No.		Pin name	I/O	Active level	Function
80-pin QFP	68-pin QFJ				
12	2	GO2	O	–	This is a general-purpose output pin. The output level of this pin is changed when "general-purpose output pin write LCW" is executed.
13	3	$\overline{\text{RxC}}$ (Receive Clock)	I	–	When in on-chip DPLL mode: This is the transmit/receive clock input for the μPD72103A's on-chip DPLL. (Enables input up to 32 MHz)
					When in external DPLL mode: This is a receive clock input pin.
14	4	RxD (Receive Data)	I	–	This is a serial receive data input pin.
15	5	NC (No Connection)	–	–	Leave this pin unconnected.
16	6	$\overline{\text{TxC}}$ (Transmit Clock)	I/O	–	When in on-chip DPLL mode: The $\overline{\text{RxC}}$ pin's input signal that was generated in the μPD72103A is divided by 16 and output via this pin as a clock signal.
					When in external DPLL mode: A transmit clock is input via this pin from an external source.
17	7	TxD (Transmit Data)	O	–	This is the serial transmit data output pin.
18	8	GI2	I	L	When not in LAP-D mode: This is a general-purpose input pin. "General-purpose input pin status change detection 1 LSW" is reported when a change in the input level is detected.
					When in LAP-D mode: This pin is used for externally applied frame transmit enable signals.
19	9	GO3	O	L	When not in LAP-D mode: This pin has no function. Leave this pin unconnected.
					When in LAP-D mode: This pin is used for externally output frame transmit request signals.
20	–	NC (No Connection)	–	–	Leave this pin unconnected.
21	–	NC (No Connection)	–	–	Leave this pin unconnected.
22	10	$\overline{\text{RESET}}$ (Reset)	I	L	This pin is used to initialize (reset) the μPD72103A's internal circuits. This requires at least seven clock cycles of the CLK signal. Bus slave mode is entered after reset.
–	–	NC (No Connection)	–	–	Leave this pin unconnected.
23	11	IC (Internally Connected)	–	–	Do not connect anything to this pin.

Pin No.		Pin name	I/O	Active level	Function	
80-pin QFP	68-pin QFJ					
24	12	$\overline{B}$/W (Byte/Word)	I	L/H	During bus master mode, this indicates the data bus used to access external memory. When $\overline{B}$/W = 0: byte unit (8 bits) When $\overline{B}$/W = 1: word unit (16 bits) The status of the $\overline{B}$/W pin should be fixed after power-on. When accessing in word units, the low-order bits in the data bus are the data contents of even-number addresses.	
25	13	TEST (Text)	I	–	When using this pin, it should be pulled up to high level.	
26	14	CLK (Clock)	I	–	System clock input Input a 1-MHz to 16-MHz clock to this pin. **Note**	
27	15	GND	–	–	Ground pins Make sure that there are several ground pins.	
28	16	GND	–	–	Ground pins Make sure that there are several ground pins.	
29	–	NC (No Connection)	–	–	Leave this pin unconnected.	
30 and 31	17 and 18	A0 and A1	I/O *	–	Bi-directional 3-state address line	During bus master mode: (output) Indicates the low-order two bits of the memory access address.
						During bus slave mode: (input) These pins are used to input addresses during I/O access to the μPD72103A by an external host.
32 to 39	19 to 26	A2 to A9	O *	–	During bus master mode: Outputs memory addresses from 2 bits to 15 bits.	
					During bus slave mode: Changes to high impedance.	
40	–	NC (No Connection)	–	–	Leave this pin unconnected.	
41	–	NC (No Connection)	–	–	Leave this pin unconnected.	
42 to 47	27 to 32	A10 to A15	O *	–	See “A2 to A9” above.	
48 and 49	33 and 34	A16D8 and A17D9	I/O *	–	These pins are for the bi-directional 3-state/data bus. They are multiplex pins for high-order 8 bits starting from bits 16 to 23 of an address and for high-order 8 bits starting from bits 8 to 15 of the data.	
50	35	NC (No Connection)	–	–	Leave this pin unconnected.	
51	–	NC (No Connection)	–	–	Leave this pin unconnected.	
52 to 54	36 to 38	A18D10 to A20D12	I/O *	–	See “A16D8 and A17D9” above.	

Note See the caution points described in “**3.4.8 Cautions regarding overrun errors**”.

Remark “*” indicates 3-state.

Pin No.		Pin name	I/O	Active level	Function	
80-pin QFP	68-pin QFJ					
55	–	NC (No Connection)	–	–	Leave this pin unconnected.	
56 to 58	39 to 41	A21D13 to A23D15	I/O *	–	See “A16D8 and A17D9” above.	
59 and 60	42 and 43	D0 and D1	I/O *	–	Bi-directional 3-state address line	During bus master mode: This pin is an output pin during write to external memory and is an input pin during read from external memory.
						During bus slave mode: This pin is normally set to high impedance. It is used to output internal register data when an external host processor executes I/O read from the μPD72103A.
61	–	NC (No Connection)	–	–	Leave this pin unconnected.	
62 to 67	44 to 49	D2 to D7	I/O *	–	See D0 and D1	
68	50	V_{DD}	–	–	+5-V power supply pin	
69	–	NC (No Connection)	–	–	Leave this pin unconnected.	
70	51	V_{DD}	–	–	+5-V power supply pin	
71	52	$\overline{CS}$ (Chip Select)	I	L	During bus master mode: Disable this pin.	
					During bus slave mode: Read/write operation from host processor is enabled when this pin is low.	
72	53	$\overline{IORD}$ (I/O Read)	I	L	An external host processor uses this pin to read the contents of the μPD72103A’s internal registers. During bus master mode: Disable this pin (by inputting a high-level signal).	
73	54	$\overline{IOWR}$ (I/O Write)	I	L	An external host processor uses this pin to write data to the μPD72103A’s internal registers. During bus master mode: Disable this pin (by inputting a high-level signal).	
74	55	GND	–	–	Ground pins Make sure that there are several ground pins.	
75	56	$\overline{MRD}$ (Memory Read)	O *	L	During bus master mode: Data is read from external memory when this pin is low.	
					During bus slave mode: This pin goes to high impedance.	
76	57	$\overline{MWR}$ (Memory Write)	O *	L	During bus master mode: Data is written to external memory when this pin is low.	
					During bus slave mode: This pin goes to high impedance.	

Remark “*” indicates 3-state.

<table>
<tr><th colspan="2">Pin No.</th><th rowspan="2">Pin name</th><th rowspan="2">I/O</th><th rowspan="2">Active level</th><th rowspan="2">Function</th></tr>
<tr><th>80-pin QFP</th><th>68-pin QFJ</th></tr>
<tr><td>77</td><td>58</td><td>$\overline{UBE}$
(Upper Byte Enable)</td><td>I/O
*</td><td>L/H</td><td>During bus master mode:
The signal that is output from this pin varies depending on the input value of the $\overline{B}$/W pin.
• Byte transfer mode ($\overline{B}$/W = 0)
$\overline{UBE}$ is always high impedance.
• Word transfer mode ($\overline{B}$/W = 1)
Indicates whether valid data is present at pins D0 to D7 and/or pins A16D8 to A23D15.
<table><tr><th>$\overline{UBE}$</th><th>A0</th><th>D0-D7</th><th>A16D8-A23D15</th></tr><tr><td>0</td><td>0</td><td>√</td><td>√</td></tr><tr><td>0</td><td>1</td><td>—</td><td>√</td></tr><tr><td>1</td><td>0</td><td>√</td><td>—</td></tr><tr><td>1</td><td>1</td><td>—</td><td>—</td></tr></table>During bus slave mode:
The $\overline{UBE}$ pin is used for input and indicates whether valid data is present at pins D0 to D7 and/or pins A16D8 to A23D15.
<table><tr><th>$\overline{UBE}$</th><th>A0</th><th>D0-D7</th><th>A16D8-A23D15</th></tr><tr><td>0</td><td>0</td><td>√</td><td>—</td></tr><tr><td>0</td><td>1</td><td>—</td><td>√</td></tr><tr><td>1</td><td>0</td><td>√</td><td>—</td></tr><tr><td>1</td><td>1</td><td>√</td><td>—</td></tr></table></td></tr>
<tr><td>78</td><td>59</td><td>INT
(Interrupt)</td><td>O</td><td>H</td><td>Interrupt signal from the μPD72103A to an external host processor.</td></tr>
<tr><td>79</td><td>60</td><td>CLRINT
(Clear Interrupt)</td><td>I</td><td>H</td><td>This pin's signal sets as inactive the INT signal that is output by the μPD72103A.
In the μPD72103A, the INT signal goes low at this signal's rising edge.</td></tr>
<tr><td>80</td><td>–</td><td>NC
(No Connection)</td><td>–</td><td>–</td><td>Leave this pin unconnected.</td></tr>
<tr><td>1</td><td>–</td><td>NC
(No Connection)</td><td>–</td><td>–</td><td>Leave this pin unconnected.</td></tr>
<tr><td>2</td><td>61</td><td>HLDRQ
(Hold Request)</td><td>O</td><td>H</td><td>This pin is for the hold request signal, which is issued to an external host processor.
During a DMA operation in the μPD72103A, this signal is active in order to switch from bus slave mode to bus master mode.</td></tr>
<tr><td>3</td><td>62</td><td>HLDAK
(Hold Acknowledge)</td><td>I</td><td>H</td><td>This pin is for the hold acknowledge signal, which is received from an external host processor.
When the μPD72103A detects that this signal is active, it begins the DMA operation after switching from bus slave mode to bus master mode.</td></tr>
</table>

Remark "*" indicates 3-state.

Pin No.		Pin name	I/O	Active level	Function
80-pin QFP	68-pin QFJ				
4	63	READY (Ready)	I	H	This is an input pin for the signal that is used to extend the width of the $\overline{MRD}$ and $\overline{MWR}$ signals. When the READY signal is low, the $\overline{MRD}$ and $\overline{MWR}$ signals are held at active low level. Change the READY signal to conform to the rated setup/hold time.
5	64	ASTB (Address Strobe)	O	H	This pin is used to externally latch addresses output by the μPD72103A.
6	65	AEN (Address Enable)	O	H	During bus master mode, this pin's signal enables latched high-order addresses, which are output via the system address bus. This signal is also used to inhibit other system bus drivers.
7	–	NC (No Connection)	–	–	Leave this pin unconnected.
8	66	CRQ (Command Request)	I	H	This pin's signal is used to request command execution from an external host processor to the μPD72103A. The μPD72103A fetches the command from external memory at the rising edge of this signal.
9	67	GI1	I	L	This is a general-purpose input pin. The "general-purpose input pin change detection 1 LSW" is reported when a change in the input level is detected.
10	68	GO1	O	L	This is a general-purpose output pin. The output level of this pin is changed when the "general-purpose output pin write LCW" command is executed.
11	1	NC (No Connection)	–	–	Leave this pin unconnected.

1.6 Initialization via Reset

The μPD72103A is initialized when a negative potential pulse that is longer than the pulse input to the CLK pin (which is seven clocks in length as set by system clock conversion) is input to the $\overline{\text{RESET}}$ pin, or when a “1” is written to the CRST bit in the control register.

Table 1-1 lists the status of output pins and input/output pins when the μPD72103A is reset.

Since the $\overline{\text{RESET}}$ signal is latched by the CLK signal, four clocks of the CLK signal are required before the reset status becomes as shown in Table 1-1.

Table 1-1. Pin Status after Reset

Pin No.		Pin name	I/O	During reset
80-pin QFP	68-pin QFJ			(same status after reset)
12	2	GO2	O	H
16	6	$\overline{\text{TxC}}$	I/O	Hi-Z
17	7	TxD	O	H
19	9	GO3	O	H
30, 31	17, 18	A0, A1	I/O 3-state	Hi-Z
32-39, 42-47	19-26, 27-32	A2-A15	O 3-state	Hi-Z
48, 49, 52-54, 56-58	33, 34, 36-41	A16D8-A23D15	I/O 3-state	Hi-Z
59, 60, 62-67	42-49	D0-D7	I/O 3-state	Hi-Z
75	56	$\overline{\text{MRD}}$	O 3-state	Hi-Z
76	57	$\overline{\text{MWR}}$	O 3-state	Hi-Z
77	58	$\overline{\text{UBE}}$	I/O 3-state	Hi-Z
78	59	INT	O	L
2	61	HLDRQ	O	L
5	64	ASTB	O	L
6	65	AEN	O	L
10	68	GO1	O	H

[MEMO]

CHAPTER 2 BUS INTERFACE

2.1 Internal Registers

The μPD72103A includes four internal registers. These registers are controlled via six pins: $\overline{\text{IORD}}$, $\overline{\text{IOWR}}$, A0, A1, $\overline{\text{UBE}}$, and $\overline{\text{CS}}$. The host processor can only have I/O access to the μPD72103A when the μPD72103A is in bus slave mode.

Table 2-1 shows an I/O port map (for details of the $\overline{\text{UBE}}$ pin, see $\overline{\text{UBE}}$ column in "**1.5 Pin Functions**").

Table 2-1. I/O Port Map

CS	$\overline{\text{IORD}}$	$\overline{\text{IOWR}}$	A1	A0	Internal register	Function
1	X	X	X	X	–	No function
0	1	0	0	0	Control register	Write
0	0	1	0	0	Internal status register	Read
0	1	0	0	1	Internal FIFO active register	When "5" is written to this register, the MSET command is written to the internal FIFO.[Note]
0	1	0	1	0	–	Setting inhibited (internal test mode)
0	1	0	1	1	Internal FIFO register	The MSET command is written to the internal FIFO.
0	0	1	1	1	–	Setting inhibited

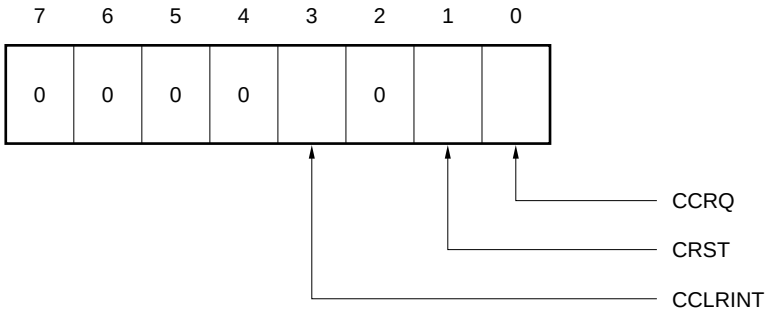
Note See "**CHAPTER 4 COMMANDS (LCW)**"

Remark X: Don't care

2.1.1 Control register

The control register is used when the host processor accesses the μPD72103A.

Figure 2-1. Control Register



Caution Be sure to write "0" to bits 2, 4, 5, 6, and 7.

Table 2-2. Control Register

Bit name	Meaning	Function
CCRQ	Control Command Request	A command is executed when "1" is written to this bit. The command execution method for this operation is the same as for the CRQ pin. Either method can be selected by host processor. Since this bit is automatically cleared to zero internally, there is no need to write a "0" after the host processor has written a "1" to this bit.
CRST	Control Reset	The μPD72103A's internal circuits are automatically reset when a "1" is written to this bit. This reset operation is the same as that controlled via the $\overline{\text{RESET}}$ pin. Since this bit is automatically cleared to zero internally, there is no need to write a "0" after the host processor has written a "1" to this bit.
CCLRINT	Control Clear INT	The INT pin is automatically reset when a "1" is written to this bit. This function is the same as when the INT pin is reset by the CLRINT pin. It does not matter which pin is selected by the host processor. Since this bit is automatically cleared to zero internally, there is no need to write a "0" after the host processor has written a "1" to this bit.

2.1.2 Internal status register

The internal status register is used to indicate the internal status of the μPD72103A. Its value immediately after reset is 0CH.

Figure 2-2. Internal Status Register

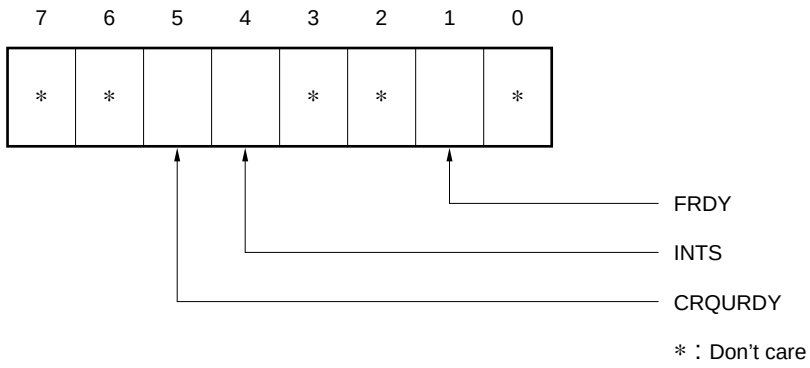


Table 2-3. Internal Status Register

Bit name	Meaning	Function
FRDY	FIFO Ready	This bit is accessed when the "memory area setting LCW[Note]" command is written to the internal FIFO. Write is enabled when this bit's value is "0". If this bit's value is "1", wait until it becomes "0" before writing to the FIFO. The value of this bit after reset is "0".
INTS	INT Status	This is the same signal as for the INT pin. The host processor can be informed of the status report timing from the μPD72103A not only by interrupts via the INT pin but also by polling this bit. The value of this bit after reset is "0".
CRQURDY	Command Request Unready	After the "memory area setting LCW" command is issued, this bit value becomes zero and a 10-ms wait period (when system clock = 8 MHz) is required before the next command can be issued. The value of this bit after reset is "0".

Note LCW: Link Command Word

2.2 DMAC (Direct Memory Access Controller)

During bus master mode, the μPD72103A uses the on-chip DMAC to read certain commands or transmit data that is stored in external memory or to write internal status contents or receive data to external memory.

Addresses used for DMA are 24 bits long, and the data length is selectable via the $\overline{B}$/W pin to support either 8-bit or 16-bit memory.

2.2.1 Block transfers

The μPD72103A uses DMA transfers to transfer long data segments. In the μPD72103A, DMA sets the HLDRQ signal as active (high) after each block is transferred.

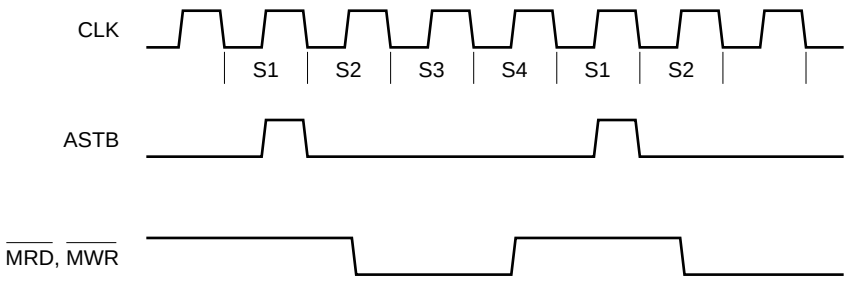
DMA transfers can be executed in either 4-byte or 8-byte blocks as set by DMAB[Note], and one bus cycle (four clocks) transfers either one byte (8 bits: byte unit) or two bytes (16 bits: word unit) of data. Accordingly, the number of bus cycles is determined by the transfer mode and the number of bytes to be transferred in data blocks, as listed in Table 2-4.

Note DMAB is a parameter of the “operation mode setting LCW” command.

Table 2-4. Bus Cycles in Byte Transfer Mode and Word Transfer Mode

Bytes per block	Byte transfer mode	Word transfer mode
4 bytes/block (DMAB = 0)	4 bus cycles	2 bus cycles (when starting from even address)
		3 bus cycles (when starting from odd address)
8 bytes/block (DMAB = 1)	8 bus cycles	4 bus cycles (when starting from even address)
		5 bus cycles (when starting from odd address)

Figure 2-3. Basic Clocks in One Bus Cycle during Block Transfer



2.2.2 Extension of active (low-level) width of $\overline{\text{MRD}}$ and $\overline{\text{MWR}}$ signals

The basic number of clocks per bus cycle in the μPD72103A's DMA is four clocks. During DMA transfer, the active (low-level) width of the $\overline{\text{MRD}}$ and $\overline{\text{MWR}}$ signals is two clocks. Either of the following methods can be used when there is not enough memory for a two-clock width.

(1) Programmable wait function

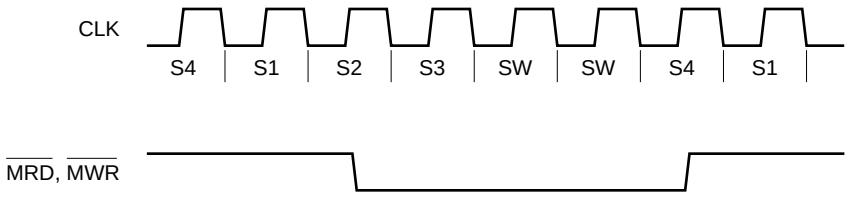
This function causes the μPD72103A to internally and automatically insert wait cycles to extend the active (low-level) width of $\overline{\text{MRD}}$ and $\overline{\text{MWR}}$. The programmable wait value can also be set via a parameter (DMAW) in the "operation mode setting LCW" command.

Figure 2-4 shows an example in which the programmable wait value is "2".

(2) Control via READY signal

This method sets the externally applied READY signal to low level to extend the active (low-level) width of $\overline{\text{MRD}}$ and $\overline{\text{MWR}}$. This method is valid when the value set to DMAW is exceeded.

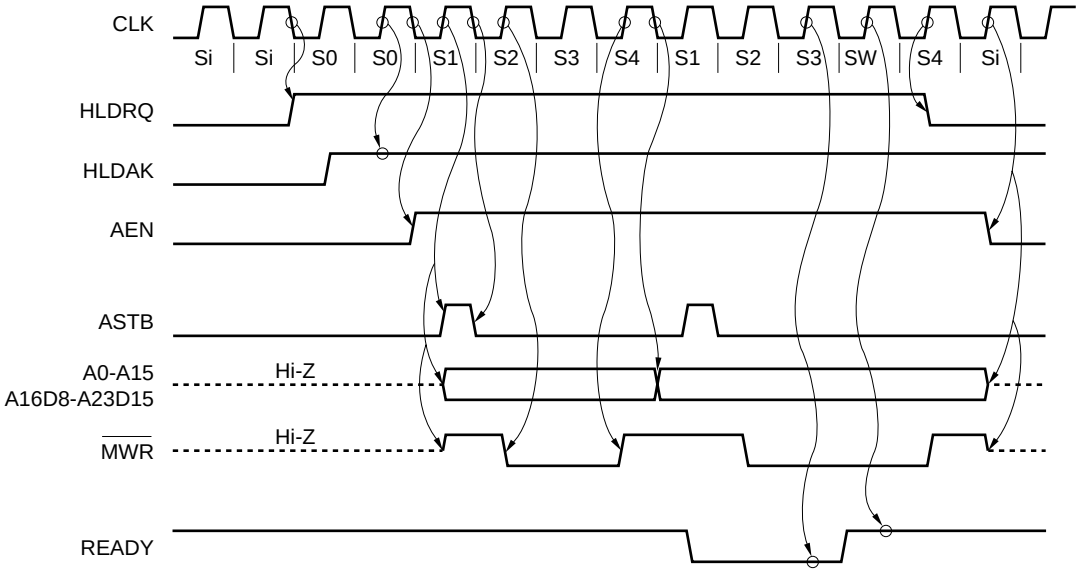
Figure 2-4. Example: Two Programmable Waits



2.2.3 Basic timing of DMA

Figure 2-5. Memory Write Timing

(a) $\overline{B}/W = 0$



(b) $\overline{B}/W = 1$

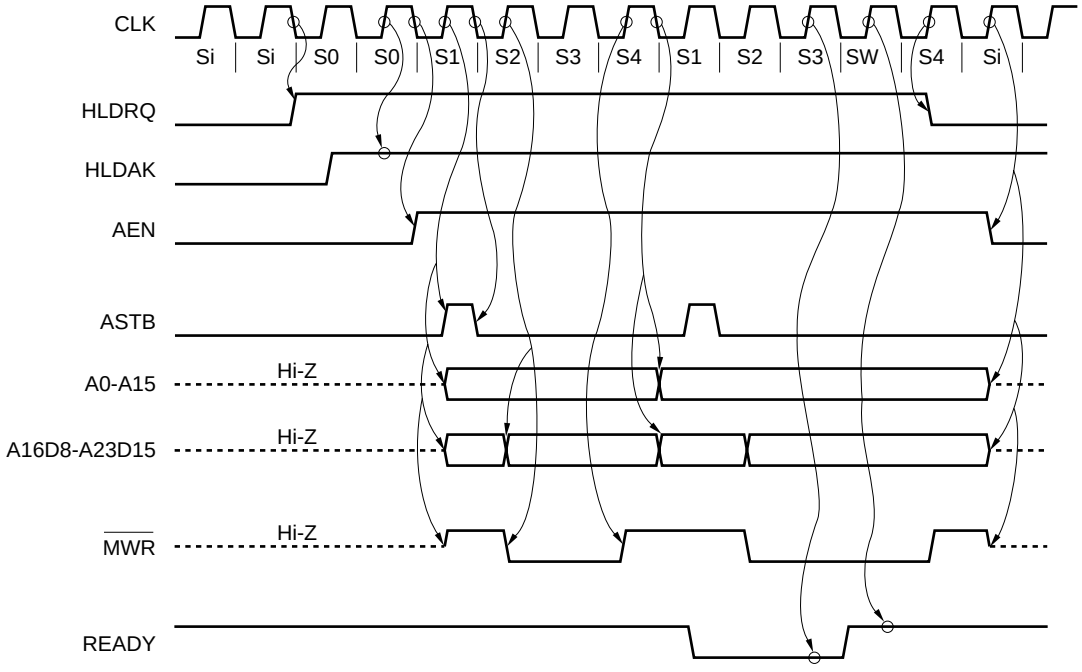
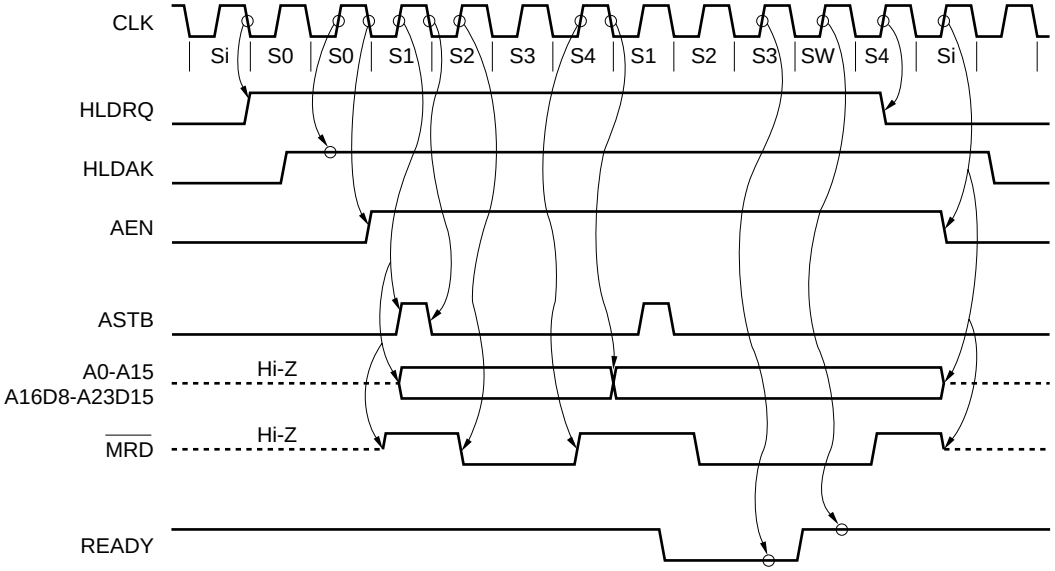
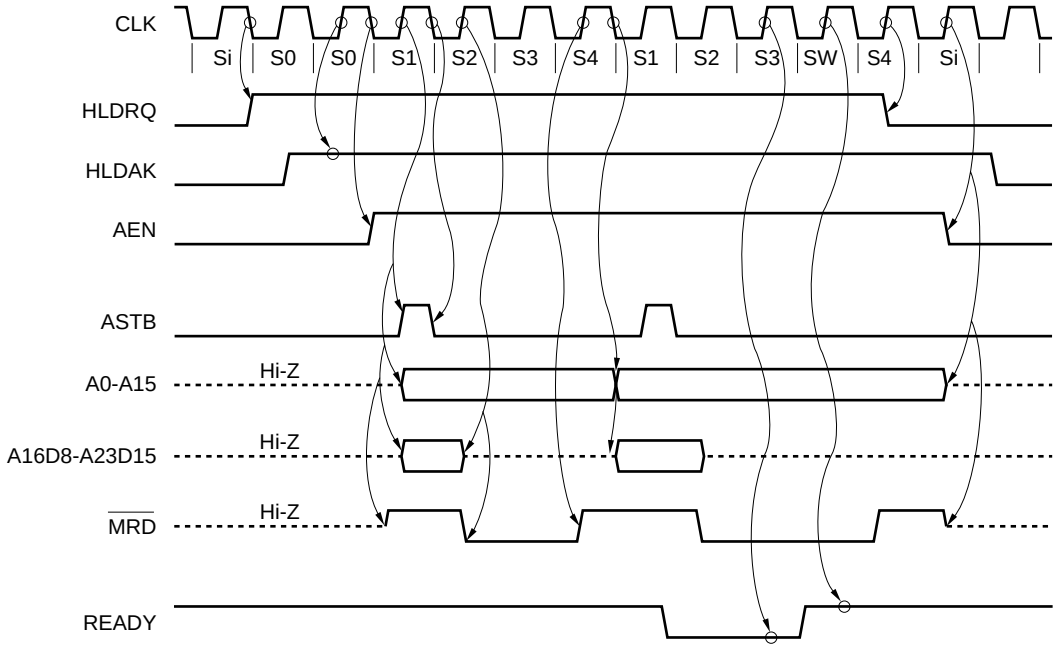


Figure 2-6. Memory Read Timing

(a) $\overline{B}$/W = 0



(b) $\overline{B}$/W = 1



2.2.4 Address/data multiplexing

Addresses and data are multiplexed as shown below.

Pin	Address	Data
A0 to A15	0 to 15	–
A16D8 to A23D15	16 to 23	8 to 15
D0 to D7	–	0 to 7

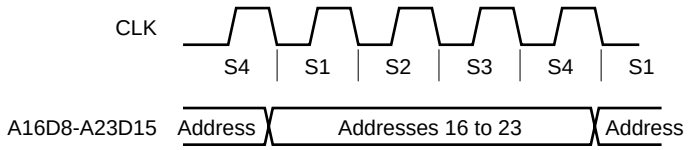
This multiplexing method is used to reduce the external address latch.

Therefore, the operation of the pins (A16D8 to A23D15) used for address/data multiplexing varies depending on the value input to the $\overline{B}$/W pin.

When external memory is configured using byte mode ($\overline{B}$/W = 0), an external address latch is not required, as is shown in Figure 2-7. When external memory is configured using word mode ($\overline{B}$/W = 1), an external address latch is not required as along as the memory contents do not exceed 64 Kbytes (requiring no more than 16 address pins), as shown in Figure 2-8. When the memory contents exceed 64 Kbytes, an external address latch is required for pins A16D8 to A23D15.

Figure 2-7. Byte Mode ($\overline{B}$/W = 0)

(a) Memory read



(b) Memory write

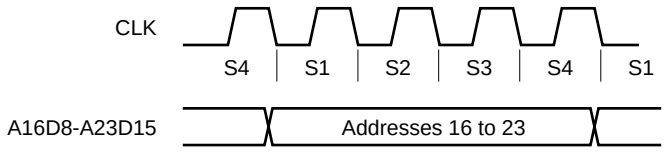
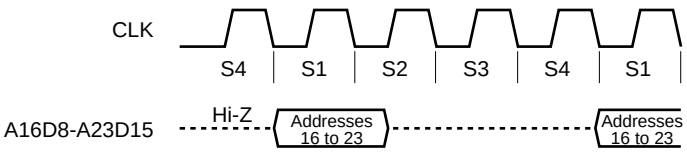
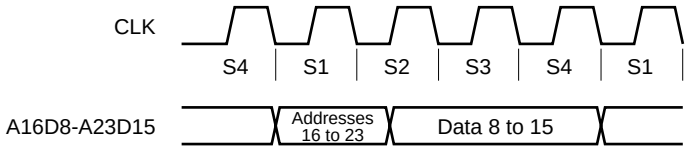


Figure 2-8. Word Mode ($\overline{B}$/W = 1)

(a) Memory read

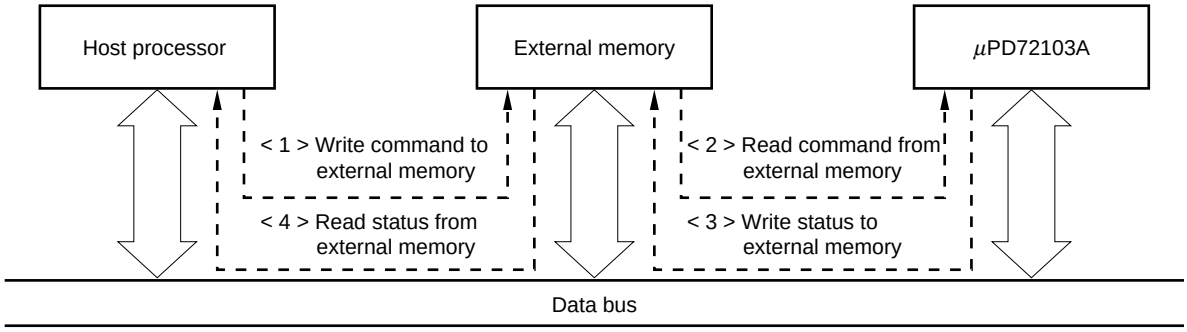


(b) Memory write



2.3 Interface between μPD72103A and Host Processor

Figure 2-9. Command/Status Handling between μPD72103A and Host Processor



As shown in Figure 2-9 above, command/status handling between the μPD72103A and the host processor is performed via DMA transfers to and from external memory.

The transmit data is written from the host processor to external memory. The μPD72103A then reads the transmit data from external memory and converts it to serial data.

For the receive data, the μPD72103A converts them from serial data to parallel data, which is then written to external memory, where it is read by the host processor.

There are two basic methods for synchronizing these operations: (1) a method that uses the CRQ pin, INT pin, and CLRINT pin and (2) a method that uses the CCRQ bit and CCLRINT bit in the control register and the INT bit in the internal status register. It is also possible to combine these two methods.

Note See "**2.1.1 Control register**".

(1) Method using the CRQ pin, INT pin, and CLRINT pin

<1> When the host processor issues a command to the μPD72103A, the command is written to a command table in external memory[Note] and the CRQ pin becomes active (high level). When this operation is completed, the μPD72103A begins reading the command.

<2> When it is necessary for the μPD72103A to report to the host processor, the host processor sets the INT pin as inactive (low level) by setting the CLRINT pin as active (high level).

<3> Next, the μPD72103A writes a status report to external memory and sets INT pin as active (high level). The host processor uses this signal as an interrupt to detect the timing of the status report from the μPD72103A.

Note See "**2.3.1 B. Method using write to external memory**".

(2) Method using the CCRQ bit and CCLRINT bit in the control register and the INTS bit in the internal status register

<1> When the host processor issues a command to the μPD72103A, the command is written to external memory as was done via method (1) above[Note 1]. After that, "1" is written to the CCRQ bit.

<2> When it is necessary for the μPD72103A to report to the host processor, the host processor writes a "1" to the CCLRINT bit in the μPD72103A's control register, which sets a "0" to the INTS bit.

<3> After the μPD72103A writes the status information to external memory, it sets "1" to the INTS bit. Since the INTS bit and the INT pin correspond to the same signal, the host processor is able to detect the status report timing simply by polling the INTS bit, and without using an interrupt for the INT pin[Note 2].

Notes 1. See "**2.3.1 B. Method using write to external memory**".

2. See "**2.1.2 Internal status register**".

2.3.1 Command issuance

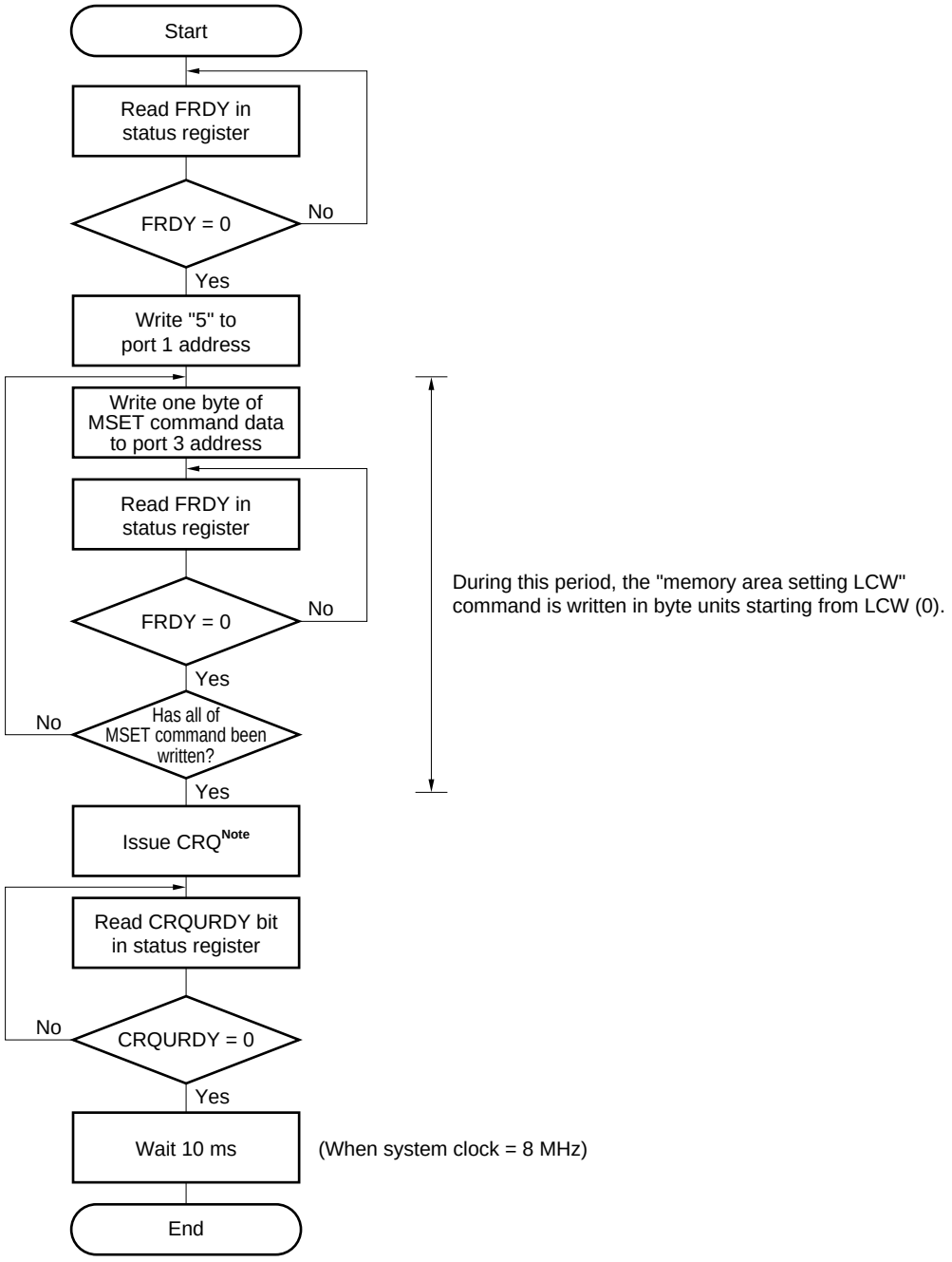
Commands can be issued via the following two methods.

- Method using write to internal FIFO
  This method is used to initiate the "memory area setting LCW" command.
- Method using write to external memory
  This method can be used to initiate the "memory area setting LCW" command or to initiate commands other than the "memory area setting LCW" command.

A. Method using internal FIFO write

Immediately after the FIFO in the μPD72103A has been reset, this method writes only the "memory area setting LCW" command. This method can only be used once when setting a start address of the system area immediately after a reset. The flow to be followed when writing to the internal FIFO is shown below.

Figure 2-10. Flow Chart for Writing “Memory Area Setting LCW” Command to Internal FIFO



Note This is done via a pulse input to the CRQ pin or by setting “1” to the CCRQ bit in the command register.

B. Method using write to external memory

Actually, there are two methods that use a write to external memory.

The first method writes the “memory area setting LCW” command in byte units immediately after a reset, starting from address 0.

After the command is executed (and the CRQ pin and CCRQ bit of the control register are active), this method is the same as when writing the “memory area setting LCW” command to the internal FIFO.

The other method writes a command to a command table. This method is used when issuing a command other than the “memory area setting LCW” command. Use the following steps to write the command.

(1) Check that the CMDS field in the LCW where a command is written is “FCH/FDH/FEH”. If the CMDS field is something else, LCW cannot be used, so wait until it becomes “FCH/FDH/FEH”.
(2) After writing the command number to LCW (0) and the command information to LCW (2) to (15), write “00H” to LCW (1). Make sure that writing to LCW (1) is the last operation in this sequence.
(3) Issue the command after the CRQ pin or CCRQ bit of the control register becomes active.

After the issued command has been executed, command execution can be confirmed by inserting “FCH/FDH/FEH” into the command area’s CMDS field or by writing a command end status to the status table.

2.3.2 Status report

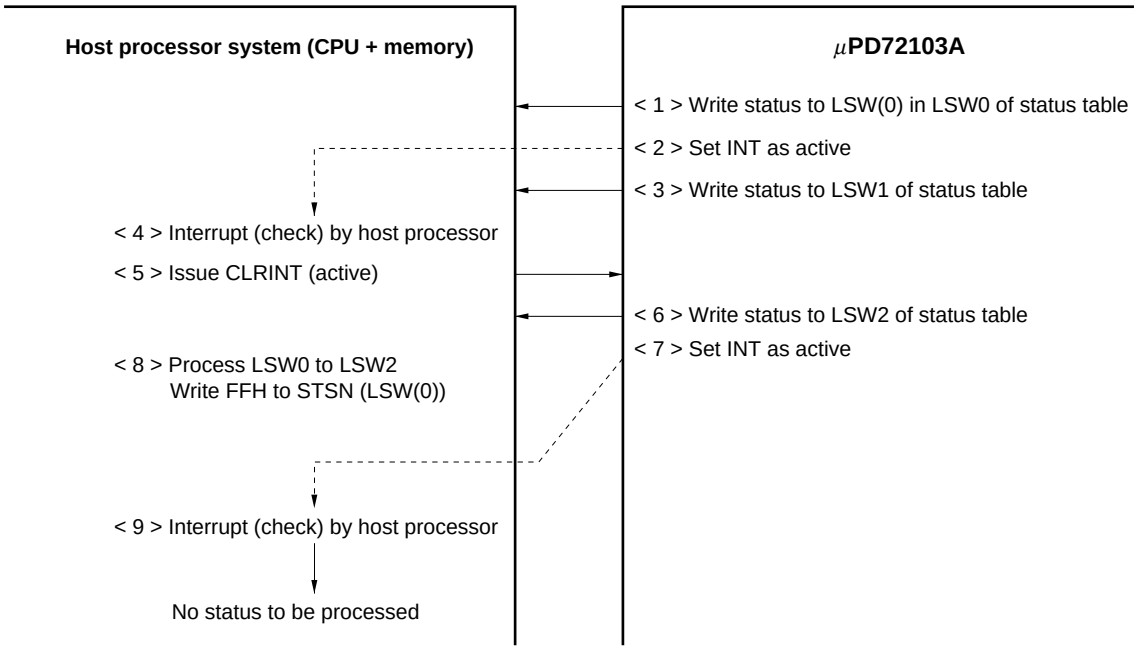
After a command has been executed or data has been received, the μPD72103A writes information to the status table, then sets the INT pin or the INTS bit as active.

Meanwhile, the host processor detects the active state of the INT pin or INTS bit, after which the status table should be checked. Use the following steps to check the status table.

(1) Set the CLRINT pin or CCLRINT bit as active and the INT pin or INTS bit as inactive.
(2) Check the status table and process all of the reported status settings. Note that several status settings may be reported for a single interrupt.
(3) After completing this processing, write FFH to LSW (0) in the status table and then release the status table.

However, in some cases when the above processing steps are used, a status check by the host processor shows that there are no status reports. This occurs when all processing has been completed during the previous round of status processing, such as is shown in Figure 2-11. Therefore, such cases do not indicate a fault or abnormality.

Figure 2-11. Status Report (when Status Area is LSW0 to LSW2)



2.3.3 Command chain function

The command chain function enables the μPD72103A to sequentially execute several commands allocated successively in memory by issuing only one command request (which is executed by setting the CRQ pin or CCRQ bit as active).

This function operates via the following sequence.

(1) The host processor sets all of the commands to be executed to external memory in advance. "FFH" is then set to LCW(1) in the command table following the last command to be executed.
(2) After the commands are set to external memory, the CRQ pin or CCRQ bit is set as active.

The μPD72103A then executes all of the commands in external memory up to where "FFH" has been set to LCW(1) in the command table.

2.4 Initialization of External Memory

After the μPD72103A has been reset, the host processor writes FFH to initialize the external memory before issuing the “memory area setting LCW” command. This empties the command table and status table.

2.5 Methods for Using External Memory

From the perspective of the μPD72103A, external memory is memory that exists externally and is used for the host interface. Set the following five areas in external memory using the methods described in sections **2.5.1** to **2.5.5** below.

(1) Command table
(2) Status table
(3) Receive buffer address table
(4) Receive buffer
(5) Transmit buffer

2.5.1 Command table

The command table is a table where commands used by the host processor to direct operations in the μPD72103A are written.

The command table’s start address is set by the “memory area setting LCW” command.

In the command table, each command area LCW (Link Command Word) consists of several (quantity = n) 16-byte LCWs. The number of command area LCWs ($1 \leq n \leq 128$, where n is an exponent of two) is set via the “memory area setting LCW” command.

The command area LCW (n - 1) that is the (nth - 1) command area LCW in the command table is linked by this method to the first command area LCW0, so if the host processor issues a command after LCW (n - 1), the next command is set to LCW0.

The command table and command fields are shown below.

Figure 2-12. Command Table

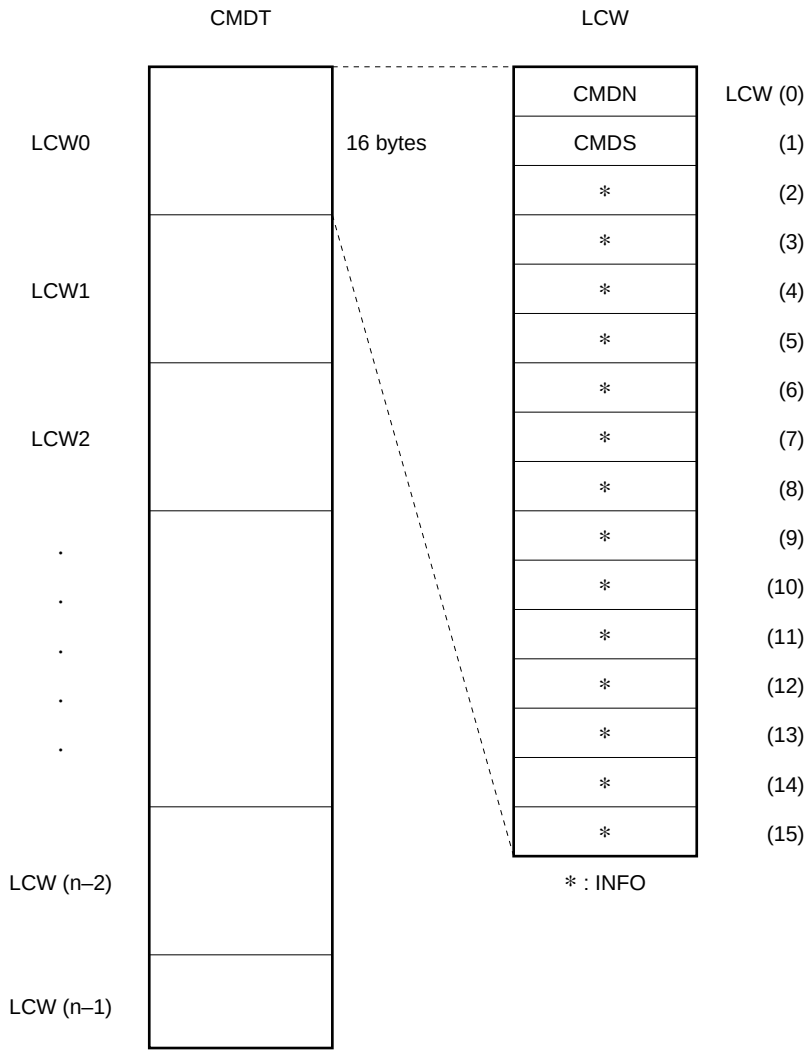


Table 2-5. Command Fields

LCW (n)	Field name	Description
0	CMDN	This is the command number field. The host processor writes the command number when the CMDS field is “FCH/FDH/FEH”.
1	CMDS	This is the command status field. After the transmit command fetch operation is completed, the μPD72103A writes “0CH” to this field. After the command has been executed, the μPD72103A writes “FCH/FDH/FEH” to this field. This operation releases the command table. When this field contains “FCH/FDH/FEH”, the host processor writes a command number and command information and then writes “00H” to this field.
2 to 15	INFO	These are the command information fields. When the CMDS field contains “FCH/FDH/FEH”, the host processor writes information to these fields. However, the number of usable command information fields differs according to the command. “00H” is written to fields that are not used.

Remark The meanings of “FCH/FDH/FEH” in the CMDS field are as follows.

FCH: Set when a execution of a command other than a transmit command has been completed

FDH: Set when a transfer is stopped after a transmit command has been executed.

FEH: Set when a transfer ends normally after a transmit command has been executed.

Figure 2-13 illustrates the μPD72103A’s command fetch operations.

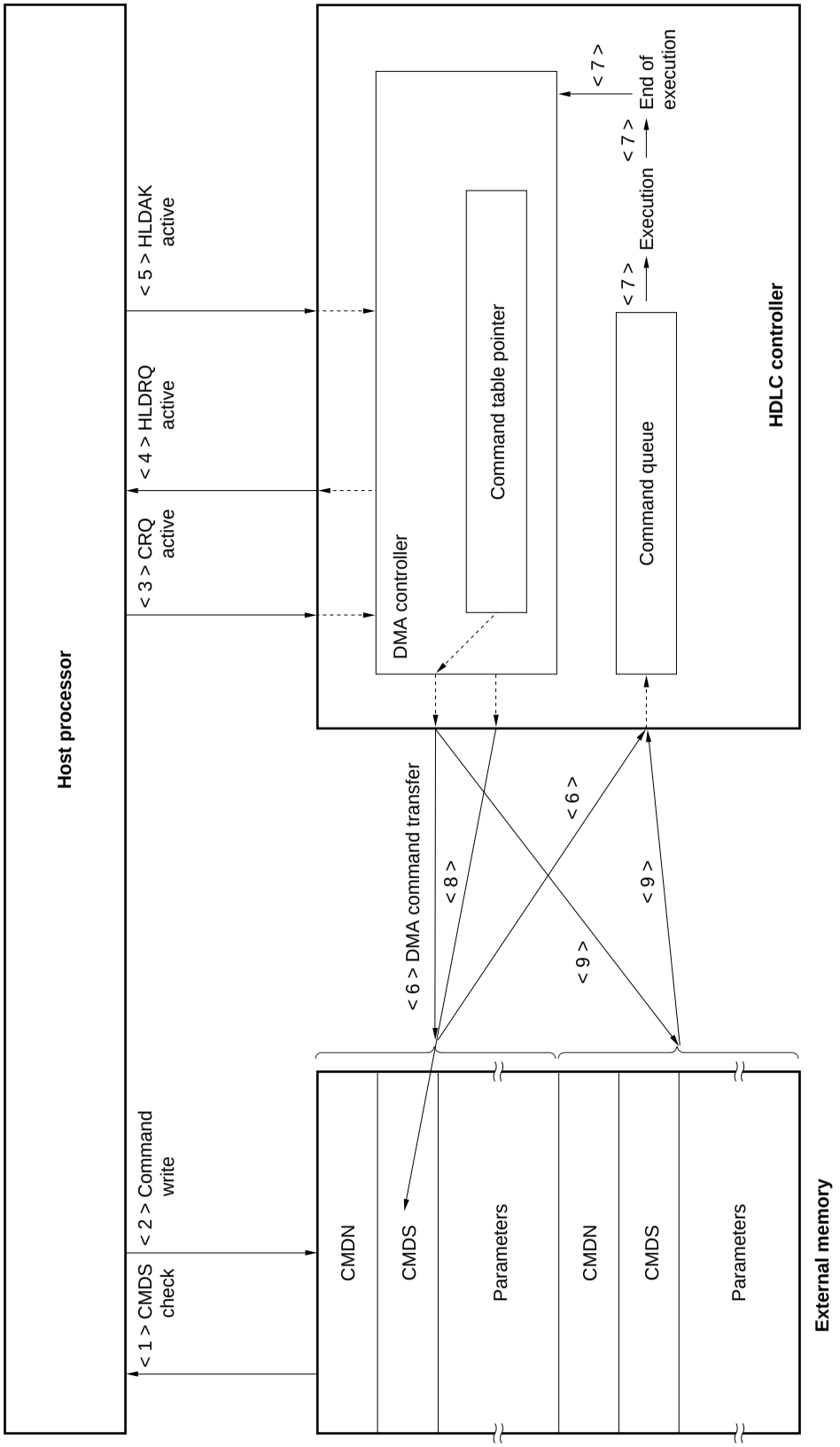


Figure 2-13. Command Fetch Operation

The operations enumerated as <1> to <9> in Figure 2-13 are described below.

<1> The μPD72103A has an internal command table pointer. Make sure that the second byte (CMDS) of the command area indicated by the command table pointer is "FXH". In this case, the host system may need to have a command table pointer (whose initial value is set by the MSET command) in memory.

<2> Write one or more commands to the command table.

<3> The host processor sets the μPD72103A's CRQ pin as active so that the command is captured by the μPD72103A.

<4> The μPD72103A issues a bus mastership request to the host processor so that it can capture the command. (HLDRQ pin active)

<5> The host processor sets the μPD72103A's HLDAK pin as active to shift bus mastership to the μPD72103A.

<6> The μPD72103A sends to the command queue (via DMA transfer) a command that it has fetched from the table indicated by its internal command table pointer.

<7> The command is executed.

<8> When command execution is completed, FXH is written to CMDS.

<9> The μPD72103A increments the command table pointer by +10H. The μPD72103A then proceeds to the next operation according to the command indicated by the incremented command table pointer.

CMDS	μPD72103A operation
FXH	Stop reading command
00H	Fetch command and execute

After this, operations <1> to <9> above are repeated.

Remark Since the μPD72103A's DMA operation is performed in either 4-byte or 8-byte units during one period when the HLDRQ pin is at high level, operations <4> and <5> above are repeated to capture commands and transfer transmit and receive data.

2.5.2 Status table

The μPD72103A uses the status table to provide status reports to the host processor.

The status table's start address is the address following the command table.

In the status table, each status area LSW (Link Status Word) consists of several (quantity = n) 16-byte LSWs.

The number of status area LSWs ($1 \leq n \leq 128$, where n is an exponent of two) is set via the "memory area setting LCW" command.

The status area LSW (n - 1) that is the (nth - 1) status area LSW in the status table is linked by this method to the first status area LSW0.

Therefore, if the μPD72103A writes a status to LSW (n - 1), the next status is written to LSW0.

The status table and status fields are shown below.

Figure 2-14. Status Table

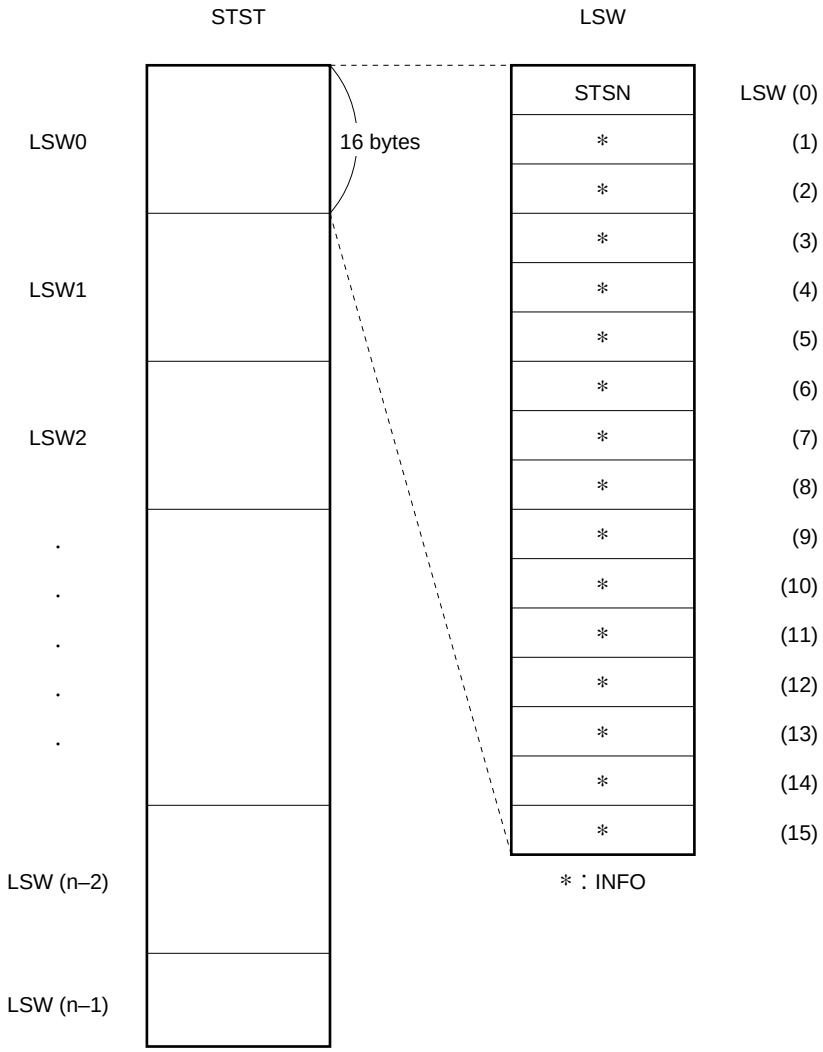
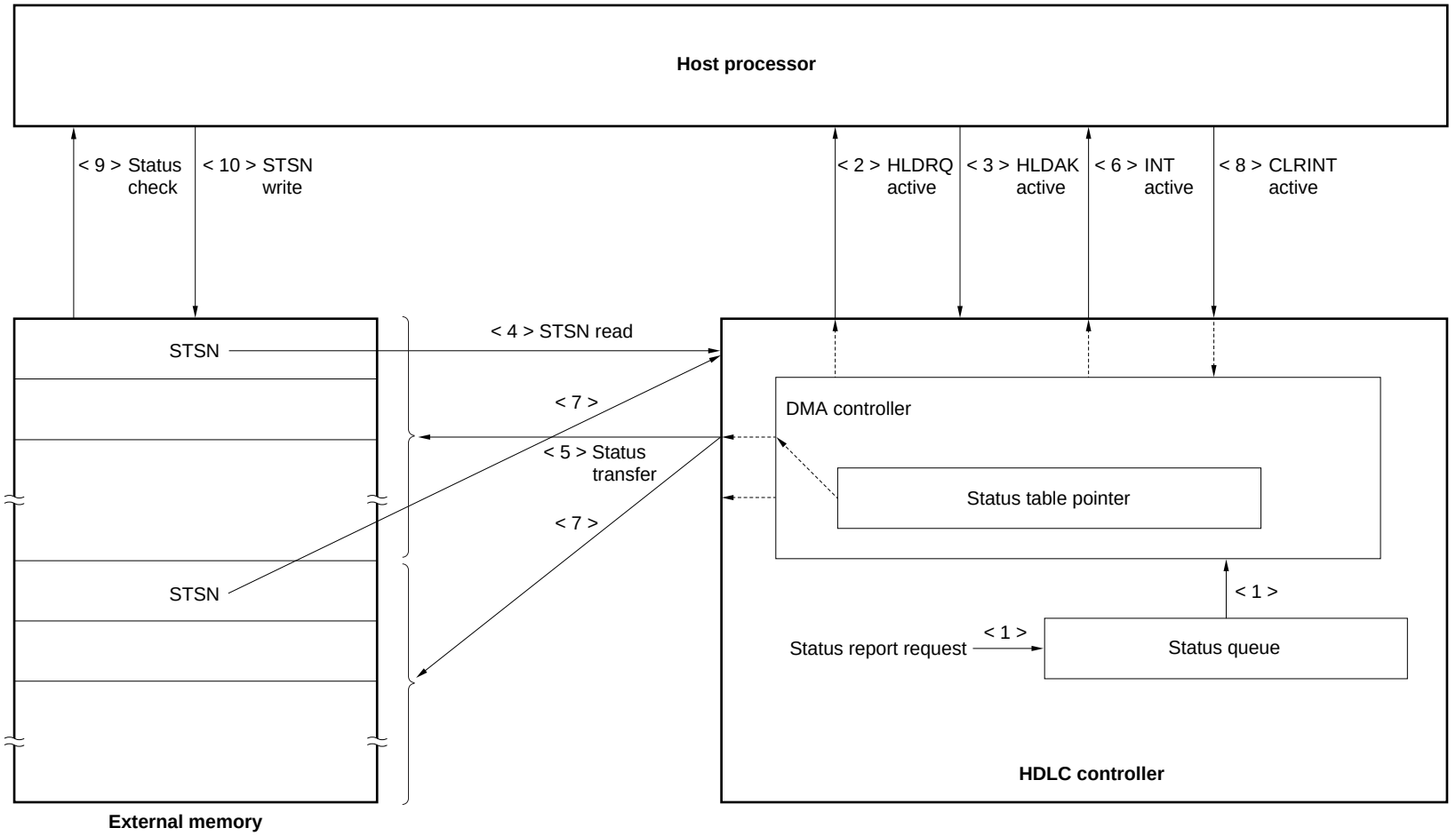


Table 2-6. Status Fields

LSW (n)	Field name	Description
0	STSN	This is the status number field. The host processor writes FFH to this field when status processing has been completed. By writing FFH to this field, the μPD72103A releases the status table.
1 to 15	INFO	These are the status information fields. However, the number of usable status information fields differs according to the status.

Figure 2-15 illustrates the μPD72103A's status information operations.

Figure 2-15. Status Information Operations



The operations enumerated as <1> to <9> in Figure 2-15 are described below.

<1> The μPD72103A internally generates status reports such as data reception reports and line open completion status reports.

<2> The μPD72103A sends the host processor a HLDRQ signal to obtain bus mastership.

<3> The host processor sets the μPD72103A's HLDAK pin as active to shift bus mastership to the μPD72103A.

<4> The μPD72103A has an internal status table pointer. A DMA read operation is performed to read the data at the address indicated by this status table pointer to check whether or not the data value is FFH. If it is not FFH, the current status is held until it becomes FFH. A status table overflow is reported when a series of status report requests are issued even though there is no empty space in the status table, which causes status to be lost.

<5> The status is written via a DMA transfer (STSN is written last).

<6> After writing the first status to the status table, the μPD72103A sets the INT pin as active.

<7> When a status report request is issued, the status is reported to the second status table via the same operation as in steps <4> and <5> above.

<8> The operation of the host processor branches to a interrupt service routine when the μPD72103A's INT pin becomes active. The INT pin is reset by setting the CLRINT pin as active at the start of this interrupt service routine.

<9> The host processor checks the status table and responds in various ways according to the cause.

<10> When a status is no longer needed, the status table's start data (STSN) is set to FFH (empty status).

2.5.3 Receive buffer address table

The receive buffer address table is a table of start addresses for several receive buffers. The μPD72103A writes the frames it receives to these receive buffers. The host processor sets up this table before receiving any frames.

The receive buffer address table begins at the address following the status table.

The receive buffer address table consists of a receive buffer address area LRBW (Link Receive Buffer Address Word) that includes several (quantity = n) 4-byte LRBWs. The number of LRBWs ($1 \leq n \leq 128$, where n is an exponent of two) is set via the “memory address setting LCW” command. Each receive buffer address area LRBW consists of four bytes.

The receive address area LRBW (n - 1) that is the (nth - 1) receive buffer address area LRBW in the receive buffer address table is linked by this method to the first receive buffer address area LRBW0.

Therefore, if the host processor issues a receive buffer address following LRBW (n - 1), it is written to LRBW0.

The receive buffer address table and receive buffer address fields are shown below.

Figure 2-16. Receive Buffer Address Table

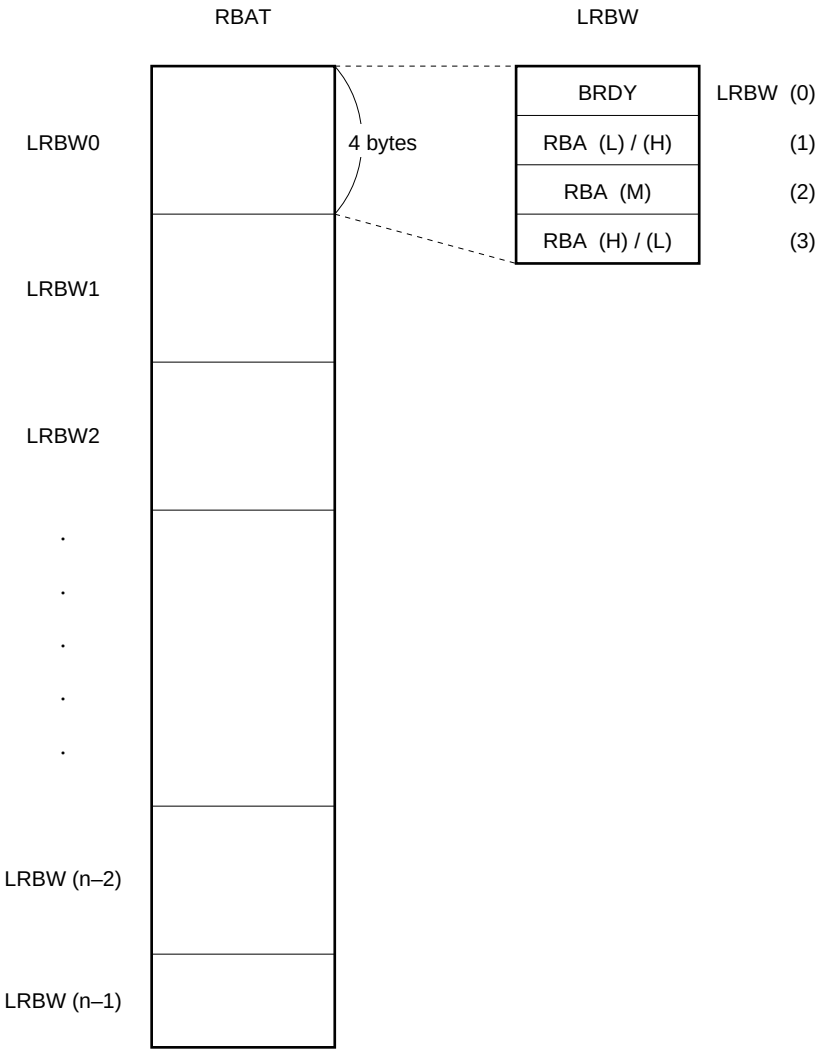


Table 2-7. Receive Buffer Address Fields

LRBW (n)	Field name	Description
0	BRDY	This is the receive buffer status field. The μPD72103A reads the receive buffer address field, and then writes FFH to this field when this field is 00H. However, when in receive buffer chain mode, F0H is first written to this field after the read operation, then FFH is written after completion of frame reception. The host processor writes 00H to this field once processing of receive data is completed. The μPD72103A releases the receive buffer once 00H has been written.
1 to 3	RBA	This is the receive buffer address field. The host processor writes the start address of the receive buffer where μPD72103A's receive data is written. Note that this field should be written to before issuing the "line open LCW" command. When setting addresses, write addresses separately to the (H), (M), and (L) positions.

Cautions 1. For LRBW (1) and LRBW (3), the (H) and (L) positions vary according to the parameter values set by the "operation mode setting LCW" command.
2. First write to LRBW (1) to LRBW (3), then finish by writing 00H to LRBW (0).
3. When a discarded frame is received, the LRBW table corresponding to the discarded frame is used as the receive buffer pointer for the frame that is received next.

Figures 2-17 to 2-23 show examples of relationships between receive buffer address tables and received frames.

(1) Initial status (line closed) (see Figure 2-17)

Before issuing the "line open LCW" command, the host processor sets receive addresses to the receive buffer address table. In the example shown in Figure 2-17, addresses 100, 200, 300, and 400 in the receive buffer address table are set as start addresses for the receive buffer.

(2) Line open status (see Figures 2-18 and 2-19)

When the "line open LCW" command is issued, the μPD72103A reads the contents of the receive buffer address table in order starting from LRBW0 and sets the data to its internal receive buffer address FIFO (RBAFIFO). Once the table has been completely read, the μPD72103A changes BRDY parameter contents to FFH (or F0H if using a receive buffer chain). In the example shown in Figure 2-18, the RBA in the LRBW0 field is set to the RBAFIFO and the BRDY parameter's value is changed to FFH.

Figure 2-19 illustrates how four RBAs are fetched and set to the RBAFIFO.

(3) Start of frame reception (see Figures 2-20 to 2-23)

When the μPD72103A receives an HDLC frame, it accepts DMA transfer of the data following the start flag to the receive buffer specified by RBA0. Figure 2-20 shows how the first frame is received and how the data values 30H and 31H are set via DMA transfer.

After the FCS and end flag are received, the FCS is checked for errors. If the frame is normal, the "data reception LSW" is reported to the status table (it is not reported if the received frame is abnormal), and the interrupt signal is set as active. Figure 2-21 shows the internal status after data is received with an FCS error. Figure 2-22 shows the status when starting to receive the second frame. Figure 2-23 shows the status when reception of the second frame ends normally, after which the "data reception LSW" is reported and the interrupt signal is set as active.

The μPD72103A also has an internal pointer for the receive buffer address table. The μPD72103A increments this pointer each time a receive buffer address is captured in the RBAFIFO. Accordingly, if the table indicated by this pointer is not empty, the μPD72103A continues to wait until the table is empty.

Figure 2-17. Initial Status (Line Closed)

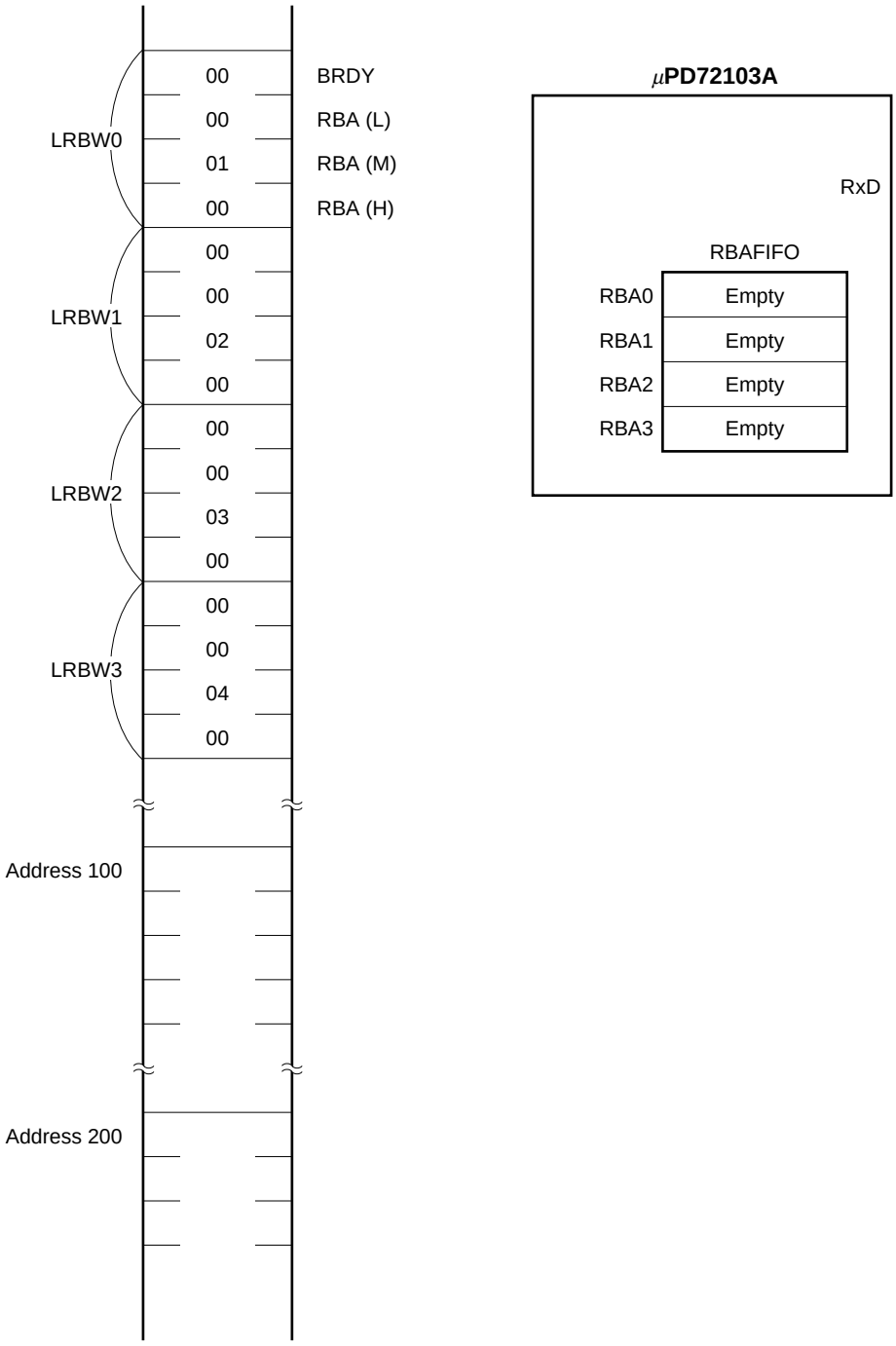
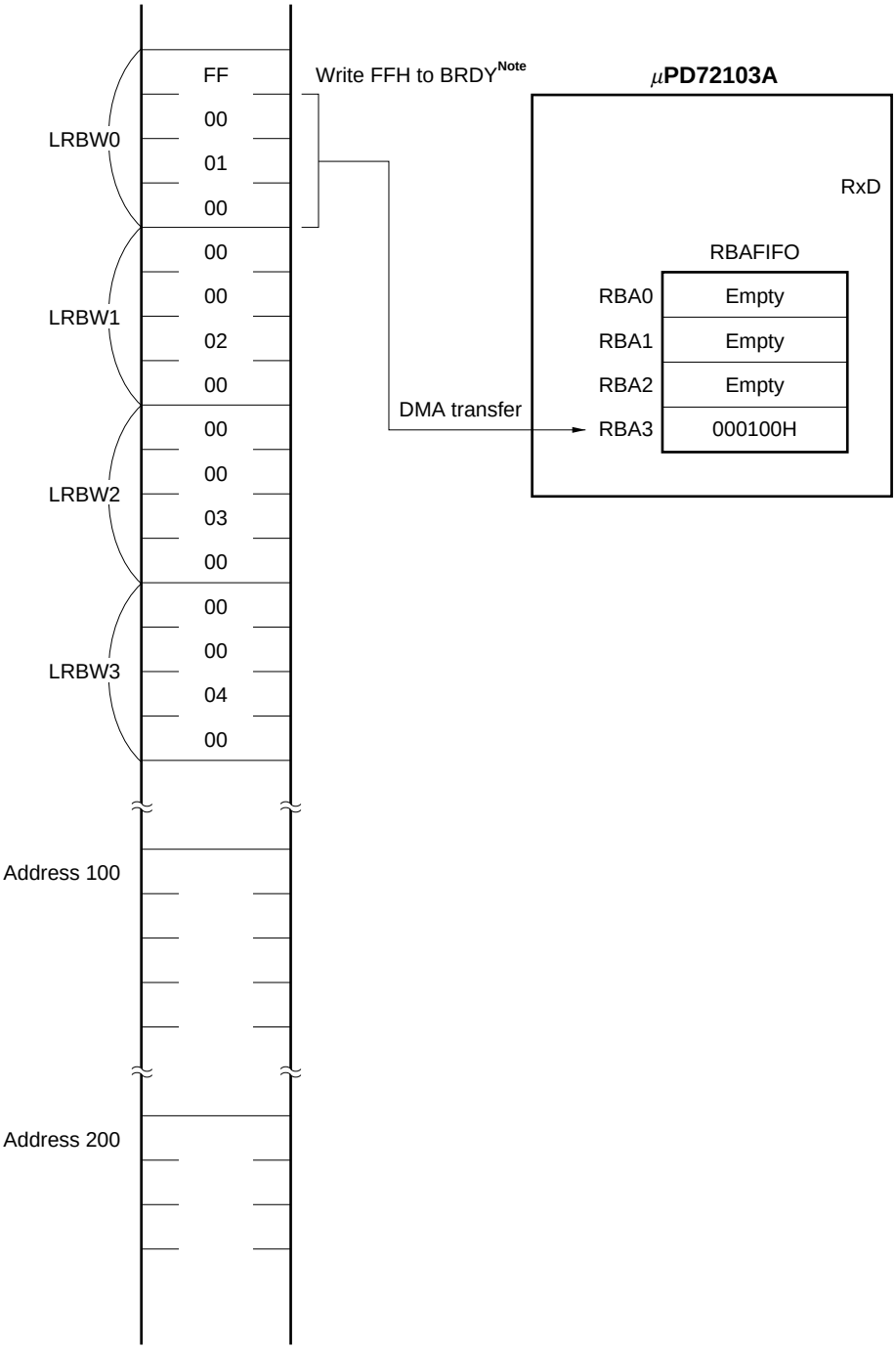


Figure 2-18. After Line Open Command Is Issued



Note F0H is written when in receive buffer chain mode.

Figure 2-19. RBAFIFO Full Status

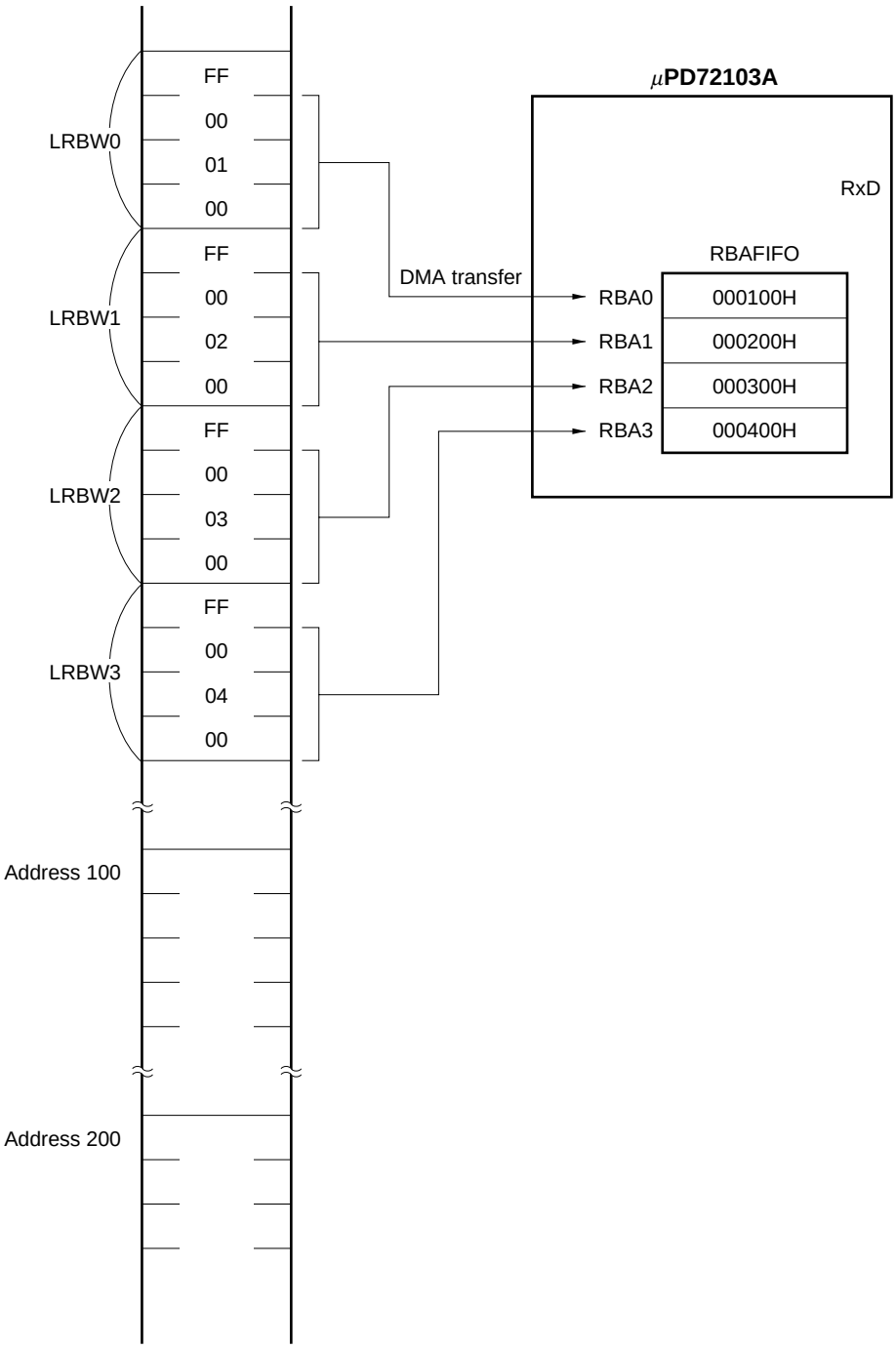


Figure 2-20. Reception of First Frame

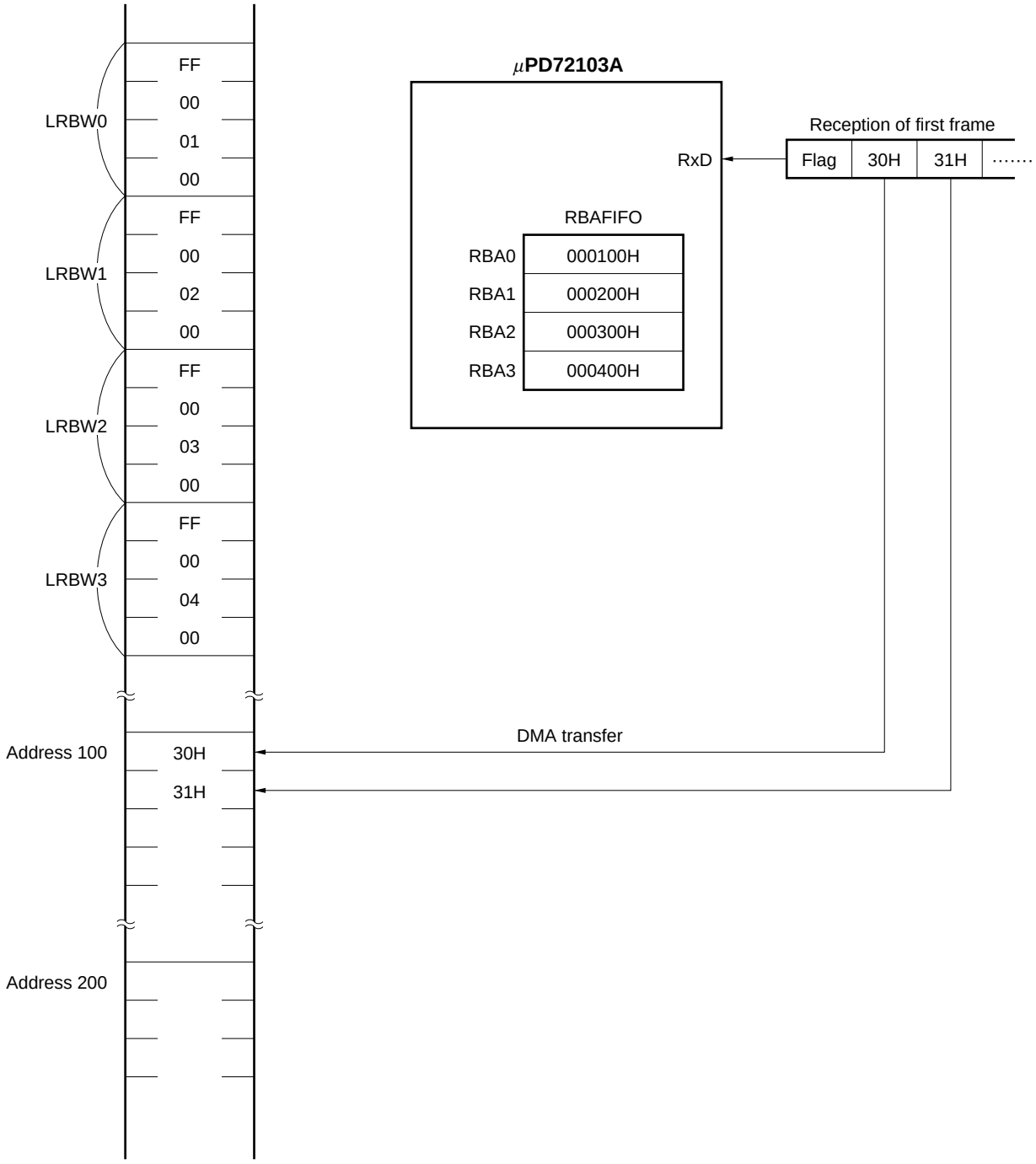


Figure 2-21. Completion of First Frame Reception (FCS Error)

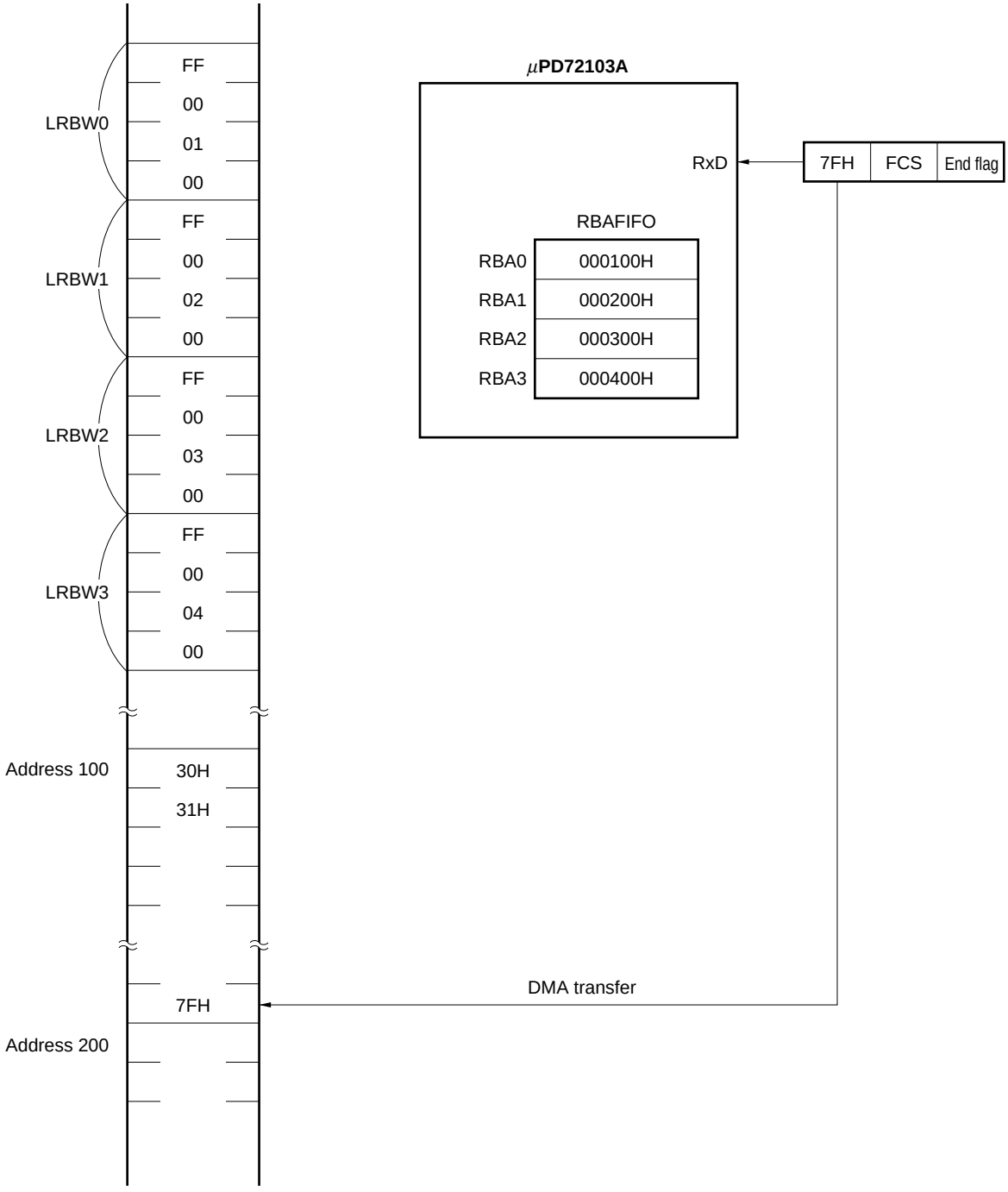


Figure 2-22. Start of Second Frame Reception

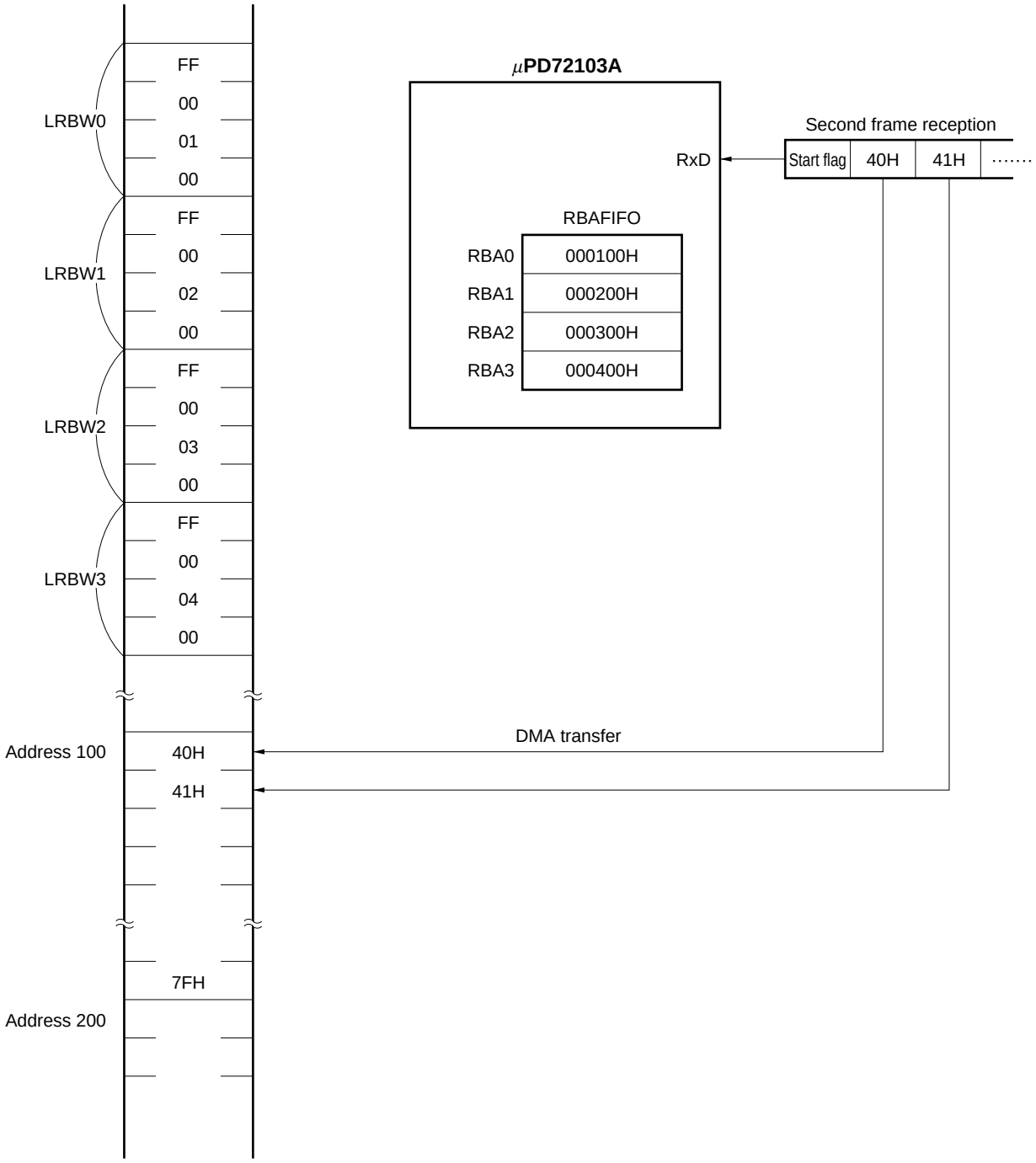
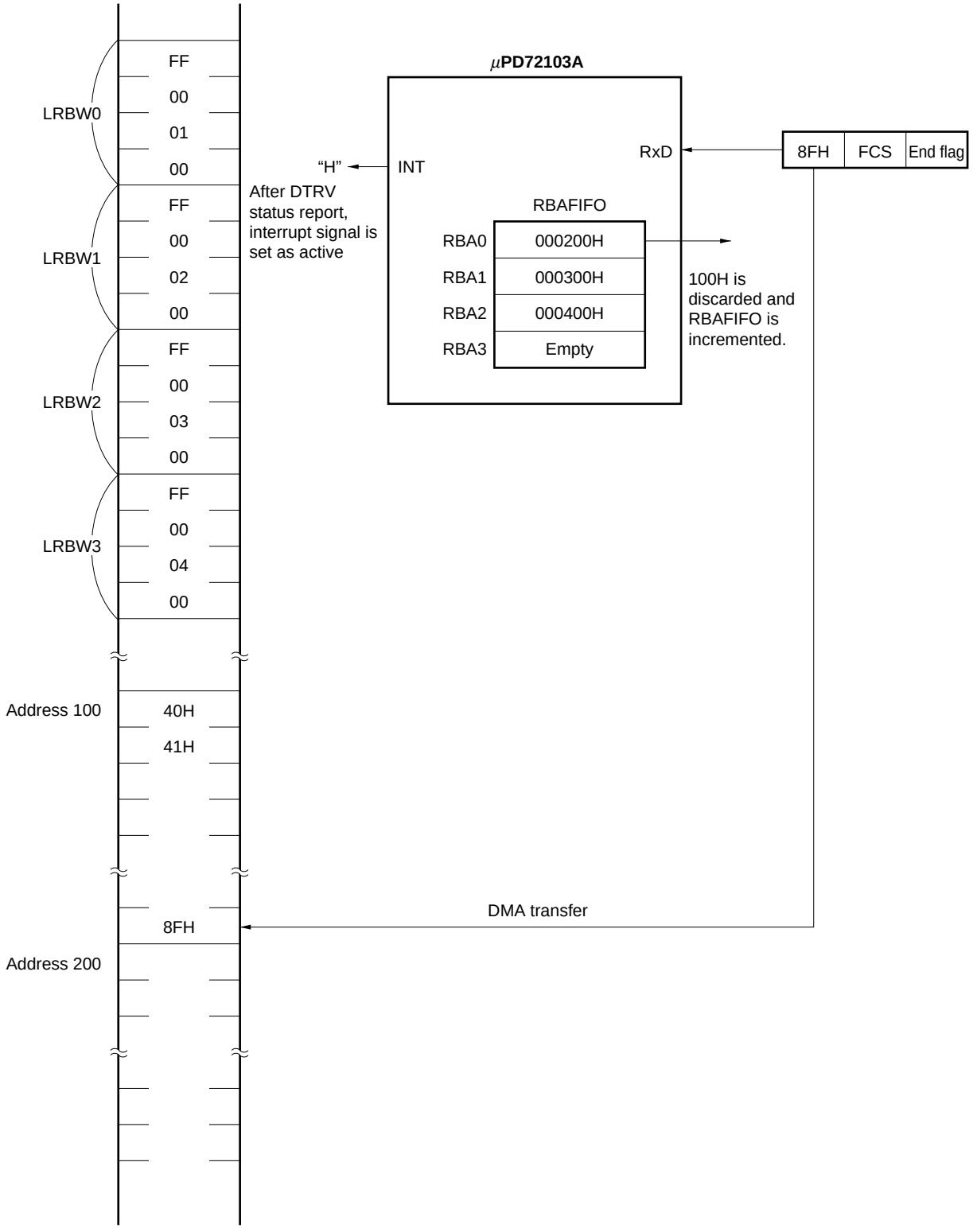


Figure 2-23. Completion of Second Frame Reception



2.5.4 Receive buffer

The receive buffer is the area where data received by the μPD72103A is written.

The receive buffer's start address is set by the host processor to the receive buffer address table.

The receive buffer's size is set via the "operation mode setting LCW" command. Any size up to 16 Kbytes can be set for the receive buffer.

2.5.5 Transmit buffer

The transmit buffer is the area where the μPD72103A writes data to be transmitted.

The host processor uses the "data transmission LCW" command to set the transmit buffer's start address and size. Any size up to 16 Kbytes can be set for the transmit buffer.

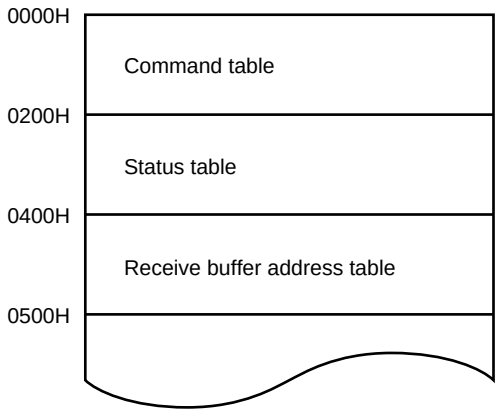
2.5.6 External memory table configuration example

Below is an external memory configuration example for the "memory area setting LCW" command.

Table 2-8. External Memory Table Configuration Example

Parameter	Function	Parameter setting example
ADDR (L), (M), (H)	Indicates the start address of the command table	000000H
NLCW	Specifies the number of blocks in the command table	20H
NLSW	Specifies the number of blocks in the status table	20H
NLRBW	Specifies the number of blocks in the receive buffer address table	40H

Figure 2-24. External Memory Configuration Example



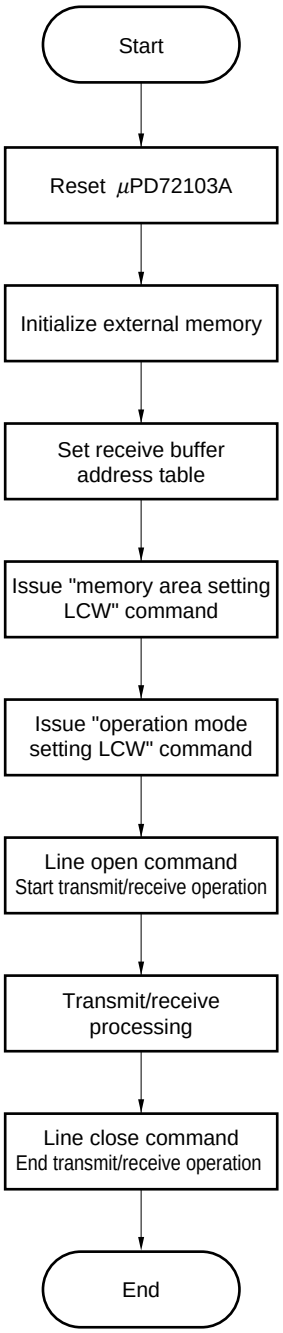
[MEMO]

CHAPTER 3 COMMUNICATION OPERATIONS

3.1 Initial Settings

The host processor initializes the μPD72103A and the external memory via the steps shown in Figure 3-1 below.

Figure 3-1. Initialization Steps for μPD72103A and External Memory



3.2 Start of Communication Control Operation and Flag Synchronization Setup

When starting a transmit/receive operation, issue “line open LCW” command and set the μPD72103A’s transmit/receive mode.

The operations following issuance of the “line open LCW” command are described below.

3.2.1 Transmit operation

This operation varies according to the TFIL setting in the “operation mode LCW” command.

TFIL = 0	Transmit flag after issuance of “line open LCW” command
TFIL = 1	Transmit idle (“1”) after issuance of “line open LCW” command

3.2.2 Receive operation

After the “line open LCW” command has been issued, the μPD72103A enters flag search mode.

3.2.3 Status reporting

After the “line open LCW” command has been issued, the μPD72103A reports a “line open completion LSW”.

The timing of “line open completion LSW” reporting varies according to the LOAK and TFIL settings in the “operation mode setting LCW” command.

- When TFIL = 0

LOAK = 0	Report status when flag transfer has begun from local side.
LOAK = 1	Report status when flag has been received from remote side.

- When TFIL = 1

  The status is reported following execution of the “line open LCW” command.

3.3 Data Transmission

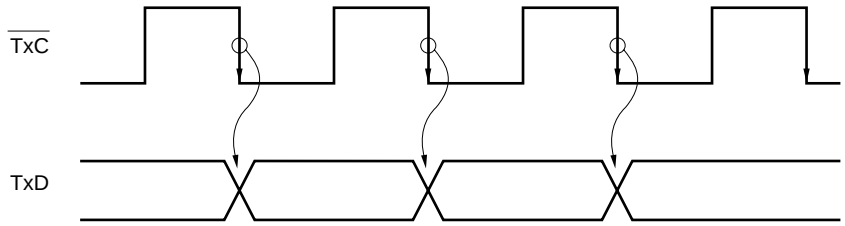
The μPD72103A transmits in BC byte units the data in the transmit buffer in external memory that is specified by the BUFA parameter in the "data transmission LCW" command.

When the μPD72103A completes transmission of the data, it reports the "data transmission completion LSW" command.

3.3.1 Transmission timing

Data transmitted via the TxD pin during the period from the falling edge of $\overline{\text{TxC}}$ to the next falling edge of $\overline{\text{TxC}}$ is output as one bit.

Figure 3-2. Transmission Timing



Remark The $\overline{\text{TxC}}$ pin is an output pin when DPLL is used and is an input pin when DPLL is not used.

3.3.2 Linkage of transmit data

Transmit data is set to the transmit buffer and the "data transmission LCW" command.

Up to eight bytes can be set to the "data transmission LCW" command.

After data is written to the transmit buffer, the "data transmission LCW" command is set and the transmit operation begins. At this time, the transmit data from the "data transmission LCW" command is lined with the transmit data specified by the BUFA parameter in the transmit buffer to form one frame.

In this case, the frame is transmitted in the following order: first the start flag is transmitted, followed by the data in the "data transmission LCW" command and then the data in the transmit buffer.

3.3.3 Transmit buffer chain

The μPD72103A transmits in BC byte units the data in the memory address that is specified by the BUFA parameter via the "data transmission LCW" command execution. In this case, the maximum data length is 16 Kbytes (data in the transmit buffer and data in the data transmission LCW).

A transmit buffer chain can be used for data transfers when the data length in one frame exceeds 16 Kbytes or when specified data in the transmit buffer is divided among several areas.

A transmit buffer chain is a continuous series of "data transmission LCW" commands that set transmit data to transmit buffers and specify the transmit data addresses corresponding to each block of data. Transmit chain bits are set corresponding to the commands for the data in the chain.

The reset bit value is assigned to the transmit chain bit for the "data transmission LCW" command corresponding to the data that is the last data in the chain.

After the "data transmission LCW" commands have been set and as soon as the CRQ pin (CCRQ bit) becomes active, the data in the transmit buffer specified by the chain is transmitted as one frame.

When using a transmit buffer chain, setting of transmit data within the "data transmission LCW" command is enabled only for the first command.

Caution When using transmit chains to transmit data, if the transmit data length corresponding to individual commands is too short, the transmit FIFO may be left empty during the period when the μPD72103A reads, parses, and executes a command and reads new transmit data, which increases the chance of a transmission underrun error. For example, if the μPD72103A is being used only for transmitting and the communication speed is 1 Mbps (system clock = 8 MHz) the minimum transmit data length is 22 or 23 bytes. If the μPD72103A is also being used for receiving, a data length of at least twice that length must be set.

3.3.4 Transmission underrun

When an underrun occurs, the μPD72103A aborts transmission of the corresponding frame.

After aborting the transmission, the μPD72103A retransmits the frame for which the underrun occurred (auto retransmission).

The "statistical information read acknowledge LSW" can be used to detect the number of underrun occurrences.

When "1" is set to the TXUR bit in the "operation mode setting LCW" command, "data transmission stop LSW" is reported when the number of underrun errors set in RETN occur.

3.4 Data Reception

When the μPD72103A receives a frame, it writes the received data to a receive buffer in external memory. The μPD72103A reports “data reception LSW” as the status information when data has been received.

3.4.1 Reception timing

The reception timing is set as shown below, according to the CLK parameter in the “operation mode setting LCW” command.

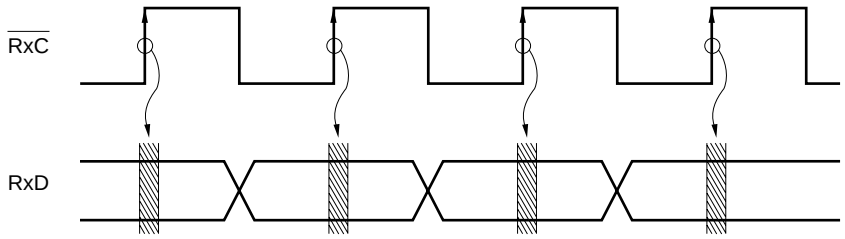
Table 3-1. Reception Timing Mode Settings

CLK parameter setting	Mode	Sampling of receive data from RxD pin
0	Reception timing determined by external receive clock	Sampling at rising edge of $\overline{\text{RxC}}$ pin
1	Reception timing when using DPLL	Sampling at rising edge of DPLL signal

(1) Reception timing determined by external receive clock

Figure 3-3 shows the reception timing when in external clock mode.

Figure 3-3. Reception Timing (External Clock Mode)



(2) Reception timing when using DPLL

Figure 3-4 shows the reception timing in DPLL mode.

The DPLL circuit includes a 4-bit counter (BRC), which counts the source clocks input from the $\overline{\text{RxC}}$ pin (at 16 times the transfer rate). This counter operates as described below.

<1> When the BRC counter value becomes “0”, the DPLL output is set to “L”.

<2> If the state of the RxD pin changes when the BRC counter’s count value N is within the range of 0 < N ≤ 7, the next incrementation of the BRC count is not executed, as shown in Figure 3-4 (b).

<3> When the BRC counter value becomes “8”, the DPLL output is set to “H”.

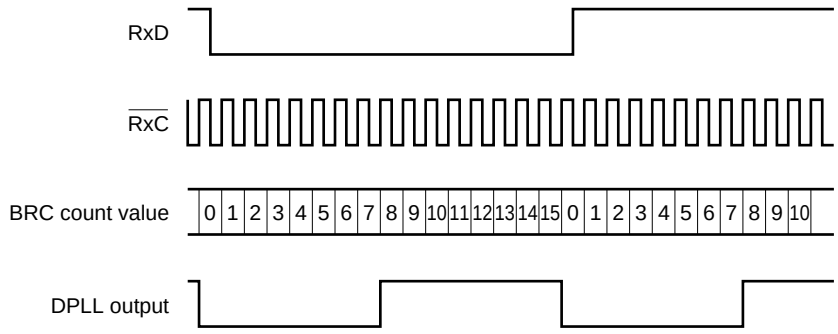
<4> If the status of the RxD pin changes when the BRC counter’s count value N is within the range of 8 ≤ N < 15, the next incrementation of the BRC count is executed as +2, as shown in Figure 3-4 (c).

<5> When the BRC counter’s count value is either 0 or 15, the increment operation does not change even if the status of the RxD pin changes.

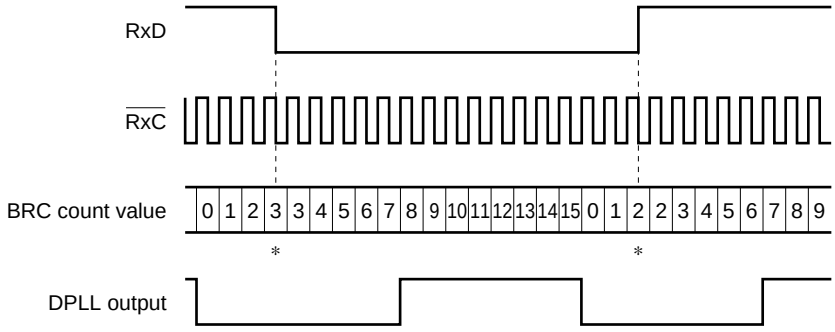
Caution If NRZ has been selected as the data format and if there is no edge information for the received data, such as when the receive data contains a series of zeros and a mark idle is being received, the DPLL's count correction operation may not be performed and a reception error may occur.

Figure 3-4. Reception Timing (DPLL Mode)

(a) Ideal waveform

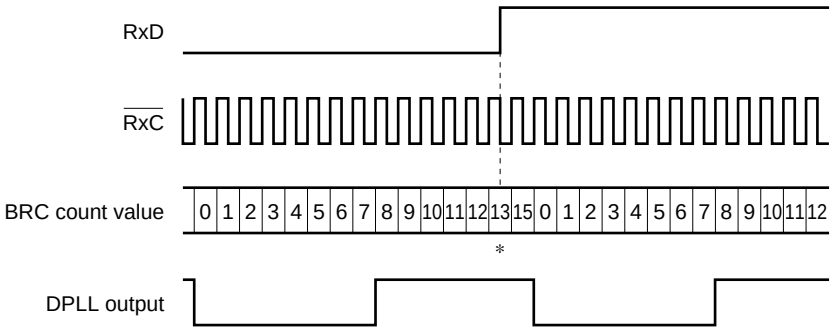


(b) Edge detected in range of 0 < BRC counter value ≤ 7



Remark *: BRC count is not incremented.

(c) Edge detected in range of 8 ≤ BRC counter value < 15



Remark *: The BRC counter count is incremented by two.

3.4.2 Separation of receive data

The μPD72103A is able to separate data in received frames into receive buffer and “data reception LSW” data areas.

The receive data that is separated into “data reception LSW” is specified by the “operation mode setting LCW” command.

When the μPD72103A receives data, it writes data beginning immediately after the start flag and in the amount indicated by “operation mode setting LCW” command to the “data reception LSW” data area.

After the received data is set to the “data reception LSW” data area, it writes the other data to the receive buffer.

3.4.3 Receive buffer chain

The μPD72103A is able to use receive buffer chains.

The receive buffer chain is set up in relation to the receive buffer size set by the “operation mode setting LCW” command.

3.4.4 Address field recognition

The μPD72103A includes a recognition function for data in the address section that immediately follows the start flag.

The data size for which address recognition is enabled is either one byte or two bytes.

The reception addresses are set within the “receive address field setting LCW” command.

All of the address values used during the reception operation are set.

3.4.5 Discarding of abnormal frames

When receiving frames, the μPD72103A discards abnormal frames and does not report a “data reception LSW”.

The “statistical information read acknowledge LSW” can be used to detect the number of abnormal frames that have occurred.

The following are examples of abnormal frames.

- FCS errors
- Overrun errors
- Frames containing a series of seven or more bits with “1” values
- Frames containing fewer bits that the number specified by the SHORT parameter in the “operation mode setting LCW” command
- Frames whose receive buffer size exceeds the size specified by the RXBS parameter in the “operation mode setting LCW” command
- Frames that contain fractional bits when “1” has been set to the OCT parameter in the “operation mode setting LCW” command
- Frames that contain address fields for addresses other than those set by the “receive address field setting LCW” command
- Frames received when there is no empty space in the status table or receive buffer address table

3.4.6 Idle monitor timer

The idle monitor timer is activated when an IDLE = 1 value follows an IDLE = 0 value; in other words, when a mark status is detected.

When this occurs, if the mark status continues, an idle monitor timer timeout status is reported when the idle monitor timer reaches the timeout limit.

After the IDLE value becomes “1” and the idle monitor timer is activated, the idle monitor timer is stopped when the IDLE value becomes “0”. Accordingly, the idle monitor timer cannot be activated or stopped in the following cases.

(i) If the IDLE value is changed from “0” to “1” during the idle detection timing period (8 ms or 100 ms), activation of the idle monitor timer is shifted to the next idle detection timing period.

(ii) Once the idle monitor timer has been activated, if the IDLE value is changed from “1” to “0” during the idle detection timing period, the idle monitor timer is not stopped until an IDLE = 0 condition is detection during the next idle detection timing period.

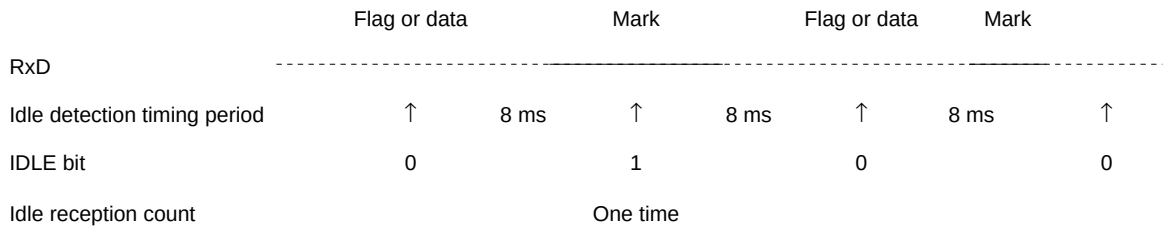
(iii) Once the idle monitor timer has been activated, if the IDLE value is changed from “1” to “0” and then back to “1” during the idle detection timing period, the idle monitor timer is not stopped.

3.4.7 Idle reception count

When mark idle status (15 continuos bits with “1” values) is detected, the μPD72103A sets the IDLE bit to “1”. Once IDLE has been set to “1”, the IDLE bit is set to “0” as soon as a “0” bit value is received.

As shown in Figure 3-5, when the idle detection timer reaches its count-out limit during the idle detection timing period (8 ms or 100 ms), if the IDLE bit value is “1”, it is counted as one idle reception occurrence.

Figure 3-5. Idle Reception Count



3.4.8 Cautions regarding overrun errors

During reception processing by the μPD72103A, any of the following four causes can slow reception DMA processing to the point where an overrun occurs when receiving frames during the processing period, in which case frames are discarded internally.

The principal causes of such overruns are described below.

[Causes]

a. Overruns caused by address search processing

When the AUTO value is set as other than 00H and address recognition is performed, it increases the time between frame reception and activation of reception DMA processing, which can result in overrun errors. Address table values set via the AFST parameter are compared consecutively with receive address field values, and when the two values match reception DMA processing begins. Accordingly, the closer the matching addresses are to the end of the address table, the more likely it is that an overrun error will occur.

b. Overruns caused by status report processing

During the period when a status report is being processed, DMA transfer activation processing for received data is prohibited (this DMA transfer activation processing includes setting receive buffer addresses for the internal DMAC and activating reception DMA channels). Consequently, if the period of status report processing overlaps with the timing period for starting frame reception, reception DMA cannot be activated until the status report processing has been completed. As a result, data accumulates in the reception FIFO and an overrun may occur if the received data exceeds 128 bytes.

c. Overruns caused by reception completion interrupt servicing

During the period of interrupt servicing for frame reception completion, any reception interrupt generated by the next frame is masked and data received during this period is accumulated in reception FIFO. This condition may eventually result in an overrun.

d. Overruns caused by reception buffer chain processing

If the receive buffer is small, increasing the transfer rate relative to the time required for receive buffer DMA activation may cause a large amount of data to be accumulated in the reception FIFO. This condition may eventually result in an overrun.

The following countermeasures are recommended as ways to avoid overrun errors.

[Countermeasures]

- Set a slow transfer rate.
- Use upper-layer software for retransmission processing.
- Use a faster system clock (up to 16 MHz).
- Increase the timer interval between receive operations.
- When using a receive buffer chain, make the receive buffer as large as possible.

Data related to causes a through c above is shown in (1) and (2) below.

The period during which reception DMA processing is prohibited for each cause varies according the parameter settings, etc.

(1) Reception DMA processing prohibit periods for settings corresponding to causes a, b, and c

Cause	Conditions	Setting and reception DMA processing category	Prohibit period [μs]
a	1	AUTO = 00H, STBC = 0	About 16
	2	AUTO = 00H, STBC = 4	About 27
	3	AUTO = 00H, STBC = 8	About 38
	4	AUTO = 01H, STBC = 4, AFST BC = 3	About 27
	5	AUTO = 01H, STBC = 4, AFST BC = 12	About 40
	6	AUTO = 01H, STBC = 8, AFST BC = 3	About 39
	7	AUTO = 01H, STBC = 8, AFST BC = 12	About 52
b	1	If there is no status report	About 17
	2	If there is a SIAK status report	About 70
	3	If there is a SIAF status report	About 31
c	1	If STBC = 0 and there is no receive buffer chain	About 65
	2	If STBC = 4 and there is no receive buffer chain	About 70
	3	If STBC = 8 and there is no receive buffer chain	About 81
	4	If there is a receive buffer chain for any of the above three conditions (number of used receive buffers = N)	(Conditions c1 to c3) + about 13 μs x N

Remarks 1. The time for the MDAK or GPAE status is about the same as for condition b1.

2. The above data was calculated based on a 16-MHz system clock.

3. This does not affect transmission operations.

(2) Upper limits for avoiding overrun errors when causes a, b, and c are combined

Cause			Upper limit (Mbps) for transfer rate to avoid overrun	**Note**
a	b	c		
1	1	1	8.0	35
	2		6.8	–
	3		8.0	67
2	1	2	8.0	46
	2		6.1	–
	3		7.9	78
4	1		8.0	52
	2		6.1	–
	3		7.9	84
5	1		8.0	75
	2		5.6	–
	3		7.2	–
3	1	3	7.5	70
	2		5.4	–
	3		6.8	102
6	1		7.4	76
	2		5.4	–
	3		6.7	108
7	1		6.8	98
	2		5.0	–
	3		6.2	–

Note This column contains frame interval times [μs] required for 2-Mbps communications.
As long as the frame interval time exceeds the above values, cause c will have no effect and 2-Mbps communications will be enabled. A dash (–) in this column indicates that 2-Mbps cannot be implemented.

Remark The above data was calculated based on a 16-MHz system clock and a 1-μs HLDRQ acknowledge time.

3.5 Completion of Transmit/Receive Operation

To stop a data transmit/receive operation, issue the “line close LCW” command.

When this command is issued, the μPD72103A sets “1” for the transmission line and stops the receive operation.

After the μPD72103A receives the “line close LCW” command and stops the data transmit/receive operation, it reports “line close completion LSW” as the current status.

3.6 Transmit and Receive Frame Flags

3.6.1 Transmit frame flags

When the “TFIL = 0” setting has been selected, the μPD72103A inserts at least three flags corresponding to the transmit frame.

Accordingly, even when a series of frames are output to the μPD72103A, three flags are inserted between each frame (it is not possible to insert fewer than three flags).

Since the μPD72103A is not able to control the number of transmit flags at the command level, the host processor’s control of the transmit data write operation can be used (to provide time for writing between frames) in cases where three or more flags must be inserted.

When the “TFIL = 1” setting has been selected, a one-byte end flag is sent after the FCS is added to the transmit frame and marks are sent until a new frame is transmitted.

After the “line open LCW” command has restored transmit mode, the μPD72103A continues to transmit flags or marks unless transmit data from the host processor is being written.

3.6.2 Receive frame flags

The μPD72103A receives frames as normal receive frames if there is at least one flag between the frames. It also receives frames as normal receive frames when the same flag is used as an end flag and start flag.

3.7 General-purpose Input/Output Pins

3.7.1 Detection of changes in general-purpose input pins

The μPD72103A checks the status of the general-purpose input pins (GI1 and GI2) once every 8 ms and detects any changes in their status (high level/low level).

To perform detection such status changes in general-purpose input pins, select “01” or “10” for “operation mode setting LCW” command’s GICS parameter.

When a pin’s level changes from 0 to 1 or 1 to 0 and is retained, the “general-purpose input pin change detection 1 LSW” or the “general-purpose input pin change detection 2 LSW” is reported.

3.7.2 Control of general-purpose output pins

The levels of the μPD72103A’s general-purpose output pins (GO1 and GO2) are controlled by the “general-purpose output pin write LCW” command.

When the μPD72103A receives a “general-purpose output pin write LCW” command issued by the host processor, execution of the LCW causes a change in the status of the general-purpose output pins.

3.7.3 General-purpose input/output pin status

The host processor issues the “general-purpose input/output pin read LCW” command after reading the status of the general-purpose input/output pins.

When the μPD72103A receives the “general-purpose input/output pin read LCW” command, it reports the “general-purpose input/output pin read acknowledge LSW”.

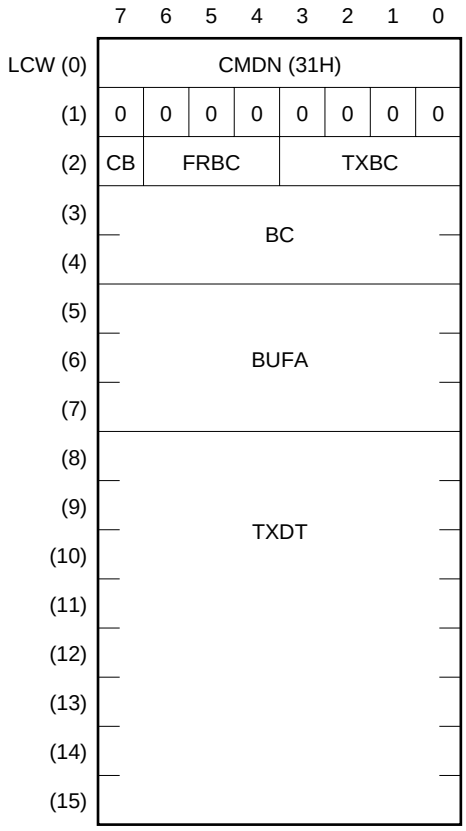
CHAPTER 4 COMMANDS (LCW)

The μPD72103A supports following commands.

Command No. (H)	Symbol	Command name
31	DTSD	Data send
34	MSET	Memory area setting
35	MDST	Operation mode setting
36	AFST	Receive address field setting
37	LOPN	Line open
38	LCLS	Line close
3A	MARD	Memory area read
3B	MDRD	Operation mode read
3C	AFRD	Receive address field read
3D	SIRD	Statistical information read
41	GOWR	General-purpose output pin write
42	GPRD	General-purpose input/output pin read
44	SIRE	Statistical information read 2
45	GPRE	General-purpose input/output pin read 2
46	MDSE	Operation mode setting 2
47	AFSE	Receive address field setting 2

Command name	Data transmission	Symbol	DTSD

Field definitions



Function

This command is used to transmit data that has been set to a command or has been stored in the transmit buffer.

Description of parameters

1. TXBC : Transmit data byte count (set within command)
   This parameter sets the number of transmit data bytes to be set within this command.
   The number of transmit data bytes can be set as 0 to 8 bytes.
   When there are more than eight bytes of transmit data, the data is set to the transmit buffer.

2. FRBC : Fractional bit count
   This sets the number of fractional bits. FRBC can be set as 0 to 7 bits.
   In the transmit data, the valid bit length is the FRBC value counted from the LSB of the last byte.

3. BC : Transmit data byte count
   This indicates the number of bytes of transmit data that are stored in the transmit buffer.
   BC can be set as 0 to 16 Kbytes (0H to 3FFFH).

4. BUFA : Transmit buffer start address
   This indicates the transmit buffer's start address.

5. CB : Transmit chain specification
   This selects the transmit buffer chain function.

   0 = No transmit buffer chain
   1 = Transmit buffer chain

6. TXDT : Transmit data
   This is the transmit data buffer that is set within the CMDN field.

Operations using μPD72103A

1. When BUFE = 0 in "operation mode setting LCW" command (mode is not transmit buffer chain mode)

(1) When TXBC = 0
This setting transmits data (having a byte count set by BC) that is stored in the transmit buffer having the start address set by BUFA.
However, when FRBC ≠ 0, the transmit data corresponds to the FRBC bit at (BC – 1) bytes plus BC bytes.

(2) When TXBC ≠ 0 and BC = 0
This setting sends the number of data bytes specified for TXBC, which have been set to TXDT.
However, when FRBC ≠ 0, the transmit data corresponds to the FRBC bit at (TXBC – 1) bytes plus TXBC bytes.

(3) When TXBC ≠ 0 and BC ≠ 0
This setting sends data (having the number of data bytes specified for TXBC) which has been set to TXDT as well as data (having a byte count set by BC) that is stored in the transmit buffer having the start address set by BUFA.
However, when FRBC ≠ 0, the transmit data corresponds to the FRBC bit at (BC – 1) bytes plus BC bytes.

2. When BUFE = 1 in "operation mode setting LCW" command (mode is transmit buffer chain mode)

(1) When first CB = 0 and TXBC = 0 (transmit buffer chain is not specified)
This setting transmits data (having a byte count set by BC) that is stored in the transmit buffer having the start address set by the first BUFA.
However, when FRBC ≠ 0, the transmit data corresponds to the FRBC bit at (BC – 1) bytes plus BC bytes.

(2) When first CB = 0, TXBC ≠ 0, and BC = 0 (transmit buffer chain is not specified)
This setting sends the number of data bytes specified for the TXBC, which have been set to the first TXDT.
However, when FRBC ≠ 0, the transmit data corresponds to the FRBC bit at (BC – 1) bytes plus BC bytes.

(3) When first CB = 0, TXBC ≠ 0, and BC ≠ 0 (transmit buffer chain is not specified)
This setting sends data (having the number of data bytes specified for TXBC) which has been set to the first TXDT as well as data (having a byte count set by BC) that is stored in the transmit buffer having the start address set by BUFA.
However, when FRBC ≠ 0, the transmit data corresponds to the FRBC bit at (BC – 1) bytes plus BC bytes.

(4) When the CB that is n – 1 from the first CB = 1, the nth CB = 0, TXBC = 0, and BC ≠ 0 (transmit buffer chain is specified)

This setting sends data (having a byte count set by BC) that is stored in the transmit buffer having the start address set by the first BUFA, data (having a byte count set by BC) that is stored in the transmit buffer having the start address set by the second BUFA, and data (having a byte count set by BC) that is stored in the transmit buffer having the start address set by the (n – 1) + nth BUFA.

However, when FRBC ≠ 0, the transmit data corresponds to the FRBC bit at (BC – 1) bytes plus BC bytes.

(5) When the CB that is n – 1 from the first CB = 1, the nth CB = 0, the first TXBC ≠ 0, the second TXBC = 0, and BC ≠ 0 (transmit buffer chain is specified)

This setting sends the number of data bytes specified for the TXBC, which have been set to the first TXDT, data (having a byte count set by BC) that is stored in the transmit buffer having the start address set by BUFA, data (having a byte count set by BC) that is stored in the transmit buffer having the start address set by the second BUFA, and data (having a byte count set by BC) that is stored in the transmit buffer having the start address set by the (n – 1) + nth BUFA.

However, when FRBC ≠ 0, the transmit data corresponds to the FRBC bit at (BC – 1) bytes plus BC bytes.

Transmit data cannot be set corresponding to the second and subsequent TXDTs.

3. End of transmission

(1) Normal end

When "1" is set to the TXED bit in the "operation mode setting LCW" command, "data transmission completion LSW" is reported.

(2) Abnormal end

When "1" is set to the TXUR bit in the "operation mode setting LCW" command, "data transmission stop LSW" is reported.

Cautions 1. FRBC is valid regardless of the OCT value set by "operation mode setting LCW" command.

2. CB is valid when BUFE = 1 has been set by "operation mode setting LCW" command.

3. When there are N (2 ≤ N ≤ NLCW) "data transmission LCW" commands in the transmit buffer chain, TXBC is valid for the first "data transmission LCW" command. In addition, FRBC is valid for the Nth "data transmission LCW" command. This setting cannot be made under any other conditions.

4. When using transmit buffer chains, "data transmission LCW" commands are set in the sequence "n → (n – 1) → ... first "data transmission LCW" command.

5. When using a transmit buffer chain, set "1" to the CB that is (n – 1) from the first CB and set "0" to the nth CB.

6. When RETN (a parameter in the "operation mode setting LCW" command) is 0, the μPD72103A continually executes the data send command (CMDS is not set to FEH) until the frame transmission is completed.

7. Be sure to set the transmission baud rate to a value greater than 0 bps. If a transmission baud rate of zero is set, the μPD72103A continually executes the data send command until a hang-up occurs.

Command name Memory area setting **Symbol** MSET

Field definitions

	7	6	5	4	3	2	1	0
LCW (0)	CMDN (34H)							
(1)	0	0	0	0	0	0	0	0
(2)						(L)		
(3)		ADDR				(M)		
(4)						(H)		
(5)	NLCW							
(6)	NLSW							
(7)	NLRBW							

Function

This command is used to set the command table, status table, and receive buffer address table.

Description of parameters

1. ADDR : Start address of command table
   This specifies the command table's start address.

2. NLCW : Number of command table blocks
   This specifies the number of command table blocks.
   The specifiable range for NLCW is 1 to 128 (exponent of two) blocks. Each block consists of 16 bytes.

3. NLSW : Number of status table blocks
   This specifies the number of status table blocks.
   The specifiable range for NLSW is 1 to 128 (exponent of two) blocks. Each block consists of 16 bytes.

4. NLRBW : Number of receive buffer address table blocks
   This specifies the number of receive buffer address table blocks. Each block consists of 4 bytes.
   The specifiable range for NLRBW is 1 to 128 (exponent of two) blocks.

Caution Set the low-order four bits of ADDR to "0".

Command name	Operation mode setting	Symbol	MDST

Field definitions

	7	6	5	4	3	2	1	0
LCW (0)	CMDN (35H)							
(1)	0	0	0	0	0	0	0	0
(2)	FCS	TFIL	CODE	CLK	DMAW		DMAB	CPU
(3)	LOOP		STEP	OCT	SHORT		AUTO	
(4)	0	LAPD	BUFE	BUFC	GICS		TXED	LOAK
(5)	0	0	0	0	STBC			
(6)	TIME							
(7)	RXBS							
(8)								
(9)	MAXD							
(10)								
(11)	HOLD							
(12)	TXUR	RETN						

Function

This command sets the operation mode.

Issue this command when the system is in idle mode.

Description of parameters

1. CPU : Host processor type

This sets the address type according to the host processor type.

The default value is “0”.

0 This is the default value. It sets the address type for NEC and Intel CPUs.

1 This sets the address type for Motorola CPUs.

Cautions 1. NEC/Intel type : this type assigns low-order data to low-order memory addresses

Motorola type : this type assigns low-order data to high-order memory addresses

2. Appendix B includes caution points concerning use of a Motorola CPU with the μPD72103A.

2. DMAB : DMA block transfer

This specifies the number of transfer bytes per data block controlled by the on-chip DMA controller.

The default value is “0”.

0 Sets transfer of four bytes per block

1 Sets transfer of eight bytes per block

3. DMAW : Number of DMA wait cycles
This specifies the number of wait cycles used by the on-chip DMA controller.
The default value is “11”.

00 No wait cycles are inserted
01 1 wait cycle is inserted
10 2 wait cycles are inserted
11 3 wait cycles are inserted

4. CLK : Transmit/receive clock
This selects input pins for the transmit and receive clocks.
The default value is “0”.

0 The transmit clock is input via the $\overline{TxC}$ pin and the receive clock is input via the $\overline{RxC}$ pin.
(When not using DPLL)
1 The transmit and receive clocks are the clock input via the $\overline{RxC}$ pin divided by 16.
(When using DPLL)

5. CODE : Coding
This selects the data format code for transmit and receive data.

0 Selects NRZ mode
If the RxD pin’s input level is “H”, the data value is “1”. If it is “L”, the data value is “0”.
1 Selects NRZI mode
If the RxD pin’s input level is inverted, the data value is “0”. If it does not change, the data value is “1”.

6. TFIL : Transmission time file
During transmission, this selects transmission of flags or marks.
The default value is “0”.

0 Selects transmission of flags
At least one flag is inserted between a frame’s end flag and the next frame’s start flag.
1 Selects transmission of marks
Marks for at least one bit are inserted between a frame’s end flag and the next frame’s start flag.

7. FCS : Number of bits in the FCS field
This specifies the number of bits in the FCS generating polynomial.
The default value is “0”.

0 Selects a 16-bit generating polynomial (FCS = 2 bytes).
The generating expression is ITU-T (formerly CCITT) $X^{16} + X^{12} + X^5 + 1$.
1 Selects a 32-bit generating polynomial (FCS = 4 bytes).
The generating expression is ITU-T (formerly CCITT) $X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X^1 + 1$.

8. AUTO : Address field detection

This detects the address field during receive operations. Either one-byte or two-byte detection can be selected.

When AUTO is specified, the receive operations use the receive data at the address specified by the receive address field setting command or the receive data at a global address.

The default value is “00”.

- 00 No address recognition for the receive data
- 01 Recognizes one byte of data immediately after the receive data’s leading flag and recognizes a one-byte address at the address specified by the receive field setting command
- 10 Recognizes the address corresponding to the second byte of the two bytes of data immediately after the receive data’s leading flag
- 11 Recognizes two bytes of data immediately after the receive data’s leading flag and recognizes the address specified by the receive field setting command

9. SHORT : Short frame detection

This specifies the number of bits for short frame detection.

A short frame is defined as when the number of bits between two flags or between a flag and an abort pattern is equal to or less than the number of bits set by this parameter.

The FCS field is not included among the bits detected under the SHORT parameter setting.

The default value is “00”.

- 00 Frame having less than 2 bytes
- 01 Frame having less than 3 bytes
- 10 Frame having less than 4 bytes
- 11 Illegal command is reported (previous setting remains valid)

10. OCT : Fractional bit frame

This specifies fractional bit frame receive operations. In this case, a fractional bit frame is any frame other than one in which one byte of data consists of exactly eight bits.

The default value is “0”.

- 0 Receive
- 1 Do not receive

11. STEP : Timer step value

This specifies the timer step time for the idle monitor timer.

This parameter is used with the TIME bit.

The idle monitor timer recognizes an idle status as when at least 15 consecutive “1” bits are received.

The TIME bit is incremented when an idle status exists during the step time period specified by the STEP parameter.

The default value is “0” (when system clock = 8 MHz).

- 0 Time step = 100 ms
- 1 Time step = 8 ms

The step value when the system clock is X MHz is as follows.

$$\text{STEP} = 0 \qquad 100 \text{ ms} \times \frac{8}{X}$$

$$\text{STEP} = 1 \qquad 8 \text{ ms} \times \frac{8}{X}$$

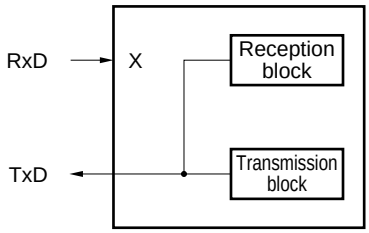
12. LOOP : Loopback mode

This specifies one of the following connection modes for the μPD72103A's internal connection between the transmission and reception blocks.

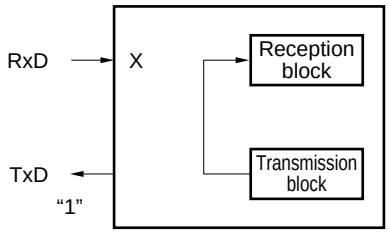
This is used for auto loopback testing, external loopback, etc.

The default value is "00".

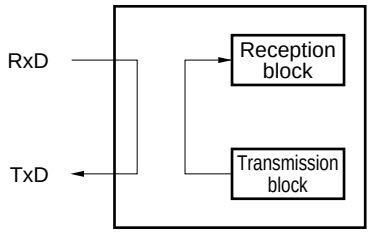
00 Transmit and receive lines have independent modes
01 Loopback mode 1
10 Loopback mode 2
11 Loopback mode 3



Loopback mode 1



Loopback mode 2



Loopback mode 3

13. STBC : Number of receive data bytes (for receive status)
This specifies the number of bytes of receive data that is captured in the status.
The specifiable range of values for the STBC parameter varies depending on the AUTO and SHORT parameter settings. These specifiable ranges are listed below.

Setting		Range for STBC
AUTO	SHORT	
00	00	STBC = 0 or 2 ≤ STBC ≤ 8
00	01	STBC = 0 or 3 ≤ STBC ≤ 8
00	10	STBC = 0 or 4 ≤ STBC ≤ 8
01/10/11	00	2 ≤ STBC ≤ 8
01/10/11	01	3 ≤ STBC ≤ 8
01/10/11	10	4 ≤ STBC ≤ 8

14. LOAK : Line open report timing
This specifies the timing of the “line open completion LSW” report.
The default value is “0”.

0 When flag has been transmitted from local terminal
1 When flag has been received from remote terminal

15. TXED : Enable/disable transmission completion report
This specifies whether or not to output a “data transmission completion LSW”.
The default value is “0”.

0 Do not output report
1 Output report

16. GICS : General-purpose input pin change report
This specifies output of the “general-purpose input pin change detection 1 LSW and the “general-purpose input pin change detection 2 LSW”.
The default value is “00”.

00 No report
01 Reports “general-purpose input pin change detection 1 LSW”
10 Reports “general-purpose input pin change detection 1 LSW” and “general-purpose input pin change detection 2 LSW”

Caution “11” is a “Don’t care” setting.

17. TIME : Timer value
This specifies the number of times that idle status is detected.
The idle status is detected based on the step time set via the STEP parameter. When an idle status is detected, this timer is incremented. The specifiable range of TIME settings is 0 to 255.
The idle status is not detected when TIME = 0.

18. RXBS : Receive buffer size

This specifies the size of the receive buffer.

The specifiable range for RXBS is 0 to 16383 (0H to 3FFFH).

19. BUFC : Select receive buffer chain

This specifies the receive buffer chain function. The default value is “0”.

0 Do not use chain function
1 Use chain function

Caution When using the receive buffer chain function, some time is required for processing a change of receive buffer addresses. Consequently, an overrun error may occur when the receive buffer size is small and the transfer rate is fast. For details, see “3.4.8 Cautions regarding overrun errors”.

20. BUFE : Select transmit chain

This specifies the transmit buffer chain function. The default value is “0”.

0 Do not use chain function
1 Use chain function

21. LAPD : LAPD mode

This specifies communication control (in LAPD mode) via the GI2 and GO3 pins. The default value is “0”.

0 No transmission control via GI2 and GO3 pins
1 Transmission control via GI2 and GO3 pins (LAPD mode)

When LAPD mode has been selected, the GO3 pin is used for the frame transmission request signal and the GI2 pin is used for the frame transmission enable signal. The operations of these pins during LAPD mode are described below.

(1) GO3 pin

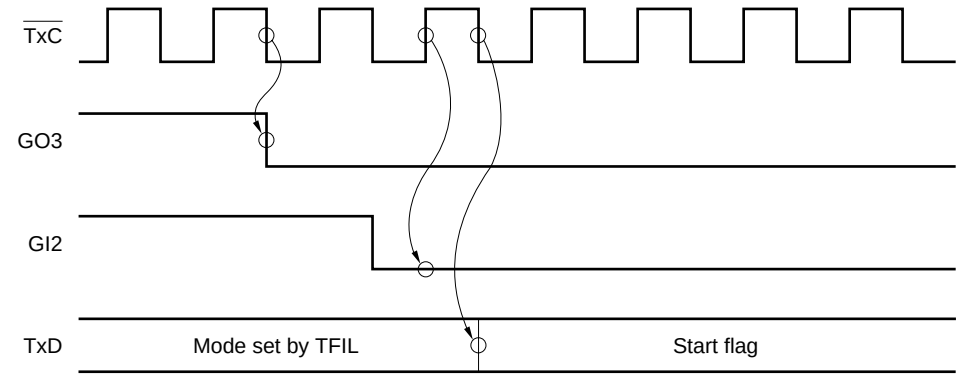
When a transmit command is fetched and the transmit data is written to the transmit FIFO, this pin goes to “L” level and a transmit request is sent to an external circuit. When the external circuit causes the GI2 pin to go to “L” level, frame transmission begins. After the end flag is transmitted, it returns to “H” level.

(2) GI2 pin

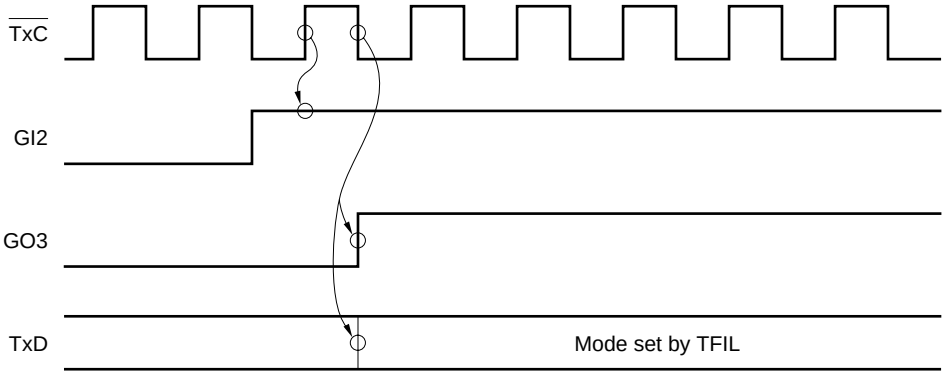
When the GO3 pin goes to “L” level, the μPD72103A samples this pin and, if it is at “L” level, frame transmission begins. During frame transmission, if this pin returns to “H” level frame transmission is stopped and the TxD pin is set to the mode specified by TFIL.

The operation timing of the GI2 and GO3 pins is described below.

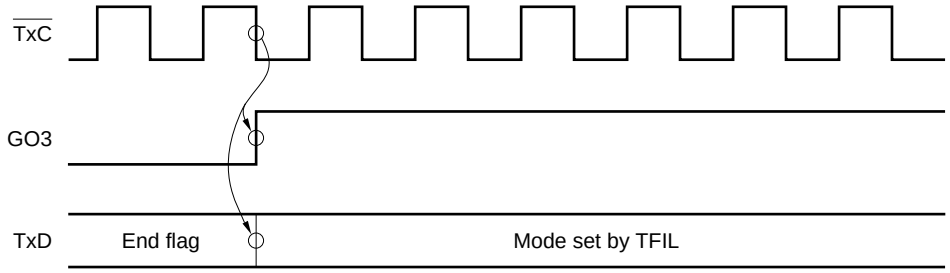
(a) Frame transmission



(b) Frame transmission stop



(c) Frame transmission end



22. MAXD : Maximum bytes of receive data

This specifies the maximum number of receive data bytes.
MAXD values can be specified in the range of 0 to 16383.
The MAXD setting is valid when BUFC = 1.
Be sure that MAXD ≤ RXBS x (NLRBW[Note] – 4).

Note NLRBW is a parameter of the "memory area setting LCW" command. Be sure to set a value of 8 or greater to make MAXD valid.

23. HOLD : Transmission wait time

This sets the time between the setting of data to the transmit FIFO and the start of data transmission from TxD.
The default value is "00".
HOLD values can be specified in the range of 0 to 255. A value of "1" is approximately equal to 4 μs.
This parameter is not related to the TFIL parameter. No matter how long a wait time is set by this parameter, the number of start flags remains just one (TFIL = 1).

24. RETN : Number of retries

This specifies the number of retries when attempting to execute the "data transmission LCW" command after an underrun occurs. The RETN value – 1 becomes the maximum number of "data transmission LCW" command execution retries.
RETN values can be specified in the range of 0 to 127. When set to "0", the "data transmission LCW" command is issued until a normal end occurs.

25. TXUR : Transmit underrun report

This specifies whether or not to report the "data transmission stop LSW". The default value is "0".

0 Do not report
1 Report

Command name Receive address field setting **Symbol** AFST

Field definitions

	7	6	5	4	3	2	1	0
LCW (0)	CMDN (36H)							
(1)	0	0	0	0	0	0	0	0
(2)	0	0	0	0	BC			
(3)	AF							
(4)								
(5)								
(6)								
(7)								
(8)								
(9)								
(10)								
(11)								
(12)								
(13)								
(14)								

Function

This command is used to set address fields for receive frames. It is valid when AUTO has been set for the operation mode setting command.

Description of parameters

1. BC : Number of receive address fields

   This specifies the number of address fields to be received. The number of address fields is determined according to the “operation mode setting LCW” command settings.

   When AUTO = 01 or 10 : $1 \leq BC \leq 12$

   When AUTO = 11 : BC = 2, 4, 6, 8, 10, 12

2. AF : Address field

   This sets the address field.

   When AUTO = 01 or 10 has been specified, the first or second byte’s address is set to LCW (3) to (14).

   When AUTO = 11 has been specified, the first byte’s address is set to LCW (3) and the second byte’s address is set to LCW (4) as a two-byte combination.

Operations using μPD72103A

1. When AUTO = 01 or 10

For the address set by AF, the address values for the number of fields specified by BC are compared to one byte in the receive data's address field.

If the address set by AF matches the receive data, the receive operation begins.

Example: When BC = 4, the receive operation begins if the received address matches the address set to LCW (3), LCW (4), LCW (5), or LCW (6).

2. When AUTO = 11

For the two-byte address unit set by AF, the address values for the number of fields specified by BC are compared to two bytes in the receive data's address field.

If the address set by AF matches the receive data, the receive operation begins.

Example: When BC = 6, the receive operation begins if the first and second bytes of the received address matches either the address set to LCW (3) and LCW (4) or LCW (5) and LCW (6).

Caution FFH is set in the AF field when reception using a global address (FFH) is required.

Command name Line open **Symbol** LOPN

Field definitions

	7	6	5	4	3	2	1	0
LCW (0)	CMDN (37H)							
LCW (1)	0	0	0	0	0	0	0	0

Function

This command is used to start data transmission or reception.

Operations using μPD72103A

The operation varies according to the TFIL setting for the “operation mode setting LCW” command.

1. **When TFIL = 0 (flag)**

   The TxD pin is set to flag transmit mode.

   The “line open completion LSW” is reported when a flag is sent from a local terminal or when a flag is received from a remote terminal based on the LOAK setting.

2. **When TFIL = 1 (mark)**

   The TxD pin is set to mark transmit mode (data value = “1”).

Command name	Line close	Symbol	LCLS

Field definitions

	7	6	5	4	3	2	1	0
LCW (0)	CMDN (38H)							
LCW (1)	0	0	0	0	0	0	0	0

Function

This command is used to stop data transmission or reception.

Operations using μPD72103A

After this command is issued, the TxD pin goes to high level.

This command also stops any receive operation for input data received via the RxD pin.

The “line close completion LSW” is reported when this command is issued.

Command name Memory area read **Symbol** MARD

Field definitions

	7	6	5	4	3	2	1	0
LCW (0)	CMDN (3AH)							
(1)	0	0	0	0	0	0	0	0

Function

This command is issued when reading various parameters set for the “memory area setting LCW” command.

Operations using μPD72103A

The “memory area read acknowledge LSW” is reported when this command is issued.

Command name Operation mode read **Symbol** MDRD

Field definitions

	7	6	5	4	3	2	1	0
LCW (0)	CMDN (3BH)							
(1)	0	0	0	0	0	0	0	0

Function

This command is issued when reading various parameters set for the “operation mode setting LCW” command.

Operations using μPD72103A

The “operation mode read acknowledge LSW” is reported when this command is issued.

Command name	**Receive address field read**	**Symbol**	**AFRD**

Field definitions

	7	6	5	4	3	2	1	0
LCW (0)	CMDN (3CH)							
(1)	0	0	0	0	0	0	0	0

Function

This command is used when reading parameters set for the “receive address field setting LCW” command.

Operations using μPD72103A

The “receive address field read acknowledge LSW” is reported when this command is issued.

Command name	Statistical information read	Symbol	SIRD

Field definitions

	7	6	5	4	3	2	1	0
LCW (0)	CMDN (3DH)							
(1)	0	0	0	0	0	0	0	0

Function

This command is issued when reading various types of statistical information[Note].

Note All statistical information read by this command is error information.

Operations using μPD72103A

The “statistical information read acknowledge LSW” is reported when this command is issued.

Command name General-purpose output pin write **Symbol** GOWR

Field definitions

	7	6	5	4	3	2	1	0
LCW (0)	CMDN (41H)							
(1)	0	0	0	0	0	0	0	0
(2)	0	0	0	0	0	0	GO2F	GO1F

Function

This command is issued to change the level of general-purpose output pins GO1 and GO2.

Description of parameters

1. GO1F : Status of GO1 pin
   This changes the output level of the GO1 pin.

GO1F bit	GO1 pin
0	L
1	H

2. GO2F : Status of GO2 pin
   This changes the output level of the GO2 pin.

GO2F bit	GO2 pin
0	L
1	H

Caution The level of each general-purpose output pin is set to “H” after reset.

Command name	General-purpose input/output pin read	Symbol	GPRD

Field definitions

	7	6	5	4	3	2	1	0
LCW (0)	CMDN (42H)							
(1)	0	0	0	0	0	0	0	0

Function

This command is issued to read the levels of general-purpose input pins GI1 and GI2 as well as general-purpose output pins GO1 and GO2.

Operations using μPD72103A

The “general-purpose input/output pin read acknowledge LSW” is reported when this command is issued.

Caution The general-purpose input/output values that are read are detected at an 8-ms interval.

Command name	Statistical information read 2	Symbol	SIRE

Field definitions

	7	6	5	4	3	2	1	0
LCW (0)	CMDN (44H)							
(1)	0	0	0	0	0	0	0	0
(2)	SIN0							
(3)	SIN1							

Function

This command is issued when reading various types of statistical information[Note].

Note All statistical information read by this command is error information.

Description of parameters

1. SIN0, SIN1 : Statistical information number

   This set the statistical information number to be read.

   Set FFH for SIN1 to read all statistical information as one type.

   00H Overrun count
   01H Underrun count
   02H Idle receive count
   03H Short frame receive count
   04H Address field error frame receive count
   05H Long frame receive count
   06H Abort frame receive count
   07H FCS error frame receive count
   08H Fractional bit frame receive count
   09H Status table overflow count
   0AH Receive buffer address table overflow count

Operations using μPD72103A

The “statistical information read acknowledge 2 LSW” is reported when this command is issued.

Command name	General-purpose input/output pin read 2	Symbol	GPRE

Field definitions

	7	6	5	4	3	2	1	0
LCW (0)	CMDN (45H)							
(1)	0	0	0	0	0	0	0	0

Function

This command is issued to read the levels of general-purpose input pins GI1 and GI2 as well as that of general-purpose output pins GO1 and GO2.

Operations using μPD72103A

The “general-purpose input/output pin read acknowledge 2 LSW” is reported when this command is issued.

Caution The input/output pin modes which are read are those used in the status report.

Command name Operation mode setting 2 **Symbol** MDSE

Field definitions

	7	6	5	4	3	2	1	0
LCW (0)	CMDN (46H)							
(1)	0	0	0	0	0	0	0	0
(2)	0	0	GICS		SHORT		AUTO	

Function

This command sets the operation mode. It is issued to change the operation mode when line open mode has been set.

Issuing this command does not affect the internal status. However, data received when this command is issued is not guaranteed.

Description of parameters

1. AUTO : Address field detection

   This detects the address field during receive operations.

   00 No address recognition for the receive data
   01 Recognizes address for first byte
   10 Recognizes address for second byte
   11 Recognizes addresses for first and second bytes

   Caution If AUTO has been set to any value other than 00, be sure to use the AFSE command to set addresses.

2. SHORT : Number of bits for short frame detection

   This specifies the number of bits for short frame detection during a receive operation.
   The FCS field is not included among the bits detected under the SHORT parameter setting.

   00 Less than 2 bytes
   01 Less than 3 bytes
   10 Less than 4 bytes

3. GICS : General-purpose input pin change detection

   This specifies output of the “general-purpose input pin change detection 1 LSW” and the “general-purpose input pin change detection 2 LSW”.

   00 No report
   01 Reports “general-purpose input pin change detection 1 LSW”
   10 Reports “general-purpose input pin change detection 1 LSW” and “general-purpose input pin change detection 2 LSW”

Command name	**Receive address field setting 2**	**Symbol**	**AFSE**

Field definitions

	7	6	5	4	3	2	1	0
LCW (0)	CMDN (47H)							
(1)	0	0	0	0	0	0	0	0
(2)	0	0	0	0	BC			
(3)	AF							
(4)								
(5)								
(6)								
(7)								
(8)								
(9)								
(10)								
(11)								
(12)								
(13)								
(14)								

Function

This command is used to set address fields for receive frames.
This command is issued when AUTO = 01, 10, or 11 has been set for “operation mode setting 2 LCW” command and the receive address field is changed in line open status.
Issuing this command does not affect the internal status. However, data that is received (or being received) when this command is issued is not guaranteed.

Description of parameters

1. BC : Number of receive address fields
   This specifies the number of address fields to be received. The number of address fields is determined according to the “operation mode setting LCW” command settings.

   When AUTO = 01 or 10 : $1 \leq BC \leq 12$
   When AUTO = 11 : BC = 2, 4, 6, 8, 10, 12

2. AF : Address field
   This sets the address field.
   When AUTO = 01 or 10 has been specified, the first or second byte’s address is set to LCW (3) to (14).
   When AUTO = 11 has been specified, the first byte’s address is set to LCW (3) and the second byte’s address is set to LCW (4) as a two-byte combination.

Operations using μPD72103A

1. When AUTO = 01 or 10

For the address set by AF, the address values for the number of fields specified by BC are compared to one byte in the receive data's address field.

If the address set by AF matches the receive data, the receive operation begins.

Example: When BC = 4, the receive operation begins if the received address matches the address set to LCW (3), LCW (4), LCW (5), or LCW (6).

2. When AUTO = 11

For the two-byte address unit set by AF, the address values for the number of fields specified by BC are compared to two bytes in the receive data's address field.

If the address set by AF matches the receive data, the receive operation begins.

Example: When BC = 6, the receive operation begins if the first and second bytes of the received address matches either the address set to LCW (3) and LCW (4) or LCW (5) and LCW (6).

Caution FFH is set in the AF field when reception using a global address (FFH) is required.

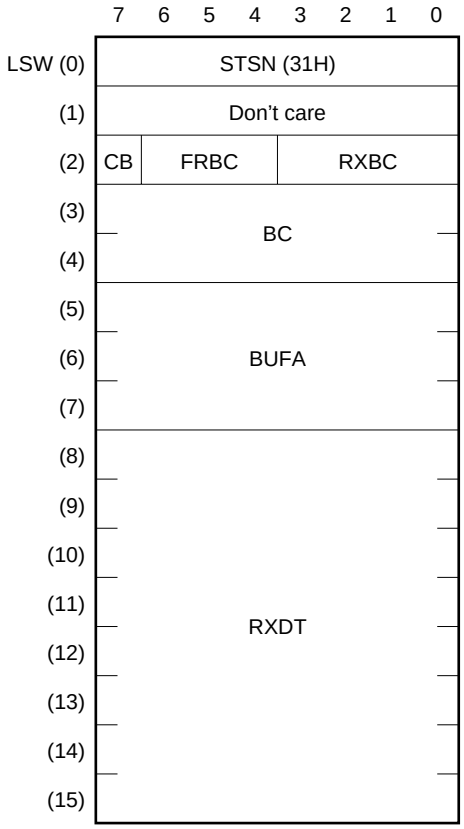
CHAPTER 5 STATUS (LSW)

The μPD72103A uses the status listed below.

Status No. (H)	Symbol	Status name
31	DTRV	Data receive
32	TXUR	Data transmission stop
33	TOUT	Idle monitor timer timeout
37	LOAK	Line open completion
38	LCAK	Line close completion
39	TXED	Data transmission completion
3A	MAAK	Memory area read acknowledge
3B	MDAK	Operation mode read acknowledge
3C	AFAK	Receive address field read acknowledge
3D	SIAK	Statistical information read acknowledge
3F	CILG	Command illegal
40	GI1C	General-purpose input pin change detection 1
41	GI2C	General-purpose input pin change detection 2
42	GPAK	General-purpose input/output pin read acknowledge
43	OLSW	Status table overflow
44	SIAF	Statistical information read acknowledge 2
45	GPAE	General-purpose input/output pin read acknowledge 2

Status name	Data receive	Symbol	DTRV

Field definitions



Report cause(s)

This status is reported when data is received.

Description of parameters

1. RXBC : Receive data byte count (set within status)
   This parameter sets the number of receive data bytes to be set within this status.
   The number of receive data bytes can be set as 0 to 8 bytes.
   When there are more than eight bytes of receive data, the data must be set to the receive buffer.

2. FRBC : Fractional bit count
   This sets the number of fractional bits. The value reported as FRBC can be set as 0 to 7.
   In the receive data at the BC value, the valid bit length is the FRBC value counted from the LSB of the last byte.

3. BC : Receive data byte count
   This indicates the number of bytes of receive data that are stored in the receive buffer.
   BC can be set as 0 to 16 Kbytes (0H to 3FFFH).

4. CB : Receive chain specification
   This selects the receive buffer chain function.

   0 = No receive buffer chain
   1 = Receive buffer chain

5. BUFA : Receive buffer start address
   This indicates the receive buffer's start address.

6. RXDT : Receive data
   This is the receive data buffer that is set within the DTRV field.

Operations using μPD72103A

The "data reception LSW" is set to one of the following modes according to the STBC parameter setting in "operation mode setting LCW" command.

A. When STBC = 0

(i) When receive data size ≤ RXBS
This setting writes data (having a byte count set by BC) that is stored in the receive buffer having a start address specified by BUFA.
However, when FRBC ≠ 0, the receive data corresponds to the FRBC bit at (BC – 1) plus BC bytes.

(ii) RXBS < receive data size ≤ MAXD
When BUFC = 1 has been set, data (having a byte count set by BC) is write via a receive buffer chain from the receive buffer having the start address specified by BUFA.
However, when FRBC ≠ 0, the receive data corresponds to the FRBC bit at (BC – 1) plus BC bytes.
When BUFC = 0, the corresponding frames are discarded internally.

B. When STBC ≠ 0

(i) When receive data size ≤ STBC
Data having a byte count set by RXBC is written to the status.
When FRBC ≠ 0, the receive data corresponds to the FRBC bit at (BC – 1) plus BC bytes.

(ii) When receive data size ≤ RXBS + STBC
Data having a byte count set by STBC is written to the status, and data having a byte count set by BC is written to the receive buffer having the start address specified by BUFA.
However, when FRBC ≠ 0, the receive data corresponds to the FRBC bit at (BC – 1) plus BC bytes.

(iii) When RXBS + STBC < receive data size ≤ MAXD + STBC
When BUFC has been set to "1", the receive buffer having the start address specified by BUFA is chained and data (having a byte count set by BC) is written.
However, when FRBC ≠ 0, the receive data corresponds to the FRBC bit at (BC – 1) plus BC bytes.
When BUFC = 0, the corresponding frames are discarded internally.

Caution When CB = 1, BUFA is the start address of the first chained receive buffer.

Status name	Data transmission stop	Symbol	TXUR

Field definitions

	7	6	5	4	3	2	1	0
LSW (0)	STSN (32H)							
(1)	TXUR							

Report cause(s)

This status is reported when the “operation mode setting LCW” command’s TXUR parameter has been set to “1”.

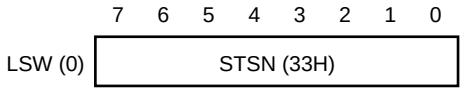
It indicates that the “data transmission LCW” command ended due to an underrun status.

Description of parameters

1. TXUR : Number of transmission underruns
   This indicates the number of “data transmission LCW” commands that have been stopped.

Status name	Idle monitor timer timeout	Symbol	TOUT

Field definitions



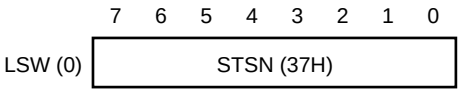
Report cause(s)

This status is reported when the “operation mode setting LCW” command’s TIME parameter ≠ 0 and a idle monitor timer timeout has occurred.

Caution This status is reported when data transmission is enabled.

Status name	Line open completion	Symbol	LOAK

Field definitions



Report cause(s)

This status is reported when the “line open LCW” command has been executed.

This status is reported when the “operation mode setting LCW” command’s TFIL parameter is set for flag transmission and while idle mode or flag reception standby mode has been set.

Status name	Line close completion	Symbol	LCAK

Field definitions

	7	6	5	4	3	2	1	0
LSW (0)	STSN (38H)							

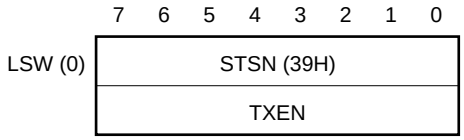
Report cause(s)

This status is reported when the “line close LCW” command has been executed.

Caution This status is reported when flag reception standby mode or data transmission enable mode has been set.

Status name	Data transmission completion	Symbol	TXED

Field definitions



Report cause(s)

This status is reported when the “operation mode setting LCW” command’s TXED parameter has been set to 1 and data transmission via the “data transmission LCW” command has been completed.

Description of parameters

1. TXEN = Number of frames whose transmission has been completed
   This indicates the number of frames that were transmitted during the period between the previous report and this report.

   Caution This status is reported when data transmission enable mode has been set.

Status name	Memory area read acknowledge	Symbol	MAAK

Field definitions

	7	6	5	4	3	2	1	0
LSW (0)	STSN (3AH)							
(1)	Don't care							
(2)	ADDR							
(3)								
(4)								
(5)	NLCW							
(6)	NLSW							
(7)	NLRBW							
(8)	Don't care							
(9)	ROM version							

Report cause(s)

This status is reported when the "memory area setting LCW" command has been executed.

Description of parameters

For details of the parameters, see the description of the "memory area setting LCW" command.

The ROM version indicates the revision history of the μPD72103A's internal firmware.

The correspondence between ROM versions and standards is shown below.

Standard	ROM version
K	. . . 50
E	. . . 60
P	. . . 60

Status name	Operation mode read acknowledge	Symbol	MDAK

Field definitions

	7	6	5	4	3	2	1	0
LSW (0)	STSN (3BH)							
(1)	Don't care							
(2)	FCS	TFIL	CODE	CLK	DMAW		DMAB	CPU
(3)	LOOP		STEP	OCT	SHORT		AUTO	
(4)	–	–	BUFE	BUFC	GICS		TXED	LOAK
(5)	–	–	–	–	STBC			
(6)	TIME							
(7)	RBS							
(8)								
(9)	MAXD							
(10)								
(11)	HOLD							
(12)	TXUR	RETN						

Report cause(s)

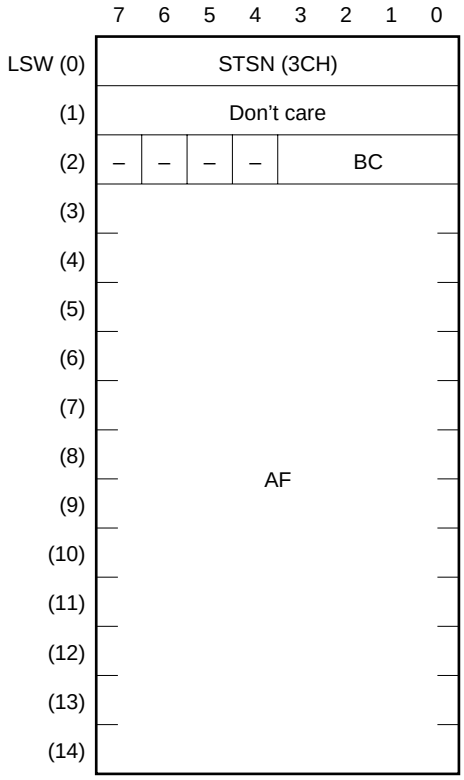
This indicates the operation mode that is reported when the "operation mode read LCW" command has been executed.

Description of parameters

For details of the parameters, see the description of the "operation mode setting LCW" command.

Status name	Receive address field read acknowledge	Symbol	AFAK

Field definitions



Report cause(s)

This status is reported when the "receive address field read LCW" command has been executed.

This status indicates the receive address field that is set via the "receive address field setting LCW" command.

Description of parameters

For details of the parameters, see the description of the "receive address field setting LCW" command.

Status name	Statistical information read acknowledge	Symbol	SIAK

Field definitions

	7	6	5	4	3	2	1	0
LSW (0)	STSN (3DH)							
(1)	COUNT							
(2)	OVRN							
(3)	UNRN							
(4)	IDLE							
(5)	SHORT							
(6)	ADDR							
(7)	LONG							
(8)	ABORT							
(9)	FCS							
(10)	FRAC							
(11)	FLSW							
(12)	FLRBW							

Report cause(s)

This status is reported when the “statistical information read LCW” command has been executed.
The status information includes various kinds of error information.
The statistical information is cleared after this status is reported.
Accordingly, once the “statistical information read LCW” command is executed, the errors that have occurred before then are reported and a new count begins of any error information that occurs subsequently in the μPD72103A.

Description of parameters

1. COUNT : Count total
   The COUNT value is 00H when the status information in LSW (2) to (12) consists entirely of 00H values.
   If error information appears in at least one field from LSW (2) to (12), the COUNT value is 01H.

2. OVRN : Overrun count
   This indicates the number of times an overrun has occurred due to full RxFIFO status during data receive operations.

3. UNRN : Underrun count
   This indicates the number of times an underrun has occurred due to empty TxFIFO status during data transmit operations.

4. IDLE : Mark idle detection count
   This indicates the number of times idle status (at least 15 consecutive “1” values) has been received.

5. ABORT : Abort detection count
   This indicates the number of times an abort pattern (at least 7 consecutive “1” values) has been received.

6. FCS : FCS error detection count
   This indicates the number of frames in which an FCS error has been detected by CRC checking of received frames.

7. ADDR : Unmatched address frame count
   This parameter is valid when the “operation mode setting LCW” command’s AUTO parameter is set to “01” or “10”.
   This indicates the number of times that a frame having an address field other than those specified by the “receive address field setting LCW” command has been received.

8. FRAC : Fractional bit frame count
   This parameter is valid when the “operation mode setting LCW” command’s OCT parameter has been set to “1”.
   This indicates the number of times that a frame containing fractional bits has been received.

9. LONG : Long frame count
   This indicates the number of times that a frame which exceeds the receive buffer size set by the “operation mode setting LCW” command’s RXBS parameter has been received. When using receive buffer chain mode, it indicates the number of times that a frame which exceeds the receive buffer size set by MAXD (a parameter in “operation mode read acknowledge LSW”) has been received.

10. FLSW : Status overflow count
    This indicates the number of times that a status table overflow has occurred for a received frame due to lack of empty space in the receive status table.

11. FLRBW : Receive buffer overflow count
    This indicates the number of received frame that have been discarded due to lack of empty space in the receive buffer address table.
    When there are several instances of error information concerning received frames, the count uses the following prioritization of causes and counts only the cause having the highest priority.

1	Overrun
2	Short frame
3	Address error frame
4	Long frame
5	Abort frame
6	FCS error frame
7	Fractional bit frame

Highest priority (H)

Lowest priority (L)

Caution The count value is FFH in cases where the various statistical information is FFH or greater.

Remark Frames in which the number of bits between a flag and an abort pattern are fewer than the number of bits set by the SHORT parameter are counted as short frames rather than abort frames.

Status name Command illegal **Symbol** CILG

Field definitions

	7	6	5	4	3	2	1	0
LSW (0)	STSN (3FH)							
(1)	ILST							
(2)	LSTN							
(3)	LCWN							
(4)	CMDN							

Report cause(s)

This status is reported when a command having an undefined command number or containing incorrect parameters has been executed.

Description of parameters

1. ILST : Illegal state
   This indicates that an illegal state exists.

   00H Indicates that an undefined command number has been issued
   01H Indicates that an error exists in at least one parameter of the issued command
   02H Unmatched state

2. LSTN : State when illegal
   This indicates the state (mode) that was in effect when the illegal command was issued.

   00H Indicates that idle mode was in effect
   01H Indicates that flag reception standby mode was in effect
   02H Indicates that data transmission mode was in effect

3. LCWN : Illegal command block
   This indicates the block number in the command table where the illegal command was issued.

4. CMDN : Illegal command number
   This indicates the illegal command's command number.

Status name General-purpose input pin change detection 1 **Symbol** GI1C

Field definitions

	7	6	5	4	3	2	1	0
LSW (0)	STSN (40H)							
(1)	–	–	SYNC	IDLE	GI2F	GI1F	GO2F	GO1F

Report cause(s)

This status is valid when the GICS parameters in the “operation mode setting LCW” and “operation mode setting 2 LCW” commands have been set to “01” or “10”. It reports that a status change has been detected in general-purpose input pin GI1.

Description of parameters

1. GO1F : GO1 pin status
   This indicates the output level of the GO1 pin.
   - 0 Indicates that GO1 pin is at low level
   - 1 Indicates that GO1 pin is at high level

2. GO2F : GO2 pin status
   This indicates the output level of the GO2 pin.
   - 0 Indicates that GO2 pin is at low level
   - 1 Indicates that GO2 pin is at high level

3. GI1F : GI1 pin status
   This indicates the input level of the GI1 pin.
   - 0 Indicates that GI1 pin is at low level
   - 1 Indicates that GI1 pin is at high level

4. GI2F : GI2 pin status
   This indicates the input level of the GI2 pin.
   - 0 Indicates that GI2 pin is at low level
   - 1 Indicates that GI2 pin is at high level

5. IDLE : Idle mode
   This indicates the state of the RxD pin.
   - 0 Not idle
   - 1 Idle

6. SYNC : Synchronization status

This indicates the status of the RxD pin.

0 Not receiving flags

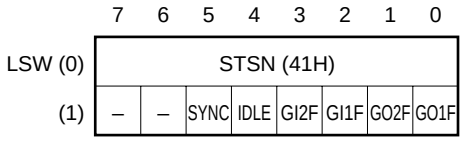
1 Receiving flags

Cautions 1. IDLE and SYNC are valid during data transmission enable mode.

2. This status indicates states that are detected at an interval of 8 ms.

Status name	General-purpose input pin change detection 2	Symbol	GI2C

Field definitions



Report cause(s)

This status is valid when the GICS parameter in the “operation mode setting LCW” command has been set to “10”. It reports that a status change has been detected in general-purpose input pin GI2.

Description of parameters

1. GO1F : GO1 pin status
   This indicates the output level of the GO1 pin.

   0 Indicates that GO1 pin is at low level
   1 Indicates that GO1 pin is at high level

2. GO2F : GO2 pin status
   This indicates the output level of the GO2 pin.

   0 Indicates that GO2 pin is at low level
   1 Indicates that GO2 pin is at high level

3. GI1F : GI1 pin status
   This indicates the input level of the GI1 pin.

   0 Indicates that GI1 pin is at low level
   1 Indicates that GI1 pin is at high level

4. GI2F : GI2 pin status
   This indicates the input level of the GI2 pin.

   0 Indicates that GI2 pin is at low level
   1 Indicates that GI2 pin is at high level

5. IDLE : Idle mode
   This indicates the status of the RxD pin.

   0 Not idle
   1 Idle

6. SYNC : Synchronization status

This indicates the status of the RxD pin.

0 Not receiving flags

1 Receiving flags

Cautions 1. IDLE and SYNC are valid during data transmission enable mode.

2. This status indicates states that are detected at an interval of 8 ms.

Status name General-purpose input/output pin read acknowledge **Symbol** GPAK

Field definitions

	7	6	5	4	3	2	1	0
LSW (0)	STSN (42H)							
(1)	–	–	SYNC	IDLE	GI2F	GI1F	GO2F	GO1F

Report cause(s)

This status indicates the status of general-purpose input/output pins as reported when the “general-purpose input/output pin read acknowledge LCW” command is executed.

Description of parameters

1. GO1F : GO1 pin status
   This indicates the output level of the GO1 pin.

   0 Indicates that GO1 pin is at low level
   1 Indicates that GO1 pin is at high level

2. GO2F : GO2 pin status
   This indicates the output level of the GO2 pin.

   0 Indicates that GO2 pin is at low level
   1 Indicates that GO2 pin is at high level

3. GI1F : GI1 pin status
   This indicates the input level of the GI1 pin.

   0 Indicates that GI1 pin is at low level
   1 Indicates that GI1 pin is at high level

4. GI2F : GI2 pin status
   This indicates the input level of the GI2 pin.

   0 Indicates that GI2 pin is at low level
   1 Indicates that GI2 pin is at high level

5. IDLE : Idle mode
   This indicates the status of the RxD pin.

   0 Not idle
   1 Idle

6. SYNC : Synchronization status

This indicates the status of the RxD pin.

0 Not receiving flags

1 Receiving flags

Cautions 1. IDLE and SYNC are valid during data transmission enable mode.

2. This status indicates states that are detected at an interval of 8 ms.

Status name	Status table overflow	Symbol	OLSW

Field definitions

	7	6	5	4	3	2	1	0
LCW (0)	STSN (43H)							
LCW (1)	–	–	–	–	GI2F	GI1F	GO2F	GO1F
	LSTN							

Report cause(s)

This indicates that a status table overflow has occurred.

The μPD72103A includes a two-part status buffer. If a status report request is issued when the buffer has not empty space, this status is reported once an empty space is available in the status table. Once this status is reported, the status that is stored in the internal status buffer is not reported.

Caution If a status report request is issued when there is no empty space in the status buffer, the status in the status buffer are discarded and a status overflow flag is set. If the status report request is for "data reception LSW", the internal discard occurs regardless of the buffer's empty/full status, so there is no status overflow in this case.

Description of parameters

1. GO1F : GO1 pin status

   This indicates the output level of the GO1 pin.

   0 Indicates that GO1 pin is at low level
   1 Indicates that GO1 pin is at high level

2. GO2F : GO2 pin status

   This indicates the output level of the GO2 pin.

   0 Indicates that GO2 pin is at low level
   1 Indicates that GO2 pin is at high level

3. GI1F : GI1 pin status

   This indicates the input level of the GI1 pin.

   0 Indicates that GI1 pin is at low level
   1 Indicates that GI1 pin is at high level

4. GI2F : GI2 pin status

   This indicates the input level of the GI2 pin.

   0 Indicates that GI2 pin is at low level
   1 Indicates that GI2 pin is at high level

5. LSTN : Link status

This indicates the state (mode) when a status table overflow has occurred.

00H Idle mode
01H Flag reception standby mode
02H Data reception enable mode

Cautions 1. IDLE and SYNC are valid during data transmission enable mode.
2. This status indicates states that are detected at an interval of 8 ms.
3. This status is reported when the status table has been released.

Status name	Statistical information read acknowledge 2	Symbol	SIAF

Field definitions

	7	6	5	4	3	2	1	0
LSW (0)	STSN (44H)							
(1)	SIN0							
(2)	SIN1							

Report cause(s)

This status is reported when the “statistical information read 2 LCW” command has been executed.
This status reports status information specified by the “statistical information read 2 LCW” command’s SIN0 and SIN1 parameters. After this report is issued, the statistical information specified by SIN0 and SIN1 is cleared. Other statistical information that was not specified by the “statistical information read 2 LCW” command is retained.

Description of parameters

For details of the parameters, see the description of the “statistical information read acknowledge LSW”.

Status name General-purpose input/output pin read acknowledge 2 **Symbol** GPAE

Field definitions

	7	6	5	4	3	2	1	0
LSW (0)	STSN (45H)							
(1)	–	–	SYNC	IDLE	GI2F	GI1F	GO2F	GO1F

Report cause(s)

This status indicates the status of general-purpose input/output pins as reported when the “general-purpose input/output pin read acknowledge 2 LCW” command is executed.

This status indicates each status as it existed at the time of the report.

Description of parameters

1. GO1F : GO1 pin status
   This indicates the output level of the GO1 pin.

   0 Indicates that GO1 pin is at low level
   1 Indicates that GO1 pin is at high level

2. GO2F : GO2 pin status
   This indicates the output level of the GO2 pin.

   0 Indicates that GO2 pin is at low level
   1 Indicates that GO2 pin is at high level

3. GI1F : GI1 pin status
   This indicates the input level of the GI1 pin.

   0 Indicates that GI1 pin is at low level
   1 Indicates that GI1 pin is at high level

4. GI2F : GI2 pin status
   This indicates the input level of the GI2 pin.

   0 Indicates that GI2 pin is at low level
   1 Indicates that GI2 pin is at high level

5. IDLE : Idle mode
   This indicates the status of the RxD pin.

   0 Not idle
   1 Idle

6. SYNC : Synchronization status
This indicates the status of the RxD pin.

0 Not receiving flags
1 Receiving flags

CHAPTER 6 SYSTEM CONFIGURATION EXAMPLES

6.1 Connection with Host System

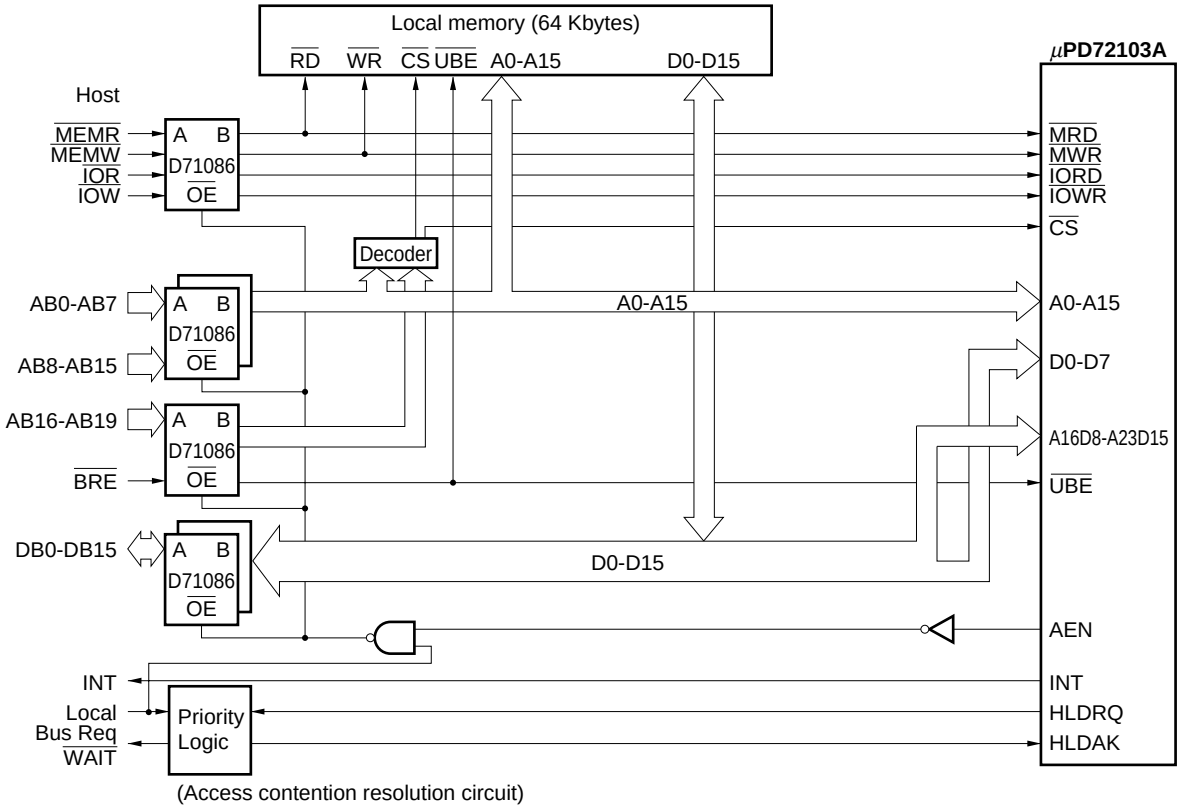
Two host system/μPD72103A system configuration examples are described below.

(1) Local memory type
(2) Main memory type

6.1.1 Local memory type

In the local memory type of system configuration, the μPD72103A accesses only the special purpose local memory. It is possible for the host system and the μPD72103A to have simultaneous access, but this requires the external addition of a priority logic circuit for contention resolution. One of the features of this configuration type is that the host system is able to be operated even when the μPD72103A is in bus master mode (i.e., during DMA transfers). One of its drawbacks is that it requires DMA transfers between the host system's main memory and local memory. Figure 6-1 shows a configuration diagram of the local memory type.

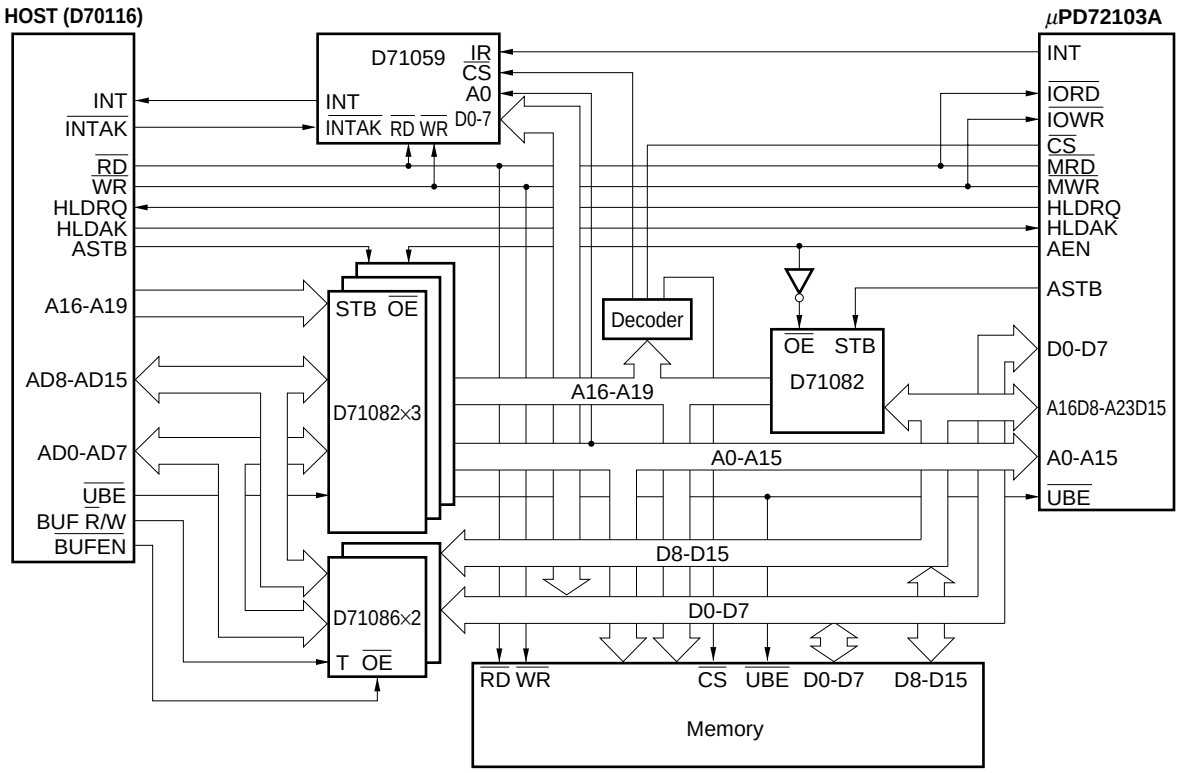
Figure 6-1. μPD72103A System Configuration Example (Local Memory Type)



6.1.2 Main memory type

The main memory type enables the μPD72103A to directly access the host system's main memory. One of its features is that it minimizes memory transfer operations for transmit and receive data. One of its disadvantages is that the host processor must be set to a hold state when the μPD72103A is in bus master mode (i.e., during DMA transfers), which reduces the host processor's operational efficiency. Figure 6-2 shows a configuration diagram of the main memory type.

Figure 6-2. μPD72103A System Configuration Example (Main Memory Type)



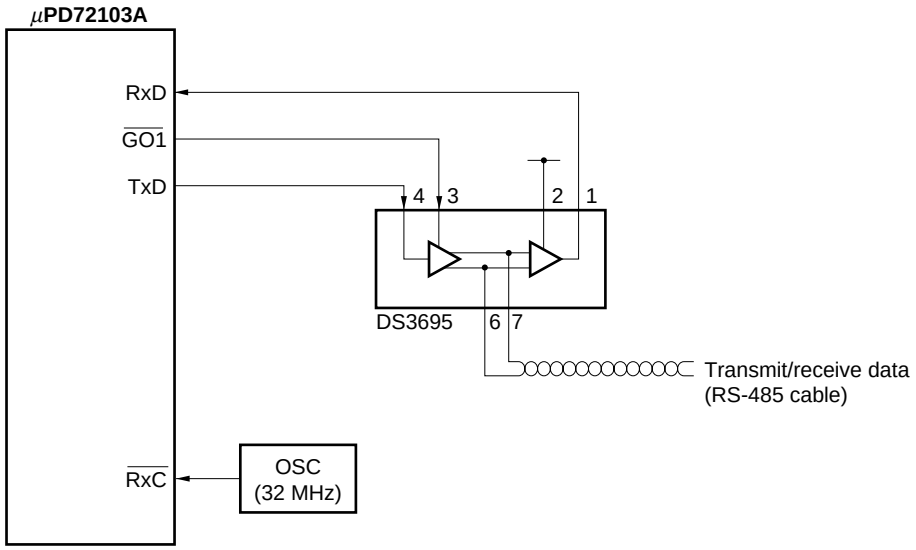
6.2 Physical Interface Examples

6.2.1 Interface example using RS-485

The μPD72103A's possible applications include LAN applications.

Figure 6-3 shows a two-wire interface example using the RS485 driver.

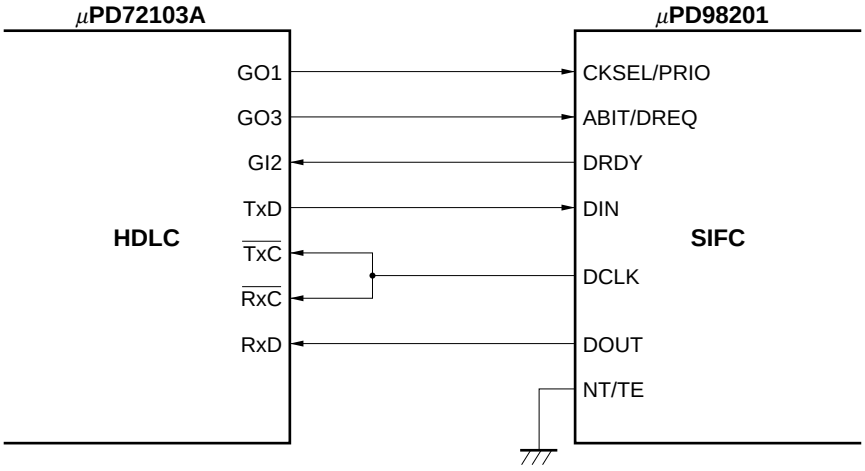
Figure 6-3. Two-wire Interface Example



6.2.2 Interface example using μPD98201

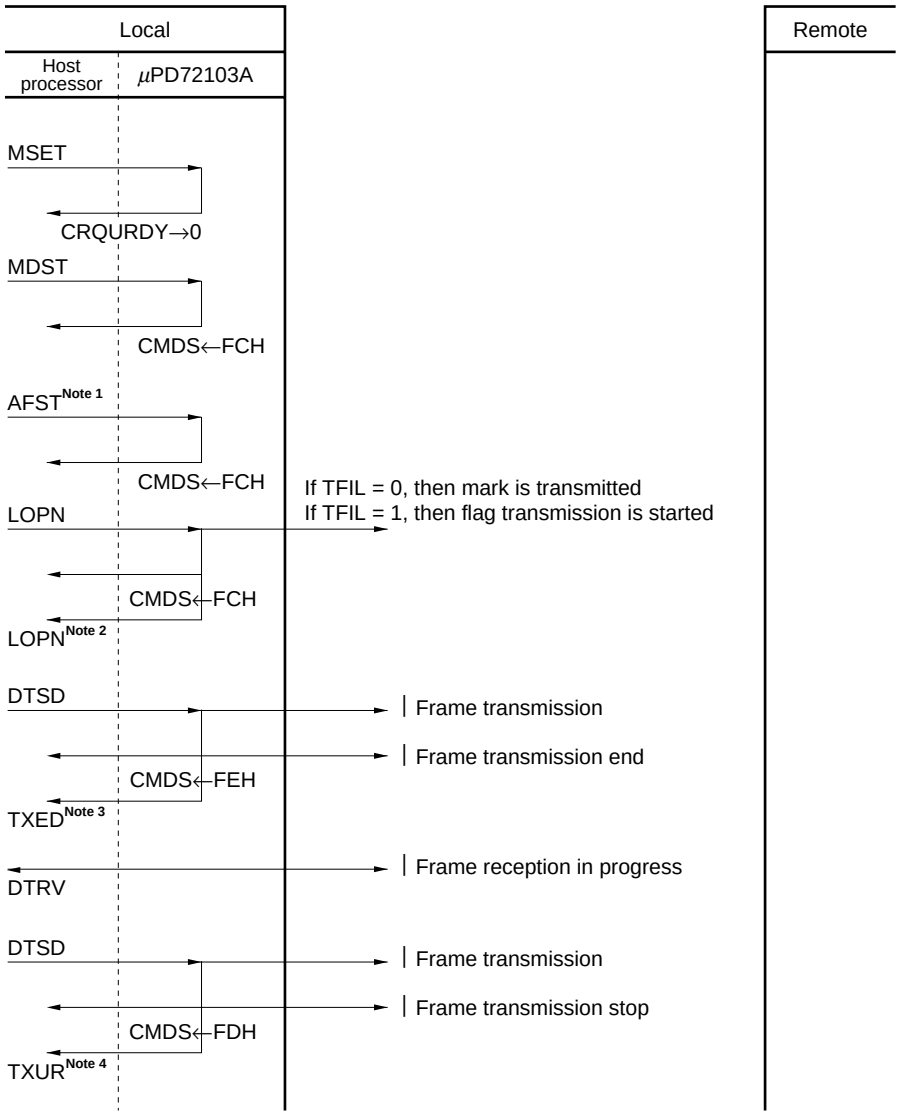
When the μPD72103A is set to LAPD mode, it can be connected with the μPD98201 to be used as a controller for D-channel communications. Figure 6-4 illustrates the connection with the μPD98201.

Figure 6-4. Connection Example with ISDN LSI (connection with SIFC [μPD98201])



[MEMO]

APPENDIX A μPD72103A OPERATION SEQUENCE EXAMPLES



Notes 1. Valid when AUTO ≠ 00

2. The report timing varies depending on the TFIL and LOAK parameter settings.

3. Reported when TXED = 1 in the mode setting.

4. Reported when TXUR = 1 in the mode setting.

[MEMO]

APPENDIX B CONNECTION BETWEEN HDLC CONTROLLER AND MOTOROLA SYSTEM

B.1 Differences between NEC/Intel Buses and Motorola Buses

The following are two points of difference between NEC/Intel buses and Motorola buses.

B.1.1 Difference in allocation of physical even-numbered byte and odd-numbered byte in 16-bit bus

In NEC and Intel buses, when the bits in a 16-bit bus are designated as D0 to D15, D0 to D7 comprise the even address byte and D8 to D15 comprise the odd address byte. In a Motorola 16-bit bus, D0 to D7 comprise the odd address byte and D8 to D15 comprise the even address byte.

NEC/Intel type		Motorola type	
D0-D7	D8-D15	D0-D7	D8-D15
Address 0	Address 1	Address 1	Address 0
Address 2	Address 3	Address 3	Address 2
Address 4	Address 5	Address 5	Address 4
Address 6	Address 7	Address 7	Address 6
:	:	:	:
:	:	:	:

B.1.2 Difference in representation order of logical 16-bit and 24-bit data

In NEC/Intel type buses, logical 16-bit or 24-bit (multiple byte) data is recognized starting from its low-order address in memory, (for 16-bit data, the order is low-order eight bits, then high-order eight bits; for 24-bit data, the order is low-order eight bits, middle eight bits, then high-order eight bits). In Motorola type buses, logical 16-bit or 24-bit (multiple byte) data is recognized starting from its high-order address in memory, (for 16-bit data, the order is high-order eight bits, then low-order eight bits; for 24-bit data, the order is high-order eight bits, middle eight bits, then low-order eight bits). For example, the following shows the representation order of the data value 123456H (hexadecimal) in these two types of buses.

	NEC/Intel type	Motorola type
Address N	56H	12H
Address N + 1	34H	34H
Address N + 2	12H	56H

B.2 Method for Connecting HDLC Controller with Motorola-based System

The HDLC controller is designed to be used with NEC/Intel buses. Accordingly, the following connection method is recommended when connecting to a Motorola-based system.

B.2.1 Data bus connection in hardware

HDLC controller		Motorola bus
D0	– – – – – – – –	D8
D1	– – – – – – – –	D9
D2	– – – – – – – –	D10
D3	– – – – – – – –	D11
D4	– – – – – – – –	D12
D5	– – – – – – – –	D13
D6	– – – – – – – –	D14
D7	– – – – – – – –	D15
A16D8	– – – – – – – –	D0
A17D9	– – – – – – – –	D1
A18D10	– – – – – – – –	D2
A19D11	– – – – – – – –	D3
A20D12	– – – – – – – –	D4
A21D13	– – – – – – – –	D5
A22D14	– – – – – – – –	D6
A23D15	– – – – – – – –	D7

This connection method resolves the difference described in **B.1.1** above.

B.2.2 HDLC controller's MDST command setting (operation mode setting LCW)

Select CPU = 1 (Motorola type).

This setting resolves the difference described in **B.1.2** above.

APPENDIX C QUESTIONS AND ANSWERS ABOUT THE μPD72103A

Table C-1. Question Categories (1 of 2)

BUS INTERFACE	
Q.1	During the DMA cycle, how much time is required before the HLDRQ signal becomes active?
2	Operation of μPD72103A when CRQ is issued
3	What is the time period between when CRQ is issued and when frame transmission begins?
4	Operations when commands are issued from μPD72103A
5	Processing when INT pin is not used
6	DMA request
7	DMA transfer time and application program processing time
8	What is the priority ranking among DMA controller operations?
9	Cascade connection example
10	AEN pin immediately after reset
11	Interrupt occurrence immediately after the INT pin goes inactive
12	Confirmation of unused pins
13	TEST pin usage/operation status
14	Regarding use of the CMOS buffer for the TxD pin
15	Number of DMA blocks transferred during transmit/receive
16	CRQ pin input
17	Minimum pulse width of CLRINT pin
18	Connection with V25+™ (μPD70325)
HOST INTERFACE	
Q.19	Sequence for issuing MSET command
20	External memory access
21	Command read sequence
22	Data transmit LCW
23	Issuance of “operation mode setting 2 LCW” command
24	Interrupt following execution of “operation mode setting LCW” command
25	What is the time period between the line open LCW command is issued and when the line open completion LSW is reported?
26	μPD72103A’s operation when status table cannot be used
27	Status table
28	Receive buffer table overflow
29	Causes of and responses to reception overrun errors
30	What is the μPD72103A’s operation when LRBWs are use-disabled?
31	Receive buffer address table
32	What does “(H)”, “(M)”, and “(L)” refer to in the User’s Manual?
33	Operation of HLDRQ signal for MSET command
34	Reception of unmatched address frame during address search
35	MAXD setting when not using receive buffer chain
36	Reception during receive status reporting
37	Full duplex operation
38	FCS error frame processing
39	Amount of data retained in FIFO

Table C-1. Question Categories (2 of 2)

40	RBA size
41	Transmit completion LSW report timing
42	Stopping command fetch operation
43	Write to command register
44	Changing AUTO parameter
45	Status completion detection method
46	Undefined status number
47	Random write for commands
48	Processing of transmit completion status during reception
49	Transmission method for fractional frames
50	STBC setting when AUTO ≠ 0
COMMUNICATION OPERATIONS	
Q. 51	Is it possible to expand the address recognition function?
52	What is the relationship between the CLK signal and the communication speed?
53	Operation when transmit clock input is lost
54	Use of $\overline{\text{TxC}}$ and $\overline{\text{RxC}}$ pins when in internal DPLL mode
55	Method for stopping transmit operation
56	Transmit/receive operations
57	Abort transmission
58	Allowable jitter for DPLL
59	Minimum number of transmitted flags
60	DPLL lock and flag reception
61	CRC polynomial equation and initial value
62	Flow control and sequence control
63	Transmission steps for transmit CRC
64	Transmit CRC example
65	Flag search during mark reception
66	Handling of TFIL parameter for reception
67	CRC calculation range
68	Idle pattern when HOLD ≥ 1
69	Stopping/starting flag transmission
70	Stopping reception only
71	Confirmation of receive completion at remote side
72	Transmit/receive frame intervals
OTHER	
Q. 73	Functional comparison with similar products
74	IC replacement
75	Address/data bus status after reset
76	Transmit complete timer function

BUS INTERFACE

During the DMA cycle, how much time is required before the HLDRQ signal becomes active?

Q.1

According to this manual, when transmitting and receiving in full duplex mode, the μPD72103A continuously performs DMA transfers (in 4-byte units).
What is the shortest possible period between the time when HLDRQ (the hold request signal) becomes inactive (L) during the previous DMA cycle and the time when it becomes active (H) during the next DMA cycle?

A.1

The minimum time period is the system clock time (t_{CYK}) × 12.

Related reference See "**2.2.1 Block transfers**" in this manual.

Operation of μPD72103A when CRQ is issued

Q.2

According to the μPD72103A User's Manual, when the host processor makes a command request, the CRQ pin or CCRQ bit becomes active.
At that time, does the μPD72103A send a hold request to the host processor? Also, does the host processor set the bus to a hold state?

A.2

The μPD72103A does send a hold request.

Think of the host processor's control method vis-a-vis the μPD72103A as exactly the same as that used by an ordinary DMA controller (such as the μPD71037).

When the host processor sends a command request (CRQ: H/CCRQ = 1) to the μPD72103A, the μPD72103A sets HLDRQ (the hold request signal) for the host processor as active in order to acquire bus access mastership. Next, the host processor responds to the HLDRQ sent from the μPD72103A by returning HLDAK (hold acknowledge signal) to enable bus access. At this point, the μPD72103A performs a DMA transfer of data from memory.

Related reference See "**2.3 Interface between μPD72103A and Host Processor**" in this manual.

What is the time period between when CRQ is issued and when frame transmission begins?

Q.3

After CRQ is issued, what is the time period before the μPD72103A actually starts transmitting frames?

A.3

There is no rating for the time period between when CRQ is issued and when frame transmission begins.

The time between issuing the transmit command and receiving the transmit command depends on the bus status.

Similarly, the bus status (timing of bus release by host processor, etc.) also determines the amount of time between receiving the transmit command and starting DMA transfer of the transmit data, and thus there is no rating for this time period either.

In other words, the time between issuing a CRQ and transmitting data depends on the μPD72103A's system configuration.

The time between transmit FIFO write and the start of data transmission can be specified in the range 0 to 1020 μs (when operating clock is 8 MHz) via the HOLD parameter setting (in the operation mode setting LCW command). The range for a 5-MHz operating clock is 0 to 1632 μs.

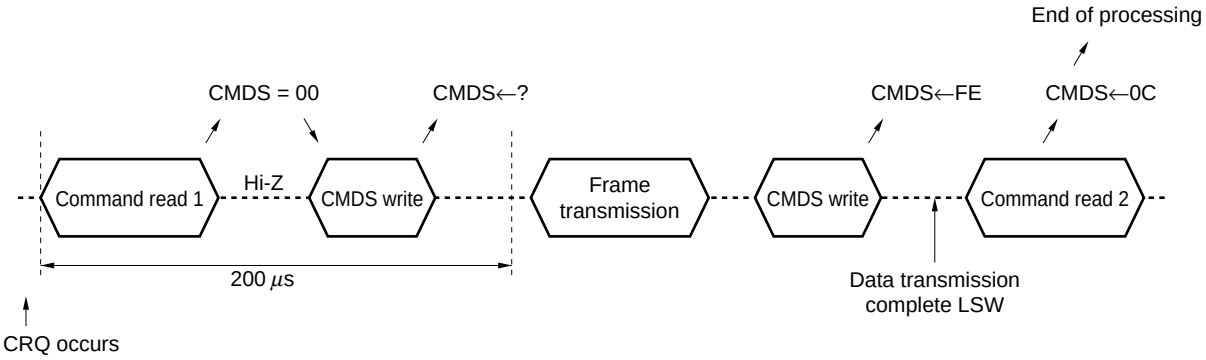
Related reference See "**3.1 Initial Settings**" and "**3.2 Start of Communication Control Operation and Flag Synchronization Setup**" in this manual.

Operations when commands are issued from μPD72103A

Q.4

(1) Is the following diagram a correct illustration of the DMA operation that occurs when a transmit command is issued?

Description of DMA processing



(2) The User's Manual does not specifically say what is written to the CMDS field during the period between when the μPD72103A reads a command and when an actual frame is transmitted.
Please explain how the CMDS value changes according to the command being executed.

(3) If a command is set (CMDS = 00) while another command is being executed, can the second command be executed without issuing a CRQ?

(4) Suppose that there is an attempt to report a data transmit complete LSW while the data transmit LCW command is being continuously issued.
In this case, which has priority: the timing by which the μPD72103A reads the next data transmit LCW command or the timing by which the data transmit completion LSW is written?

A.4

(1) Yes, the diagram is correct.

(2) CMDS is written to 0CH after the command is received. When the transmission has been completed, either FDH or FEH is written to CMDS.

(3) Yes, the second command can be executed.
Since each command can be executed once it has been read, it is possible to execute a new command that is written during execution of another command without issuing a CRQ.

(4) If a command read request and a status write request occur internally at the same time, the status write request takes priority. Therefore, the data transmit LSW also takes priority.

Related reference See "**2.5.1 Command table**" in this manual.

Processing when INT pin is not used

Q.5

Does leaving the μPD72103A's INT output as active (H) cause any problems for the controller operations?

A.5

Leaving the μPD72103A's INT output as active does not affect the controller operations.

Related reference See "**1.5 Pin Functions**" in this manual.

DMA request

Q.6

These questions concern DMA requests.

(1) In the μPD72103A, how much data must accumulate in the TxFIFO and RxFIFO before a DMA request is issued?

(2) In the μPD72103A, if DMA requests are issued (asynchronously) from both the TxFIFO and the RxFIFO, which is selected: the transmit DMA or the receive DMA?

A.6

(1) Concerning the RxFIFO, a DMA request is issued when four bytes of data have accumulated (when DMAB = 0) or when the end of the frame is reached. As for the TxFIFO, a DMA request is issued whenever there is even one byte of empty space.

(2) The receive DMA takes priority.

DMA transfer time and application program processing time

Q.7

Because the μPD72103A has an on-chip DMA function, a bus is dedicated for DMA transfer with the host processor, which reduces the bus occupancy time for executing ordinary application programs.
What are the DMA transfer time and (minimum) application program processing time under the following conditions?

Conditions

- Transfer rate : 64 kbps
- Transfer data : 1024 bits
- System clock : 8 MHz

A.7

The μPD72103A's DMA controller sets the HLDRQ signal as active once per 4 μs (minimum).

The DMA transfer time uses 4 clocks per byte and operates using either four-byte or eight-byte blocks as set by the DMAB parameter[Note]. Consequently, when using 4-byte transfer mode (DMAB = 0), the transfer time is about 16 clocks (or 2 μs when operating at 8 MHz). For 64-Kbps transfers, the μPD72103A's bus occupancy time can be calculated as follows.

1 ÷ 64000 (bps) × 8 (bit) × 4 (byte) = 500 μs

During this 500-μs transmission period for transmit/receive data, two DMA transfers are performed: one transmit and one receive (the period for each is 2 μs). Accordingly, when expressed as a ratio relative to the bus occupancy periods for the μPD72103A and the host processor, the bus occupancy period for an application program would be 500 : 4 (or, as a percentage, 0.8%).

Actually, the ratio is a little larger than 500 : 4, due to the time required for reading the command, writing the status, etc.

This has not created any problems during free running tests that NEC has performed using an evaluation board.

Note The DMAB parameter belongs to the operation mode setting LCW command.

Related reference See "**2.2 DMAC (Direct Memory Access Controller)**" in this manual.

What is the priority ranking among DMA controller operations?

Q.8

What are the DMA controller's operations in a situation where the data transmit LCW command is executed while a frame is being received and while the μPD72103A's status table is use-enabled?

A.8

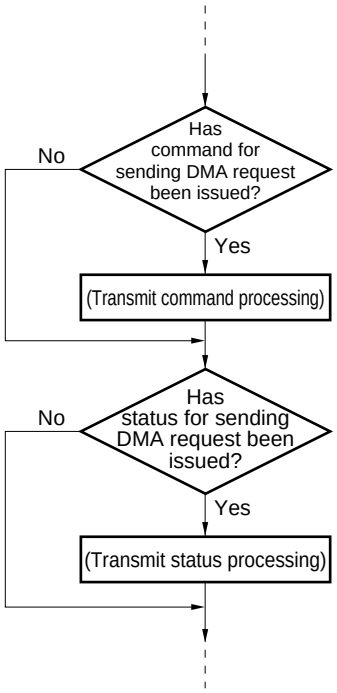
(1) In this situation, the μPD72103A performs a receive DMA operation.
The μPD72103A's DMA controller uses the following three DMA channels.

Highest priority (H)

1	Channel for sending receive data to receive buffer
2	Channel for sending command/status data
3	Channel for sending transmit data from transmit buffer

Lowest priority (L)

DMA requests for sending command/status data are processed via firmware.
The following is a flow chart of DMA request processing.



Cascade connection example

Q.9

Are there any standard methods or caution points concerning cascade connections of several μPD72103A chips?

A.9

To control several μPD70103A devices, connect them as slave devices to a DMA controller (such as the μPD71071). When using this method, we recommend using a priority rotation mode to suppress receive overrruns and transmit underruns.

AEN pin immediately after reset

Q.10

When a reset occurs while the $\overline{\text{RESET}}$ signal is active, the AEN pin goes to high level. Is this the correct operation?

A.10

When a system reset is performed using the $\overline{\text{RESET}}$ signal, the status is as shown in Table 1-1 after four system clocks. The status prior to the four system clocks is undefined. Check whether or not the system clocks have been input.

Interrupt occurrence immediately after the INT pin goes inactive

Q.11

After an interrupt occurs (INT pin = “H”), if another interrupt occurs during the brief period when the CCLRINT bit is set and the INT pin is being set as inactive, what happens to the INT pin?

A.11

If the CLRINT signal conflicts with the setting of the internal INT signal to make the INT pin active, setting of the INT signal takes priority. Therefore, the INT pin may not become inactive when CLRINT is issued. Accordingly, we recommend using a level trigger to detect the INT signal in such cases.

Confirmation of unused pins

Q.12

Does having the CLRINT pin, CRQ pin, INT pin, ASTB pin, and READY pin set as unused pins cause any problems under the following conditions?

- All control and status registers are used for processing related to interrupt detection and INT pin reset operations
- Control register is used for processing related to issuing CRQ
- No-wait processing of DMA transfers

A.12

There is no problem in the CLRINT pin, CRQ pin, INT pin, ASTB pin, and READY pin set as unused pins. For any input pin, the corresponding pin function should be disabled when the pin is not used.

- CLRINT pin or CRQ pin : connect to GND
- READY pin : connect to V_{DD}

TEST pin usage/operation status

Q.13

Regarding the TEST pin, when the manual says “when using/operating” this pin, which pin status is it referring to? What is this pin used for, and what is its operation when pulled down?

A.13

“When using/operating” refers to when a user is using the μPD72103A. However, the TEST pin is used only during NEC’s pre-shipment inspections. The LSI will not operate if this pin is pulled down.

Regarding use of the CMOS buffer for the TxD pin

Q.14

Although the TxD pin’s high-level signal voltage specification is $V_{OH} = 0.7V_{DD}$ ($I_{OH} = -400\ \mu A$), when driving one CMOS buffer, the I_{OH} value is only about $-1\ \mu A$. Therefore, do you think that a CMOS buffer can be used instead of a TTL?

A.14

The V_{IH} rating for a high-speed CMOS device is $0.7V_{DD}$ with no margin, but it is possible to connect such a device to the μPD72103A. Under the standard rating of $V_{DD} = 4.5$ V and when $I_{OH} = -400\ \mu A$, the V_{OH} value is about 4.34 V (reference value).

Number of DMA blocks transferred during transmit/receive

Q.15

During one DMA transfer, data can be transferred in either 4-byte or 8-byte units. Does this also apply for transmit/receive data?

A.15

The 4-byte or 8-byte unit refers to the rating for the maximum number of bytes per DMA transfer. Under certain conditions, the number of bytes per DMA may be fewer. For example, when a frame that is 19 bytes long is received, if DMA transfer is in 4-byte mode, there will be four cycles of 4-byte transfers followed by one cycle during which the remaining three bytes are transferred. The same is true when issuing commands and reporting status.

CRQ pin input

Q.16

To control the CRQ pin, is it enough simply to change the pin mode from “L” to “H” to “L” when issuing a command?

A.16

Yes, that is sufficient.

Minimum pulse width of CLRINT pin

Q.17

When generating signals via a PLD and inputting them to the CLRINT pin, how does the μPD72103A respond if a signal having a pulse width less than the rated value (MIN. 100 ns) is illegally input to the CLRINT pin?

A.17

Depending on the signal's pulse width, the characteristics of the LSI's internal transistors, the ambient temperature, the power supply voltage, and other use environment conditions, a CRQ pin acknowledge in preparation for command execution is possible, but the μPD72103A would not execute any operation except reading the command.

Connection with V25+ (μPD70325)

Q.18

Does using the V25+ and the μPD72103A in combination cause a problem for the μPD72103A's bus release operation?

A.18

t_{DHQHA} refers to the time period between when the μPD72103A sets HLDRQ signal as inactive and when the V25+ sets the HLDAK signal as inactive, and t_{DHAC} refers to the time until the V25+ enters bus master mode. The minimum value for t_{DHQHA} is about three clocks (although it is not mentioned in the manual, there is no problem because three internal clocks are used to generate a signal) and the minimum value for t_{DHAC} is 1 clock – 50 ns. If the V25+ clock and the μPD72103A's clock are the same, the time period between when the μPD72103A's HLDRQ signal goes inactive to when the AEN signal goes inactive is only about one clock, which means there should not be any problem. Use these specifications as a reference for design.

HOST INTERFACE

Sequence for issuing MSET command

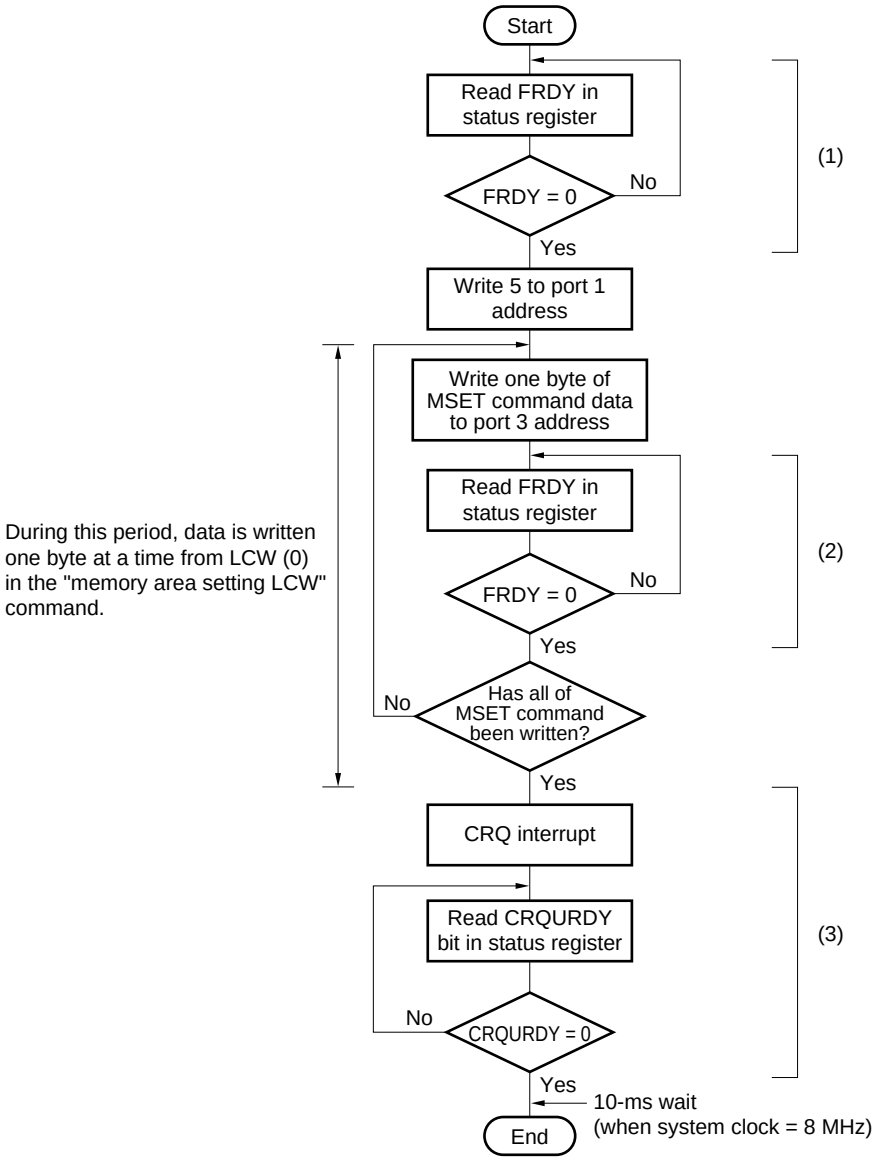
Q.19

The figure below shows the sequence by which the MSET command is issued, as described in this manual (Figure 2-1). What is the maximum time period that the μPD72103A requires for each of the operations indicated by (1), (2), and (3) in the figure?

(1) The period between when the μPD72103A is reset and when the status register's FRDY bit is set to 0

(2) The period between when one byte of MSET command data is written to the port 3 address and when the status register's FRDY bit is set to 0

(3) The period between when a CRQ interrupt occurs and when the status register's CRQURDY bit is set to 0



A.19

There are no maximum time ratings for these, but the following times can be established based on the number of internal firmware instructions.

(1) After completion of reset operation (7 clocks after the RESET signal goes inactive)
(2) 20 clocks after the data write operation
(3) 5000 clocks after the CRQ is issued. However, the CRQ for the next command can be issued 10 ms after the CRQURDY bit is set to 1.

Related reference See "**2.3.1 Command issuance**" in this manual.

External memory access

Q.20

When $\overline{B}$/W pin is set to high level

(1) When the μPD72103A accesses the CMDS at the second byte in the command table, does it access in byte access or word access (A0 and $\overline{UBE}$ are both low)?
(2) Does the μPD72103A use byte access mode or word access mode when accessing the status table's STSN field?

A.20

(1) It uses byte access mode.
(2) It uses byte access mode.

Related reference See "**1.5 Pin Functions**" in this manual.

Command read sequence

Q.21

When the host processor has set the μPD72103A's CCRQ bit (CRQ pin) as active, does the μPD72103A always start reading a command from the LCW0 field in the command table?

A.21

The μPD72103A reads the command from the area following the command table area used in the previous command execution. For example, the processing flow may be as follows.

<1> The host processor writes the "operation mode setting LCW" command (the address specified by the MSET command's ADDR parameter), then issues a CRQ.
<2> The μPD72103A reads this command from LCW0 and then executes the "operation mode setting LCW" command.
<3> After the "operation mode setting LCW" command has been completed, the μPD72103A reads to LCW1. However, when FXH is the CMDS (command status field) value in LCW1, the μPD72103A stops reading the command table.
<4> The host processor writes a new command to a new table (LCW1: address value is 10H), then issues a CRQ.

Related reference See "**2.5.1 Command table**" in this manual.

Data transmit LCW

Q.22

(1) When five data transmit LCW commands are chained and an underrun is detected for one of the data transmit LCW commands, does the μPD72103A report the data transmit completion LSW (TXEN parameter = 4) and/or the data transmission stop LSW (TXUR parameter = 1)? Also, does the μPD72103A report the data transmit completion LSW after reading the data transmit LCW commands?

(2) When FRBC = 1 and the data transmit LCW command is issued, is it the LSB in the last transmit data that is transmitted?

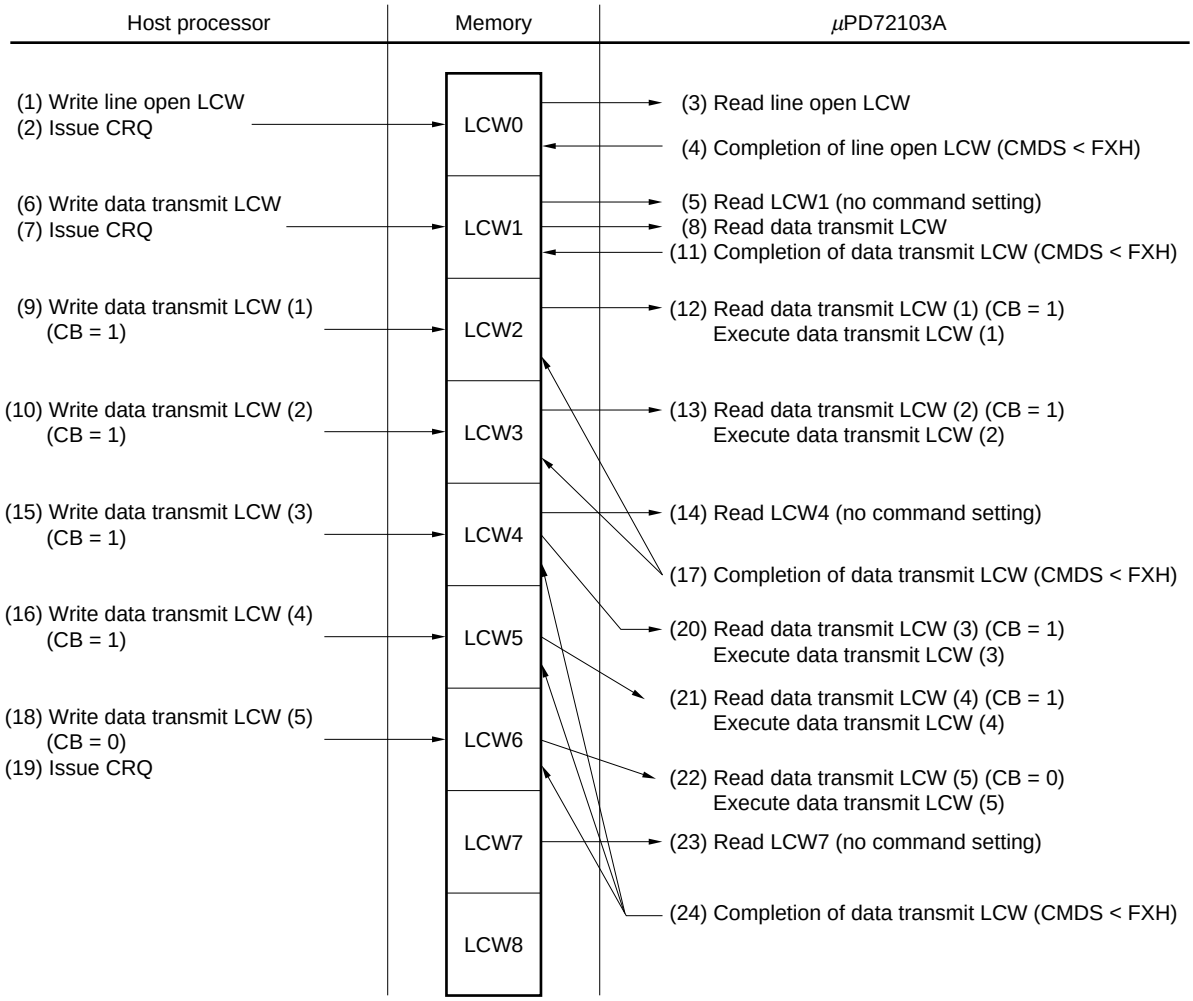
(3) Why is it that the nth data transmit LCW command must be the first to be written when transmitting via a transmit buffer chain?

A.22

(1) The following two cases can be considered.
If the status table is empty, the μPD72103A reports the data transmit completion LSW or the data transmission stop LSW after each data transmit LCW command is completed.
However, when the status table is full, the TXUR and TXEN parameters are incremented. When the status becomes empty again, the μPD72103A reports the data transmit completion LSW or the data transmission stop LSW.

(2) Yes, it is. When FRBC = 4, D0 to D4 in the last byte is transmitted.

(3) This is due to the operation shown in the following figure.



Remark If a transmit buffer chain frame that includes data transmit LCW (1) to (5) is to be sent but the host processor has not checked for command completion, the μPD72103A divides the frame into two frames, one for data transmit LCW (1) and (2) and one for data transmit LCW (3) to (5), and then transmits them.

Related reference See the data transmission command description in "**CHAPTER 4 COMMANDS (LCW)**" of this manual.

Issuance of "operation mode setting 2 LCW" command

Q.23

Does the "operation mode setting 2 LCW" command need to be issued only when the μPD72103A has received a flag or idle status?

A.23

Issuance of the "operation mode setting 2 LCW" is not related to the μPD72103A's internal status. However, any data received after this command has been issued is not guaranteed.

Related reference See the operation mode setting 2 LCW command description in "**CHAPTER 4 COMMANDS (LCW)**" of this manual.

Interrupt following execution of "operation mode setting LCW" command

Q.24

Does the INT signal become active after the "operation mode setting LCW" command is executed?

A.24

No, it does not become active.

After the "operation mode setting LCW" command is executed, there is no active interrupt signal from the μPD72103A to the host processor.

What is the time period between when the line open LCW command is issued and when the line open completion LSW is reported?

Q.25

Setting condition: the timing of line open completion status report is when a flag has been transmitted from a local source (set via LOAK = 0).

Given the above setting condition, what is the time period between when the line open command is issued to the μPD72103A and when the line open completion status is reported?

A.25

There is no rating for the maximum time, but a value of 1800 clocks can be calculated under the following conditions and based on the number of internal firmware instructions.

Conditions: 100% bus ownership; no command is issued to the μPD72103A; RxD pin has high-level status (status during which the μPD72103A can only perform the line open task).

μPD72103A's operation when status table cannot be used

Q.26

What are the μPD72103A's operations when the status table cannot be used (when no STSN with a value of FFH is available)?

A.26

Since the μPD72103A includes a two-part status buffer, everything except the data reception LSW is retained.

If a status report request is issued when the buffer is full, a status table overflow LSW is reported and the buffer is cleared once an empty space is available in the status table.

However, any data reception LSW is internally discarded regardless of the buffer's internal status if the status table is not empty.

For details, see also the **μPD72103 Application Note**.

Related reference See the status table overflow description in "**CHAPTER 5 STATUS (LSW)**" of this manual.

Status table

Q.27

Condition: Eight LSWs are set for the host processor. After executing two commands, the μPD72103A has written to LSW0 and LSW1.

<1> At that point, does the μPD72103A write the status to LSW2 when the next command is completed?
<2> What kind of processing does the μPD72103A perform if a new status report request for a data reception LSW is generated?
<3> If LSW2 cannot be used (if LSW2 in the STSN file is not FFH), does the μPD72103A check the STSN field in LSW3?

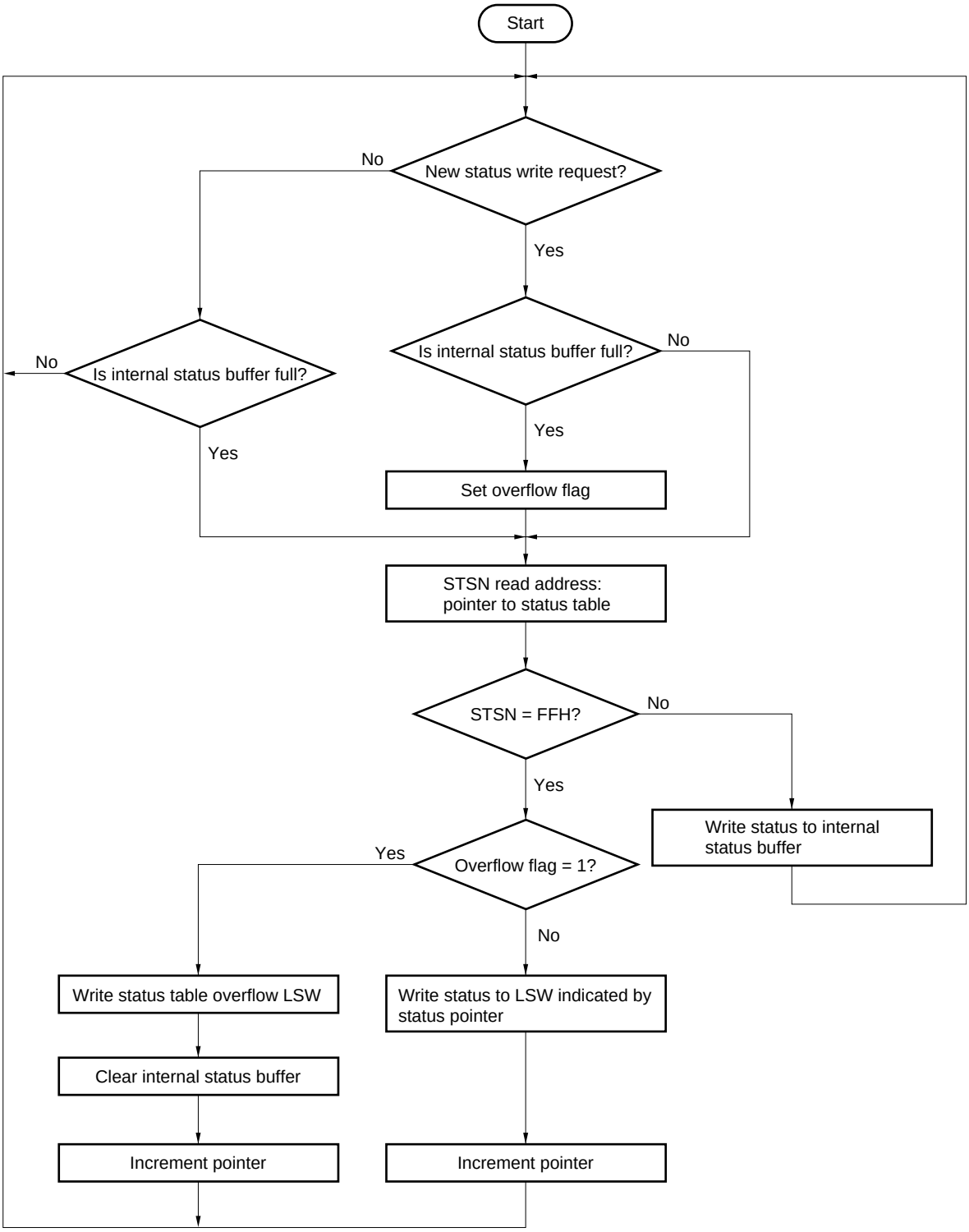
A.27

The μPD72103A has a status address pointer. This pointer is incremented when the μPD72103A writes a status to the status table.

<1> If a new status report request has been generated, the μPD72103A attempts to write a status to LSW2 but cannot because LSW2 cannot be used (it must wait until LSW2 is use-enabled).
Neither can it write to LSW3 or the other LSWs.
<2> The data reception LSW is discarded.
<3> Two following two cases can be considered.
If LSW2 is use-disabled (but the other LSWs are use-enabled), when a new status report request (any except for data reception LSW) has been generated, the μPD72103A writes a status to the internal status buffer[Note].
After LSW2 becomes use-enabled, the μPD72103A writes the status to LSW2.
If three or more new status report requests occur while LSW2 is use-disabled, the μPD72103A sets the status table overflow flag. Next, the μPD72103A waits until LSW2 can be used for the status table overflow, after which it reports the status to LSW2.
The following is a flow chart of the status reporting operations.

Note The μPD72103A includes a two-part status buffer.

Status Reporting Flow Chart



Related references See **"2.5.2 Status table**" in this manual.
See "**1.2.2 Status reporting sequence**" in the **μPD72103 Application Note**.

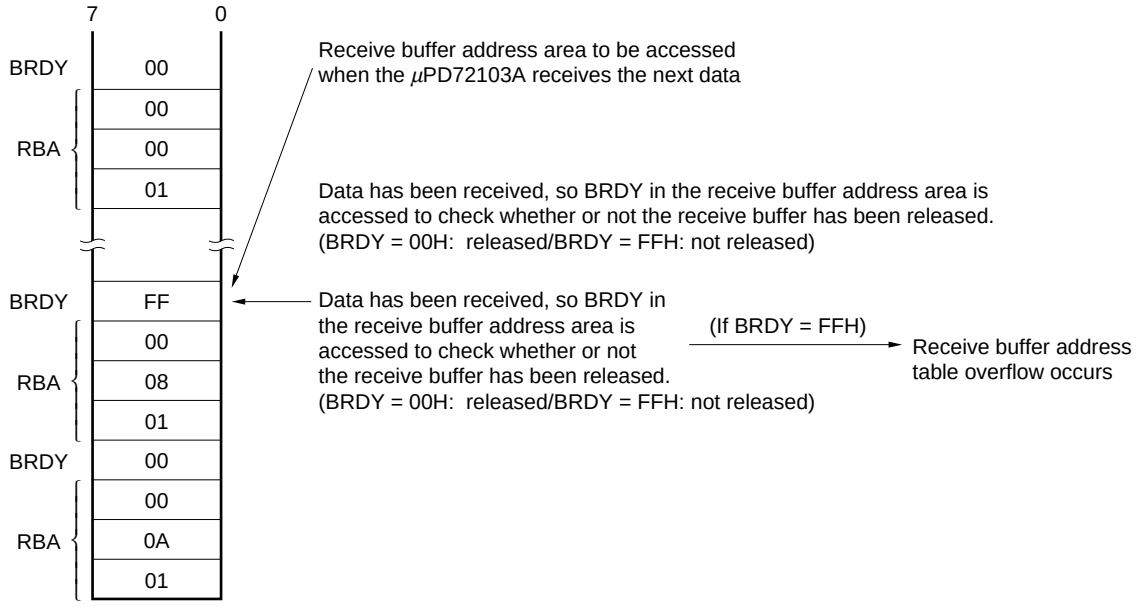
Receive buffer overflow table

Q.28

The following kinds of events occurred when I attempted to operate the μPD72103A. Are these operations correct?

(1) When the μPD72103A received the next data, the area in the receive buffer table that was to be accessed indicated that the receive buffer had not been released (BRDY = FFH) while other areas showed that the receive buffer had been released (BRDY = 00). At that point, the receive data was discarded even though the receive buffer had been released for the next area.

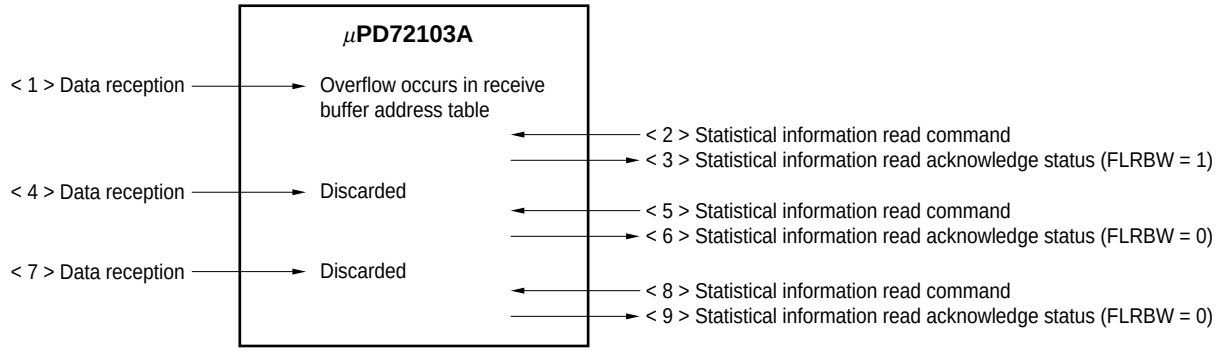
Receive buffer address table



(2) After the statistical information read acknowledge status is read to confirm that "1" has been written to FLRBW (see <3> in the figure below), data is received while overflow status is still in effect (see <4> in the figure below, where the receive data is discarded).

Later, the value of FLRBW remains 0 at the area (<6> in the figure) where the statistical information read acknowledge status was read (all of the receive data is discarded).

If the statistical information read acknowledge status was read when an overflow occurred in the receive buffer address table, why isn't the statistical information subsequently updated even when data has been discarded several times?



A.28

(1) The receive data was discarded because the status table was not empty.

Since each table in the μPD72103A is a link buffer, each command or status is executed in order starting at the top.

If the status table is not empty, the μPD72103A must wait for it to become empty, during which time it reports a status table overflow LSW and then clears the buffer contents[Note]. However, in the case of a data reception LSW, the buffer contents are discarded regardless of the buffer's internal status unless the status table is empty.

Therefore, since the status table is not empty during the method (data receive) described in your question, the buffer contents are discarded.

Note The μPD72103A includes a two-part status buffer.

(2) In this case, the statistical information is not updated for the following reasons.

The first receive frame is counted when data is received while there is no empty space in the receive buffer address table and status table, but subsequent frames are not counted when data is received while there is no empty space.

Accordingly, with reference to the timing shown with the question, the count is cleared by the statistical information read command <2>and the count operation is not performed for subsequent receive data, so the FLRBW value remains "0" in the statistical information read acknowledge status indicated by <6> and <9>.

Related references See "**2.5.3 Receive buffer address table**" in this manual.
See the status table overflow description in "**CHAPTER 5 STATUS (LSW)**" of this manual.

Causes of and responses to reception overrun errors

Q.29

Reception overrun errors have occurred when using the μPD72103A under the conditions listed in the following table (occurrence rate: 0.08%). What are the causes of these errors and what responses should be made?

Use conditions

Communication mode	Full duplex
System clock	5 MHz
Transfer rate	2 Mbps
Amount of receive data	500 bytes per frame
Receive frame interval	Every 3 ms
Reception time fill	Flag
Reception command chain	None
Amount of transmit data	50 bytes per frame
Transmit frame interval	Flag
Transmit time fill	Every 100 ms
Transmit command chain	None
DMA data access unit	Word unit
DMA transfer time per block	2 μs (measured), two bus cycles

A.29

In the case of 4-byte block transfers (DMAB = 0), if the receive DMA's interval is 16 μs, all of the receive data in the receive FIFO can be transferred, but the receive DMA interval becomes longer if a transmit operation is being performed at the same time.

For example, if the receive DMA interval is 20 μs, then logically one byte remains in the receive FIFO for each receive DMA transfer, which eventually causes an overrun in the receive FIFO.

To avoid this, try one of the following responses.

- Set DMA transfers to 8-byte block transfer mode (DMAB = 1).
- Set the system clock to 8 MHz and speed up the firmware processing rate.
- Shorten the DMA interval.

Communication operations were performed without problems using NEC's evaluation system, in which the system clock speed is 8 MHz and the transfer rate is 4 Mbps.

Related reference See "**3.4.8 Cautions regarding overrun errors**" in this manual.

What is the μPD72103A's operation when LRBWs are use-disabled?

Q.30

Conditions: Four LRBWs have been set by the host processor.
The μPD72103A receives frames and uses LRBW0. When the μPD72103A starts receiving the next frame, it checks LRBW1.

If LRBW1 becomes use-disabled under the above conditions, does the μPD72103A keep searching for an LRBW that has been released? Also, is the frame discarded at that point?

A.30

The received frame is discarded and the μPD72103A waits until the BRDY value (in LRBW1) becomes FFH.

The μPD72103A includes three internal receive buffer address FIFOs and a receive buffer address table (RBAT) pointer. The μPD72103A uses this pointer to search for the LRBW indicated by the pointer.

For example, after LRBW0 is used to receive the first frame, LRBW1 indicates the RBAT pointer.

If LRBW1 is used-disabled and the internal receive buffer address FIFO is empty, when the μPD72103A receives the next receive frame, it discards the receive data and waits until the BRDY value in LRBW1 becomes FFH. Also, when the μPD72103A reads the LRBW indicated by the RBAT pointer, RBA is set to the internal receive buffer address table FIFO and the receive buffer address table's pointer is incremented.

Related reference See "**2.5.3 Receive buffer address table**" in this manual.

Receive buffer address table

Q.31

(1) Can three receive buffer addresses be stored in the RBA FIFO?

(2) Conditions: When the μPD72103A receives a frame, it reads LRBW1 (use-enabled) and stores the value to the internal RBA FIFO's receive address. The μPD72103A then increments the pointer to the receive buffer address table.
In this case, after the μPD72103A has received a frame, does it read the receive buffer address from the RBA FIFO and report the receive buffer address in the data receive LSW?

(3) If the μPD72103A discard any frames it receives while the 128-byte RxFIFO is full and LRBW1 is use-disabled?

A.31

(1) Yes, they can be stored there.
The μPD72103A always reads the LRBW indicated by the pointer.
When the BRDY (receive buffer status field) value is 00H, the μPD72103A reads the RBA and stores the value in the RBA FIFO (FFH is then written to BRDY).

(2) Yes, that is correct.

(3) Yes, that is correct.
The μPD72103A discards frames as it receives them and continues to read LRBW1.

Related reference See "**2.5.3 Receive buffer address table**" in this manual.

What does “(H)”, “(M)”, and “(L)” refer to in this manual?

Q.32

What does “(H)”, “(M)”, and “(L)” refer to in connection with the RBA in section “**2.5.3 Receive buffer address table**” of this manual?

A.32

They refer to high, middle, and low values among memory addresses. Whenever “(H)”, “(M)”, and “(L)” appear in this manual, they refer to high, middle, and low values among memory addresses (in Intel products, low-order memory addresses are low).

Related reference See “**2.5.3 Receive buffer address table**” in this manual.

Operation of HLDRQ signal for MSET command

Q.33

I am using a method whereby the “memory area setting LCW” command is issued by writing to the internal FIFO. When using this method, setting the control register’s CCRQ bit causes the HLDRQ signal to become active. Is this operation correct?

A.33

Yes, it is correct.

Reception of unmatched address frame during address search

Q.34

When the AUTO parameter in the “operation mode setting LCW” command has been set to “01”, receiving a frame that does not contain a setting address field causes ADDR in the statistical information to be incremented, but is the receive data transferred?

A.34

There is no DMA transfer of the receive data.

MAXD setting when not using receive buffer chain

Q.35

This manual says that MAXD is valid when BUFC = 1, but can MAXD also be used as a discard condition for the buffer even when BUFC = 0?

A.35

MAXD is not used when BUFC = 0. The buffer discard condition in this case is RXBS.

Reception during receive status reporting

Q.36

What happens when new data is received while receive status processing is still being performed?

A.36

Even while the host is busy processing a previously received frame, data in the next frame to be received can be accumulated in the receive FIFO. When that data accumulates beyond a certain amount (threshold value), it is transferred to the receive buffer via a DMA transfer. When reception of the next frame is completed (when an FCS check has detected that it is a normal frame), the receive status is written to the status table and, as a final step, the interrupt pin is again set as active. No matter what kind of processing the host is performing, as long as the μPD72103A's receive block has empty space in its receive buffer and status table it can continue to receive frames and report status.

Full duplex operation

Q.37

As part of full duplex communications, is it possible for reception interrupt servicing and transmit command processing to be performed at the same time? If so, does DMA access alternate between the transmit data read and receive data write operations?

A.37

Yes, they can be performed at the same time. However, since receive processing has priority in the μPD72103A, when a transmit command request occurs at the same time, the transmit command processing must wait for completion of receive processing. This means that the two types of processing do not necessarily alternate.

FCS error frame processing

Q.38

When the received frame is normal, it is written to external memory. Then, what happens if the received frame is abnormal?

A.38

Receive data that has been accumulated in the receive FIFO before the abnormality was detected is transferred to the receive buffer. For example, in the case of an FCS error the FCS check results are not known until the FCS is received, so all of the data prior to the FCS is temporarily transferred to the receive buffer. In cases where the receive data is discarded, this occurs simply by assigning the receive buffer address pointer as reusable.

Amount of data retained in FIFO

Q.39

Is there a way to externally detect how much data has accumulated in the transmit FIFO and receive FIFO at any particular time?

A.39

No, there is no way to detect that.

RBA size

Q.40

When the manual says “any size up to 16 Kbytes can be set for the receive buffer”, does that refer to one receive buffer that occupies 16 Kbytes starting at the receive buffer address (RBA) that is set to the receive buffer address table, or does it mean the entire receive buffer in external memory can be 16 Kbytes in size?

A.40

Unless the receive buffer chain mode is being used, the receive buffer is the 16 Kbytes that begin at the receive buffer address set to the receive buffer address table.

When using the receive buffer chain mode, since maximum MAXD value is 16 Kbytes, the receive buffer size must be MAXD ≤ RXBS × (NLRBW – 4).

In either case, there is no need to restrict the size of the entire receive buffer in external memory to 16 Kbytes.

Transmit completion LSW report timing

Q.41

Is it correct that the “transmit completion LSW” is reported after the FCS field is detected?

A.41

Yes, that is correct.

Stopping command fetch operation

Q.42

Is the command fetch operation stopped only when the CMDS value is FFH? Is it ever stopped when CMDS is FCH, FDH, or FEH?

A.42

The command fetch operation is stopped if the CMDS value is FXH. This means that it is stopped if the CMDS value is FCH, FDH, or FEH (but not FFH).

Write to command register

Q.43

The INT pin is set as active to facilitate software processing related to the control register. At a certain point, the CCRQ bit is set to “1”, the CCLRINT bit is set to “0”, and the register is accessed expressly so that a CRQ can be issued. Does it cause a problem when, afterward, the CCRQ bit is set to “0”, the CCLRINT bit is set to “1”, and the register is accessed so as to set the INT pin as inactive? Also, is it possible to check the values that have been written to the control register?

A.43

No, it does not cause a problem. Setting a control register bit to “1” enables the corresponding function to be executed, and setting it to “0” does not affect other bits. There is no way to check the values that have been written to the control register.

Changing AUTO parameter

Q.44

After AFST is used to set the receive address with AUTO set to the initial value (“01”), when the MDSE command is used to set AUTO to “00” during communication (line open status) and to “01” afterward, the frame at the receive address field set via AFST is received. Why does this happen?

A.44

When the MDSE command is used to set AUTO to “00” during communication, all internally set addresses are cleared. Later, when AUTO is set to “01”, the receive address has been lost, so the AUTO = “00” remains. Consequently, after changing the AUTO setting from “AUTO = 00” to “AUTO ≠ 00”, be sure to use the AFSE command to reset the receive address.

Status completion detection method

Q.45

Statuses have been written in order to the status table. When host performs status processing, does it proceed in order from the area where the previous status was processed to the next area until it reaches an “STSN = FFH” setting?

A.45

Yes, it does.

Undefined status number

Q.46

Are undefined status numbers reported to STSN? And if they are, can FFH be written to STSN, just like for the normal operation?

A.46

Undefined statuses are not reported. If one were somehow to be reported and FFH is written to STSN, it would not affect the operation.

Random write for commands

Q.47

When executing a series of commands, successive command areas are used. However, when only one command is issued in response to one command request, does it cause a problem to randomly use the command areas?

A.47

Like the status table, the command table is written to starting from the command table header (LCW0) before a command is executed. Therefore, it is not possible to randomly use the command areas. When a command is written, it should always be written to the area that follows the area used for the previous command.

Processing of transmit completion status during reception

Q.48

What is the status report timing on the transmitting and receiving sides when several transmit commands are written and transmissions are performed for several destinations while issuing only one CRQ? Is a status report done after each command is completed? Also, please explain the INT pin's set/reset conditions during this process.

A.48

The transmitting side performs a transmit completion status report after each frame has been transmitted. However, if a factor occurs that requires high-priority processing similar to frame receive processing, the number of transmitted frames are internally counted until the high-priority processing is completed. Later, when a status report can be made, the transmit completion status is reported. Accordingly, it is possible that just one transmit completion status may be used to report completion of several frame transmissions.

The receiving side performs a receive completion status report after each frame has been received. The INT pin is set as active after each receive status is written. The INT pin can be set as inactive only by setting the control register's CCLRINT bit to "1" or by inputting a high-level pulse signal to the CLRINT pin.

Transmission method for fractional frames

Q.49

When the "operation mode setting LCW" command's BUFE parameter has been set to "0", how can the transmit command's parameters be set to transmit a fractional frame consisting of 16 bytes plus 5 bits (assuming that TXBC = 0)?

A.49

The fractional bit length can be expressed by setting "5H" as the FRBC value. However, for the BC parameter be sure to set "11H" to include the fractional bits rather than setting 10H ("16" in decimal notation).

STBC setting when AUTO ≠ 0

Q.50

Can STBC be set to "0" when AUTO ≠ 0?

A.50

As was indicated in the table that was provided with the description of the "operation mode setting LCW" command's STBC parameter, STBC cannot be set to "0" when AUTO ≠ 0.

COMMUNICATION OPERATIONS

Is it possible to expand the address recognition function?

Q.51

When at least three bytes of bits are needed in an address field, can the address field be expanded?

A.51

No, it cannot be expanded. The μPD72103A's address recognition function works for up to two bytes. If there are three or more bytes, they should be processed using host software.

Related reference See "**3.4.4 Address field recognition**" in this manual.

What is the relationship between the CLK signal and the communication speed?

Q.52

The frequency range for the μPD72103A's system clock input is 1 to 16 MHz. Does the relationship with communication speed place any restrictions on this input range?

A.52

Basically, there is no mutual relationship between the CLK signal and the communication speed.

However, since the CLK signal is captured via DMA transfer timing, transmit underrun or overrun errors may frequently occur if the CLK signal is too slow.

Accordingly, in such situations it is possible that the system may cease to support communications functions.

Related reference See "**1.5 Pin Functions**" in this manual.

Operation when transmit clock input is lost

Q.53

When in a mode that uses the $\overline{\text{TxC}}$ pin as an input, if the line open operation is performed normally but the signal to be input to the $\overline{\text{TxC}}$ pin is lost (due to line breakage, etc.). The other input signals (to $\overline{\text{TxD}}$ and RxD, etc.) remain normal.

(1) If the above occurs, does the μPD72103A notify the host processor?
(2) How would the μPD72103A operate if the above occurred during a transmit operation?
(3) How would the μPD72103A operate if the "data transmit LCW" command is issued after the above occurs?

A.53

(1) No, it does not notify the host processor.
When the $\overline{\text{TxC}}$ signal is fixed at H or L, the result is the same as when a zero baud-rate CLK signal is input. Accordingly, the user learns of the above event when, after a transmit command has been executed and the timer has been activated, a timeout occurs indicating that input to the $\overline{\text{TxC}}$ pin has stopped.
(2) The μPD72103A stops the transmit operation. The receiving side receives an abort pattern.
(3) The μPD72103A cannot accurately receive a newly issued data transmit command until the $\overline{\text{TxD}}$ signal has been input again.

Use of $\overline{\text{TxC}}$ and $\overline{\text{RxC}}$ pins when in internal DPLL mode

Q.54

Please explain the use of the $\overline{\text{TxC}}$ and $\overline{\text{RxC}}$ pins when internal DPLL mode has been selected.

A.54

When in internal DPLL mode, input a CLK signal to the $\overline{\text{RxC}}$ pin at 16 times the baud rate. The $\overline{\text{TxC}}$ pin functions as an output during internal DPLL mode.

Related reference See "**4. Serial Timing**" in the Data Sheet.

Method for stopping transmit operation

Q.55

How can a transmit operation be stopped?

A.55

Perform the following steps to stop transmission when using a transmit command chain.

<1> The μPD72103A captures transmit commands from the command table in top-to-bottom order. After capturing a command, it sets "00H" to CMDS.

<2> Set "0" to the CB parameter in a command for which the CMDS value is not 00H to stop the transmit command chain operation.

<3> Change the CMDN and CMDS values to "FFH" in the next transmit command.

Example: If the chain contains eight transmit commands, the following can be done to stop the chain transmission at the sixth transmit command in the chain.
After the host processor confirms that the fifth command's CMDS value is not 00H, change the sixth transmit command's CMDN and CMDS parameters to "FFH" while the CB parameter is set to "0".
If the fifth command's CMDS value has already been changed to 00H, use the above operation for the sixth and seventh transmit commands.

Cautions 1. Transmit operations cannot be stopped except when in transmit command chain mode.

2. Make sure that the CB parameter value is "0". It is not possible to change the CMDN parameter to FFH. In a transmit buffer chain, the CMDN and CMDS values are not checked in the second and subsequent commands, so the transmit operation continues based on the remaining parameters.

Transmit/receive operations

Q.56

(1) If a "line close LCW" command is issued while the μPD72103A is transmitting data, does the μPD72103A abort the transmission?
(2) What does the μPD72103A do if a "line close LCW" command is issued while it is receiving data?
(3) If a transmission underrun occurs while executing the "operation mode setting LCW" command (RETN = 0), does the μPD72103A continue to execute the "data transmit LCW" command until a normal end occurs?

A.56

(1) The μPD72103A reads and executes one command at a time, so it will not attempt to execute a "line close LCW" command while a "data transmit LCW" command is still being executed. Consequently, no transmission is aborted.
(2) The μPD72103A reads the "line close LCW" command and immediately executes it, then stops data reception. At that point, the receive frame is discarded.
(3) Yes, it does. If the RETN parameter has been set to "0", the μPD72103A will continue to execute the "data transmit LCW" command until a normal end occurs.

Related references See the line close command description in "**CHAPTER 4 COMMANDS (LCW)**" of this manual.
See the operation mode setting command description in "**CHAPTER 4 COMMANDS (LCW)**" of this manual.

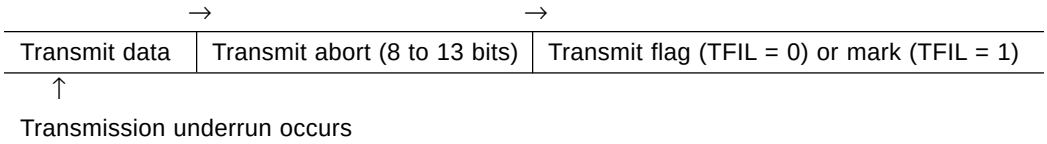
Abort transmission

Q.57

(1) When a transmission underrun has occurred, does the μPD72103A automatically transmit an abort pattern? Does it attach a flag afterward?
(2) What is the length of the abort pattern transmitted by the μPD72103A?

A.57

(1) Yes, the μPD72103A transmits an abort pattern when a transmission underrun occurs. After it transmits the abort pattern, it transmits a mark if TFIL = 1 [Note] or a flag pattern if TFIL = 0.
The following diagram shows the state transition following occurrence of a transmission underrun.



Note TFIL is a parameter in the "operation mode setting LCW" command.

(2) As shown in the above diagram, the abort pattern's length is 8 to 13 bits.

Related reference See "**3.3.4 Transmission underrun**" in this manual.

Allowable jitter for DPLL

Q.58

What is the percentage of allowable jitter for the μPD72103A's on-chip DPLL?

A.58

As was explained in section "**3.4.1 Reception timing**" of this manual, the μPD72103A's on-chip DPLL increments or decrements the count position of a divide-by-16 BRC counter depending on the counter's count position and the inversion position of data input to the RxD pin. It generates a reception clock signal that follows the jitter in the reception data. In other words, it allows for jitter up to 1/16th of the bit period if there is an edge-based inversion at each bit (if using NRZI format, "0" sets continuous reception).

However, during actual communications, it is rare that an edge inversion would occur at every bit. For example, if a flag has been selected as the time fill setting, under NRZI format, up to six consecutive "1" bits (flag pattern) would be input. In other words, if there is one edge per 7 bits, jitter would be (1 ÷ 16 ÷ 7 =) 0.9%. If mark has been selected as the time fill setting, there are no edges during mark idle reception, so the DPLL cannot provide any effect during this period and, in the worst case, a negative-phase lock may occur. Thus, whenever possible, the flag setting should be used for idle mode to enable adjustment for jitter.

Minimum number of transmitted flags

Q.59

At least three flags are inserted for a transmit frame. Why are at least three flags needed?

A.59

This is a restriction imposed by the μPD72103A's internal circuitry and is not related at all to communication operations. The μPD72103A's flag transmission circuitry is divided into an end flag transmission circuit, an idle flag transmission circuit (or mark pattern transmission circuit when IDLE = 1), and a circuit that transmits the next frame's start flag. Consequently, at least three flags are required.

DPLL lock and flag reception

Q.60

When using the DPLL during reception, can flags be detected if the DPLL is not locked?

A.60

There is no relationship at all between flag-based synchronization and DPLL locking. Flag detection is performed by sampling the RxD pin at the clock's rising edge, and a flag is detected when the sampled pattern is "01111110". There is absolutely no need to lock the DPLL's clock signal in this case. Note, therefore, that no temporal relationship between flag-based synchronization and DPLL locking is determined.

CRC polynomial equation and initial value

Q.61

Is the CRC–16 ($X^{16} + X^{12} + X^5 + 1$) format for CRC calculations supported? What is the initial setting for the CRC calculator?

A.61

CRC–16 is not supported. The initial setting is FFH.

Flow control and sequence control

Q.62

Does the μPD72103A provide sequence control and flow control like the μPD72107 (LAPB controller) does? Also, are SLDC loops supported?

A.62

Unlike the μPD72107, the μPD72103A does not provide sequence control and flow control. It performs only HDLC framing control. Other types of control should be implemented via host software. The μPD72103A does not support SLDC loops.

Transmission steps for transmit CRC

Q.63

What are the steps for sending transmit CRC calculation results?

A.63

Not only the μPD72103A but also every other communication controller that support CRC calculations inverts the transmit CRC calculation result logic and sends the results starting from the MSB.

Transmit CRC example

Q.64

Please show an example of transmit CRC calculation results.

A.64

Shown below are CRC calculation results obtained after transmission of each byte of the following transmit data.

Transmit data	00H	01H	10H	FFH
CRC calculation result	E1F0	7078	60F8	FF00
Actual data	78→F0	F1→71	F9→D0	00→FF

Flag search during mark reception

Q.65

When at least 8 bits of mark status is input to the RxD pin while line open status is in effect, does the μPD72103A's receive circuit automatically enter flag search mode? Also, is there any relationship between the idle monitor timer used during mark status and the receive circuit?

A.65

When at least 8 bits of mark status is detected, flag search mode is automatically set. The idle monitor timer and the receive circuit operate independently and therefore do not affect each other.

Handling of TFIL parameter for reception

Q.66

The “operation mode setting LCW” command has a TFIL parameter that relates to transmission, but is there also a setting related to reception?

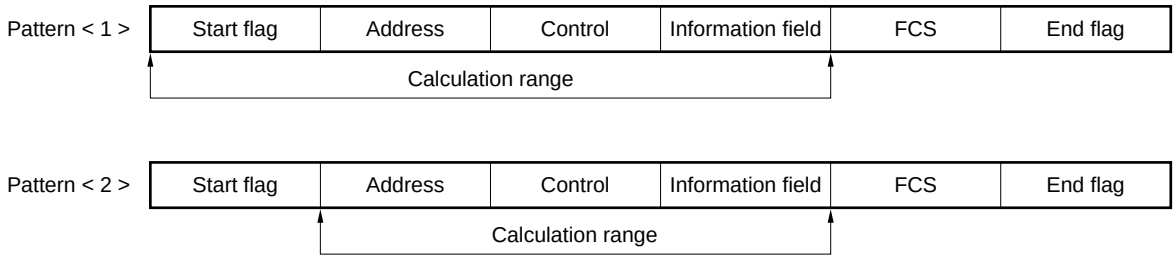
A.66

No, there is no such parameter. In the μPD72103A, reception is continued regardless of whether it is a flag or a mark that is used in idle mode.

CRC calculation range

Q.67

Which pattern shows the correct range for CRC calculations?



A.67

Pattern <2> shows the correct range for CRC calculations for any HDLC device manufactured by NEC or any other company.

Idle pattern when HOLD ≥ 1

Q.68

When a value of 1 or greater is set as the HOLD parameter, is it correct to assume that the pattern set by TFIL will be sent during the period in which the transmit data is transmitted?

A.68

Yes, that is correct.

Stopping/starting flag transmission

Q.69

Is it possible to start and/or stop flag transmission without stopping the receive operation while line open status is in effect?

A.69

It is not possible to control this via software, but LAPD mode can be used to implement external hardware-based port control. When doing this, be sure that TFIL is set to “1”.

Stopping reception only

Q.70

Is it possible to stop reception only while line open status is in effect?

A.70

No, it is not possible to stop reception only.

Confirmation of receive completion at remote side

Q.71

When transmit completion status is reported, does that mean that data transmission to the remote side has ended normally?

A.71

The transmit completion status is a status that is reported to indicate that a frame has been transmitted from the TxD pin without causing any transmission underrun in the μPD72103A and it does not indicate whether or not the remote side has correctly received the transmitted frame. The μPD72103A is an LSI that performs HDLC-type framing only and it does not provide sequence control or flow control functions. Confirmation of correct reception at the remote side should be implemented via host software.

Transmit/receive frame intervals

Q.72

When transmitting and receiving 6-byte frames in full duplex mode at 2.2 Mbps, is it possible to set a transmission interval of 600 μs and an interval ranging from 0 to 300 μs between transmitting and receiving?

A.72

During the command handling operation, the internal firmware checks whether or not a CRQ has been issued when the command reaches the CRQ program check module within the main routine. If a CRQ has been issued, processing jumps to the corresponding command's program. When using loopback mode (transmit/receive interval = 0), a 2-Mbps transfer rate, and evaluation of transmit data length as 10 bytes, an average transmission interval of 625 μs is determined. However, this applies to a case in which transmission and reception occur at almost the same time. If there is any fluctuation in the transmit/receive interval, the reception processing is delayed and the time required for confirming the CRQ (one processing cycle of the main routine) may become longer. Therefore, it is impossible to fix the transmission interval at 600 μs.

OTHER

Functional comparison with similar products

Q.73

Please provide a chart comparing the functions of the μPD72305, μPD72107, μPD72001, μPD72103A, and μPD72002.

A.73

A function comparison chart is shown below.

Manufacturer		NEC	NEC	NEC
Part number		μPD72305	μPD72103A	μPD72002
Supported standards/ recommendations		ITU-T 1.440 and 1.441 (LAPD) HDLC control, sequence control Flow control, multi-link support	HDLC	Asynchronous (Asynchronous) COP (Character Oriented Protocol) BOP (Bit Oriented Protocol) HDLC, SDLC
Number of channels		1	1	1
HDLC frame control	Flag detection/generation	√	√	√
	Auto zero fill	√	√	√
	CRC generating polynomial	Same as μPD72103A	When 16-bit: $X^{16} + X^{12} + X^5 + 1$ When 32-bit: $X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X^1 + 1$	$X^{16} + X^{12} + X^5 + 1$
	CRC add/check	√	√	√
	Abort generate/delete	√	√	√
	Address addition/recognition	2-byte addition/recognition	1-byte or 2-byte addition/recognition (programmable)	1-byte addition/recognition
Maximum transfer rate		4 Mbps	8 Mbps	2.2 Mbps
Transmit/receive buffers		Transmit buffer, 16 levels Receive buffer, 32 levels	Transmit FIFO, 32 levels Receive FIFO, 128 levels	Transmit buffer, 2 levels Receive buffer, 4 levels
Data between frames		Same as μPD72103A	Flag pattern is “01111110”, selectable as all “1”	Flag pattern is “01111110”, selectable as all “1”
DMA controller		24-bit address Byte/word transfer options (switchable via external pin connection)	8/16-bit data 24-bit address	Transmit DMA/Receive DMA
Serial interface		Same as μPD72103A	External channel required for using time slot interface	External channel required for using time slot interface
Processor interface		Same as μPD72103A	Connectable to Intel/Motorola bi-directional interface	Connectable to Intel/Motorola bi-directional interface
Custom software for manufacturer		None	None	None
Voltage		+5 V ± 10%	+5 V ± 10%	+5 V ± 10%
Process		CMOS	CMOS	CMOS
Operating ambient temperature		–40 to +85°C	–40 to +85°C	–10 to +70°C
Package		64-pin shrink DIP, 68-pin QFJ, 80-pin QFP	68-pin QFJ, 80-pin QFP	40-pin DIP, 44-pin QFP, 44-pin QFJ, 44-pin TQFP

Manufacturer		NEC	NEC	
Part number		μPD72107	μPD72001	
			–11	–A
Supported standards/recommendations		ITU-T X.25 (LABD) compliant HDLC control, sequence control Flow control Supports ITU-T X.75	Asynchronous (Asynchronous) COP (Character Oriented Protocol) BOP (Bit Oriented Protocol) HDLC, SDLC	
Number of channels		1	2	
HDLC frame control	Flag detection/generation	√	√	
	Auto zero fill	√	√	
	CRC generating polynomial	Same as μPD72103A	$X^{16} + X^{12} + X^5 + 1$	
	CRC add/check	√	√	
	Abort generate/delete	√	√	
	Address addition/recognition	1-byte or 2-byte addition/recognition (programmable)	1-byte addition/recognition	
Maximum transfer rate		4 Mbps	2.2 Mbps	1.6 Mbps
Transmit/receive buffers		Transmit buffer, 16 levels Receive buffer, 32 levels	Transmit buffer, 2 levels Receive buffer, 4 levels } × 2	
Data between frames		Same as μPD72103A	Flag pattern is “01111110”, selectable as all “1”	
DMA controller		24-bit address Byte/word transfer options (switchable via external pin connection)	Transmit DMA/Receive DMA × 2	
Serial interface		Same as μPD72103A	External channel required for using time slot interface	
Processor interface		Same as μPD72103A	Connectable to Intel/Motorola bi-directional interface	
Custom software for manufacturer		None	None	
Voltage		+5 V ± 10%	+5 V ± 10%	+3.3 V ± 0.3 V
Process		CMOS	CMOS	
Operating ambient temperature		–40 to +85°C	–10 to +70°C	
Package		64-pin shrink DIP, 68-pin QFJ, 80-pin QFP	40-pin DIP, 52-pin QFP, 52-pin QFJ, 44-pin TQFP Note	

Note μPD72001-11 only

IC replacement

Q.74

I would like to replace hardware that uses the μPD72107 (LAPB controller) with the μPD72103ALP (HDLC controller) and μPD72305L (LAPD controller) ICs. To do this, which hardware components do I need to change?

A.74

No hardware needs to be changed except for the general-purposes input/output pins.

Address/data bus status when reset

Q.75

(1) What are the statuses of the address and data pins while the $\overline{\text{RESET}}$ pin is active?

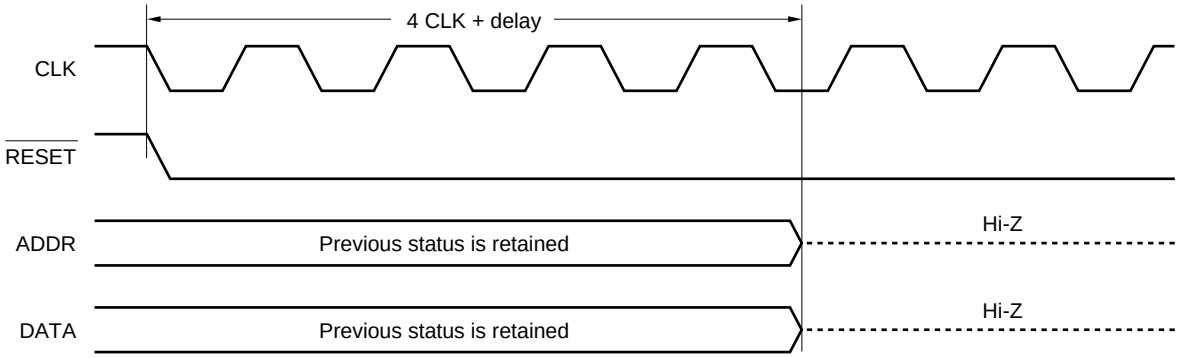
(2) I am using the μPD72103A with byte mode and 4-byte transfer settings.
What happens if HLDAK (the hold acknowledge pin) goes inactive (L) during transmission of the second byte?

(3) When HLDAK goes low while the μPD72103A is in bus master mode, does the μPD72103A release its buses (address/cycle data buses for high-impedance status) during the last DMA bus cycle?

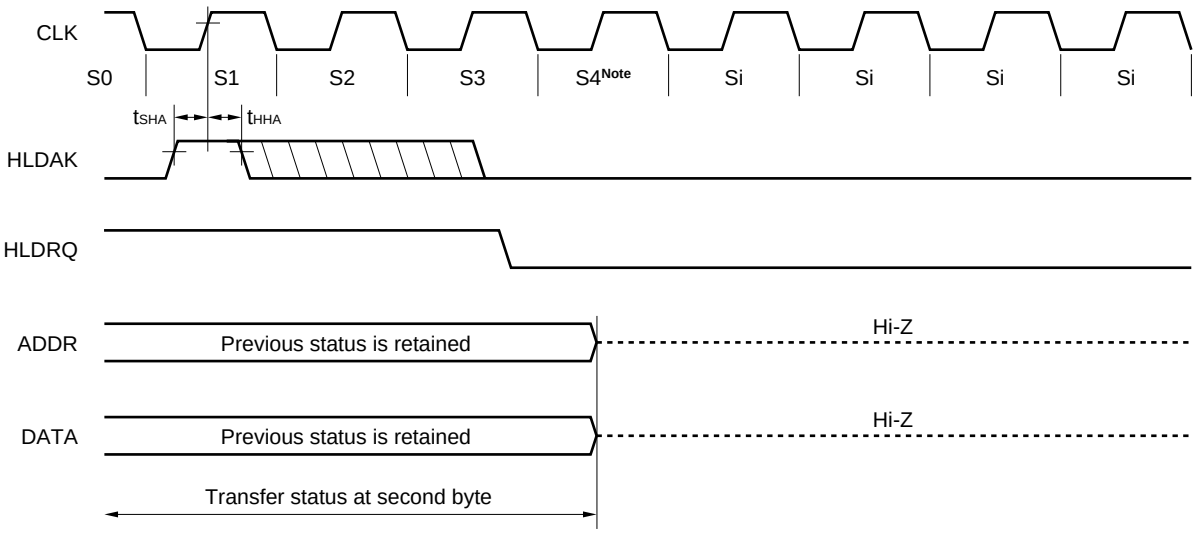
(4) During a 4-byte block transfer, if HLDAK goes inactive during a two-byte transfer, what happens to the remaining two bytes?

A.75

(1) These statuses are described in the following timing chart.



(2) Please refer to the timing chart shown below.
As was described in Figure 2-5 and Figure 2-6 in the User's Manual, the μPD72103A samples at the rising edge of the S0, which comes before S1 in the DMA cycle. If high level is maintained for at least the t_{HHA} time period, the cycle from S1 to S4 (one bus cycle) operates in bus master mode. When the HLDAK pin is again sampled at the rising edge of S4, if it is still at high level, the next bus cycle begins.
Accordingly, if four bus cycles are used for one block transfer, if the HLDAK pin's status should be maintained for the t_{HHA} time period after the rising edge of S4 during three bus cycles (t_{HHA}: 20 ns minimum). See the bus master-mode timing charts shown in the μPD72103A's Data Sheet.



Note Check whether or not the next state transition occurs at the rising edge of S4.
See the AC characteristics listed in the μPD72103A's Data Sheet for information on HLDAK and HLDRQ setup and hold times corresponding to S4.

(3) Yes, that is correct. The μPD72103A uses S4 timing to sample the HLDAK pin. If the HLDAK pin is low, the HLDRQ pin is set as inactive (L) at the end of the S4 timing.

Related reference See "**5. ELECTRICAL CHARACTERISTICS**" in the Data Sheet.

(4) The remaining two bytes are transferred via DMA transfer 4.5 clocks after the S4 cycle of the previous bus cycle has been completed and when the HLDRQ signal becomes active.

Transmit complete timer function

Q.76

Is there a function that will automatically increment a counter when a transmit command is completed and report the status when a specified count value is reached?

A.76

No, there is no such function.

Table D-1. COMMAND LIST (1/2)

Command No.	Symbol	Byte 0 / Byte 8	Byte 1 / Byte 9	Byte 2 / Byte 10	Byte 3 / Byte 11	Byte 4 / Byte 12	Byte 5 / Byte 13	Byte 6 / Byte 14	Byte 7 / Byte 15	Page
Data send	DTSD	31H	0 0 0 0 0 0 0 0	CB | FRBC | TXBC	BC	BC	BUFA	BUFA	BUFA	60
		TXDT	TXDT	TXDT	TXDT	TXDT	TXDT	TXDT	TXDT	
Memory -area setting	MSET	34H	0 0 0 0 0 0 0 0	ADDR (L)	ADDR (M)	ADDR (H)	NLCW	NLSW	NLRBW	63
Operation mode setting	MDST	35H	0 0 0 0 0 0 0 0	FCS | TFIL | CODE | CLK | DMAW | DMAB | CPU	LOOP | STEP | OCT | SHORT | AUTO	0 | LAPD | BUFE | BUFC | GICS | TXED | LOAK	0 0 0 0 | STBC	TIME	RXBS	64
		RXBS	MAXD	MAXD	HOLD	TXUR | RETN				
Receive address field setting	AFST	36H	0 0 0 0 0 0 0 0	0 0 0 0 | BC	AF	AF	AF	AF	AF	72
		AF	AF	AF	AF	AF	AF	AF		
Line open	LOPN	37H	0 0 0 0 0 0 0 0							74
Line close	LCLS	38H	0 0 0 0 0 0 0 0							75
Memory area read	MARD	3AH	0 0 0 0 0 0 0 0							76
Operation mode read	MDRD	3BH	0 0 0 0 0 0 0 0							77

Table D-1. COMMAND LIST (2/2)

Command No.	Symbol	Byte 0 / Byte 8	Byte 1 / Byte 9	Byte 2 / Byte 10	Byte 3 / Byte 11	Byte 4 / Byte 12	Byte 5 / Byte 13	Byte 6 / Byte 14	Byte 7 / Byte 15	Page
Receive address field read	AFRD	3CH	0 0 0 0 0 0 0 0							78
Statistical information read	SIRD	3DH	0 0 0 0 0 0 0 0							79
General-purpose output pin write	GOWR	41H	0 0 0 0 0 0 0 0	0 0 0 0 0 0 GO2F GO1F						80
General-purpose input/output pin read	GPRD	42H	0 0 0 0 0 0 0 0							81
Statistical information read 2	SIRE	44H	0 0 0 0 0 0 0 0	SIN0	SIN1					82
General-purpose input/output pin read 2	GPRE	45H	0 0 0 0 0 0 0 0							83
Operation mode setting 2	MDSE	46H	0 0 0 0 0 0 0 0	0 0 GICS SHORT AUTO						84
Receive address field setting 2	AFSE	47H	0 0 0 0 0 0 0 0	0 0 0 0 BC	AF	AF	AF	AF	AF	85
		AF	AF	AF	AF	AF	AF	AF		

Table E-1. STATUS LIST (1/2)

Status No.	Symbol	Byte 0 / Byte 8	Byte 1 / Byte 9	Byte 2 / Byte 10	Byte 3 / Byte 11	Byte 4 / Byte 12	Byte 5 / Byte 13	Byte 6 / Byte 14	Byte 7 / Byte 15	Page
Data receive	DTRV	31H	Don't care	CB, FRBC, RXBC	BC	BC	BUFA	BUFA	BUFA	88
		RXDT	RXDT	RXDT	RXDT	RXDT	RXDT	RXDT	RXDT	
Data transmission stop	TXUR	32H	TXUR							90
Idle monitor timer timeout	TOUT	33H								91
Line open completion	LOAK	37H								92
Line close completion	LCAK	38H								93
Data transmission completion	TXED	39H	TXEN							94
Memory area read acknowledge	MAAK	3AH	Don't care	ADDR	ADDR	ADDR	NLCW	NLSW	NLRBW	95
		Don't care	ROM Version							
Operation mode read acknowledge	MDAK	3BH	Don't care	FCS, TFIL, CODE, CLK, DMAW, DMAB, CPU	LOOP, STEP, OCT, SHORT, AUTO	TXUR, BUFE, BUFC, GICS, TXED, LOAK	STBC	TIME	RBS	96
		RBS	MAXD	MAXD	HOLD	RETN				

Table E-1. STATUS LIST (2/2)

Status No.	Symbol	Byte 0 / Byte 8	Byte 1 / Byte 9	Byte 2 / Byte 10	Byte 3 / Byte 11	Byte 4 / Byte 12	Byte 5 / Byte 13	Byte 6 / Byte 14	Byte 7 / Byte 15	Page
Receive address field read acknowledge	AFAK	3CH	Don't care	| | | | | BC	AF	AF	AF	AF	AF	97
		AF	AF	AF	AF	AF	AF	AF		
Statistical information read acknowledge	SIAK	3DH	COUNT	OVRN	UNRN	IDLE	SHORT	ADDR	LONG	98
		ABORT	FCS	FRAC	FLSW	FLRBW				
Command illegal	CILG	3FH	ILST	LSTN	LCWN	CMDN				101
General-purpose input pin change detection 1	GI1C	40H	| | SYNC IDLE GI2F GI1F GO2F GO1F							102
General-purpose input pin change detection 2	GI2C	41H	| | SYNC IDLE GI2F GI1F GO2F GO1F							104
General-purpose input/output pin read acknowledge	GPAK	42H	| | SYNC IDLE GI2F GI1F GO2F GO1F							106
Status table overflow	OLSW	43H	| | | | GI2F GI1F GO2F GO1F	LSTN						108
Statistical information read acknowledge 2	SIAF	44H	SIN0	SIN1						110
General-purpose input/output pin read acknowledge 2	GPAE	45H	| | SYNC IDLE GI2F GI1F GO2F GO1F							111

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