# APT POWER MOS IV™ COMMERCIAL AND CUSTOM DIE



## INTRODUCTION:

The purpose of this APT Note is to describe the **Power MOS IV™** Transistor Die available from Advanced Power Technology. These Power MOSFET Devices provide the same technology, high performance and reliability as the equivalent series of APT packaged products. Hybrid/Module type packaging applications will benefit from APT's design efficiency. The following sections: Device Characteristics, Wafer and Die Processing, Product Handling and Shipping, Quality Indicator Points, Assembly Techniques, Optional Testing, and Special Requirements are included to aid the customer with respect to APT's unique product.

## POWER MOS IV™ DIE FEATURES AND ADVANTAGES TO USERS:

| | |
|---|---|
| Power MOS IV™ Design | Faster Switching Speeds lower capacitances |
| Large Die Sizes | Higher usable currents lower "on" resistances lower thermal resistances |
| Broad Product Range | Full range of blocking voltages from 200 - 1000 volts and "on" resistances from 0.021 to 4.2 ohms |
| Multiple Round Source Bond Pads | Flexibility in hybrid package layout |
| Thick (2 micron) top aluminum metalization | Excellent wire bondability |
| Ti-Ni-Ag Backmetal (1 micron thick) | Excellent die bondability |
| Complete wafer fab capability located in Bend, Oregon | Die availability 6 weeks ARO (many die currently in stock or in-process and available sooner) |
| Product available in wafer or die form | Maximum manufacturing flexibility |

## DEVICE CHARACTERISTICS:

Five standard APT **Power MOS IV™** Die sizes are currently available. Die sizes are Die 104, Die 105, Die 106, Die 107, and Die 108 from smallest to largest respectively.

APT's **Power MOS IV™** die are individually probed at room temperature to the electrical specifications defined in Table 1. Due to limitations imposed when probing wafers, some specifications/conditions of equivilent packaged devices cannot be tested in die form. Parameters such as Thermal Resistance ($R_{\theta}JC$), Total Power Dissipation ($P_D$), Safe Operating Area (SOA), and Clamped Inductive Current (ILM) are dependent upon packaging techniques. High current package test conditions like those associated with RDS(on) and Vds(on) are scaled down to one-ampere for probing as shown in Table 1.

Dynamic characteristics such as capacitance, gate charge, and switching times as well as source-drain diode reverse recovery time/charge are guaranteed by design. Please refer to referenced product data sheets for detailed dynamic parameters.

Figure 1 presents die topographical layout details.

## WAFER AND DIE PROCESSING:

Figure 2 describes the standard Commercial **Power MOS IV™** process flow for die sales products. The flow describes major process steps with associated quality indicator points. Operations like 100% wafer probe, post wafer saw visual and electrical inspection, and post die pack visual and electrical inspection are included and crucial to process control.

**QUALITY INDICATOR POINTS:**

**Die Visual Inspection** - occurs throughout the wafer fabrication process as well as the following process points:

- Post Wafer Mount And Saw
- Post Die Pack
- Final outgoing QA

Die products are 100% visual inspected for chips, scratches, metal and passivation voids, and foreign materials.

**Die Electrical Inspection** - Die samples are probed for critical electrical parameters at the above process points to insure processing integrity.

**Product Handling and Shipping** - APT **Power MOS IV™** die should be handled with extreme caution, using a soft pick-up tool. Handling care is exercised from die singulation through Pack and Ship. Dice are arranged in antistatic die packs and layered with antistatic material for additional ESD protection and to eliminate die shuffling within the package during shipping and transportation or storage. Die packs are then vacuum sealed in antistatic bags prior to shipment.

APT die products are passivated for maximum moisture and mechanical protection. However, once opened, apply ESD and handling precautions that one would use with all MOS semiconductor products. Minimal die surface handling and dry inert storage should be emphasized.

**ASSEMBLY TECHNIQUES:**

**Pre-Assembly Die Cleaning** - If pre-assembly cleaning is performed, it is suggested that the process include:

- Cascading Deionized Water Rinse
- Agitated Isopropy Alcohol Bath
- Pressurized $N_2$ blow-off

**Die Mount** - Solder preforms compatible with titanium-nickel-silver backside metal (drain contact) can be used, although final selection should be determined by package design and subsequent operations. A belt furnace with a forming gas atmosphere and a peak temperature of 450-475°C is recommended. Die mount surfaces should be free of contaminants that would inhibit wetting of the preform material. For specific applications, contact Advanced Power Technology's Product Engineering Department.

**Wire Bond** - It is recommended that the source wires be 10 or 12 mil aluminum wire and the gate wire 4-5 mil aluminum wire. An example bonding diagram is enclosed. All bonds must be **limited to the pad area.** We suggest that each source pad is bonded for optimized current handling capability. Gate bonding should be performed as follows:

- Die 104,105,and 106 either bond pad
- * Die 107 should as a minimum, have **both outside or both inside** bond pads wirebonded
- Die 108 should have any gate pad bonded

**Seal/Encapsulation** - Prior to hermetic seal, units should be dehydrated in a 175°C oven at greater than 26 inches vacuum for a minimum of 4 hours. An inert gas sealing atmosphere containing less than 50 PPM moisture must be maintained. It is suggested for non-hermetic package type processes that a die coat material be used prior to encapsulation.

**Optional Testing** - Systems are developed for customer procurement of APT **Power MOS IV™** die assembled and tested to various military/custom classifications and options. The standard options are defined in Figure 3 and are available for most die sizes using the TO-3 Package.
We are pleased to provide you with die and invite you to call us to discuss the results of your evaluation.

**Notes:**

*Advanced Power Technology cannot be held responsible for **Power MOS IV™** die exposed to further assembly related processes, i.e., Die Mount, Wire Bond, and Encapsulation.
*Standard static sensitive device handling precautions should be followed.
*Non-Conformance to specification must be reported to APT in writing within 30 days of receipt of shipped product lot.
*APT reserves the right to improve its process and/or design without notice.
*Storing die products in vacuum sealed bags and under dry/clean N2, users can expect a 5 year storage life.

## ELECTRICAL SPECIFICATIONS FOR APT POWER MOS IV DICE



| WER MOS IV DIE SIZE | APT PART NUMBER | RATED BVDSS @ ID=.25mA (V) MIN | RDS(ON) @ ID=1A VGS=10V (OHMS) MAX | VGS(th) @ ID=1mA VDS=VGS MIN(V) | MAX | IGSS @ VGS=30V (nA) MAX | IDSS @ MAX RATED BVDSS (mA) MAX | VDS(ON) @ ID=1A (mV) MAX |
|---|---|---|---|---|---|---|---|---|
| 104 | APT1004RDN | 1000 | 4 | | | | | |
| 99 X 204 | APT904RDN | 900 | 4 | | | | | |
| (MILS) | APT802R4DN | 800 | 2.4 | | | | | |
| | APT752R4DN | 750 | 2.4 | | | | | |
| | APT601R3DN | 600 | 1.3 | 2 | 4 | 100 | 0.25 | 900 |
| | APT551R3DN | 550 | 1.3 | | | | | |
| | APT5085DN | 500 | 0.85 | | | | | |
| 49/DIE | APT4585DN | 450 | 0.85 | | | | | |
| PACK | APT4065DN | 400 | 0.65 | | | | | |
| | APT3565DN | 350 | 0.65 | | | | | |
| 105 | APT1002RDN | 1000 | 2 | | | | | |
| 90 X 250 | APT902RDN | 900 | 2 | | | | | |
| (MILS) | APT801R2DN | 800 | 1.2 | | | | | |
| | APT751R2DN | 750 | 1.2 | | | | | |
| | APT6060DN | 600 | 0.6 | 2 | 4 | 100 | 0.25 | 850 |
| | APT5560DN | 550 | 0.6 | | | | | |
| | APT5040DN | 500 | 0.4 | | | | | |
| 25/DIE | APT4540DN | 450 | 0.4 | | | | | |
| PACK | APT4030DN | 400 | 0.3 | | | | | |
| | APT3530DN | 350 | 0.3 | | | | | |
| | APT1001RDN* | 1000 | 1 | | | | | |
| | APT901RDN* | 1000 | 1 | | | | | |
| 106 | APT1001R1DN | 1000 | 1.1 | | | | | |
| 54 X 414 | APT901R1DN | 900 | 1.1 | | | | | |
| (MILS) | APT8075DN | 800 | 0.75 | | | | | |
| | APT7575DN | 750 | 0.75 | | | | | |
| | APT6040DN | 600 | 0.4 | | | | | |
| | APT5540DN | 550 | 0.4 | | | | | |
| | APT6030DN* | 600 | 0.3 | 2 | 4 | 100 | 0.25 | 800 |
| | *APT5530DN* | 550 | 0.3 | | | | | |
| 60/DIE | APT5025DN | 500 | 0.25 | | | | | |
| PACK | APT4525DN | 450 | 0.25 | | | | | |
| | APT5023DN* | 500 | 0.23 | | | | | |
| | APT4523DN* | 450 | 0.23 | | | | | |
| | APT5020DN* | 500 | 0.2 | | | | | |
| | APT4520DN* | 450 | 0.2 | | | | | |
| | APT4020DN | 400 | 0.2 | | | | | |
| | APT3520DN | 350 | 0.2 | | | | | |
| 107 | APT10040DN | 1000 | 0.4 | | | | | |
| 88 X 388 | APT9040DN | 900 | 0.4 | | | | | |
| (MILS) | APT8030DN | 800 | 0.3 | | | | | |
| | APT7530DN | 750 | 0.3 | | | | | |
| | APT6017DN | 600 | 0.17 | | | | | |
| | APT5517DN | 550 | 0.17 | 2 | 4 | 100 | 0.25 | 750 |
| | APT5011DN | 500 | 0.11 | | | | | |
| | APT4511DN | 450 | 0.11 | | | | | |
| 25/DIE | APT40M80DN | 400 | 0.08 | | | | | |
| PACK | APT35M80DN | 350 | 0.08 | | | | | |
| | APT20M40DN | 200 | 0.04 | | | | | |
| | APT10021DN | 1000 | 0.21 | | | | | |
| 108 | APT9021DN | 900 | 0.21 | | | | | |
| 85 X 738 | APT8016DN | 800 | 0.16 | | | | | |
| (MILS) | APT7516DN | 750 | 0.16 | | | | | |
| | APT60M90DN | 600 | 0.09 | | | | | |
| | APT55M90DN | 550 | 0.09 | 2 | 4 | 100 | 0.25 | 700 |
| | APT50M60DN | 500 | 0.06 | | | | | |
| | APT45M60DN | 450 | 0.06 | | | | | |
| /DIE | APT40M42DN | 400 | 0.042 | | | | | |
| ACK | APT35M42DN | 350 | 0.042 | | | | | |
| | APT20M21DN | 200 | 0.021 | | | | | |

* PRELIMINARY, CONTACT FACTORY FOR ADDITIONAL INFORMATION.

# DIE TOPOGRAPHICAL LAYOUT FOR APT POWER MOS IV™ DIE

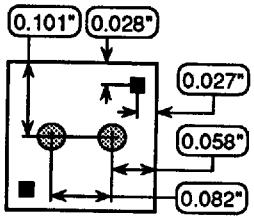


## APT-104

Die Size = .199" x .203"

Source Pads = .035" Dia.

Gate Pads = .018" x .019"

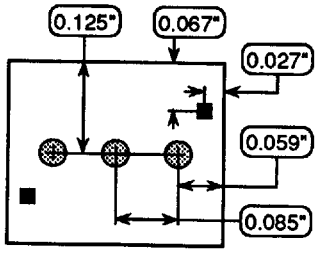



## APT-105

Die Size = .290" x .250"

Source Pads = .035" Dia.

Gate Pads = .018" x .019"

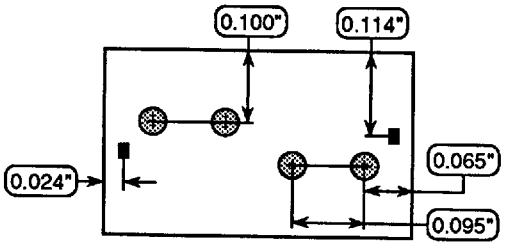



## APT-106

Die Size = .414" x .254"

Source Pads = .035" Dia.

Gate Pads = .014" x .019"

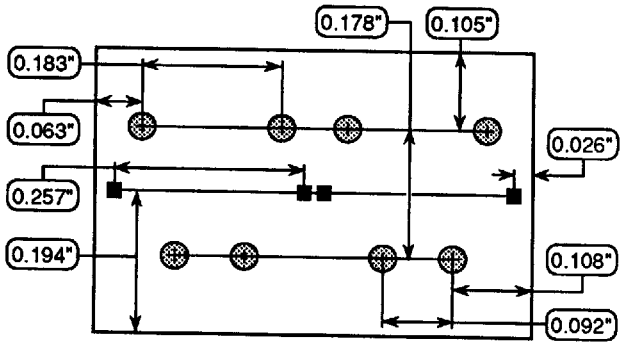



## APT-107

Die Size = .588" x .388"

Source Pads = .035" Dia.

Gate Pads = .018" x .019"




## APT-108

Die Size = .738" x .585"

Source Pads = .032" x .046"

Gate Pads = .019" x .019"

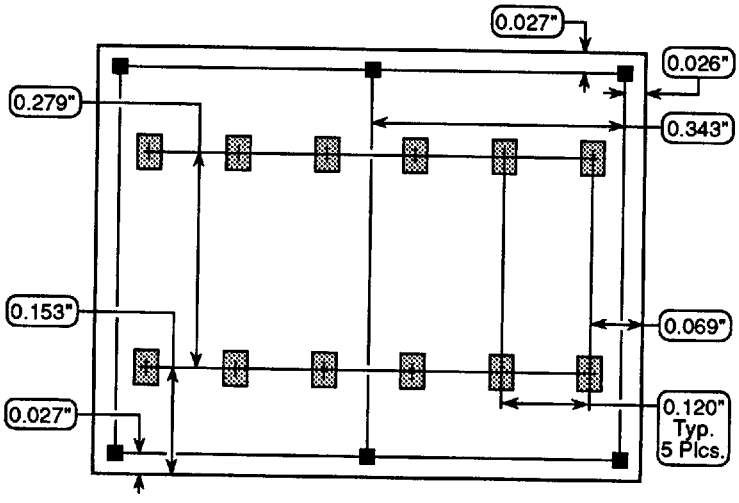



**FIGURE 1**