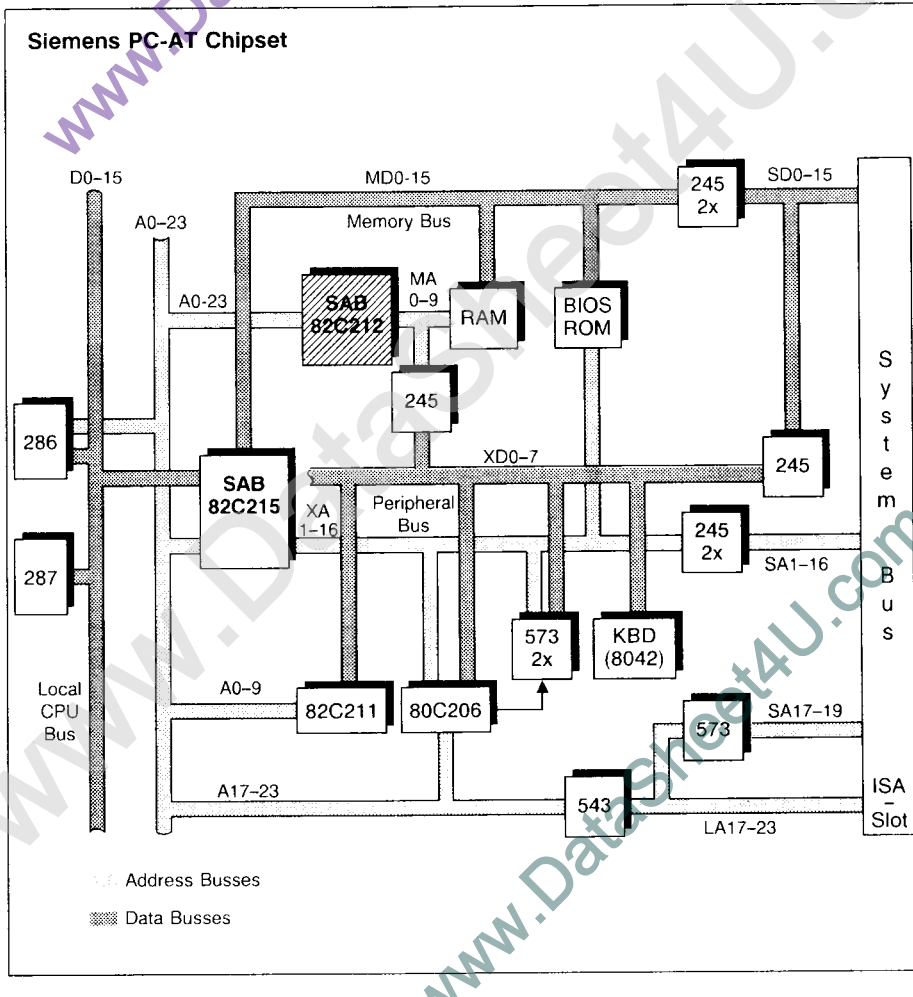
SIEMENS

SAB 82C212

Page/Interleave Memory Controller of Siemens PC-AT™ Chipset

Advance Information



- Higher performance of DRAM accesses using page mode access together with a interleaved memory accessing scheme
- Page interleaved operation with 16 MHz CPU and 100 ns DRAMs.
- Remapping of DRAM resident in 640 K to 1 MByte area as extended memory
- Supports Expanded Memory System (LIM-EMS 4.0) address translation logic
- Shadow RAM feature for fast BIOS code execution.
- Supports up to 8 MByte on-board DRAM (1 M/256 K DRAM's)
- Optimized fast switching between SAB 80286 protected and real mode for OS/2
- Staggered DRAM refresh for power supply noise reduction
- CMOS implementation for high speed and low power requirements
- 84-pin plastic leaded chip carrier package (PL-CC-84)

As a member of the Siemens PC-AT Chipset the SAB 82C212 memory controller provides an interleaved memory subsystem design with page mode operation. Also EMS address translation and shadow RAM for BIOS execution are supported.
The SAB 82C211 CPU/Bus controller, the SAB 82C212 memory controller, the SAB 82C215 data/address buffer and the SAB 82C206 integrated peripheral controller provide a highly integrated high performance system solution for PC-AT compatible systems.
The SAB 82C212 is fabricated in Siemens ACMOS technology and packaged in a 84-pin plastic leaded chip carrier package (PL-CC-84).

Ordering Information

Type	Ordering code	Package	Function
SAB 82C212-12-N	Q67120-P294	PL-CC-84 (SMD)	Page/Interleaved Memory Controller for Siemens PC-AT Chipset (12 MHz)
SAB 82C212-16-N	Q67120-P295	PL-CC-84 (SMD)	Page/Interleaved Memory Controller for Siemens PC-AT Chipset (16 MHz)

Figure 1
Logic Symbol

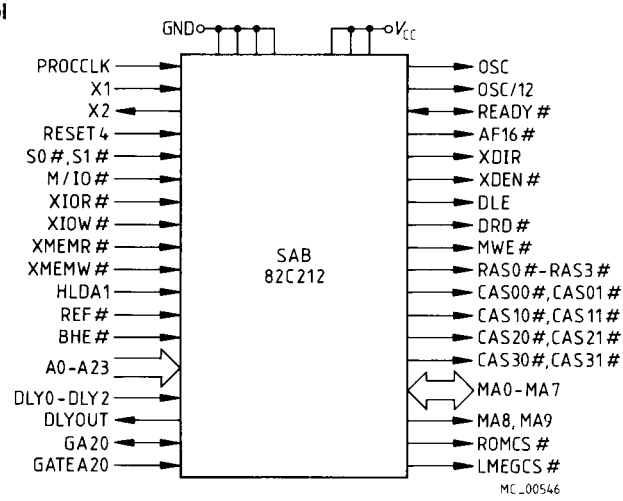
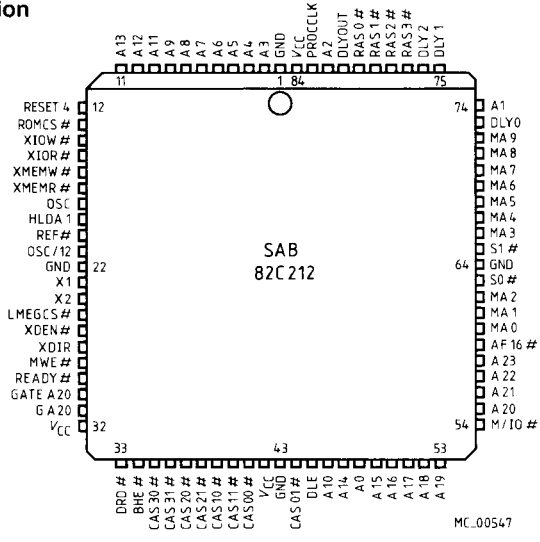


Figure 2
Pin Configuration



Pin Definitions and Functions

Symbol	Pin	Input (I) Output (O)	Function
Clocks and Control			
PROCCLK	83	I	**Processor Clock** PROCCLK is the clock input line from the SAB 82C211.
X1	23	I	**Crystal 1** X1 is the input of the crystal oscillator circuit. Typically a 14.31818 MHz crystal is connected to X1.
X2	24	O	**Crystal 2** X2 is the output of the crystal oscillator circuit. Typically a 14.31818 MHz crystal is connected to X2.
OSC	18	O	**Oscillator Output** OSC is the oscillator output for the system clock at 14.31818 MHz and has a drive capability of 24 mA.
OSC/12	21	O	**Oscillator/12 Output** OSC/12 is an output with a clock frequency equal to 1/12 of the crystal frequency across the X1, X2 pins.
RESET4	12	I	**Reset Line 4** RESET 4 is the active high reset input from the SAB 82C211. It resets the configuration registers to their default values. When active, RAS0-3# and CAS00-31# remain high, OSC and OSC/12 remain inactive.
REF#	20	I	**Refresh#** REF# is an active low input for DRAM refresh control from the SAB 82C211. It initiates a refresh cycle for the DRAMs.
S1# S0#	65 63	I I	**Status Inputs 0, 1#** S0#, S1# are the status lines from the 80286 CPU. These lines are monitored to detect the start of a cycle.
M/IO#	54	I	**Memory/IO Control#** M/IO# is a signal from the 80286 CPU. If high it indicates a memory cycle. If low, it indicates an I/O cycle.
XIOR#	15	I	**X-Bus I/O Read#** XIOR# is the active low I/O read command line.

Pin Definitions and Functions

Symbol	Pin	Input (I) Output (O)	Function
Clocks and Control (cont'd)			
XIOW#	14	I	**X-Bus I/O Write#** XIOW# is the active low I/O write command line.
XMEMR#	17	I	**X-Bus Memory Read#** XMEMR# is the active low memory ready command line.
XMEMW#	16	I	**X-Bus Memory Write#** XMEMW# is the active low memory write command line.
HLDA1	19	I	**Hold Acknowledge 1** HLDA1 is an active high input from the SAB 82C211. It is used to generate RAS# and CAS# signals for DMA cycles, in response to a hold request.
ROMCS#	13	O	**ROM Chip Select#** ROMCS# is an active low chip select output to the BIOS EPROM. It can be connected to the output enable pin of the EPROM.
A0-A23	1)	I	**Address Inputs 0-23** A0-23 are the address input lines from the local CPU bus.
BHE#	34	I	**Byte High Enable#** BHE# is an active low input from the CPU for transfer of data on the upper byte.
READY#	29	I/O	**Ready#** READY# is the system ready signal to the CPU. It is an active low output after requested memory or I/O data transfer is completed. It is an input when the current bus cycle is an AT bus cycle and is an output for local memory and I/O cycles.
AF16#	59	O	**AF16#** AF16# is an active low output asserted on local memory (EPROM or DRAM) cycles. It is high for all other cycles. This signal is sampled by the SAB 82C211.

1) For detailed pin numbers see figure 2 (Pin configuration).

Pin Definitions and Functions

Symbol	Pin	Input (I) Output (O)	Function
DRAM Interface			
RAS0-3#	80-77	O	**Row Address Strobe 0-3#** RAS0-3# are active low outputs used as RAS# signals to the DRAMs for selecting different banks. RAS3# selects the highest bank and RAS0# selects the lowest bank. These signals should be buffered and line terminated with 75 Ω resistors to reduce ringing before driving the DRAM RAS# lines.
CAS00#	41	O	**Column Address Strobe 00#** CAS00# is an active low output used to select the low byte DRAMs of bank 0. This signal should be line terminated with a 75 Ω resistor to reduce ringing before driving the DRAM CAS# line.
CAS01#	44	O	**Column Address Strobe 01#** CAS01# is an active low output used to select the high byte DRAMs of bank 0. This signal should be line terminated with a 75 Ω resistor to reduce ringing before driving the DRAM CAS# line.
CAS10#	39	O	**Column Address Strobe 10#** CAS10# is an active low output used to select the low byte DRAMs of bank 1. This signal should be line terminated with a 75 Ω resistor to reduce ringing before driving the DRAM CAS# line.
CAS11#	40	O	**Column Address Strobe 11#** CAS11# is an active low output used to select the high byte DRAMs of bank 1. This signal should be line terminated with a 75 Ω resistor to reduce ringing before driving the DRAM CAS# line.
CAS20#	37	O	**Column Address Strobe 20#** CAS20# is an active low output used to select the low byte DRAMs of bank 2. This signal should be line terminated with a 75 Ω resistor to reduce ringing before driving the DRAM CAS# line.
CAS21#	38	O	**Column Address Strobe 21#** CAS21# is an active low output used to select the high byte DRAMs of bank 2. This signal should be line terminated with a 75 Ω resistor to reduce ringing before driving the DRAM CAS# line.

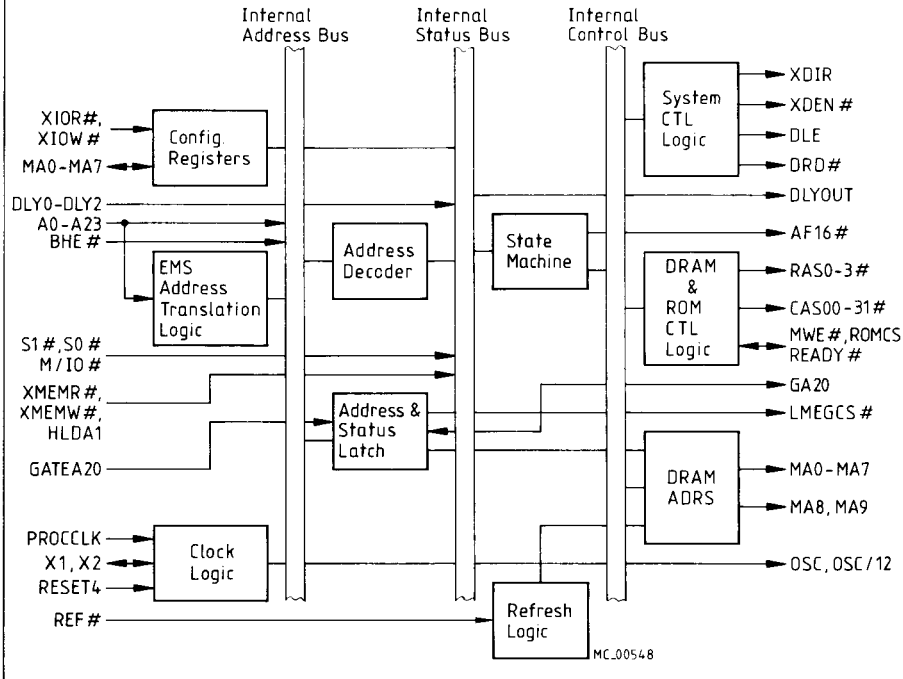
Pin Definitions and Functions

Symbol	Pin	Input (I) Output (O)	Function
DRAM Interface (cont'd)			
CAS30#	35	O	**Column Address Strobe 30#** CAS30# is an active low output used to select the low byte DRAMs of bank 3. This signal should be line terminated with a 75 Ω resistor to reduce ringing before driving the DRAM CAS# line.
CAS31#	36	O	**Column Address Strobe 31#** CAS31# is an active low output used to select the high byte DRAMs of bank 3. This signal should be line terminated with a 75 Ω resistor to reduce ringing before driving the DRAM CAS# line.
MWE#	28	O	**Memory Write Enable#** MWE# is an active low output for DRAM write enable.
DLE	45	O	**Data Latch Enable** DLE is an active high output used to enable the local memory data buffer latch in the SAB 82C215.
DRD#	33	O	**Data Read#** DRD# is an active low output used to transfer data from the memory bus to the local CPU bus in the SAB 82C215. If high it sets the data path from the local CPU bus to the memory bus.
DLYOUT	81	O	**Delay Line Out** DLYOUT is an active high output to the delay line for generating the DRAM control signals.
DLY0 DLY1 DLY2	73 75 76	I I I	**Delay Input 0-2** DLY0-2 are active high inputs from the first to third taps of the delay line used to generate DRAM control signals.
XDEN#	26	O	**X-Data Buffer Enable#** XDEN# is an active low output asserted during I/O accesses to locations 22 H and 23 H. These locations contain the index and data registers for the Siemens PC-AT Chipset. It is used to enable the buffers between the XD and MA buses for accessing the SAB 82C212 internal registers.

Pin Definitions and Functions

Symbol	Pin	Input (I) Output (O)	Function
DRAM Interface (cont'd)			
XDIR	27	O	**X-Bus Direction** XDIR is used to control the drivers between the X and S busses. The driver should be used such that data flow is from the S to X bus when XDIR is high and in the other direction when XDIR is low.
MA8 MA9	71 72	O O	**Multiplexed DRAM Address 8, 9** The MA8, 9 address lines should be buffered and line terminated with 75 Ω resistors before driving the DRAM address lines.
MA0-2 MA3-7	60-62 66-70	I/O I/O	**Multiplexed DRAM Address 0-7** MA0-MA7 are used as bi-directional lines to read write to the internal registers of the SAB 82C212. An external 74ALS245 buffer is required to isolate this path during normal DRAM operation. These lines should be buffered and line terminated with 75 Ω resistors before driving the DRAM address lines.
Miscellaneous			
GA20	31	I/O	**Gated Address Line A20** GA20 is the gated A20 address bit which is controlled by GATEA20.
GATEA20	30	I	**Gate Address 20** GATEA20 is an input used to force GA20 low when GATEA20 is low. When high it propagates A20 onto the GA20 line. It is used to keep address under 1 Mbyte during DOS operation.
LMEGCS#	25	O	**Low Meg Memory Chip Select** LMEGCS# is an unlatched active low output asserted when the low Meg memory address space (0 to 1024 Kbytes) is accessed or during refresh cycles. It is used to disable SMEMR# and SMEMW# signals on the AT bus if access are made beyond the 1 Mbyte address space to maintain PC and PC XT compatibility.
V_{CC}	32, 42, 84	–	Power Supply (+ 5 V)
GND	1, 22, 43, 64	–	Ground (0 V)

Figure 3
Block Diagram



Functional Description

The SAB 82C212 Page/Interleave memory controller of the Siemens PC-AT Chipset provides the following functional submodules:

- EPROM and DRAM control logic
- System control logic
- Memory mapping and refresh logic
- Oscillator clock generation logic
- Configuration registers

Prior to the description of these functional submodules the following section describes some principles of the SAB 82C212 integrated features.

Overview

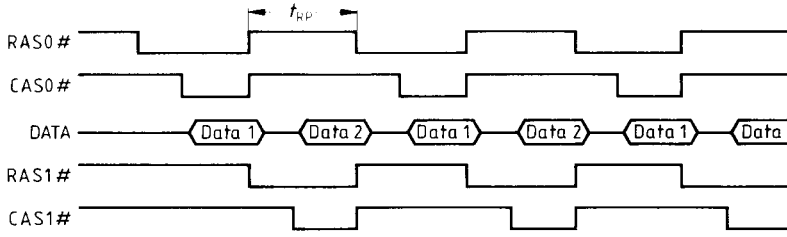
The SAB 82C212 performs the memory control functions in the Siemens PC-AT Chipset system, utilizing page mode access DRAMs. The various possible memory array configurations and page/interleaved mode operation are discussed in this section.

Memory Array Configuration

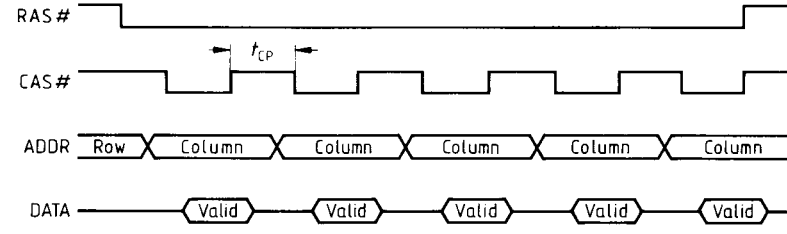
The SAB 82C212 organizes memory as banks of 18-bit modules, consisting of 16-bits of data and 2-bits of parity information. The 16-bits of data are split into high and low order bytes, with one parity bit for each byte. This configuration can be implemented by using eighteen 1-bit wide DRAMs or by using four 4-bit wide DRAMs for data with two 1-bit wide DRAMs for parity. The minimum configuration can be a single bank operating in non-interleaved mode or can be a pair of DRAM banks operating in two way interleaved mode. If the SAB 82C212 uses a two way interleaving scheme, the DRAMs within a pair of banks must be identical. However, each bank of DRAM pairs can be different from other pairs. For example, banks 0, 1 may have 256 K by 1-bit DRAMs and banks 2 and 3 could have 1 M by 1-bit DRAMs. A typical system may be shipped with one or two banks of smaller DRAM types (e.g. 256 K by 1-bit DRAMs) and later upgraded with additional pairs of banks of larger DRAMs (e.g. 1 M by 1-bit DRAMs).

Figure 4
DRAM Access Schemes

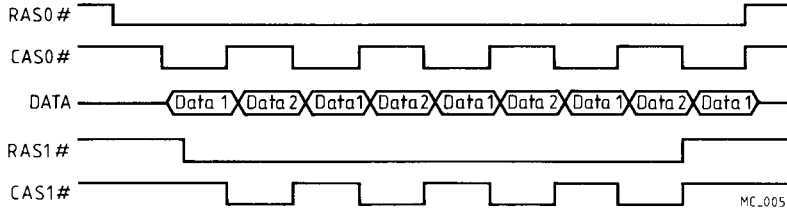
a) 2-Way DRAM Interleaved Operation



b) DRAM Page Mode Operation



c) 2-Way DRAM Page/Interleave Operation



Page/Interleaved Operation

The SAB 82C212 uses a page/interleaved design that is different from most interleaved memory designs. Typical two way interleaving schemes use two banks of DRAMs with even word addresses on one bank and odd word addresses on the other bank. If memory accesses are sequential, the RAS# precharge time of one bank overlaps the access time of the other bank. Typically, programs consist of instruction fetches interspersed with operand accesses. The instruction fetches tend to be sequential and the operand accesses tend to be random.

Figure 4a is a sequence diagram for a memory interleaved scheme using two banks 0 and 1. The RAS# signals of the two banks are interleaved so that the RAS# precharge time (t_{RP}) of one bank is used for the RAS# active time in the other bank. This requires sequential accesses to be alternating between the two banks. For non-sequential accesses, it is possible to get wait states due to a 'miss'. Typically, this results in a 50 % hit ratio (possible zero wait state accesses).

Figure 4b is a sequence diagram of a paged mode DRAM operation. In paged mode DRAMs, once a row access has been made, it is possible to access subsequent column addresses within that row, without the RAS# precharge penalty. However, after a RAS# active timeout, there is a RAS# precharge period which typically occurs every 10 micro-seconds. Since the CAS# precharge time t_{CP} is small, it is possible to make fast random accesses within a selected row. Typically, page mode access times are half the normal DRAM access times. For 256 K × 1 DRAMs, each row has 512-bits. If eighteen 256 K × 1-bit DRAMs are used to implement a bank, a page would have 512 × 2 Bytes (excluding 2-bits for parity) = 1 Kbytes. Thus paged mode DRAMs could be interleaved at 1 Kbyte boundaries rather than 2 Byte boundaries as in the regular interleaved mode operation. Any access to the currently active RAS# page would occur in a short page access time and any subsequent access could be anywhere in the same 1 Kbyte boundary, without incurring any penalty due to RAS# precharge. If memory is configured to take advantage of this DRAM organization, significantly better performance can be achieved over normal interleaving because:

1. Page mode access time is shorter than normal DRAM access time. This allows more time in the DRAM critical paths, to achieve penalty free accesses or 'hits'.
2. The possibility of the next access being fast is significantly higher than in a regular interleaving scheme. This is because instructions and data tend to cluster together by principle of locality of reference.

Figure 4c is a sequence diagram of a two way page/interleaved scheme using page mode DRAMs. As seen, it is possible to make zero wait state accesses between the two banks 0 and 1, by overlapping CAS# precharge time of the other bank. The DRAM RAS# lines for both banks can be held active till the RAS# active time out period, at which time a RAS# precharge for that bank is required. Typical hit ratios higher then 80 % are possible using this scheme. With the SAB 82C212 memory controller, using the page interleaved scheme, 150 ns access time DRAMs can be used at 12 MHz and 100 ns access time DRAMs at 16 MHz.

The SAB 82C212 supports both two and four way interleaved mode. If four way interleaved mode is used, the DRAMs used in the four banks must be identical. Table 1 shows the 0 wait state hit space for possible banks configurations.

Table 1
Average 0 Wait State Hit Space

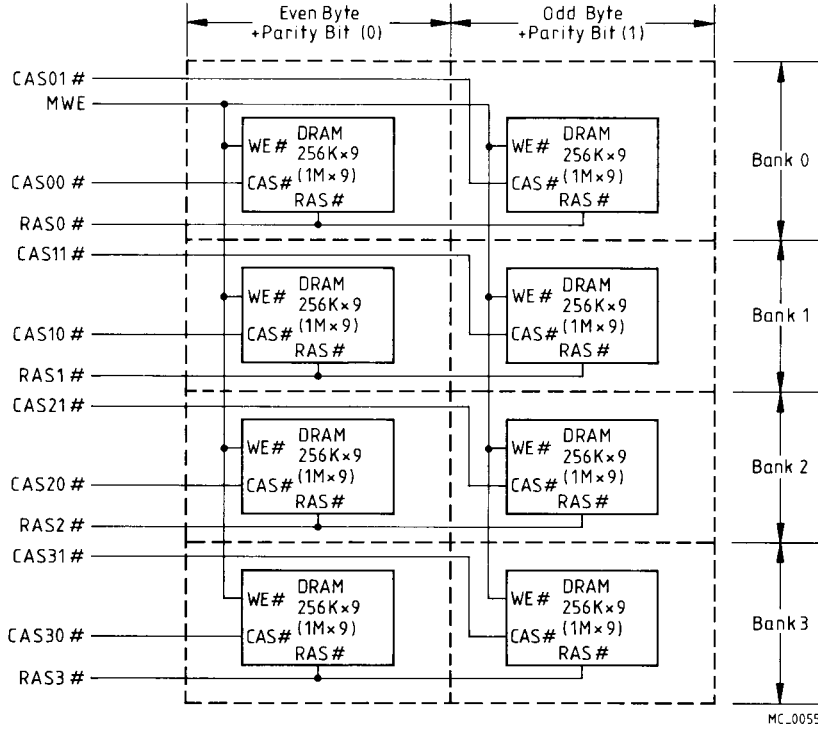
DRAM Type				Two Way Interleaved	Four Way Interleaved
Bank 0	Bank 1	Bank 2	Bank 3		
256 K	256 K	0	0	2 K	NA
256 K	256 K	256 K	256 K	2 K	4 K
256 K	256 K	1 M	1 M	3 K	NA
1 M	1 M	0	0	4 K	NA
1 M	1 M	1 M	1 M	4 K	8 K

OS/2 Optimization

The Siemens PC-AT Chipset architecture features OS/2 optimization using REG6F.1 of the SAB 82C212 in conjunction with REG60.5 of the SAB 82C211. OS/2 makes frequent DOS calls while operating in protected mode of the SAB 80286 CPU. In order to service these DOS calls, the SAB 80286 CPU has to switch from protected to real mode quickly. Typcial PC/AT architectures require the processor to issue two commands to the 8042 (or 8742) keyboard controller in order to reset the processor (to switch it into protected mode) and to activate GATEA20.

REG60.5 of the SAB 82C211 is to used to invoke a software reset to the SAB 80286 processor and REG6F.1 is used to activate GATEA20. Since this involves two I/O writes, it is possible to execute a "Fast GATEA20". In an OS/2 environment, where frequent DOS calls are made, this feature provides significant performance improvement.

Figure 5
DRAM Organization



EPROM and DRAM Control Logic

The EPROM and DRAM control logic in the SAB 82C212 is responsible for the generation of the RAS#, CAS# and MWE# signals for DRAM accesses and the generation of ROMCS# for EPROM accesses. This sub-module also generates READY# to the CPU upon completion of the desired local memory operation. The appropriate number of wait states are inserted, as programmed by software (or by default) in the wait state register of the SAB 82C212. Figure 5 is a block diagram of the DRAM organization for the Siemens PC-AT Chipset architecture. As seen, each RAS# line drives each 256 K × 18-bit bank (or 1 M × 18-bit bank). The CAS# lines are used to drive individual bytes within each bank. MWE# is connected to each DRAM bank write enable input.

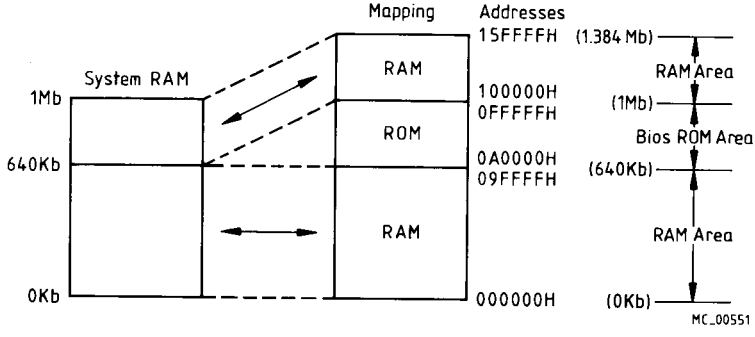
System Control Logic

This sub-module of the SAB 82C212 generates XDEN#, DLE, DRD#, AF16# for system control. XDEN# is issued for I/O accesses to the internal registers of the SAB 82C212. It is used to enable the XD0-7 lines onto the MA0-7 lines from an external buffer, for accessing the internal registers of the SAB 82C212. The DLE and DRD# signals are generated for enabling and controlling the direction of data between the CPU data bus and the memory data bus (MD bus). AF16# is issued by the SAB 82C212 state machine. It is active for local memory accesses and meets the set up and hold times with respect to PROCCLK for the SAB 82C211.

Memory Mapping and Refresh Logic

The SAB 82C212 has an extensive set of memory mapping registers for various memory organizations. Through the memory mapping logic, for up to 1 Mbyte of system RAM, it is possible to map RAM that overlaps the EPROM area (640 Kbyte - 1 Mbyte) above the 1 Mbyte area, as shown in figure 6. Hence, for 1 Mbyte of on board RAM, the software can address it from 0 to 640 Kbytes and from 1 Mbyte to 1.384 Mbytes. The EPROM can be addressed from the 640 Kbyte area to the 1 Mbyte area. For normal mode of operation, only one bank of DRAMs may be used. However, for the page/interleaved mode of operation, RAM bank pairs must be used.

Figure 6
System RAM/ROM Mapping for 1 Mbyte System RAM



Shadow RAM Feature

For efficient execution of BIOS, it is preferable to execute BIOS code through RAM rather than through slower EPROMs. The SAB 82C212 provides the shadow RAM feature which if enabled allows the BIOS code to be executed from system RAM resident at the same physical address as the BIOS EPROM. The software should transfer code stored in the BIOS EPROMs to the system RAM, before enabling the shadow RAM feature. This feature significantly improves the performance in BIOS-call intensive applications. Performance improvements as high as 300 to 400 % have been observed in benckmark tests on the shadow RAM. The shadow RAM feature is invoked by enabling the corresponding bits in the ROM enable register and the RAM mapping register.

If more than 1 Mbyte of system RAM exists, it is mapped as shown in figure 7a, if the shadow RAM feature is not invoked. This means that RAM in the 640 Kbyte to 1 Mbyte area cannot be accessed. If the shadow RAM feature is used, then the RAM is mapped as shown in figure 7b, overlapping or shadowing the EPROM area. In both cases, for accesses beyond the 1 Mbyte address range, the processor is switched from real to protected mode from BIOS.

Figure 7
RAM/ROM Mapping

a) RAM/ROM Mapping without Shadow RAM (More Than 1 Mbyte of RAM)

b) RAM Mapping with Shadow RAM (More Than 1 Mbyte of RAM)

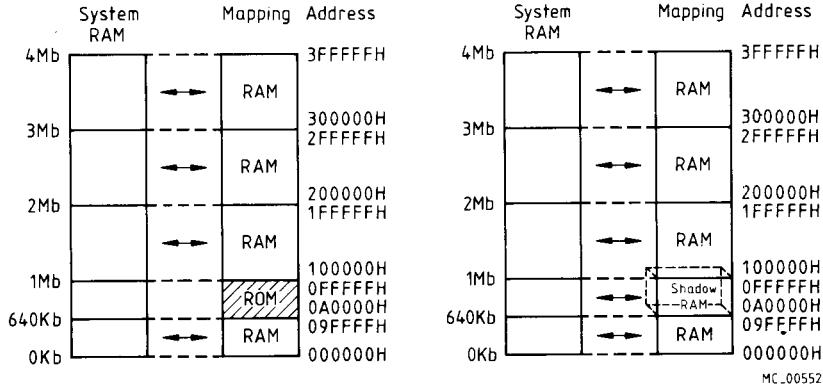
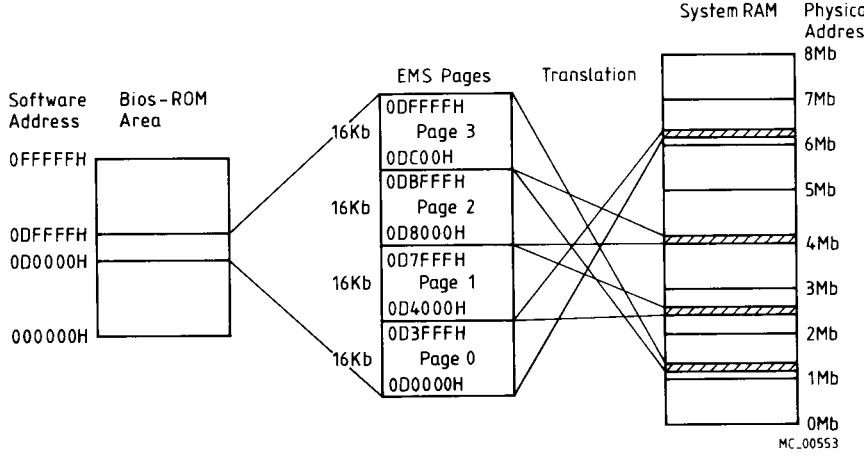


Figure 8
EMS Mapping



EMS Address Translation Logic

Expanded Memory System or EMS is a memory mapping scheme used to map a 64 Kbyte block of memory in the EPROM area D0000H-DFFFFH to anywhere in the 1 Mbyte - 8 Mbyte area. This 64 Kbyte memory block is segmented into four 16 Kbyte pages. Through a translation table, each 16 Kbyte segment can be mapped anywhere in the 1 Mbyte to 8 Mbyte area. Since the SAB 82C212 uses the translation table in the EMS mode, address lines A14 to A22 are translated by the appropriate EMS mapping register. Hence, this scheme does not require switching between user and protected mode. Figure 8 shows the EMS organization with a possible translation scheme. It is possible for the SAB 82C212 to map this 64 Kbyte block to anywhere in the 0 to 8 Mbyte area. However, it is desirable to map this block above the 1 Mbyte area in order to not use the RAM space in the 0 to 640 Kbyte area. Although the EMS scheme translates the 64 Kbyte block in the D0000H-DFFFFH area, it is possible to select a 64 Kbyte block from any other area.

Refresh Logic

During a refresh cycle, the SAB 82C211 outputs the refresh address on the A0-A9 address lines and asserts the REF# signal low to the SAB 82C212. The SAB 82C212 uses these signals to generate the refresh address on the MA0-MA9 address lines, the RAS# signals and LMEGCS#. The SAB 82C212 performs a staggered mode refresh to reduce the power supply noise generated during RAS# switching. Prior to a refresh, all RAS# lines are pulled high to ensure RAS# precharge. Following this RAS0# and RAS3# are asserted low. RAS1# and RAS2# are staggered by one delay unit using an external delay line, with respect to RAS0# and RAS3#. The RAS0#-RAS3#, RAS1#-RAS2# bundling is provided so that staggering is effective for a minimal 2 bank or a full 4 bank configuration.

Memory Configurations

It is possible to use 1-Mbit or 256-Kbit (and, in one case, 64-Kbit) DRAMs for system memory in the Siemens PC-AT Chipset. Each memory bank can be implemented with eighteen 1-bit wide DRAMs, or with four 4-bits wide plus two 1-bit wide DRAMs. Possible configurations for on-board memory are listed in table 2. Each bank is 16 bits wide plus two bits for parity. Page/interleaving is possible only for those combinations with similar pairs of DRAMs. In table 2, page/interleaving is possible with combinations 5, 6, 11, 13 and 14.

Table 2
Onboard Memory Configurations

	DRAM Type				Total	EMS
	Bank 0	Bank 1	Bank 2	Bank 3	Memory	Range
1	0	0	0	0	disable	0
2	256 K	0	0	0	512 Kbyte	0
3	1 M	0	0	0	2 Mbyte	1 Mbyte to 2 Mbyte
4	256 K	64 K	0	0	640 Kbyte	0
5	256 K	256 K	0	0	1 Mbyte	1 Mbyte to 1.384 Mbyte
6	1 M	1 M	0	0	4 Mbyte	1 Mbyte to 4 Mbyte
7	256 K	256 K	256 K	0	1.5 Mbyte	1 Mbyte to 1.5 Mbyte
8	256 K	256 K	1 M	0	3 Mbyte	1 Mbyte to 3 Mbyte
9	1 M	1 M	1 M	0	6 Mbyte	1 Mbyte to 6 Mbyte
10	256 K	64 K	256 K	256 K	1.64 Mbyte	1 Mbyte to 1.64 Mbyte
11	256 K	256 K	256 K	256 K	2 Mbyte	1 Mbyte to 2 Mbyte
12	256 K	64 K	1 M	1 M	4.64 Mbyte	1 Mbyte to 4.64 Mbyte
13	256 K	256 K	1 M	1 M	5 Mbyte	1 Mbyte to 5 Mbyte
14	1 M	1 M	1 M	1 M	8 Mbyte	1 Mbyte to 8 Mbyte

Clock Generation Logic

The SAB 82C212 has an oscillator circuit which uses a 14.31818 MHz crystal to generate the OSC and OSC/12 clocks. The 1.19381 MHz OSC/12 clock is used internally to generate the RAS# timeout clocks, one for each bank. RAS# is desserted for each bank when its RAS# timeout counter times out after about 10 Microseconds.

Configuration Registers

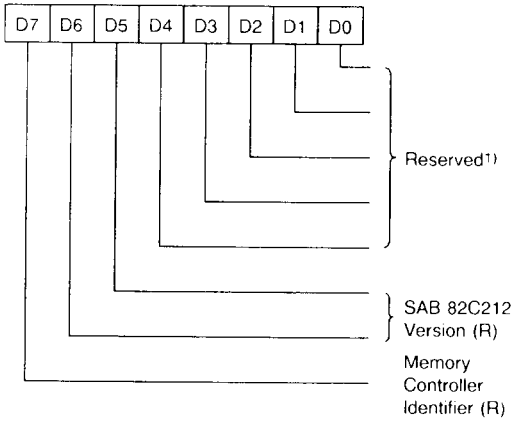
There are twelve configuration and diagnostics registers in the SAB 82C212, RB0-RB11. These are accessed through I/O ports 22 H and 23 H normally found in the interrupt controller module of the SAB 82C206 IPC. An indexing scheme is used to reduce the number of I/O addresses required to access all of the registers needed to configure and control the memory controller. Port 22 H is used as an index register that points to the required data value accessed through port 23 H. A write of the index value for the required data is performed to location 22 H. This is then decoded and controls the multiplexers gating the appropriate register to the output bus. Every access to port 23 H must be preceded by a write of the index value to port 22 H even if the same data register is being accessed again. All bits marked as "Reserved" are set to zero by default and must be maintained that way during write operations. Table 3 lists these registers.

Table 3
Indexes of Configuration Registers

Register Number	Register Name	Index
RB0	Version	64 H
RB1	ROM Configuration	65 H
RB2	Memory Enable-1	66 H
RB3	Memory Enable-2	67 H
RB4	Memory Enable-3	68 H
RB5	Memory Enable-4	69 H
RB6	Bank 0/1 Enable	6AH
RB7	DRAM Configuration	6BH
RB8	Bank 2/3 Enable	6CH
RB9	EMS Base Address	6DH
RB10	EMS Address Extension	6EH
RB11	Miscellaneous	6FH

Table 4
Version Register RB0

Index register port: 22 H
Data register port: 23 H
Index: 64 H

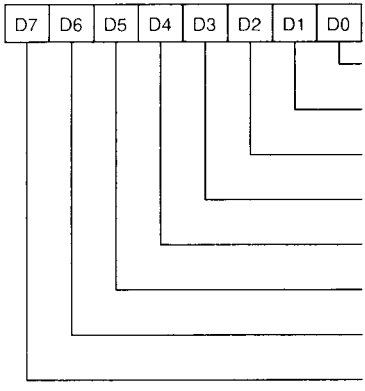


Bits	Function
7	NEAT memory controller identifier. 0 = SAB 82C212
6, 5	SAB 82C212 revision number. 00 = initial revision number
4-0	Reserved and default to 0[1].

[1] The reserved bits are recommanded to be initialized to 1.

Table 5
ROM Configuration Register RB1

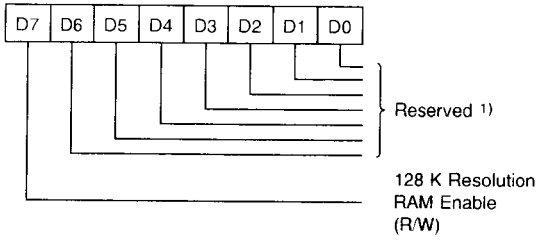
Index register port: 22 H
Data register port: 23 H (R/W)
Index: 65 H



Bits	Function
0	ROM at F0000H-FFFFH (BIOS). Default = 0 = ROM enabled. ROMCS# is generated.
1	ROM at E0000H-EFFFFH. Default = 1 = ROM disabled, Shadow RAM enabled. ROMCS# is not generated unless bit is set to 0.
2	ROM at D0000H-DFFFFH. Default = 1 = ROM disabled, Shadow RAM enabled. ROMCS# is not generated unless bit is set to 0.
3	ROM at C0000H-CFFFFH (EGA). Default = 1 = ROM disabled, Shadow RAM enabled. ROMCS# is not generated unless bit is set to 0.
4	Shadow RAM at F0000H-FFFFFH in Read/Write mode. 0 = Read/Write (default), 1 = Read only (Write protected).
5	Shadow RAM at E0000H-EFFFFH in Read/Write mode. 0 = Read/Write (default), 1 = Read only (Write protected).
6	Shadow RAM at D0000H-DFFFFH in Read/Write mode. 0 = Read/Write (default), 1 = Read only (Write protected).
7	Shadow RAM at C0000H-CFFFFH in Read/Write mode. 0 = Read/Write (default), 1 = Read only (Write protected).

Table 6
Memory Enable-1 Register RB2

Index register port: 22 H
Data register port: 23 H
Index: 66 H

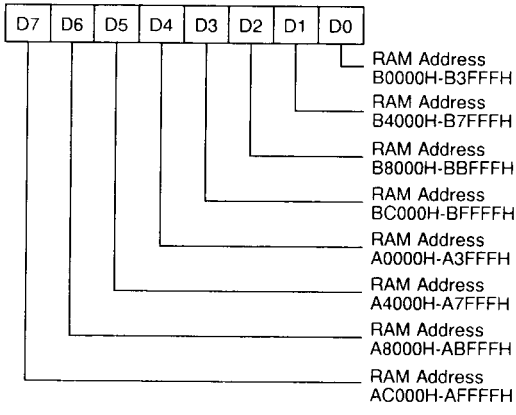


Bits	Function
0-6	Reserved and default to 0[1].
7	Address map RAM on system board in 80000H-9FFFFH area. 0 = Address is on the I/O channel (Default), 1 = Address is on the system board and is put out by the SAB 82C212.

[1] The reserved bits are recommanded to be initialized to 1.

Table 7
Memory Enable-2 Register RB3

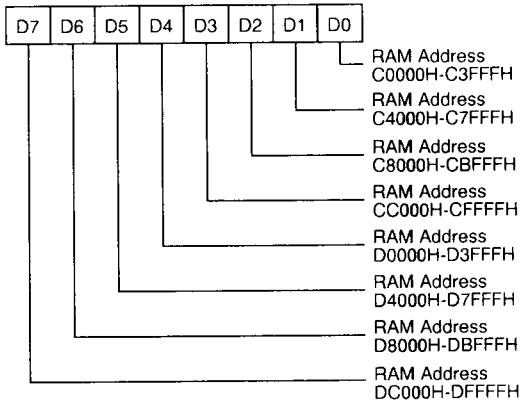
Index register port: 22 H
Data register port: 23 H (R/W)
Index: 67 H



Bits	Function
0	Enable Shadow RAM in B0000H-B3FFFH area. Disable = 0, Enable = 1.
1	Enable Shadow RAM in B4000H-B7FFFH area. Disable = 0, Enable = 1.
2	Enable Shadow RAM in B8000H-BBFFFH area. Disable = 0, Enable = 1.
3	Enable Shadow RAM in BC000H-BFFFFH area. Disable = 0, Enable = 1.
4	Enable Shadow RAM in A0000H-A3FFFH area. Disable = 0, Enable = 1.
5	Enable Shadow RAM in A4000H-A7FFFH area. Disable = 0, Enable = 1.
6	Enable Shadow RAM in A8000H-ABFFFH area. Disable = 0, Enable = 1.
7	Enable Shadow RAM in AC000H-AFFFFH area. Disable = 0, Enable = 1.

Table 8
Memory Enable-3 Register RB4

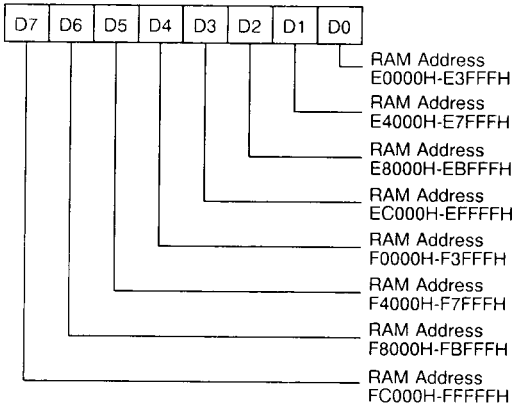
Index register port: 22 H
Data register port: 23 H (R/W)
Index: 68 H



Bits	Function
0	Enable Shadow RAM in C0000H-C3FFFH area. Disable = 0, Enable = 1.
1	Enable Shadow RAM in C4000H-C7FFFH area. Disable = 0, Enable = 1.
2	Enable Shadow RAM in C8000H-CBFFFH area. Disable = 0, Enable = 1.
3	Enable Shadow RAM in CC000H-CFFFFH area. Disable = 0, Enable = 1.
4	Enable Shadow RAM in D0000H-D3FFFH area. Disable = 0, Enable = 1.
5	Enable Shadow RAM in D4000H-D7FFFH area. Disable = 0, Enable = 1.
6	Enable Shadow RAM in D8000H-DBFFFH area. Disable = 0, Enable = 1.
7	Enable Shadow RAM in DC000H-DFFFFH area. Disable = 0, Enable = 1.

Table 9
Memory Enable-4 Register RB5

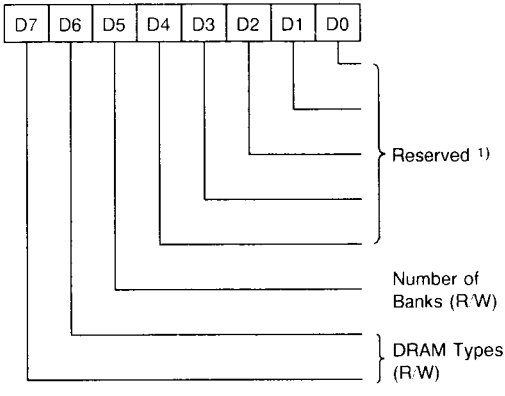
Index register port: 22 H
Data register port: 23 H (R/W)
Index: 69 H



Bits	Function
0	Enable Shadow RAM in E0000H-E3FFFH area. Disable = 0, Enable = 1.
1	Enable Shadow RAM in E4000H-E7FFFH area. Disable = 0, Enable = 1.
2	Enable Shadow RAM in E8000H-EBFFFH area. Disable = 0, Enable = 1.
3	Enable Shadow RAM in EC000H-EFFFFH area. Disable = 0, Enable = 1.
4	Enable Shadow RAM in F0000H-F3FFFH area. Disable = 0, Enable = 1.
5	Enable Shadow RAM in F4000H-F7FFFH area. Disable = 0, Enable = 1.
6	Enable Shadow RAM in F8000H-FBFFFH area. Disable = 0, Enable = 1.
7	Enable Shadow RAM in FC000H-FFFFFH area. Disable = 0, Enable = 1.

Table 10
Bank 0/1 Enable Register RB6

Index register port: 22 H
Data register port: 23 H
Index: 6AH



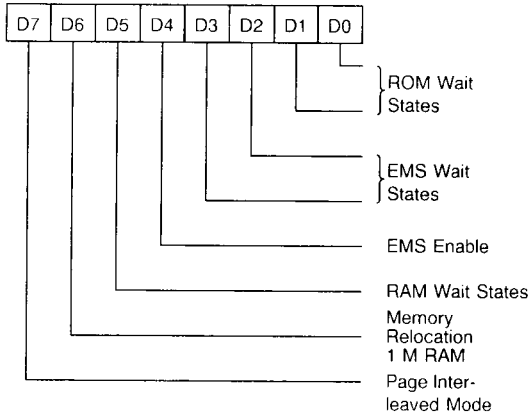
Bits	Function
0-4	Reserved and default to 0. 1)
5	Number of RAM banks used. 0 = one bank, non-interleaved mode (Default), 1 = two banks
7, 6	These bits contain the information for the DRAM types used on the system board. POST/BIOS should use the DRAM configuration data stored in the CMOS RAM of the SAB 82C206 IPC.

7	6	DRAM Types
0	0	Disabled
0	1	256 K and 64 K bit DRAMs used (for 640 Kbyte combination only)
1	0	256 K bit DRAMs used (Default)
1	1	1 Mbit DRAMs used

1) The reserved bits are recommanded to be initialized to 1.

Table 11
DRAM Configuration Register

Index register port: 22 H
Data register port: 23 H (R/W)
Index: 6BH



Bits	Function
1, 0	ROM access wait states control.

1	0	Wait States
0	0	0
0	1	1
1	0	2
1	1	3 (Default)

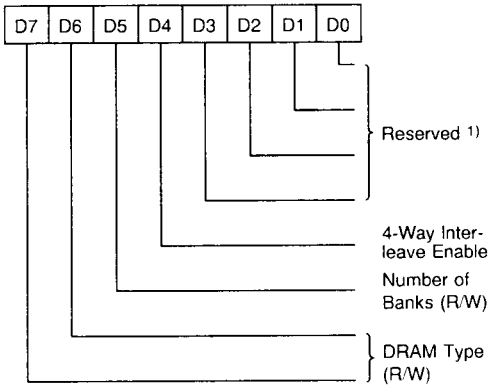
Bits	Function
3, 2	EMS memory access wait states.

3	2	Wait States
0	0	0

Bits	Function
4	EMS enable bit. If set to 0, EMS is disabled (Default). If set to 1, EMS is enabled.
5	RAM access wait states. If set to 0, accesses have 0 wait state. If set to 1 (Default), accesses will have 1 wait state.
6	640 Kbyte to 1 Mbyte RAM relocation bit. A zero does not relocate local RAM. A one (Default) relocates local RAM from 0A0000-0FFFFF to 100000H-15FFFFH, provided total local RAM is 1 Mbyte only.
7	Page/Interleaved mode enable. A 0 disables the page/interleaved mode, allowing useage of normal mode for the DRAMs (Default). A 1 enables page/interleaved mode for the DRAMs.

Table 12
Bank 2/3 Enable Register RB8

Index register port: 22 H
Data register port: 23 H
Index: 6CH



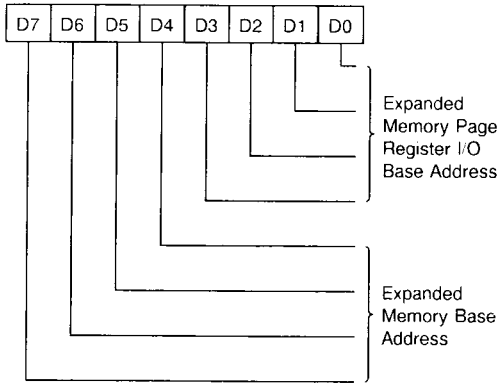
1) The reserved bits are recommanded to be initialized to 1.

Bits	Function
3-0	Reserved and default to 0[1].
4	A zero enables the 2-way page interleaved mode. A one (Default) enables the 4-way page interleaved mode if all 4 banks are the same DRAM devices.
5	Number of local RAM banks used. 0 = one bank used, non-interleaved mode only (Default). 1 = two banks used.
7, 6	These bits indicate the local DRAM type as listed:

7	6	DRAM Type
0	0	none (Default)
0	1	Reserved
1	0	256 Kbit
1	1	1 Mbit

Table 13
EMS Base Address Register RB9

Index register port: 22 H
Data register port: 23 H (R/W)
Index: 6DH



Bits	Function
0-3	These bits are used for the EMS page register I/O base address. The bits are encoded as follows, with unused combinations being reserved:

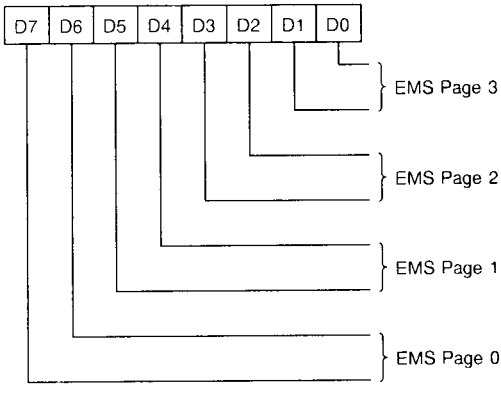
3	2	1	0	I/O Base
0	0	0	0	208H/209H
0	0	0	1	218H/219H
0	1	0	1	258H/259H
0	1	1	0	268H/269H
1	0	1	0	2A8H/2A9H
1	0	1	1	2B8H/2B9H
1	1	1	0	2E8H/2E9H

7-4 These bits are used for selecting the expanded memory base addresses. They are encoded as follows, with all unused combinations being reserved:

7	6	5	4	EMS Base Addresses
0	0	0	0	C0000H,C4000H, C8000H,CC000H
0	0	0	1	C4000H,C8000H, CC000H,D0000H
0	0	1	0	C8000H,CC000H, D0000H,D4000H
0	0	1	1	CC000H,D0000H, D4000H,D8000H
0	1	0	0	D0000H,D4000H, D8000H,DC000H
0	1	0	1	D4000H,D8000H, DC000H,E0000H
0	1	1	0	D8000H,DC000H, E0000H,E4000H
0	1	1	1	DC000H,E0000H, E4000H,E8000H
1	0	0	0	E0000H,E4000H, E8000H,EC000H

Table 14
EMS Extension Register RB10

Index register port: 22 H
Data register port: 23 H (R/W)
Index: 6EH

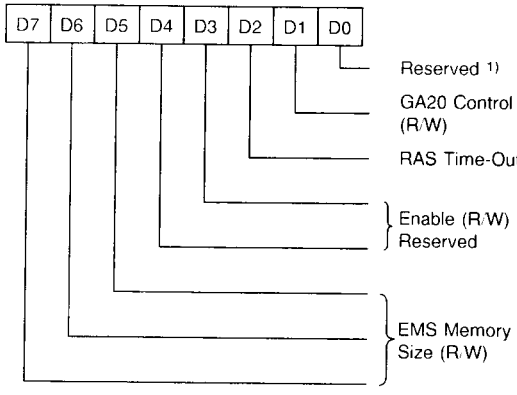


Bits	Function		
1(A22) 0(A21)	EMS Page 3 address extension bits.		
	1	0	Block of EMS Memory
	0	0	0 Mbyte to 2 Mbyte
	0	1	2 Mbyte to 4 Mbyte
	1	0	4 Mbyte to 6 Mbyte
	1	1	6 Mbyte to 8 Mbyte
3(A22) 2(A21)	EMS Page 2 address extension bits.		
	3	2	Block of EMS Memory
	0	0	0 Mbyte to 2 Mbyte
	0	1	2 Mbyte to 4 Mbyte
	1	0	4 Mbyte to 6 Mbyte
	1	1	6 Mbyte to 8 Mbyte
5(A22) 4(A21)	EMS Page 1 address extension bits.		
	5	4	Block of EMS Memory
	0	0	0 Mbyte to 2 Mbyte
	0	1	2 Mbyte to 4 Mbyte
	1	0	4 Mbyte to 6 Mbyte
	1	1	6 Mbyte to 8 Mbyte
7(A22) 6(A21)	EMS Page 0 address extension bits.		
	7	6	Block of EMS Memory
	0	0	0 Mbyte to 2 Mbyte
	0	1	2 Mbyte to 4 Mbyte
	1	0	4 Mbyte to 6 Mbyte
	1	1	6 Mbyte to 8 Mbyte

Address lines A22 and A21 are used in EMS Address translation logic.

Table 15
Miscellaneous Register RB11

Index register port: 22 H
Data register port: 23 H
Index: 6FH



1) The reserved bits are recommanded to be initialized to 1.

Bits	Function
0	Reserved and default to 0[1].
1	This bit is used for address line A20 control and provides OS/2 optimization while switching between real and protected modes: If the bit is set to 0 it enables A20 onto GA20. The bit default to 1 and sets GA20 = 0.
2	This bit is used to enable the RAS# time-out counter for page mode operation. The counter is disabled if set to 0 (Default) and is enabled if set to 1.
3, 4	Reserved and default to 1 (bit 4), 0 (bit 3).
7-5	These bits are used to set the EMS memory space according to the following coding:

7	6	5	EMS Memory Size
0	0	0	less than 1 Mbyte
0	0	1	1 Mbyte
0	1	0	2 Mbytes
0	1	1	3 Mbytes
1	0	0	4 Mbytes
1	0	1	5 Mbytes
1	1	0	6 Mbytes
1	1	1	7 Mbytes

Table 16
EMS Page Registers

Page 0: 2X8/2X9H
Page 1: 42X8/42X9H
Page 2: 82X8/82X9H
Page 3: C2X8/C2X9H

X can be 0, 1, 5, 6, A, B, E

Bits	Function
0-6	0 - A14 1 - A15 2 - A16 3 - A17 4 - A18 5 - A19 6 - A20
7	0 - page disable 1 - page enable

Absolute Maximum Ratings

Ambient temperature under bias ..... 0 to 70 °C
Storage temperature ..... – 65 to + 150 °C
Supply voltage ..... – 0.5 to + 7.0 V
Voltage on any pin with respect to ground ..... – 0.5 to V_{CC} + 0.5 V
Power dissipation ..... 1 W

Note: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum ratings for extended periods may affect device reliability.*

DC Characteristics

T_A = 0 to 70 °C; V_{CC} = 5 V ± 5 %; GND = 0 V

Parameter	Symbol	Limit values		Unit	Test condition
		min.	max.		
Input low voltage	V_{IL}	–	0.8	V	–
Input high voltage	V_{IH}	2.0	–	V	–
Output low voltage	V_{OL}	–	0.45	V	I_{OL} = 4 mA
Output high voltage	V_{OH}	2.4	–	V	I_{OH} = –4 mA
Input leakage current	I_{IL}	–	+ 10	µA	0 V < V_{IN} < V_{CC}
Power supply current	I_{CC}	–	75	mA	@16 MHz
Output tristate leakage current	I_{OZ1}	–	+ 10	µA	0.45 V < V_{OUT} < V_{CC}
Standby power supply current	I_{CCSB}	–	1.0	mA	–

AC Characteristics

T_A = 0 to 70 °C; V_{CC} = 5 V ±5 %; GND = 0 V

Parameter	Symbol	Limit values		Unit	Test condition
		min.	max.		
RASi# active delay from CLK2 ↓	t_1	11	16	ns	–
RASi# inactive delay from CLK2 ↓	t_2	15	25	ns	–
DLYOUT active delay from RASi# ↓	t_3	0	4	ns	–
DLYOUT inactive delay from RASi# ↑	t_4	0	6	ns	–
Column address stable from DLY0 ↑	t_5	8	18	ns	–
Column address hold from DLY0 ↓	t_6	6	–	ns	–
CASi# active delay from DLY1 ↑	t_7	7	14	ns	–
CASi# inactive delay from DLY1 ↓	t_8	11	18	ns	–
AF16# active delay from CLK2 ↓	t_9	7	19	ns	SAB 82C212-12
		7	16	ns	SAB 82C212-16
AF16# inactive delay from CLK2 ↓	t_{10}	8	21	ns	SAB 82C212-12
		8	18	ns	SAB 82C212-16
READY# active delay from CLK2 ↓	t_{11}	15	25	ns	–
READY# inactive delay from CLK2 ↓	t_{12}	11	20	ns	–
DRD# active delay from CLK2 ↓	t_{13}	10	19	ns	–
DRD# hold from DLE ↓	t_{14}	13	–	ns	–
DLE active delay from DLY1# ↓	t_{15}	6	16	ns	–
DLE inactive delay from CLK2 ↓	t_{16}	9	18	ns	–
LMEGCS# active from CLK2 ↓	t_{17}	12	21	ns	–
LMEGCS# inactive from CLK2 ↓	t_{18}	11	20	ns	–
GA20 valid delay from CPU A20 valid	t_{19}	7	20	ns	SAB 82C212-12
		7	16	ns	SAB 82C212-16
GA20 invalid delay from CPU A20 invalid	t_{20}	4	16	ns	SAB 82C212-12
		4	12	ns	SAB 82C212-16
MWE# active delay from CLK2 ↓	t_{22}	11	20	ns	–
MWE# inactive delay from CLK2 ↑	t_{23}	4	12	ns	–
CASi# active delay from CLK2 ↓	t_{26}	10	25	ns	SAB 82C212-12
		10	19	ns	SAB 82C212-16
CASi# inactive delay from CLK2 ↓	t_{27}	11	26	ns	SAB 82C212-12
		11	21	ns	SAB 82C212-16

AC Characteristics (cont'd)

Parameter	Symbol	Limit values		Unit	Test condition
		min.	max.		
DRD# inactive delay from CLK2 ↓	t_{28}	12	23	ns	–
CASi# inactive delay from DLE inactive	t_{29}	2	–	ns	–
RASi# active delay from CLK2 ↓	t_{30}	10.5	16	ns	–
Row address setup time to RASi# ↓	t_{31}	8	–	ns	–
Row address hold time from CLK2 ↓	t_{32}	6	22	ns	–
RASi# inactive delay from CLK2 ↓	t_{33}	15	25	ns	–
RASi# precharge time (interleaved mode)	t_{34}	4 × CLK2	–	–	–
ROMCS# active from CLK2 ↓	t_{35}	11	20	ns	–
ROMCS# inactive from CLK2 ↓	t_{36}	10	20	ns	–
DLE hold time from DRD# ↑	t_{37}	0	7	ns	–
RAS0-3# inactive from REF# ↓	t_{38}	13	24	ns	–
RAS0,3# active from XMEMR# ↓	t_{39}	9	17	ns	–
RAS0,3# inactive from XMEMR# ↑	t_{40}	10	19	ns	–
RAS1,2# active from RAS0,3# ↓	t_{41}	7	15	ns	–
RAS1,2# inactive from RAS0,3# ↑	t_{42}	11	20	ns	–
Address setup time from XMEMR# ↓	t_{43}	10	–	ns	–
Address hold time from REF# ↑	t_{44}	4	–	ns	–
Refresh address delay	t_{45}	0	–	ns	–
LMEGCS# delay from REF# ↓	t_{47}	8	16	ns	–
LMEGCS# delay from REF# ↑	t_{48}	10	19	ns	–
RAS0-3# inactive from HLDA1 ↑	t_{49}	11	20	ns	–
RASi# active from command active	t_{50}	10	18	ns	–
RASi# inactive from command inactive	t_{51}	12	21	ns	–
Column address stable from DLY0 ↑	t_{54}	9	18	ns	–
CASi# active delay from DLY1 ↑ (while XMEMW# active)	t_{55}	6	14	ns	–
CASi# inactive delay from command inactive	t_{56}	9	18	ns	–
AF16# active from command active	t_{57}	9	17	ns	–
AF16# inactive from command inactive	t_{58}	6	14	ns	–

Figure 9
Read Timing, 0 WS, Non-Interleaved Mode

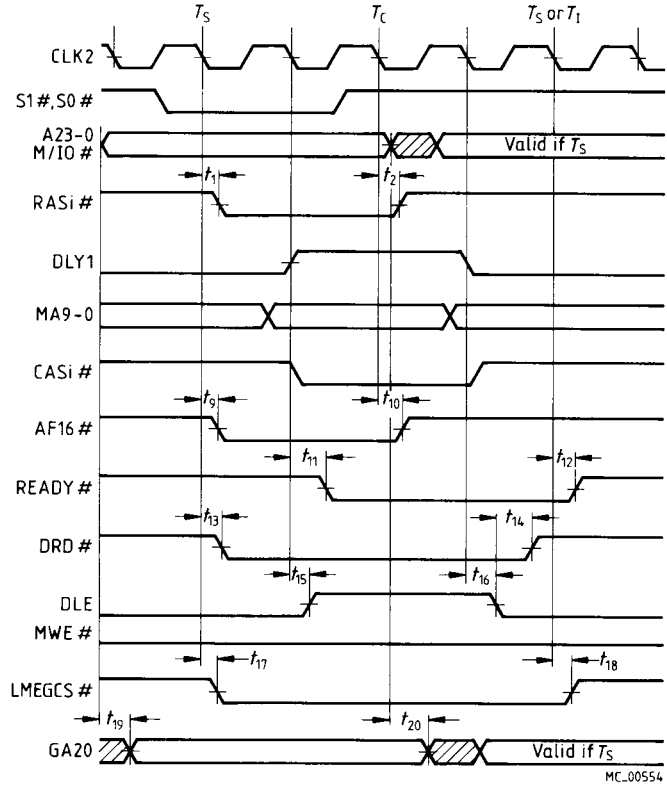


Figure 10
Write-Followed by Read-Timing, 0 WS, Non-Interleaved Mode

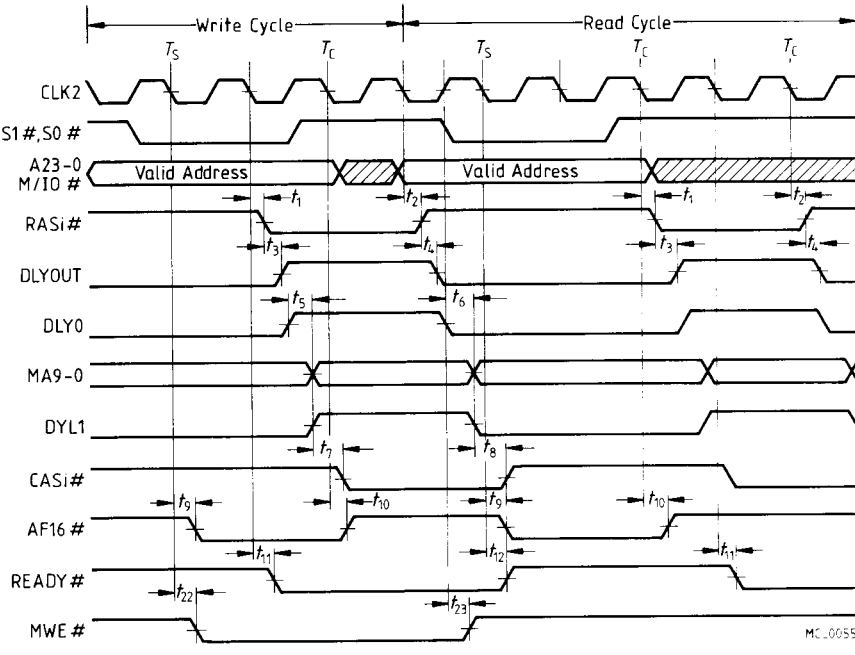


Figure 11
Write Cycle, 0 WS, Non-Interleaved Mode

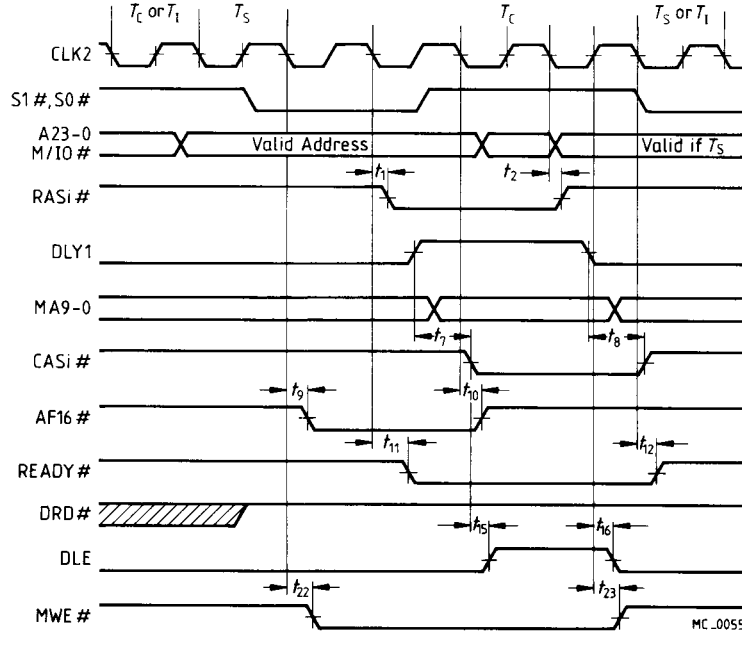


Figure 12
Read/Write, 1 WS, Non-Interleaved Mode

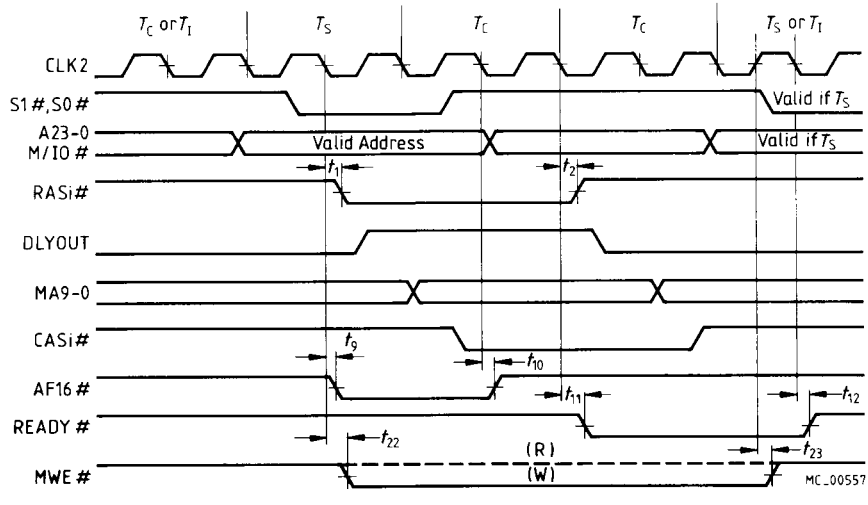


Figure 13
Write Cycle with RAS# Being Inactive, 0 WS, Interleaved Mode

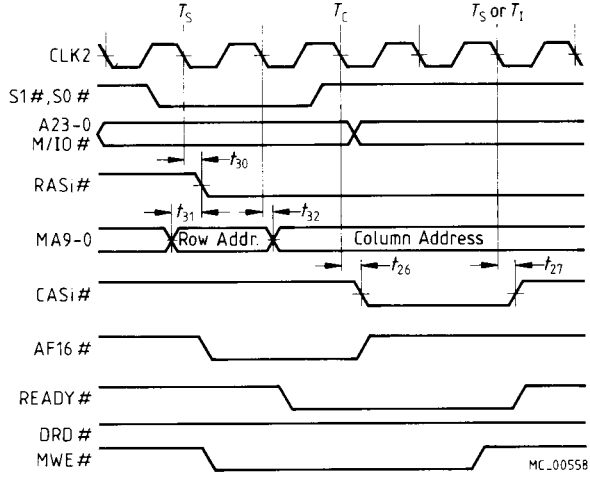


Figure 14
Read Cycle with RAS# Being Inactive, 0 WS, Interleaved Mode

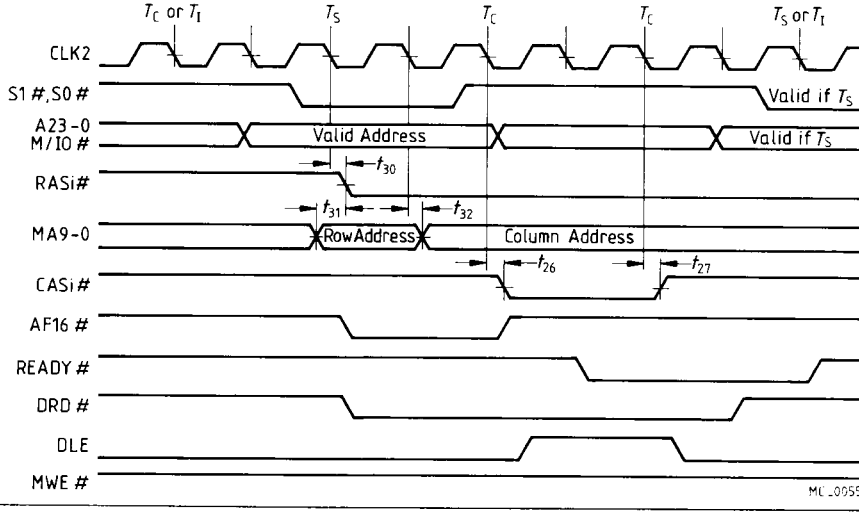


Figure 15
Write Cycle, 0 WS (RAS# active), Interleaved Mode

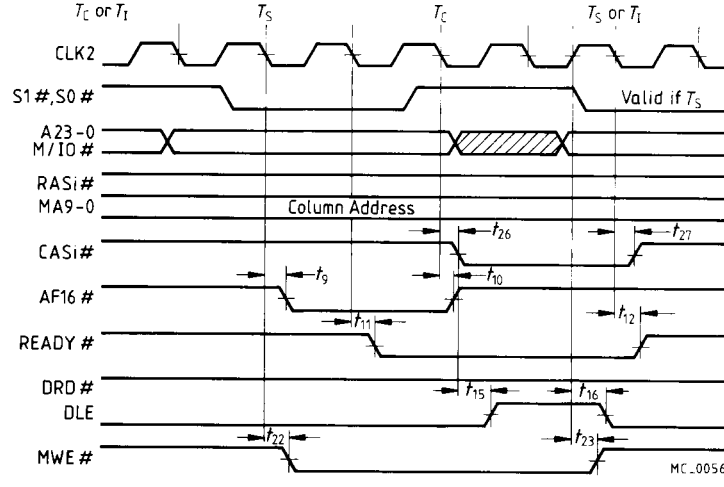


Figure 16
Read after Write, 0 WS (RAS# active), Interleaved Mode

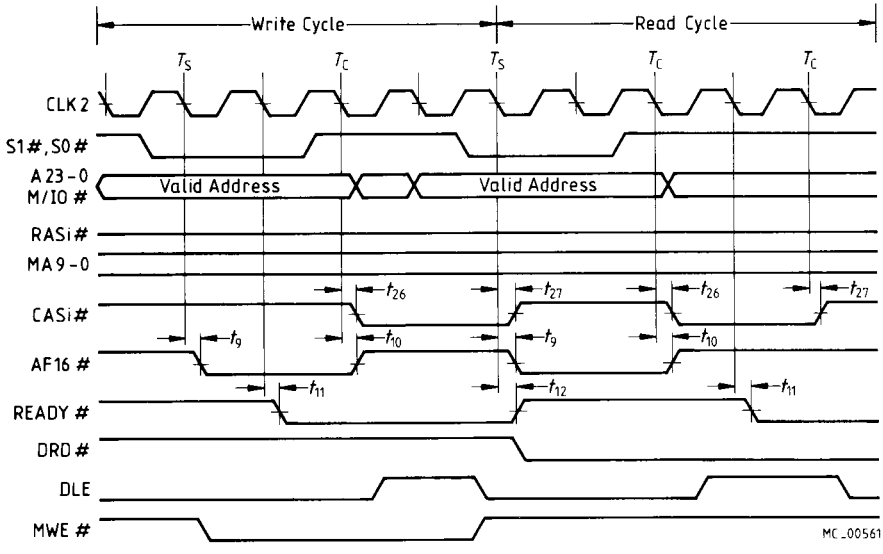


Figure 17
Read Cycle, 0 WS (RAS# active), Interleaved Mode

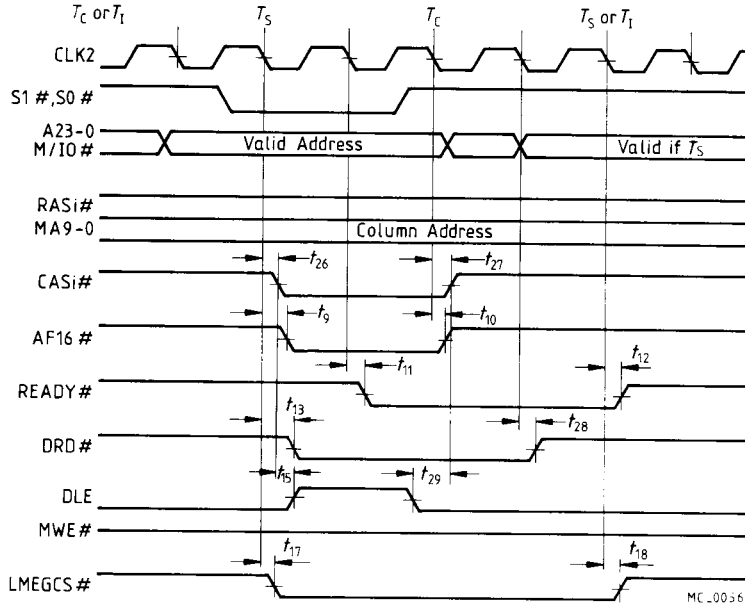


Figure 18
Read Miss Cycle, Interleaved Mode

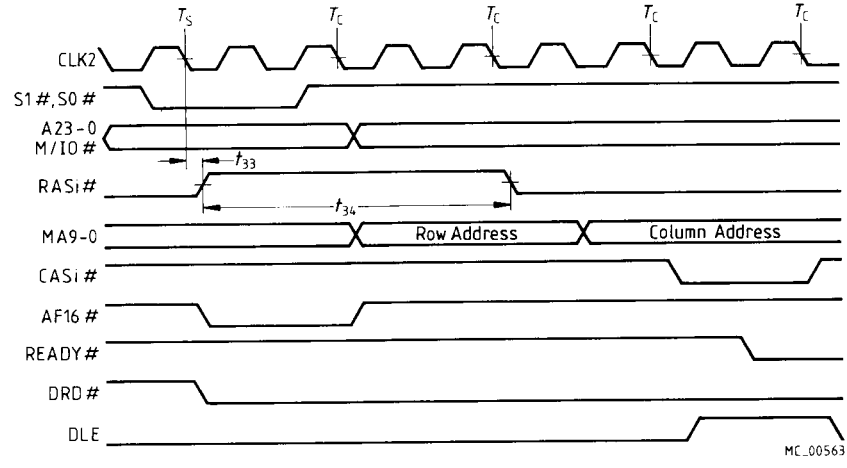


Figure 19
ROM Read Cycle

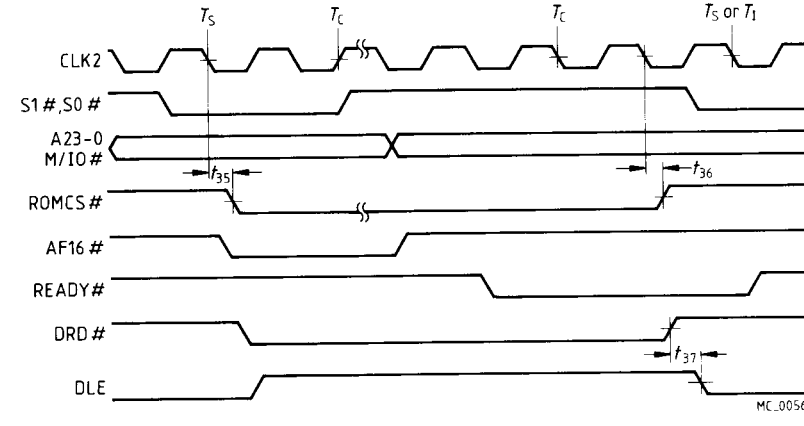


Figure 20
Refresh Cycle

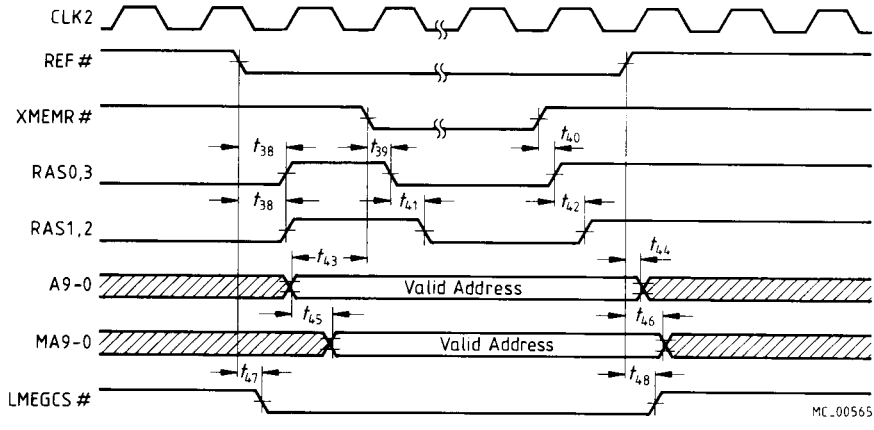


Figure 21
DMA Cycle

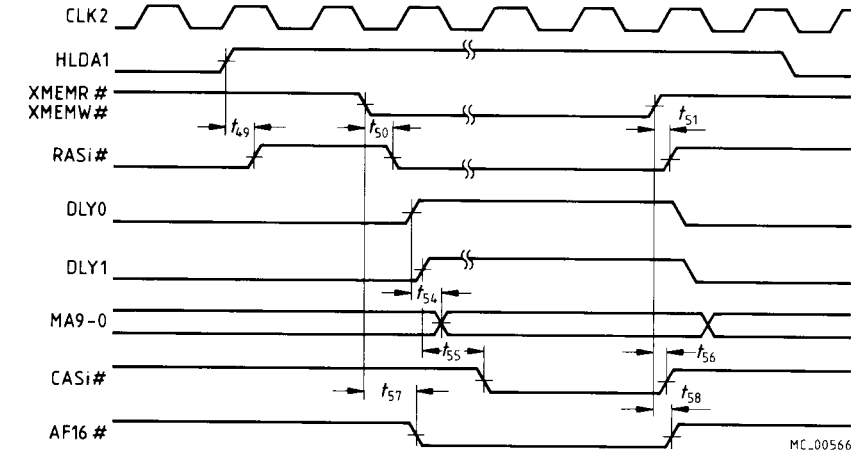
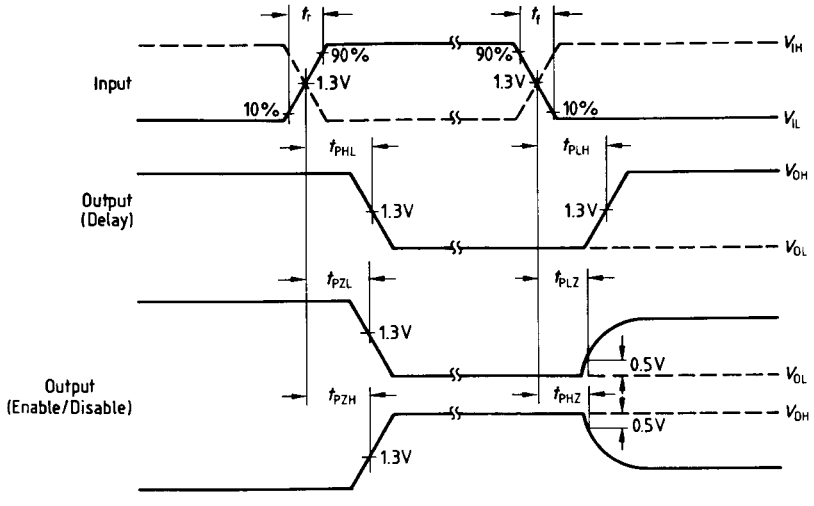
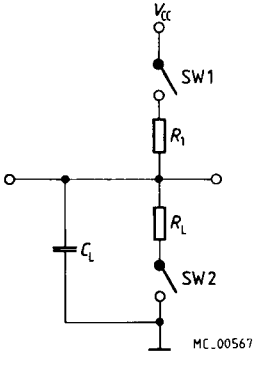


Figure 22
Load Circuit and AC Characteristics Measurement Waveform



V_{IH} = 3V, V_{IL} = 0V, $t_r \leq 10$ns, $t_f \geq 5$ns



Load Circuit Measurement Conditions

Parameter	Output Type	Symbol	C_L (pF)	R_1 (kΩ)	R_L (kΩ)	SW_1	SW_2
Propagation	Totem Pole						
Delay Time	Tristate	t_{PLH}	50	–	1.0	OFF	ON
	Bidirectional	t_{PHL}	50	–	1.0	OFF	ON
Propagation	Open Drain or	t_{PLH}	50	0.5	–	ON	OFF
Delay Time	Open Collector	t_{PHL}	50	0.5	–	ON	OFF
Disable Time	Tristate	t_{PLZ}	5	0.5	1.0	ON	
	Bidirectional	t_{PHZ}	5	0.5	1.0	OFF	ON
Enable Time	Tristate	t_{PZL}	50	0.5	1.0	ON	ON
	Bidirectional	t_{PZH}	50	0.5	1.0	OFF	ON