STRUCTURE	Silicon Monolithic Integrated Circuit
PRODUCTSERIES	Strobe Charge Control IC
TYPE	BD4210EKN
FEATURES	1. Adjustable transformer primary-side peak current 2. Built-in IGBT driver 3. Includes charge complete signal output (FULL) pin. 4. Includes charge voltage detection (VC) pin (can be set externally).

○ Absolute Maximum Ratings (Ta=25℃)

Parameter	Symbol	BD4210EKN	Unit
Supply voltage	VCC	10	V
PVC pin (DC characteristics)	PVCDC	36	V
PVC pin (PULSE characteristics) *1	PVCPULSE	50	V
Output current	IPVC	2.2	A
FULL pin voltage	VFULL	10	V
START pin voltage	VSTART	10	V
IGBT driver voltage	VDD2	7	V
IGBT driver input voltage range	VIGBT_IN	-0.3～VDD2+0.3	V
Operating temperature range	Topr	-35～+85	℃
Storage temperature range	Tstg	-55～+125	℃
Power dissipation	Pd	2.25	W
Junction temperature *2	Tjmax	125	℃

*1: Pulse width of 100 μs or less.
*2: Reduced by 22.5 mW/°C over Ta = 25°C. (When mounted on 70 mm × 70 mm × 1.6 mm, glass epoxy)

○ Recommended Operating Ranges (Ta=-35～85℃)

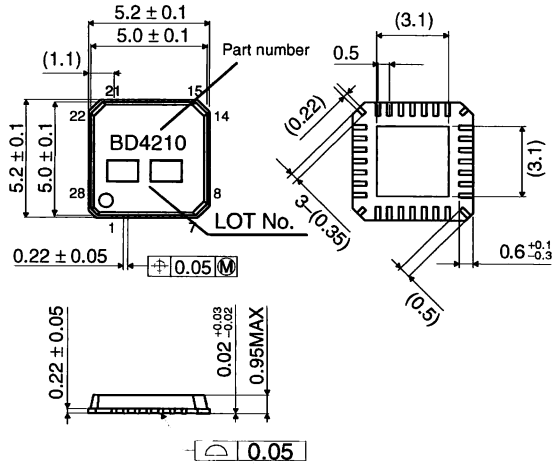
Parameter	Symbol	BD4210EKN	Unit
VCC supply voltage range	VCC	2.5～9	V
PVC voltage range	VPVC	～35	V
VDD2 supply voltage range	VDD2	2.5～6	V
I_ADJ pin input voltage range	VI_ADJ	0.05～1	V
Primary-side peak current setting range	IPVC	0.5～2.0	A
RT pin resistance range	RT	10～200	kΩ

○ Electrical Characteristics (Ta=25℃, VCC=3.0V,VDD2=2.5V)

Parameter	Symbol	Limits			Unit	Conditions
		Min.	Typ.	Max.		
[Overall device]						
Average operating current consumption	ICCA	—	25	30	mA	START=3V,Ipeak=1A
Circuit current during standby operation	ICCS	—	0	1	μA	START=0V
[Reference voltage]						
Output voltage	VREF	1.480	1.520	1.560	V	IREF=-1mA
Output current	IVREF	1	—	—	mA	
Current capacity when shorted	ISHORT	3.5	5.5	—	mA	
[Standby control START pin]						
START pin high voltage	VSTH	2.0	—	—	V	
START pin low voltage	VSTL	—	—	0.3	V	
Input bias current	IST	50	70	100	μA	START=3V
[Protection circuit block]						
UVLO detection voltage	VUVLOT	—	2.1	2.25	V	
OVP comparator detection voltage	VOVPTH	1.490	1.520	1.550	V	
OVP pin sink current	IOVPI	—	0.1	1	μA	VOVP=3V
OVP_SW pin on resistance	ROVP_SW	—	200	500	Ω	
[Transformer primary-side driver block]						
Leak current when driver off	Ileak	—	—	1.0	μA	VPVC=36V
PVC saturation voltage*	VPVCE	—	0.25	0.3	V	IPVC=1A
I_ADJ source current	I_ADJI	—	0.1	1	μA	VI_ADJ=0V
Primary-side peak current detection comparator offset voltage	ΔVcomp1	-10	—	10	mV	
[Off time determination block]						
RT pin open voltage 1	VRTO1	0.20	0.3	0.4	V	VC=0V,RT=200kΩ
RT pin open voltage 2	VRTO2	1.470	1.5	1.530	V	VC=1.5V,RT=200kΩ
Off time 1	TOFF1	7.65	9.0	10.35	μs	VC=0.5V,RT=200kΩ
Off time 1'	TOFF1'	3.8	4.5	5.2	μs	VC=0.5V,RT=100kΩ
Off time 2	TOFF2	2.8	3.3	3.8	μs	VC=1.4V,RT=200kΩ
Off time 2'	TOFF2'	1.35	1.6	1.85	μs	VC=1.4V,RT=100kΩ
[Transformer secondary-side detection block]						
Full charge detection voltage	VCTH	1.505	1.520	1.535	V	
FULL pin low voltage when charging	VFULLL	—	0.3	1	V	VDD2=3.0V, RFULL=10kΩ
FULL pin leak current	IFULLH	—	—	1	μA	VDD2=3.0V
[IGBT driver block]						
High level current consumption	IDD2H	—	0.6	1	mA	IGBT_OUTP, IGBT_OUTN are shorted
Low level current consumption	IDD2L	—	—	1	μA	
High level input voltage	VINH	VDD2*0.8	—	VDD2	V	
Low level input voltage	VINL	—	—	1.0	V	
High level input sink current	IINH	—	10	20	μA	IGBT_IN=2.5V
Low level input sink current	IINL	—	—	1	μA	
Turn-on rise time	tr	—	300	500	ns	C=4700pF
Turn-off fall time	tf	—	300	500	ns	C=4700pF
Turn-on delay time	tdon	—	170	500	ns	C=4700pF
Turn-off delay time	tdoff	—	100	500	ns	C=4700pF
On resistance at high output	RONH	—	10	30	Ω	
On resistance at low output	RONL	—	4.5	30	Ω	

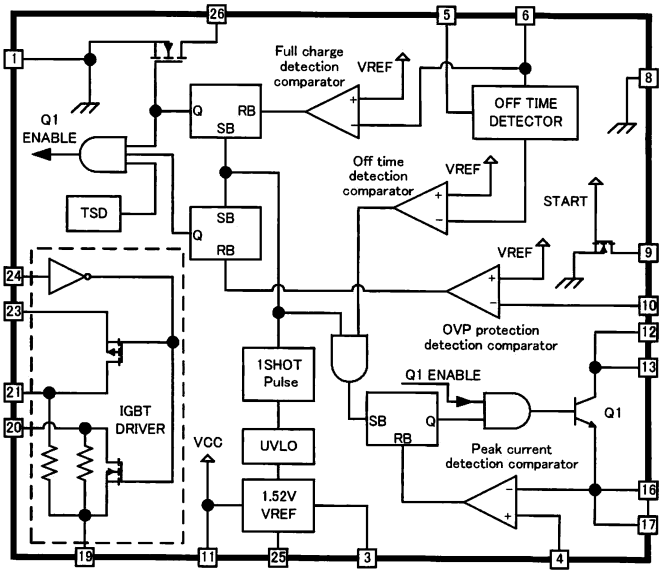
*Design guarantee. (Not all units are inspected.)

○ PACKAGE



HQFN28V(UNIT : mm)

○ Block Diagram



○ PIN No. PIN Name

PIN No.	PIN Name	Function
1	GND	System ground pin
2	N/C	–
3	VREF	1.52 V reference voltage output pin
4	I_ADJ	Primary-side peak current setting pin
5	RT	Off time setting pin
6	VC	Full charge detection pin
7	N/C	–
8	PGND1	Power ground pin
9	OVP_SW	OVP detection switching pin
10	OVP	OVP detection pin
11	VCC	Power supply pin
12	PVC	Power transistor collector pin
13	PVC	Power transistor collector pin
14	N/C	–

PIN No.	PIN Name	Function
15	N/C	–
16	PVE	Power transistor emitter pin
17	PVE	Power transistor emitter pin
18	N/C	–
19	PGND2	IGBT driver ground pin
20	IGBT_OUTN	IGBT driver low-side output pin
21	IGBT_OUTP	IGBT driver high-side output pin
22	N/C	–
23	VDD2	IGBT driver power supply pin
24	IGBT_IN	IGBT driver input pin
25	START	Charge start pin
26	FULL	Charge complete signal output pin
27	N/C	–
28	N/C	–

*N/C is non connected pin in electrical open.

○Precautions

1. Absolute maximum ratings
Use of the IC in excess of absolute maximum ratings such as the applied voltage or operating temperature range may result in IC deterioration or damage. Assumptions should not be made regarding the state of the IC (short mode or open mode) when such damage is suffered. A physical safety measure such as a fuse should be implemented when use of the IC in a special mode where the absolute maximum ratings may be exceeded is anticipated.

2. GND potential
Ensure a minimum GND pin potential in all operating conditions. In addition, ensure that no pins other than the GND pin carry a voltage less than or equal to the GND pin, including during actual transient phenomena.
The PVC pin may be exposed to negative voltages due to the characteristics of the external transformer.
It is recommended to connect a schottky diode between the PVC and GND pins when variations in electrical characteristics or damage is possible due to the PVC pin carrying a negative voltage.

3. Thermal design
Use a thermal design that allows for a sufficient margin in light of the power dissipation (Pd) in actual operating conditions.

4. Inter-pin shorts and mounting errors
Use caution when orienting and positioning the IC for mounting on printed circuit boards. Improper mounting may result in damage to the IC. Shorts between output pins or between output pins and the power supply GND pin caused by the presence of a foreign object may result in damage to the IC.

5. Common impedance
Power supply and ground wiring should reflect consideration of the need to lower common impedance and minimize ripple as much as possible (by making wiring as short and thick as possible or rejecting ripple by incorporating inductance and capacitance).

6. IC pin input
This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P/N junctions are formed at the intersection of these P layers with the N layers of other elements to create a variety of parasitic elements.
For example, when a resistor and transistor are connected to pins as shown in Fig. 16, the P/N junction functions as a parasitic diode when GND > (Pin A) for the resistor or GND > (Pin B) for the transistor (NPN).
Similarly, when GND > (Pin B) for the transistor (NPN), the parasitic diode described above combines with the N layer of other elements to operate as a parasitic NPN transistor.
The formation of parasitic elements as a result of the relationships of the potentials of different pins is an inevitable result of the IC's architecture. The operation of parasitic elements can cause interference with circuit operation as well as IC malfunction and damage. For these reasons, it is necessary to use caution so that the IC is not used in a way that will trigger the operation of parasitic elements, such as by the application of voltages lower than the GND (P substrate) voltage to input and output pins.
The PVC pin may be exposed to negative voltages due to the characteristics of the external transformer. It is recommended to connect a schottky diode between the PVC and GND pins when variations in electrical characteristics or damage is possible due to the PVC pin carrying a negative voltage.

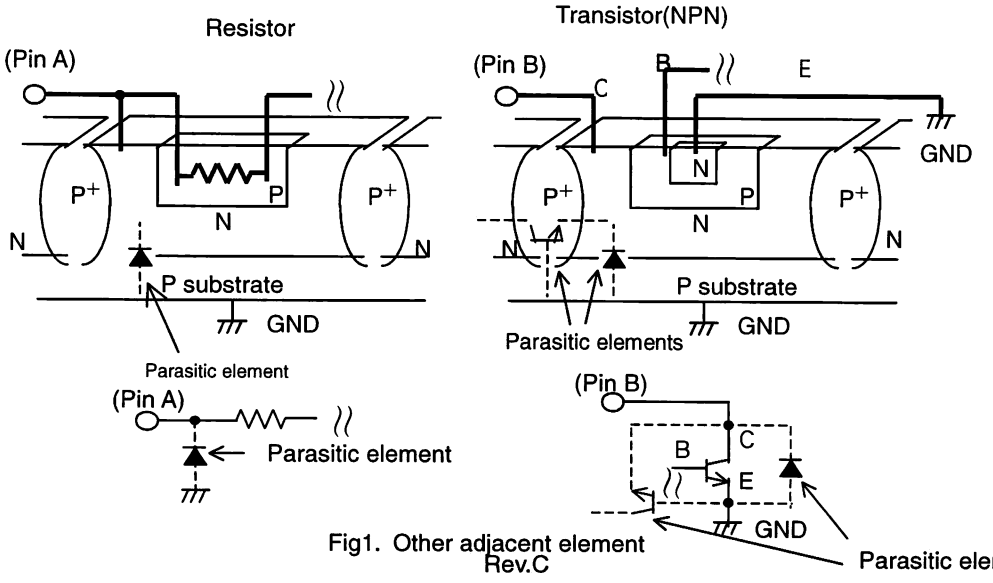


Fig1. Other adjacent element

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