Am27S35/S35A/Am27S37/S37A

8,192-Bit (1024x8) Bipolar Registered PROM
with Programmable INITIALIZE Input

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- Slim, 24-pin, 300-mil lateral center package occupies approximately 1/3 the board space required by standard discrete PROM and register
- Consumes approximately 1/2 the power of separate PROM/register combination for improved system reliability
- Versatile programmable asynchronous or synchronous enable for simplified word expansion
- Buffered common $\overline{\text{INITIALIZE}}$ input either asynchronous (Am27S35) or synchronous (Am27S37)
- Platinum-Silicide fuses guarantee high reliability, fast programming and exceptionally high programming yields (typ. > 98%)

GENERAL DESCRIPTION

The Am27S35 and the Am27S37 (1024 words by 8 bits) are fully decoded, Schottky array, TTL Programmable Read-Only Memories (PROMs), incorporating D-type master-slave data registers on chip. These devices have three-state outputs compatible with low-power Schottky bus standards capable of satisfying the requirements of a variety of microprogrammable controls and state machines.

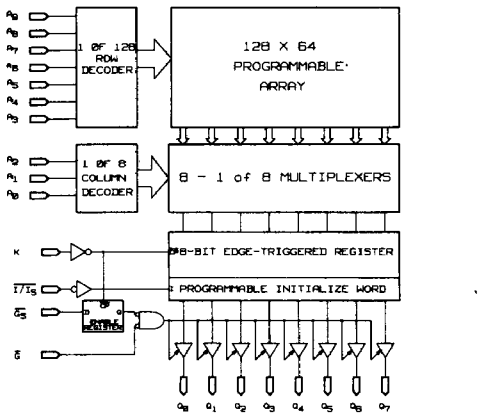
These devices contain an 8-bit parallel data register in the array-to-output path which allows PROM data to be stored while other data is being addressed. This meets the requirements for pipelined microprogrammable control stores where instruction execute and instruction fetch are performed in parallel.

To offer the system designer maximum flexibility, these devices contain both asynchronous ($\overline{G}$) and synchronous ($\overline{G_S}$) output enables.

These devices contain a single pin initialize function capable of loading any arbitrary microinstruction for system interrupt or initialization. On the Am27S35 this function operates asynchronously, independent of clock. The Am27S37 provides synchronous operation of this function.

Upon power-up the outputs ($Q_0 - Q_7$) will be in a floating or high-impedance state.

BLOCK DIAGRAM



BD006352

PRODUCT SELECTOR GUIDE

Part Number Asynchronous Initialize	Am27S35A		Am27S35	
Part Number Synchronous Initialize	Am27S37A		Am27S37	
Address Setup Time	35 ns	40 ns	40 ns	45 ns
Clock-to-Output Delay	20 ns	25 ns	25 ns	30 ns
Operating Range	C	M	C	M

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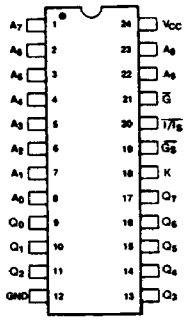
Issue Date: January 1989

CONNECTION DIAGRAMS
Top View

DIPs*



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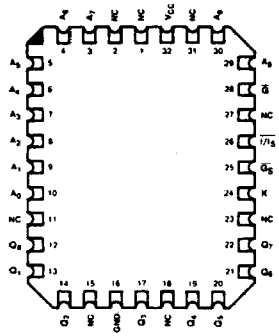
LCCs**



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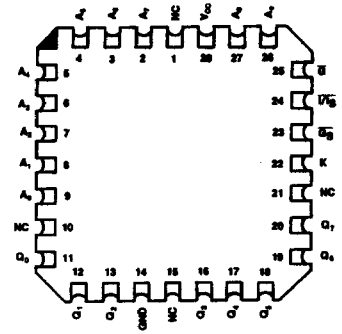

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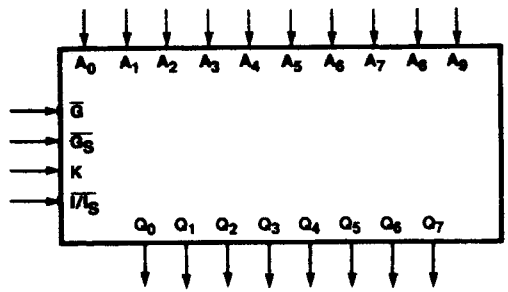
*Also available in a 24-pin Flatpack. Pinout identical to DIPs.
**Also available in a 28-pin Square PLCC. Pinout identical to LCC.

Note: Pin 1 is marked for orientation.

LOGIC SYMBOL

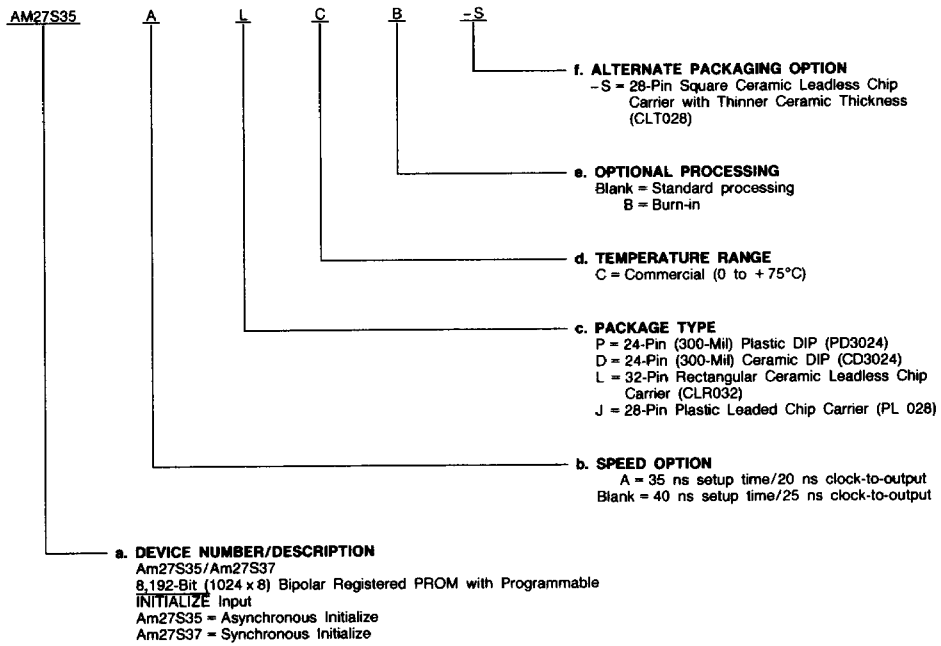


LS000172

ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of: **a. Device Number**
b. Speed Option (if applicable)
c. Package Type
d. Temperature Range
e. Optional Processing
f. Alternate Packaging Option



Valid Combinations	
AM27S35	DC, DCB, PC, PCB, LC, LCB, LC-S, LCB-S, JC, JCB
AM27S35A	
AM27S37	
AM27S37A	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

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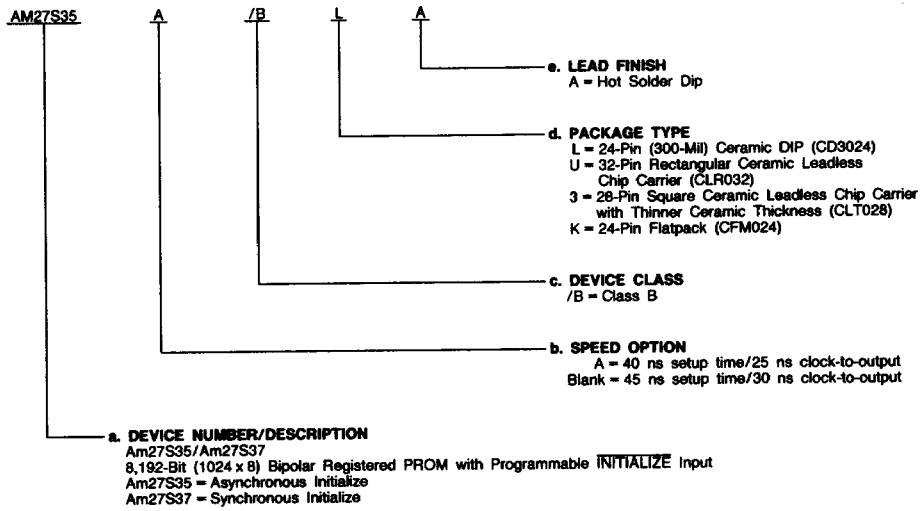
MILITARY ORDERING INFORMATION

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) for APL products is formed by a combination of: **a. Device Number**
b. Speed Option (if applicable)
c. Device Class
d. Package Type
e. Lead Finish



Valid Combinations	
AM27S35	/BLA, /BKA /BUA, /B3A
AM27S35A	
AM27S37	
AM27S37A	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

Group A Tests

Group A tests consist of Subgroups 1, 2, 3, 7, 8, 9, 10, 11.

MILITARY BURN-IN

Military burn-in is in accordance with the current revision of MIL-STD-883, Test Method 1015, Conditions A through E. Test conditions are selected at AMD's option.

PIN DESCRIPTION

$A_0 - A_9$ Address Inputs
The 10-bit field presented at the address inputs selects one of 1024 memory locations to be read from.

K Clock
The clock is used to load data into the parallel registers from the memory array. Data transfer occurs on the LOW-to-HIGH transition of K.

$Q_0 - Q_7$ Data Output Port
Parallel data output from the pipeline register. The disabled state of these outputs is floating or high impedance.

$\overline{G}$ Asynchronous Output Enable
Provides direct control of the Q-output, three-state drivers independent of K.

$\overline{G_S}$ Synchronous Output Enable
Controls the state of the Q-output, three-state drivers in conjunction with K. This is useful where more than one registered PROM is bussed together for word-depth expansion. In this case, the enable becomes the most significant address bit and, as such, must be synchronized with the data.

$\overline{I}$ Asynchronous Initialize (Am27S35)
Control pin used to initialize the output data registers from a programmable word independent of K. This can be used to generate any arbitrary microinstruction for system interrupt or initialization.

$\overline{I_S}$ Synchronous Initialize (Am27S37)
Control pin used to initialize the output data registers from a programmable word in conjunction with K. This can be used to generate any arbitrary microinstruction for system interrupt or initialization.

V_{CC} Device Power Supply Pin
The most positive of the logic power supply pins.

GND Device Power Supply Pin
The most negative of the logic power supply pins.

FUNCTIONAL DESCRIPTION

The Am27S35A/35 and Am27S37A/37 are Schottky TTL programmable read only memories (PROMs) incorporating true D-type, master-slave data registers on chip. These devices feature the versatile 1024-word by 8-bit organization and are available with three-state outputs. Designed to optimize system performance, these devices also substantially reduce the cost and size of pipelined microprogrammed systems and other designs where accessed PROM data is temporarily stored in a register. The Am27S35A/35 and Am27S37A/37 also offer maximum flexibility for memory expansion and data bus control by providing both synchronous and asynchronous output enables.

When V_{CC} power is first applied, the synchronous enable ($\overline{G_S}$) flip-flop will be in the set condition causing the outputs (Q_0–Q_7) to be in the OFF or high-impedance state. This occurs regardless of the state of the asynchronous enable input. A LOW-to-HIGH transition of the clock input (K) while $\overline{G_S}$ input is low is required after power-up in order to enable the outputs to an active state. Reading data is accomplished by first applying the binary word address to the address inputs (A_0–A_9) and a logic LOW to the synchronous enable ($\overline{G_S}$). During the address setup time, stored data is accessed and loaded into the master flip-flops of the data register. Since the synchronous enable setup time is less than the address setup requirement, additional decoding delays may occur in the enable path without reducing memory performance. Upon the next LOW-to-HIGH transition of the clock (K), data is transferred to the slave flip-flops which drive the output buffers. Provided that the asynchronous enable ($\overline{G}$) is also LOW, stored data will appear on the outputs (Q_0–Q_7). If ($\overline{G_S}$) is HIGH when the positive clock edge occurs, outputs go to the OFF or high-impedance state regardless of the value of ($\overline{G}$). The outputs may be disabled at any time by switching ($\overline{G}$) to a HIGH level. Following the positive clock edge, the address and synchronous enable inputs are free to change; changes will not affect the outputs until another positive clock edge occurs. This unique feature allows the PROM decoders and sense amplifiers to access the next location while previously addressed data remains stable on the outputs. For less complex applications either enable may be effectively eliminated by tying it to ground.

These devices also contain a built-in initialize function. When activated, the initialize control input ($\overline{I}$) causes the contents of an additional (1025th) 8-bit word to be loaded into the on-chip register. This extra word is user programmable. Since each bit is individually programmable, the initialize function can be used to load any desired combination of HIGHs and LOWs into the register. In the unprogrammed state, activating $\overline{I}$ will perform a register CLEAR (all outputs LOW). If all bits of the initialize word are programmed, activating $\overline{I}$ performs a register PRESET (all outputs HIGH).

This ability to tailor the initialize outputs to the system requirements simplifies system design and enhances performance. The initialize function is useful during power-up and timeout sequences. This flexible feature can also facilitate implementation of other sophisticated functions such as a built-in "jump-start" address.

The Am27S35A/35 has an asynchronous initialize input ($\overline{I}$). Applying a LOW to the $\overline{I}$ input causes an immediate load of the programmed initialize word into the slave flip-flops of the register independent of all other inputs (including K). The initialize data will appear at the device outputs after the outputs are enabled by bringing the asynchronous enable ($\overline{G}$) LOW.

The Am27S37A/37 has a synchronous $\overline{I_S}$ input. Applying a LOW to the $\overline{I_S}$ input causes an immediate load of the programmed initialize word into the master flip-flops of the register only independent of all other inputs (including K). To bring this data to the device outputs, the synchronous enable ($\overline{G_S}$) should be held LOW until the next LOW-to-HIGH transition of the clock (K). Following this, the data will appear on the outputs after the asynchronous enable ($\overline{G}$) is brought LOW.

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ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65 to +150°C
Ambient Temperature with
Power Applied ..... −55 to +125°C
Supply Voltage ..... −0.5 V to +7.0 V
DC Voltage Applied to Outputs
(Except During Programming) ..... −0.5 V to +V_{CC} Max.
DC Voltage Applied to Outputs
During Programming ..... 21 V
Output Current into Outputs During
Programming (Max. Duration of 1 sec) ..... 250 mA
DC Input Voltage ..... −0.5 V to +5.5 V
DC Input Current ..... −30 mA to +5 mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Ambient Temperature (T_A) ..... 0 to +75°C
Supply Voltage (V_{CC}) ..... +4.75 V to +5.25 V

Military (M) Devices*
Case Temperature (T_C) ..... −55 to +125°C
Supply Voltage (V_{CC}) ..... +4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

*Military product 100% tested at T_C = +25°C, +125°C, and −55°C.

DC CHARACTERISTICS over operating ranges unless otherwise specified (for APL Products, Group A, Subgroups 1, 2, 3 are tested unless otherwise noted)

Parameter Symbol	Parameter Description	Test Conditions		Min.	Typ.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −2.0 mA V_{IN} = V_{IH} or V_{IL}		2.4			V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 16 mA V_{IN} = V_{IH} or V_{IL}				0.50	V
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs (Note 1)		2.0			V
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs (Note 1)				0.8	V
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = 0.45 V				−0.250	mA
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = V_{CC}				40	μA
I_{SC}	Output Short-Circuit Current	V_{CC} = Max., V_{OUT} = 0.0 V (Note 2)		−20		−90	mA
I_{CC}	Power Supply Current	All inputs = GND, V_{CC} = Max.				185	mA
V_I	Input Clamp Voltage	V_{CC} = Min., I_{IN} = −18 mA				−1.2	V
I_{CEX}	Output Leakage Current	V_{CC} = Max. $V_{\overline{G}}$ = 2.4 V	V_O = V_{CC}			40	μA
			V_O = 0.4 V			−40	
C_{IN}	Input Capacitance	V_{IN} = 2.0 V @ f = 1 MHz (Note 3) V_{CC} = 5 V, T_A = 25°C			5		pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V @ f = 1 MHz (Note 3) V_{CC} = 5 V, T_A = 25°C			12		

Notes: 1. V_{IL} and V_{IH} are input conditions of output tests and are not themselves directly tested. V_{IL} and V_{IH} are absolute voltages with respect to device ground and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
2. Only one output should be shorted at a time. Duration of the short-circuit test should not be more than one second.
3. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

SWITCHING CHARACTERISTICS over operating ranges unless otherwise specified (For APL Products, Group A, Subgroups 9, 10, 11 are tested unless otherwise noted*) (Note 1)

No.	Parameter Symbol	Parameter Description		Am27S35A/ Am27S37A Min.	Am27S35A/ Am27S37A Max.	Am27S35/ Am27S37 Min.	Am27S35/ Am27S37 Max.	Unit
1	TAVKH	Address to K HIGH Setup Time	COM'L	35		40		ns
			MIL	40		45		
2	TKHAX	Address to K HIGH Hold Time	COM'L	0		0		ns
			MIL	0		0		
3	$TKHQV_1$	Delay from K HIGH to Output Valid, for initially active outputs (HIGH or LOW)	COM'L		20		25	ns
			MIL		25		30	
4	TKHKL TKLKH	K Pulse Width (HIGH or LOW)	COM'L	20		20		ns
			MIL	20		20		
5	TGLQV	Asynchronous Output Enable LOW to Output Valid (HIGH or LOW) (See Note 3)	COM'L		25		30	ns
			MIL		30		35	
6	TGHQZ	Asynchronous Output Enable HIGH to Output Hi-Z (See Notes 2 & 3)	COM'L		25		30	ns
			MIL		30		35	
7	TGSVKH	$\overline{G_S}$ to K HIGH Setup Time (See Note 4)	COM'L	15		15		ns
			MIL	15		15		
8	TKHGSX	$\overline{G_S}$ to K HIGH Hold Time (See Note 4)	COM'L	5		5		ns
			MIL	5		5		
9	TKHQV2	Delay from K HIGH to Output Valid, for initially Hi-Z outputs (See Note 4)	COM'L		25		30	ns
			MIL		30		35	
10	TKHQZ	Delay from K HIGH to Output Hi-Z (See Notes 2 & 4)	COM'L		25		30	ns
			MIL		30		35	
11	TILQV	Delay from $\overline{I}$ LOW to Output Valid (HIGH or LOW) (See Note 5)	COM'L		30		35	ns
			MIL		35		40	
12	TIHKH	Asynchronous $\overline{I}$ Recovery Time (See Note 5)	COM'L	20		20		ns
			MIL	20		25		
13	TILIH	Asynchronous $\overline{I}$ Pulse Width (See Note 5)	COM'L	25		25		ns
			MIL	30		30		
14	TISVKH	$\overline{I_S}$ to K HIGH Setup Time (See Note 6)	COM'L	25		30		ns
			MIL	30		35		
15	TKHISX	$\overline{I_S}$ to K HIGH Hold Time (See Note 6)	COM'L	0		0		ns
			MIL	0		0		

See also Switching Test Circuits.

Notes: 1. Tests are performed with input transition time of 5 ns or less, timing reference levels of 1.5 V, and input pulse levels of 0 to 3.0 V using test load in A under Switching Test Circuits.
2. TGHQZ and TKHQZ are measured at steady state HIGH output voltage −0.5 V and steady state LOW output voltage +0.5 V output levels using the test load in B under Switching Test Circuits.
3. Applies only when Asynchronous Enable ($\overline{G}$) function is used.
4. Applies only when Synchronous Enable ($\overline{G_S}$) function is used.
5. Applies only to the Am27S35 (Asynchronous Initialize ($\overline{I}$)) version.
6. Applies only to the Am27S37 (Synchronous Initialize ($\overline{I_S}$)) version.

*Subgroups 7 and 8 apply to functional tests.

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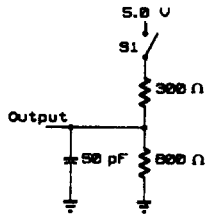
SWITCHING TEST CIRCUITS



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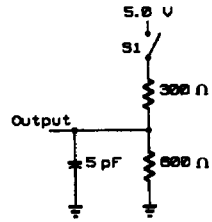
A. Output Load for All AC Tests Except TGHQZ and TKHQZ



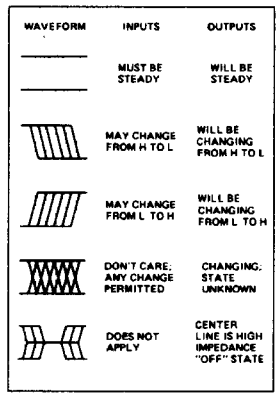
TC003452

B. Output Load for TGHQZ and TKHQZ

Notes: 1. All device test loads should be located within 2" of device output pin.
2. S_1 is open for Output Data HIGH to Hi-Z and Hi-Z to Output Data HIGH tests. S_1 is closed for all other AC tests.
3. Load capacitance includes all stray and fixture capacitance.

SWITCHING WAVEFORMS

KEY TO SWITCHING WAVEFORMS



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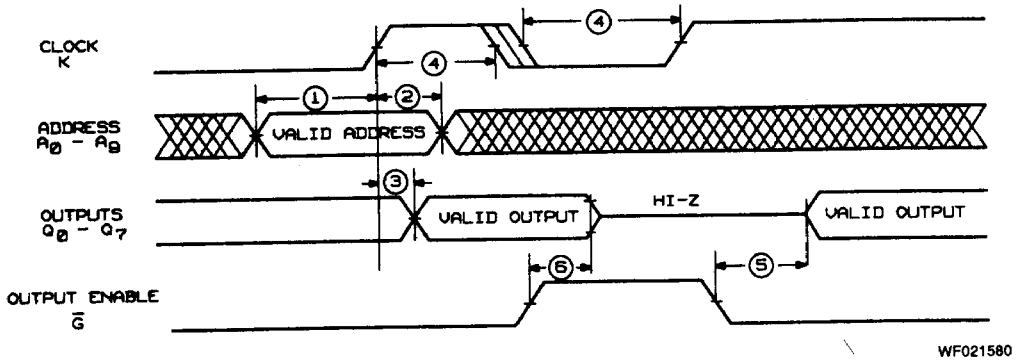
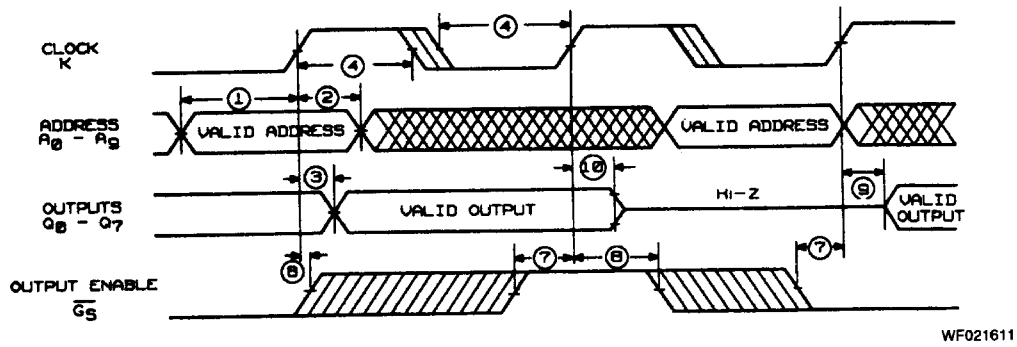
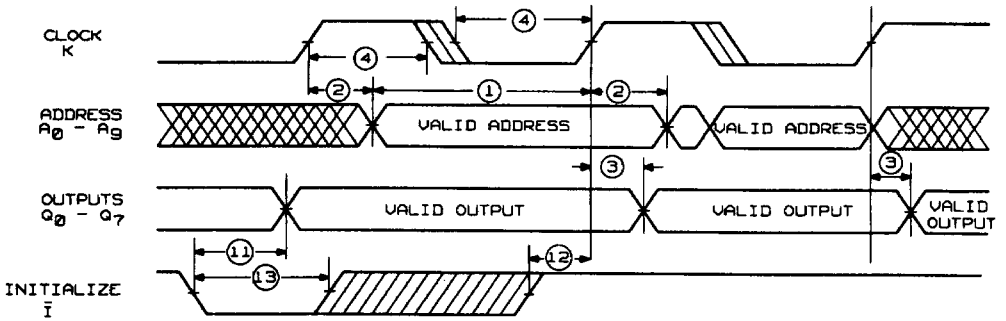


Timing Set 1. Using Asynchronous Enable



Timing Set 2. Using Synchronous Enable



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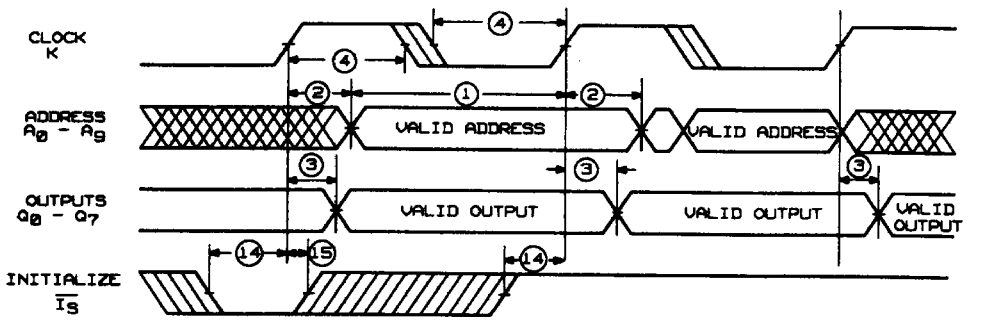
Timing Set 3. Using Asynchronous Initialize
Am27S35 Only



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Timing Set 4. Using Synchronous Initialize
Am27S37 Only