Am2602/9602

Dual Retriggerable Resettable Monostable Multivibrator

Distinctive Characteristics:

- Retriggerable 0 to 100% duty cycle.
- 50ns to ∞ output pulse width range.
- Am2602 guaranteed pulse width change over temperature range.
- 100% reliability assurance testing including high temperature bake, temperature cycling, centrifuge and package hermeticity testing in compliance with MIL-STD-883.
- Mixing privileges for obtaining price discounts. Refer to price list.
- Electrically tested and optically inspected dice for the assemblers of hybrid products.

FUNCTIONAL DESCRIPTION

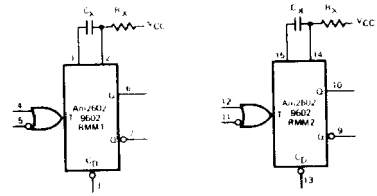
The Am2602 and Am9602 are dual DC-level sensitive resettable retriggerable monostable multivibrators which provide an output pulse whose duration and accuracy depend on external timing components.

Provision is made for triggering on the rising or falling edge of an input signal. All inputs are DC coupled making triggering independent of input rise and fall times. Each time the output from the OR trigger gate goes from a FALSE (LOW) to TRUE (HIGH) condition triggering occurs independent of the state of the monostable.

The direct clear facility allows a timing cycle to be terminated at any time during the cycle. A LOW signal on the $\overline{C}_D$ input resets the monostable independent of other conditions.

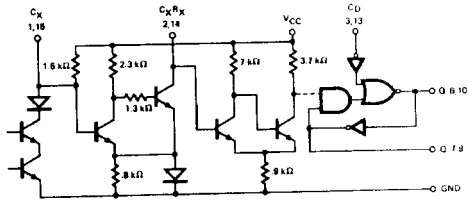
The Am2602 is a selected Am9602 with a guaranteed pulse width change of less than 1% over the temperature range of 0°C to +75°C.

LOGIC DIAGRAM



V_{CC} = Pin 16
Gnd = Pin 8

INTERNAL TIMING CIRCUITRY

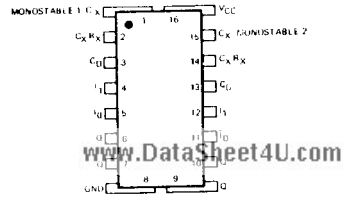


ORDERING INFORMATION

Part Number	Package Type	Temperature Range	Order Number
Am2602	Molded DIP	0°C to +75°C	AM260259A
Am2602	Hermetic DIP	0°C to +75°C	AM260259E
Am2602	Hermetic DIP	−55°C to +125°C	AM260251E
Am2602	Hermetic Flat Pak	−55°C to +125°C	AM260251N
Am2602	Dice	Note	AM2602XXD
Am9602	Molded DIP	0°C to +75°C	U6M960259X
Am9602	Hermetic DIP	0°C to +75°C	U7B960259X
Am9602	Hermetic DIP	−55°C to +125°C	U7B960251X
Am9602	Hermetic Flat Pak	−55°C to +125°C	U4L960251X
Am9602	Dice	Note	UXX9602XXD

Note: The dice supplied will contain units which meet both 0°C to +75°C and −55°C to +125°C temperature ranges.

CONNECTION DIAGRAM
Top View



MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150
Temperature (Ambient) Under Bias	−55°C to +125°
Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous	−0.5 V to +8
DC Voltage Applied to Outputs for High Output State	−0.5 V to +V_{CC} ma
DC Input Voltage	−0.5 V to +5.5
Output Current Into Outputs When Output is LOW	50 m
DC Input Current	−30 mA to +5 m

ELECTRICAL CHARACTERISTICS

Am2602S9/9602S9X T_A = 0°C to +75°C V_{CC} = 4.75 to 5.25 V (COM grade)
Am2602S1/9602S1X T_A = −55°C to +125°C V_{CC} = 4.50 to 5.50 V (MIL grade)

DC Characteristics Over Operating Range (Note 1)

Parameters	Operating Range	Test Conditions		LIMITS T_A = MIN Min	Max	T_A = +25°C Min	Typ	Max	T_A = MAX Min	Max	Units
V_{OH} Output HIGH Voltage	MIL or COM	V_{CC} = MIN., I_{OH} = −0.96 mA		2.40		2.40	3.6		2.40		Volts
V_{OL} Output LOW Voltage	MIL	I_{OL} = 8 x I_{IL} MAX.			0.40		0.2	0.40		0.40	Volts
	COM	I_{OL} = 8 x I_{IL} MAX.			0.45		0.2	0.45		0.45	
V_{IH} Input HIGH Voltage	MIL			2.00		1.70			1.50		Volts
	COM			1.90		1.80			1.60		
V_{IL} Input LOW Voltage	MIL				0.85			0.90		0.85	Volts
	COM				0.85			0.85		0.85	
I_{IL} Input Load Current	MIL	V_{IN} = 0.40 V	V_{CC} = MAX.		−1.60		−1.10	−1.60		−1.60	mA
			V_{CC} = MIN.		−1.24		−0.97	−1.24		−1.24	
	COM	V_{IN} = 0.45 V	V_{CC} = MAX.		−1.60		−1.00	−1.60		−1.60	
			V_{CC} = MIN.		−1.41		−0.90	−1.41		−1.41	
I_{IH} Reverse Input Current	MIL or COM	V_{CC} = MAX., V_{IN} = 4.5 V			60		2	60		60	µA
I_{SC} Short Circuit Current	MIL	V_{CC} = 5.0 V, V_O = 1.0 V				−8		−25			mA
	COM	V_{CC} = 5.0 V, V_O = 1.0 V				−8		−35			
I_{PD} Power Supply Current	9602 MIL	V_{CC} = 5.0 V	GND Pins 5 and 11		45		35	45		45	mA
	9602 COM		R_X = 10 kΩ		52		35	50		52	
	2602 COM	V_{CC} = MAX.	GND Pins 5 and 11		56		35	56		56	
	2602 MIL		R_X = 10 kΩ								

Switching Characteristics (T_A = 25°C)

Parameters			Test Conditions	2602 9602 MIL Min	Typ	Max	9602 COM Min	Typ	Max	Units
t_{pd+}	Turn Off Delay Negative Trigger Input to True Output		V_{CC} = 5.0 V, C_L = 15 pF R_X = 5 kΩ, C_X = 0 pF		25	35		25	40	ns
t_{pd-}	Turn On Delay Negative Trigger Input to False Output				25	35		25	40	ns
t_{pw} (min)	Minimum Output Pulse Width	True Output (Q)			45	65		50	70	ns
		False Output ($\overline{Q}$)			55	75		60	80	
t_{pw}	Pulse Width		V_{CC} = 5.0 V, C_L = 15 pF R_X = 10 kΩ, C_X = 1000 pF	3.08	3.42	3.76	3.08	3.42	3.76	µs
R_X	Timing Resistor over Temperature Range (Note 2)			5		50	5		50	kΩ
t_{pd-} ($\overline{C_D}$)	Delay from $\overline{C_D}$ to Q output LOW				11	17		11	17	ns

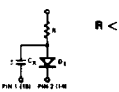
Am2602			Min	Typ	Max	
Δt_{pw} (T)	Maximum change in Pulse Width True Output over temperature range 0°C to +75°C	V_{CC} = 5.0 V, C_L = 15 pF R_X = 10 kΩ, C_X = 1000 pF		2.5	4.0	%
	Maximum change in Pulse Width True Output over temperature range −55°C to +125°C (Am2602 MIL)			4.0	7.0	

Notes: 1. Tests are conducted with a 10 kΩ resistor placed between Pin 2 (14) and V_{CC} unless otherwise noted.
2. Maximum permissible R_X when used below 0°C is 25 kΩ.

OPERATION RULES

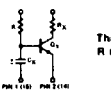
1. An external resistor R_x and an external capacitor C_x are required as shown in the logic diagram. The values of R_x may vary from 5.0 kΩ to 50 kΩ for 0°C to +75°C operation and 5.0 kΩ to 25 kΩ for −55°C to +125°C operation. C_x may vary from 0 to any value necessary and obtainable.
2. If a fixed value of R_x is used, the following values are recommended: R_x = 30 kΩ for 0°C to +75°C operation; R_x = 10 kΩ for −55°C to +125°C operation.
3. The output pulse width T is defined as follows:

   $T = 0.32\ R_xC_x\ [1 + \frac{0.7}{R_x}]$ (For C_x greater than 10^3 pF) Where: R_x is in kΩ, C_x is in pF, T is in ns. For $C_x < 10^3$ pF see Fig. 2
4. If electrolytic type capacitors are to be used, it is recommended that they have low leakage. For capacitors with a high reverse leakage the following circuits can be used:



$R < 0.6\ R_x$ (Max)

D_1: any silicon type diode, such as FD700



This circuit also allows larger value of R to be used for longer output pulse width.

$R < R_x\ (0.7)\ (h_{FE}Q_1)$

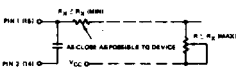
R_x (min) < R_x < R_x (max)

Q_1: Any NPN silicon device with sufficient h_{FE} at low currents, such as 2N2511

Both circuits prevent reverse voltage across C_x. The pulse width T for the circuits is defined as follows:

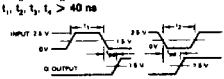
$T \approx 0.30\ RC_x\ [1 + \frac{0.7}{R}]$ Where: R is in kΩ, C_x is in pF, T is in ns.

5. To obtain variable pulse width, by remote trimming, the following circuit is recommended:

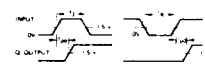


6. Under any operating condition, C_x and R_x (min) must be kept as close to the circuit as possible to minimize stray capacitance and reduce noise pickup.
7. Input Trigger Pulse Rules. $t_1, t_2, t_3, t_4 > 40$ ns

Input to Pin 5 (11) = LOW
Pin 4 (12) = HIGH
Pin 3 (13) = HIGH



Input to Pin 4 (12)
Pin 5 (11) = HIGH
Pin 3 (13) = HIGH



8. The retriggerable pulse width is calculated as shown below:

   $t_w = t_{pw} + t_{pd+} = 0.32\ R_xC_x\ (1 + \frac{0.7}{R_x}) + t_{pd+}$

   The retrigger pulse width is equal to the pulse width t_{pw} plus a delay time. For pulse widths greater than 500 ns, t_w can be approximated as t_{pw}.

   NOTE: Retriggering will not occur if the retrigger pulse comes within $0.32\ R_xC_x(\frac{0.7}{R_x})$ ns after the initial trigger pulse.
9. Reset Operation — The Am2602/9602 have an active LOW reset facility. By applying a low to the reset input, any timing cycle can be terminated or any new cycle inhibited until the low reset input is removed. Trigger inputs will not produce spikes in the output when the reset is held low.

DEFINITION OF TERMS

SUBSCRIPT TERMS:

H HIGH, applying to a HIGH logic level or when used with V_{CC} to indicate high V_{CC} value.

I Input.

L LOW, applying to LOW logic level or when used with V_{CC} to indicate low V_{CC} value.

O Output.

OPERATIONAL TERMS:

I_{IL} Forward input load current.

I_{OH} Output HIGH current, forced out of output in V_{OH} test.

I_{OL} Output LOW current, forced into the output in V_{OL} test.

I_{IH} Reverse input load current.

Negative Current Current flowing out of the device.

Positive Current Current flowing into the device.

V_{IH} Minimum logic HIGH input voltage. Refer to figure 2.

V_{IL} Maximum logic LOW input voltage. Refer to figure 2.

V_{OH} Minimum logic HIGH output voltage with output HIGH current I_{OH} flowing out of output.

V_{OL} Maximum logic LOW output voltage with output LOW current I_{OL} into output.

FUNCTIONAL TERMS:

$\overline{C}_D$ The asynchronous direct clear input. A LOW on this input resets the monostable independent of other conditions.

Fan-Out The logic HIGH or LOW output drive capability in terms of Input Unit Loads.

$\overline{I}_0$ The active LOW input of the monostables. With input I_1 LOW a HIGH to LOW transition on $\overline{I}_0$ will cause triggering.

I_1 The active HIGH input of the monostables. With $\overline{I}_0$ HIGH a LOW to HIGH transition on I_1 will cause triggering.

Input Unit Load One T^2L gate input load.

Q The TRUE output of the monostables.

$\overline{Q}$ The FALSE output of the monostables.

Triggering The switching of the monostable from the stable state to the unstable state and start of the timing cycle.

SWITCHING TERMS:

t_{pd+} The propagation delay from a HIGH to LOW transition on $\overline{I}_0$ to the true (Q) output LOW to HIGH transition.

t_{pd-} The propagation delay from a HIGH to LOW transition on $\overline{I}_0$ to the false ($\overline{Q}$) output HIGH to LOW transition.

t_{pw}**(min)** The minimum true (Q) output pulse width with R_x = 5kΩ, C_x = 0 pF.

t_{pw} The pulse width obtained with R_x = 10kΩ, C_x = 1000 pF.

Δt_{pw}**(T)** The maximum percentage change in pulse width of the true (Q) output for the Am2602 over the temperature range from the pulse width at 25°C.

Am 2602
Normalized Output Pulse Width Versus Ambient Temperature

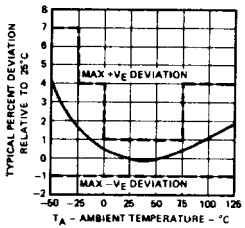
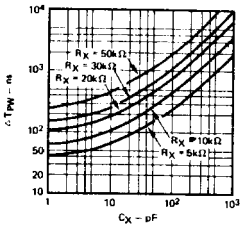


Figure 1

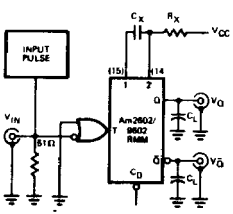
Output Pulse Width (ΔT_{pw}) Using Low Values of C_X



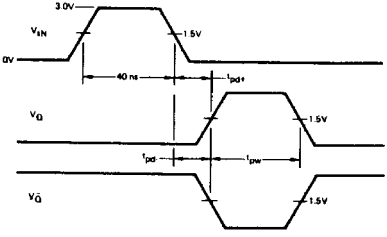
NOTE: Above $C_X = 10^3$ pF Use $\Delta T_{PW} = 0.32\, C_X\, R_X\, (1+0.7/R_X)$

Figure 2

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



VCC = Pin 16
Gnd. = Pin 8



INPUT PULSE
f ≃ 100 kHz
Duty cycle ≃ 40%
Width ≃ 40 ns
$t_r = t_f \leq 10$ ns

Figure 3

TRUTH TABLE

Am2602/9602
For Each Monostable

$\overline{I}_0$	I_1	$\overline{C}_D$	Operation
H→L	L	H	Trigger
H	L→H	H	Trigger
X	X	L	Reset

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
H→L = HIGH to LOW Voltage Level transition
L→H = LOW to HIGH Voltage Level transition

Table I

MSI INTERFACING RULES

Interfacing Digital Family	Equivalent Input Unit Load HIGH	LOW
Advanced Micro Devices 9300/2500 Series	1	1
FSC Series 9300	1	1
TI Series 54/7400	1	1
Signetics Series 8200	2	2
National Series DM 75/85	1	1
DTL Series 930	12	1

Table III

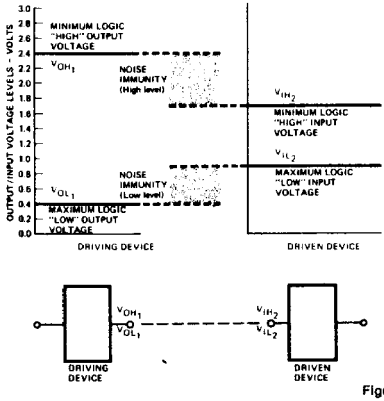
Am2602/9602 LOADING RULES

Input/Output	Pin No.'s	Input Unit Load	Fanout Output HIGH	Fanout Output LOW
Monostable 1 C_x	1	—	—	—
$C_x R_x$	2	—	—	—
$\overline{C}_D$	3	1	—	—
I_1	4	1	—	—
$\overline{I}_0$	5	1	—	—
Q	6	—	16	8
$\overline{Q}$	7	—	16	8
GND	8	—	—	—
Monostable 2 $\overline{Q}$	9	—	16	8
Q	10	—	16	8
$\overline{I}_0$	11	1	—	—
I_1	12	1	—	—
$\overline{C}_D$	13	1	—	—
$C_x R_x$	14	—	—	—
C_x	15	—	—	—
V_{CC}	16	—	—	—

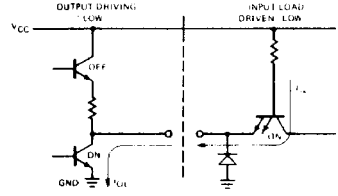
Table II

INPUT/OUTPUT INTERFACE CONDITIONS

Voltage Interface Conditions — LOW & HIGH



Current Interface Conditions — LOW



Current Interface Conditions — HIGH

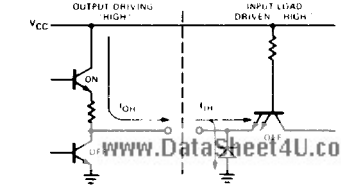
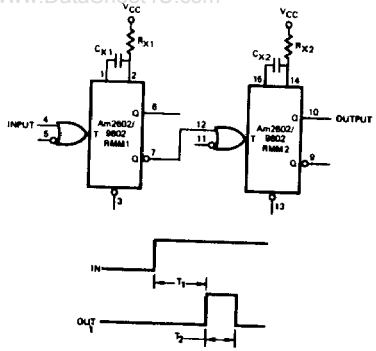


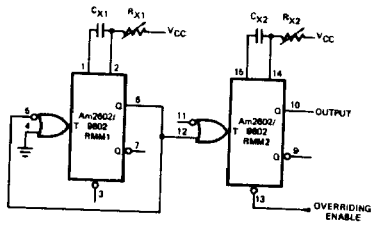
Figure 4



Delayed Pulse Generation

Figure 5

The first monostable determines the time T_1 before the initiation of the output pulse. The second monostable determines T_2, the output pulse width.



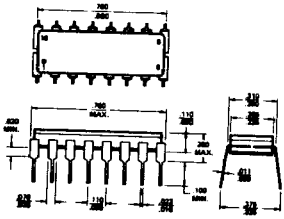
Pulse Generator

Figure 6

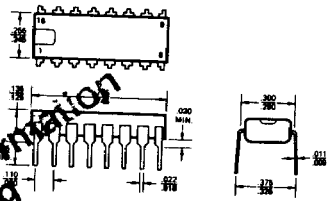
The output frequency produced with the above configuration is determined by C_{X1} and R_{X1}, while the pulse width is determined by C_{X2} and R_{X2}. Monostable 1 forms an astable multivibrator with an output pulse width of approximately 25 ns, while monostable 2 extends the pulse width to the required value.

PHYSICAL DIMENSIONS

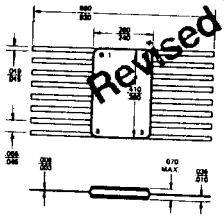
Hermetic
Dual-In-Line



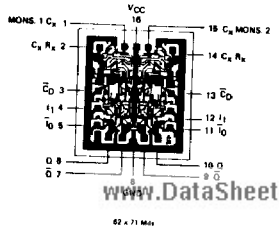
Molded



Flat Package



Metallization and Pad Layout



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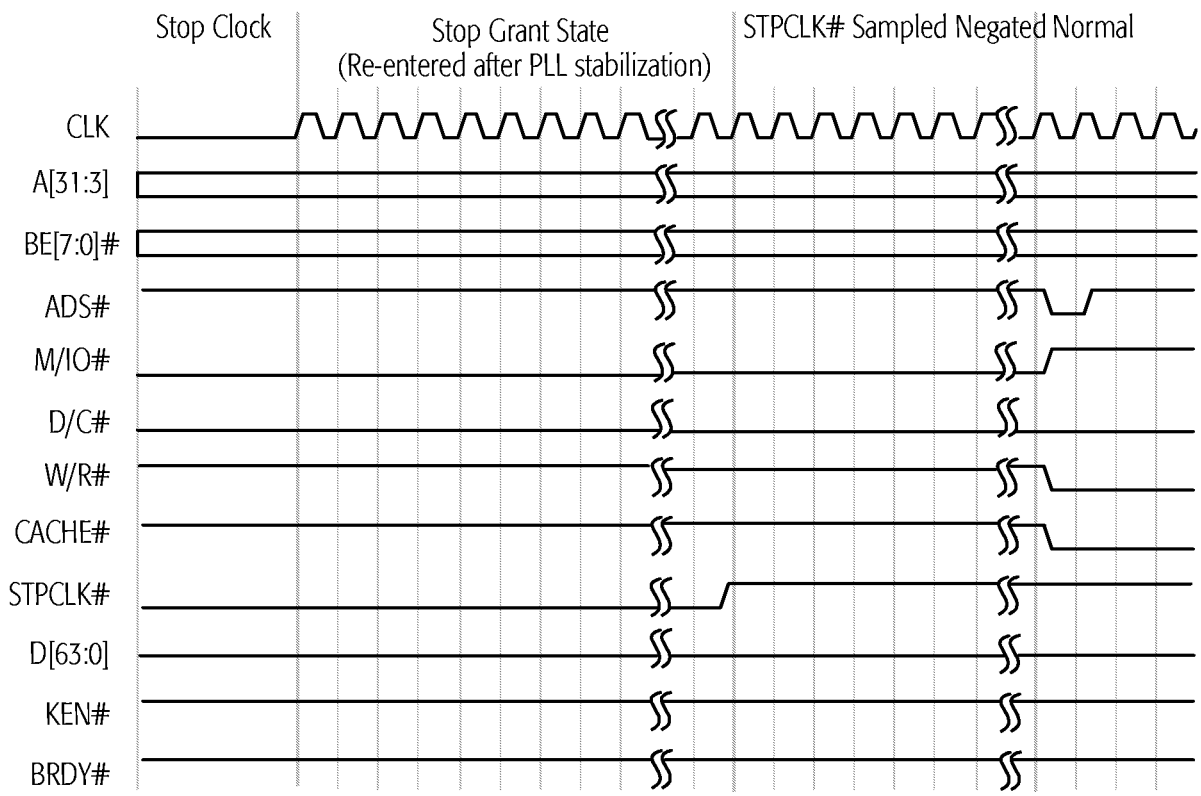

Figure 75. Stop Grant and Stop Clock Modes, Part 2

INIT-Initiated Transition from Protected Mode to Real Mode

INIT is typically asserted in response to a BIOS interrupt that writes to an I/O port. This interrupt is often in response to a Ctrl-Alt-Del keyboard input. The BIOS writes to a port (similar to port 64h in the keyboard controller) that asserts INIT. INIT is also used to support 80286 software that must return to Real mode after accessing extended memory in Protected mode.

The assertion of INIT causes the processor to empty its pipelines, initialize most of its internal state, and branch to address FFFF_FFF0h—the same instruction execution starting point used after RESET. Unlike RESET, the processor preserves the contents of its caches, the floating-point state, the MMX state, Model-Specific Registers (MSRs), the CD and NW bits of the CR0 register, the time stamp counter, and other specific internal resources.

Figure 76 shows an example in which the operating system writes to an I/O port, causing the system logic to assert INIT. The sampling of INIT asserted starts an extended microcode sequence that terminates with a code fetch from FFFF_FFF0h, the reset location. INIT is sampled on every clock edge but is not recognized until the next instruction boundary. During an I/O write cycle, it must be sampled asserted a minimum of three clock edges before BRDY# is sampled asserted if it is to be recognized on the boundary between the I/O write instruction and the following instruction. If INIT is asserted synchronously, it can be asserted for a minimum of one clock. If it is asserted asynchronously, it must have been negated for a minimum of two clocks, followed by an assertion of a minimum of two clocks.

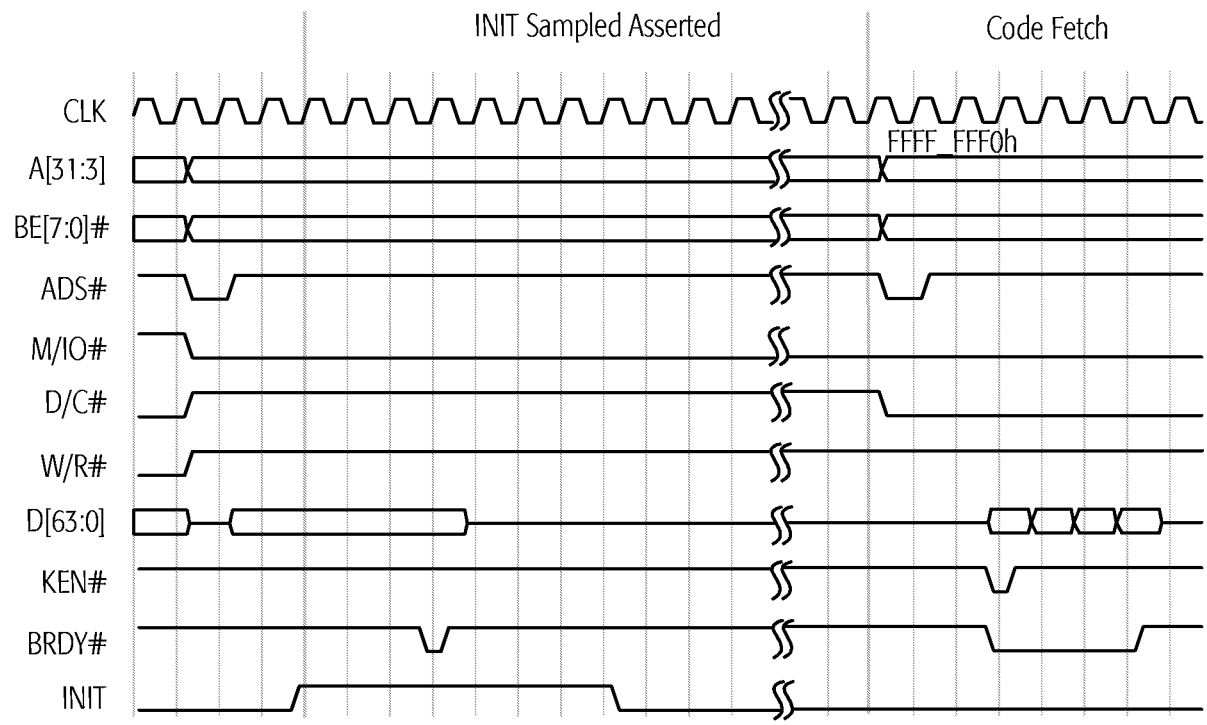

Figure 76. INIT-Initiated Transition from Protected Mode to Real Mode

6 Power-on Configuration and Initialization

On power-on the system logic must reset the AMD-K6-2 processor by asserting the RESET signal. When the processor samples RESET asserted, it immediately flushes and initializes all internal resources and its internal state, including its pipelines and caches, the floating-point state, the MMX and 3DNow! states, and all registers. Then the processor jumps to address FFFF_FFF0h to start instruction execution.

6.1 Signals Sampled During the Falling Transition of RESET

FLUSH# FLUSH# is sampled on the falling transition of RESET to determine if the processor begins normal instruction execution or enters Tri-State Test mode. If FLUSH# is High during the falling transition of RESET, the processor unconditionally runs its Built-In Self Test (BIST), performs the normal reset functions, then jumps to address FFFF_FFF0h to start instruction execution. (See "Built-In Self-Test (BIST)" on page 217 for more details.) If FLUSH# is Low during the falling transition of RESET, the processor enters Tri-State Test mode. (See "Tri-State Test Mode" on page 218 and "FLUSH# (Cache Flush)" on page 103 for more details.)

BF[2:0] The internal operating frequency of the processor is determined by the state of the bus frequency signals BF[2:0] when they are sampled during the falling transition of RESET. The frequency of the CLK input signal is multiplied internally by a ratio defined by BF[2:0]. (See "BF[2:0] (Bus Frequency)" on page 92 for the processor-clock to bus-clock ratios.)

BRDYC# BRDYC# is sampled on the falling transition of RESET to configure the drive strength of A[20:3], ADS#, HITM#, and W/R#. If BRDYC# is Low during the fall of RESET, these outputs are configured using higher drive strengths than the standard strength. If BRDYC# is High during the fall of RESET, the standard strength is selected. (See "BRDYC# (Burst Ready Copy)" on page 95 for more details.)

6.2 RESET Requirements

During the initial power-on reset of the processor, RESET must remain asserted for a minimum of 1.0 ms after CLK and V_{CC} reach specification. (See "CLK Switching Characteristics" on page 255 for clock specifications. See "Electrical Data" on page 247 for V_{CC} specifications.)

During a warm reset while CLK and V_{CC} are within specification, RESET must remain asserted for a minimum of 15 clocks prior to its negation.

6.3 State of Processor After RESET

Output Signals

Table 31 shows the state of all processor outputs and bidirectional signals immediately after RESET is sampled asserted.

Table 31. Output Signal State After RESET

Signal	State	Signal	State
A[31:3], AP	Floating	LOCK#	High
ADS#, ADSC#	High	M/IO#	Low
APCHK#	High	PCD	Low
BE[7:0]#	Floating	PCHK#	High
BREQ	Low	PWT	Low
CACHE#	High	SCYC	Low
D/C#	Low	SMIACT#	High
D[63:0], DP[7:0]	Floating	TDO	Floating
FERR#	High	VCC2DET	Low
HIT#	High	VCC2H/L#	Low
HITM#	High	W/R#	Low
HLDA	Low	–	–

Registers

Table 32 on page 175 shows the state of all architecture registers and Model-Specific Registers (MSRs) after the processor has completed its initialization due to the recognition of the assertion of RESET.