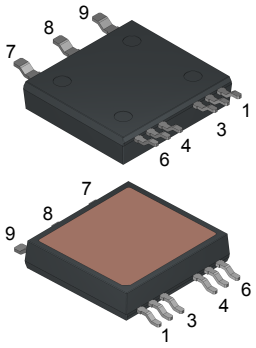
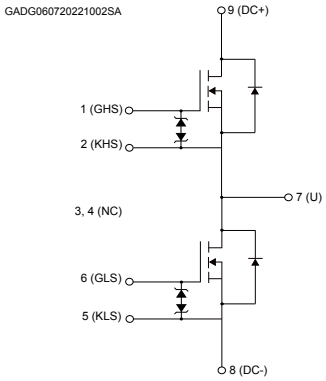
SH68N65DM6AG

Datasheet

Automotive-grade N-channel 650 V, 35 mΩ typ., 64 A MDmesh DM6 half-bridge topology Power MOSFET in an ACEPACK SMIT package



ACEPACK SMIT



Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D
SH68N65DM6AG	650 V	41 mΩ	64 A

- AQG 324 qualified
- Half-bridge power module
- 650 V blocking voltage
- Fast recovery body diode
- Very low switching energies
- Low package inductance
- Dice on direct bond copper (DBC) substrate
- Low thermal resistance
- Isolation rating of 3.4 kVrms/min

Applications

- Switching applications

Description

This device combines two MOSFETs in a half-bridge topology. The ACEPACK SMIT is a very compact and rugged power module in a surface mount package for easy assembly. Thanks to the DBC substrate, the ACEPACK SMIT package offers low thermal resistance coupled with an isolated top-side thermal pad. The high design flexibility of the package enables several configurations, including phase legs, boost, and single switch through different combinations of the internal power switches.

Product status link
SH68N65DM6AG

Product summary	
Order code	SH68N65DM6AG
Marking	H68N65DM6
Package	ACEPACK SMIT
Packing	Tape and reel

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	±25	V
I_D	Drain current (continuous) at T_C = 25 °C	64	A
I_D	Drain current (continuous) at T_C = 100 °C	40	A
I_{DM} (1)	Drain current (pulsed)	280	A
P_{TOT}	Total power dissipation at T_C = 25 °C	379	W
dv/dt (2)	Peak diode recovery voltage slope	100	V/ns
di/dt (2)	Peak diode recovery current slope	1000	A/µs
dv/dt (3)	MOSFET dv/dt ruggedness	100	V/ns
V_{ISO}	Isolation withstand voltage applied between each pin and heat sink plate (AC voltage (50/60 Hz, t = 60 s)	3.4	kVrms
T_{STG}	Storage temperature range	-55 to 150	°C
T_J	Operating junction temperature range		°C

1. *Pulse width limited by safe operating area.*
2. *I_{SD} ≤ 64 A, V_{DS} (peak) < $V_{(BR)DSS}$, V_{DD} = 400 V.*
3. *V_{DS} ≤ 520 V.*

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Thermal resistance, junction-to-case	0.33	°C/W

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not repetitive (t_p limited by T_J max)	9	A
E_{AS}	Single pulse avalanche energy (starting T_J = 25 °C, I_D = I_{AR})	1.9	J

2 Electrical characteristics

T_C = 25 °C unless otherwise specified

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V, I_D = 1 mA	650			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = 650 V			5	µA
		V_{GS} = 0 V, V_{DS} = 650 V, T_C = 125 °C (1)			300	
I_{GSS}	Gate-body leakage current	V_{DS} = 0 V, V_{GS} = ±25 V			±5	µA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	3.25	4	4.75	V
$R_{DS(on)}$	Static drain-source on resistance	V_{GS} = 10 V, I_D = 23 A		35	41	mΩ

1. *Defined by design, not subject to production test.*

Table 5. Dynamic characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 100 V, f = 1 MHz, V_{GS} = 0 V	-	5900	-	pF
C_{oss}	Output capacitance		-	260	-	
C_{rss}	Reverse transfer capacitance		-	2.6	-	
$C_{oss\ eq.}$ (1)	Equivalent output capacitance	V_{DS} = 0 to 520 V, V_{GS} = 0 V	-	867	-	
R_G	Intrinsic gate resistance	f = 1 MHz, I_D = 0 A	-	1.4	-	Ω
Q_g	Total gate charge	V_{DD} = 520 V, I_D = 72 A, V_{GS} = 0 to 10 V (see Figure 13. Test circuit for gate charge behavior)	-	116	-	nC
Q_{gs}	Gate-source charge		-	37	-	
Q_{gd}	Gate-drain charge		-	45	-	

1. *$C_{oss\ eq}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}.*

Table 6. Switching characteristics (resistive load)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 325 V, I_D = 36 A, R_G = 4.7 Ω , V_{GS} = 10 V (see Figure 12. Switching times test circuit for resistive load and Figure 17. Switching time waveform)	-	42	-	ns
t_r	Rise time		-	19	-	ns
$t_{d(off)}$	Turn-off delay time		-	108	-	ns
t_f	Fall time		-	11	-	ns

Table 7. Switching characteristics (inductive load)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(v)}$	Voltage delay time	V_{DD} = 400 V, V_{GS} = 0 to 10 V, I_D = 72 A, R_G = 6.8 Ω (see Figure 14. Test circuit for inductive load switching and diode recovery times and Figure 18. Turn-off switching time waveform on inductive load)	-	117	-	ns
$t_{r(v)}$	Voltage rise time		-	10	-	
$t_{f(i)}$	Current fall time		-	18	-	
t_c(off)	Crossing time off		-	24	-	
$t_{d(i)}$	Current delay time	V_{DD} = 400 V, V_{GS} = 0 to 10 V, I_D = 72 A, R_G = 82 Ω (see Figure 14. Test circuit for inductive load switching and diode recovery times and Figure 19. Turn-on switching time waveform on inductive load)	-	354	-	
$t_{f(i)}$	Current rise time		-	140	-	
$t_{f(v)}$	Voltage fall time		-	14	-	
t_c(on)	Crossing time on		-	252	-	

Table 8. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		64	A
I_{SDM}(1)	Source-drain current (pulsed)		-		280	A
V_{SD}(2)	Forward on voltage	V_{GS} = 0 V, I_{SD} = 46 A	-		1.6	V
t_{rr}	Reverse recovery time	I_{SD} = 72 A, di/dt = 100 A/µs, V_{DD} = 60 V (see Figure 14. Test circuit for inductive load switching and diode recovery times)	-	166		ns
Q_{rr}	Reverse recovery charge		-	1.1		µC
I_{RRM}	Reverse recovery current		-	11		A
t_{rr}	Reverse recovery time	I_{SD} = 72 A, di/dt = 100 A/µs, V_{DD} = 60 V, T_J = 150 °C (see Figure 14. Test circuit for inductive load switching and diode recovery times)	-	336		ns
Q_{rr}	Reverse recovery charge		-	5.1		µC
I_{RRM}	Reverse recovery current		-	26		A

1. *Pulse width is limited by safe operating area.*
2. *Pulsed: pulse duration = 300 µs, duty cycle 1.5%.*

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

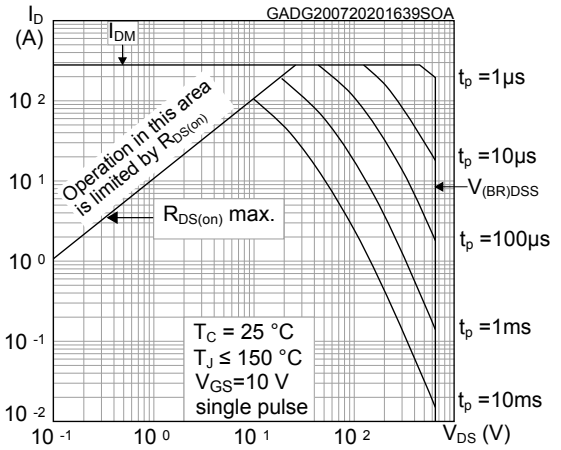


Figure 2. Maximum transient thermal impedance

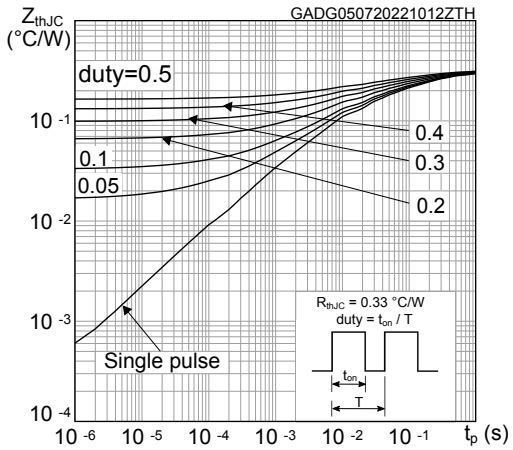


Figure 3. Typical output characteristics

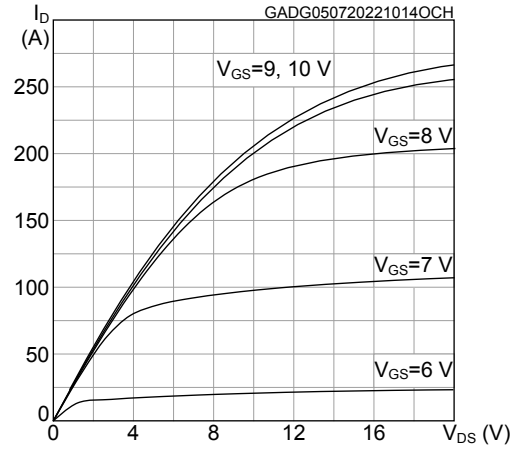


Figure 4. Typical transfer characteristics

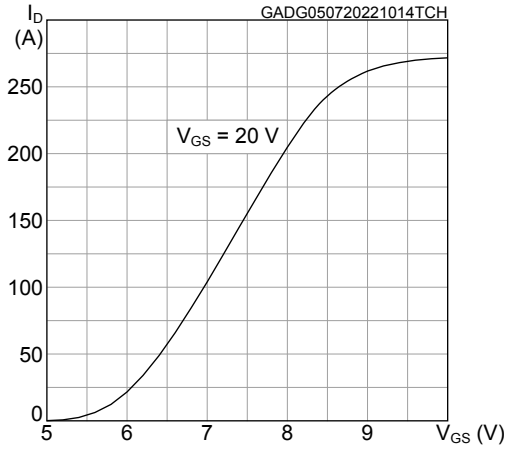


Figure 5. Typical gate charge characteristics

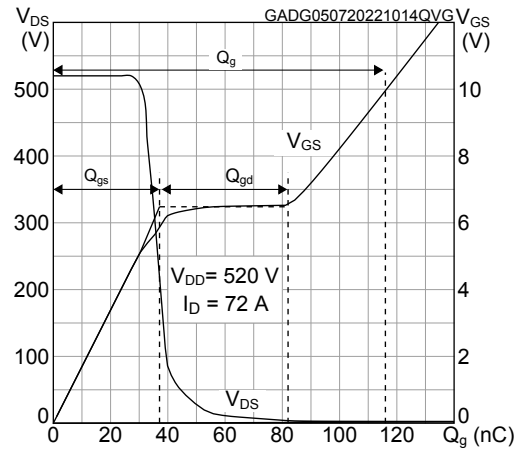


Figure 6. Typical drain-source on-resistance

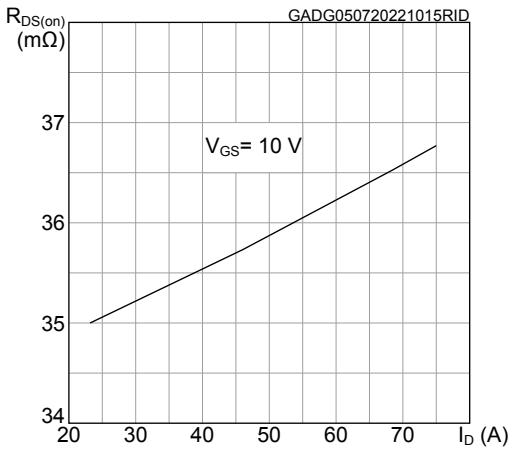


Figure 7. Typical capacitance characteristics

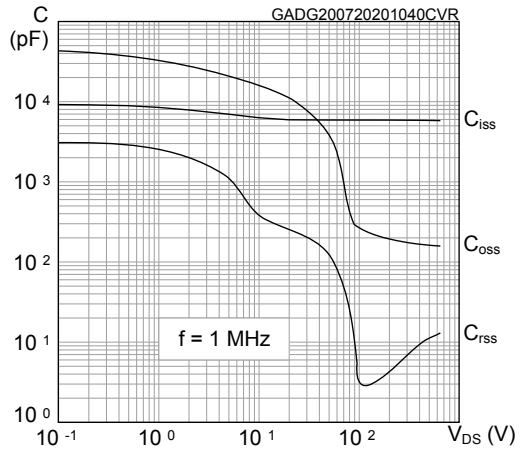


Figure 8. Normalized gate threshold vs temperature

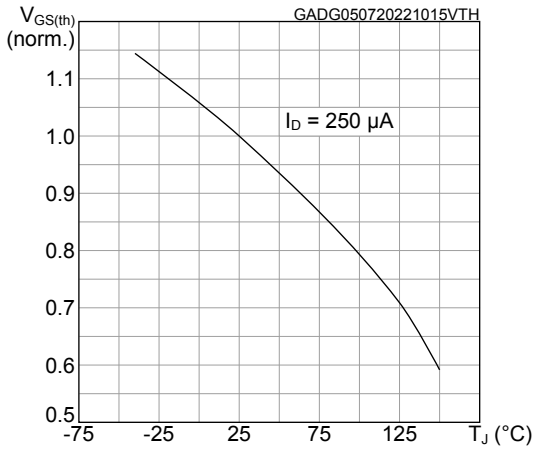


Figure 9. Normalized on-resistance vs temperature

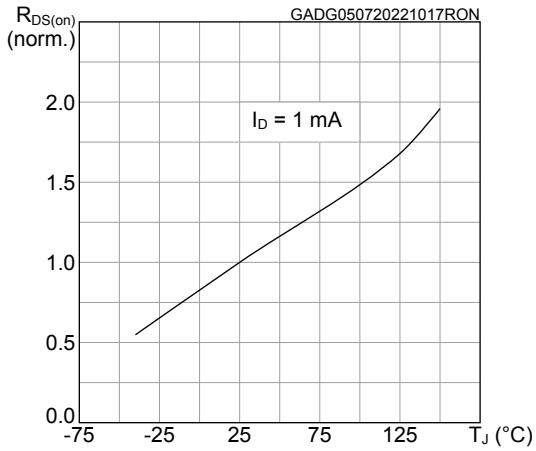


Figure 10. Normalized breakdown voltage vs temperature

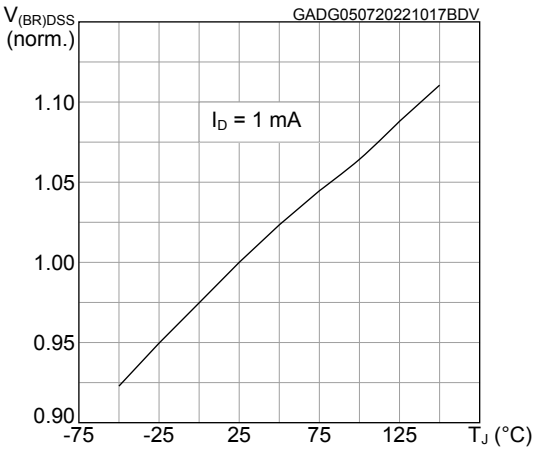
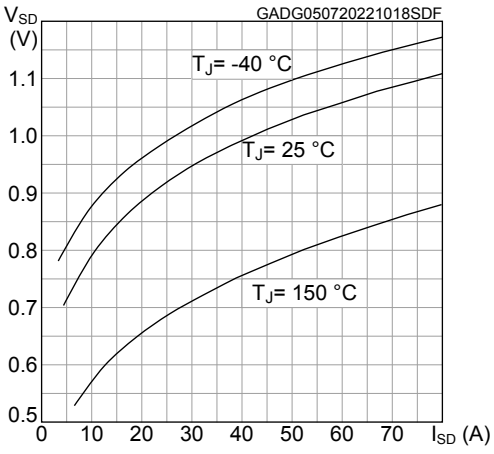


Figure 11. Typical reverse diode forward characteristics



3 Test circuits

Figure 12. Switching times test circuit for resistive load

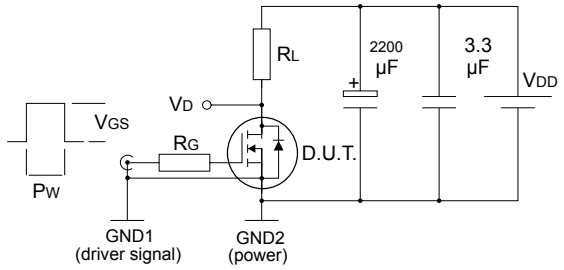


Figure 13. Test circuit for gate charge behavior

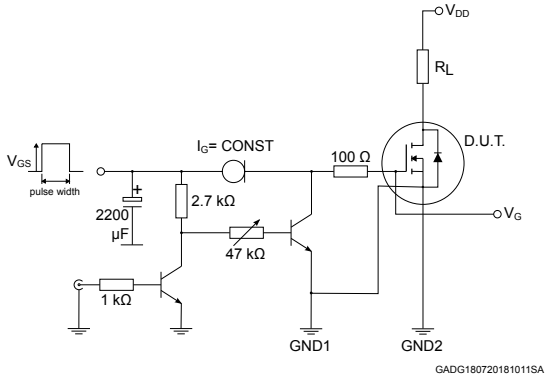


Figure 14. Test circuit for inductive load switching and diode recovery times

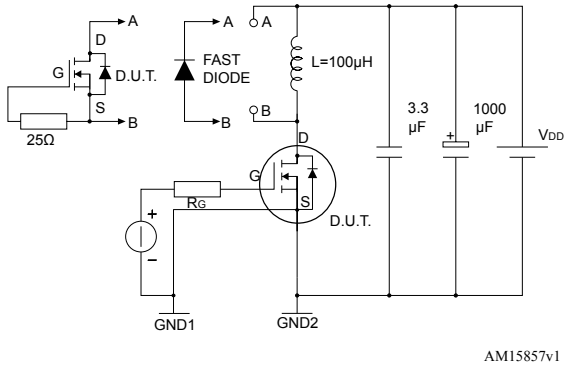


Figure 15. Unclamped inductive load test circuit

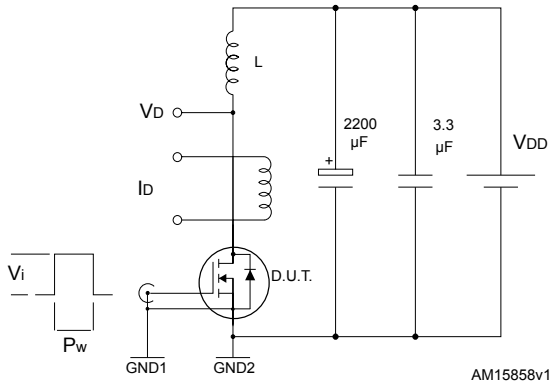


Figure 16. Unclamped inductive waveform

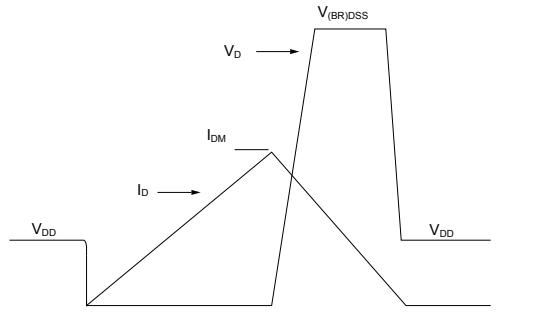


Figure 17. Switching time waveform

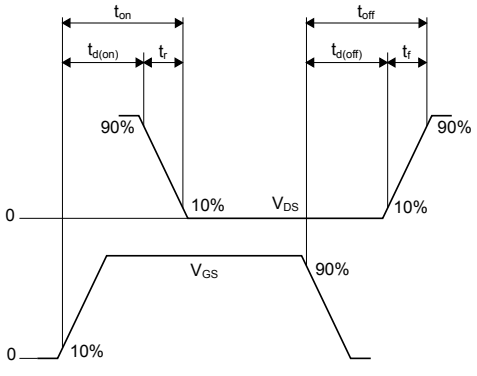


Figure 18. Turn-off switching time waveform on inductive load

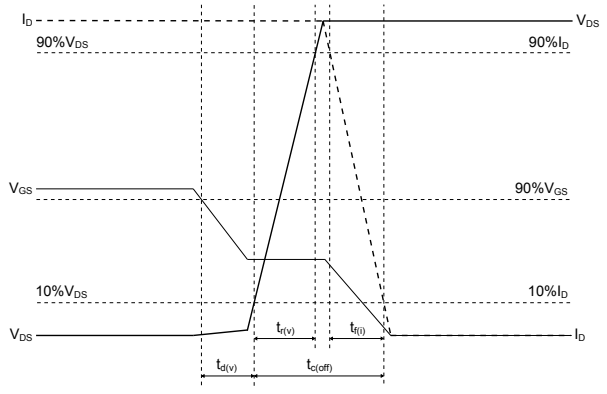
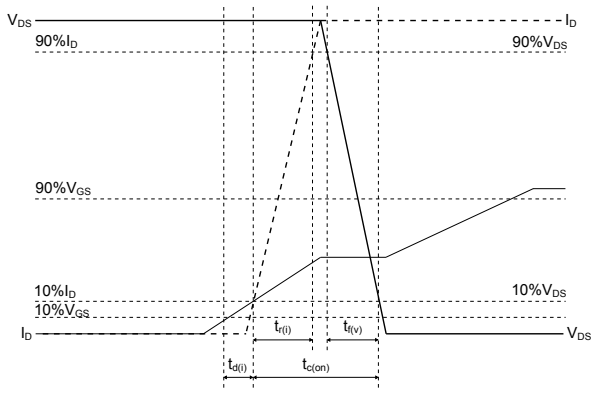


Figure 19. Turn-on switching time waveform on inductive load

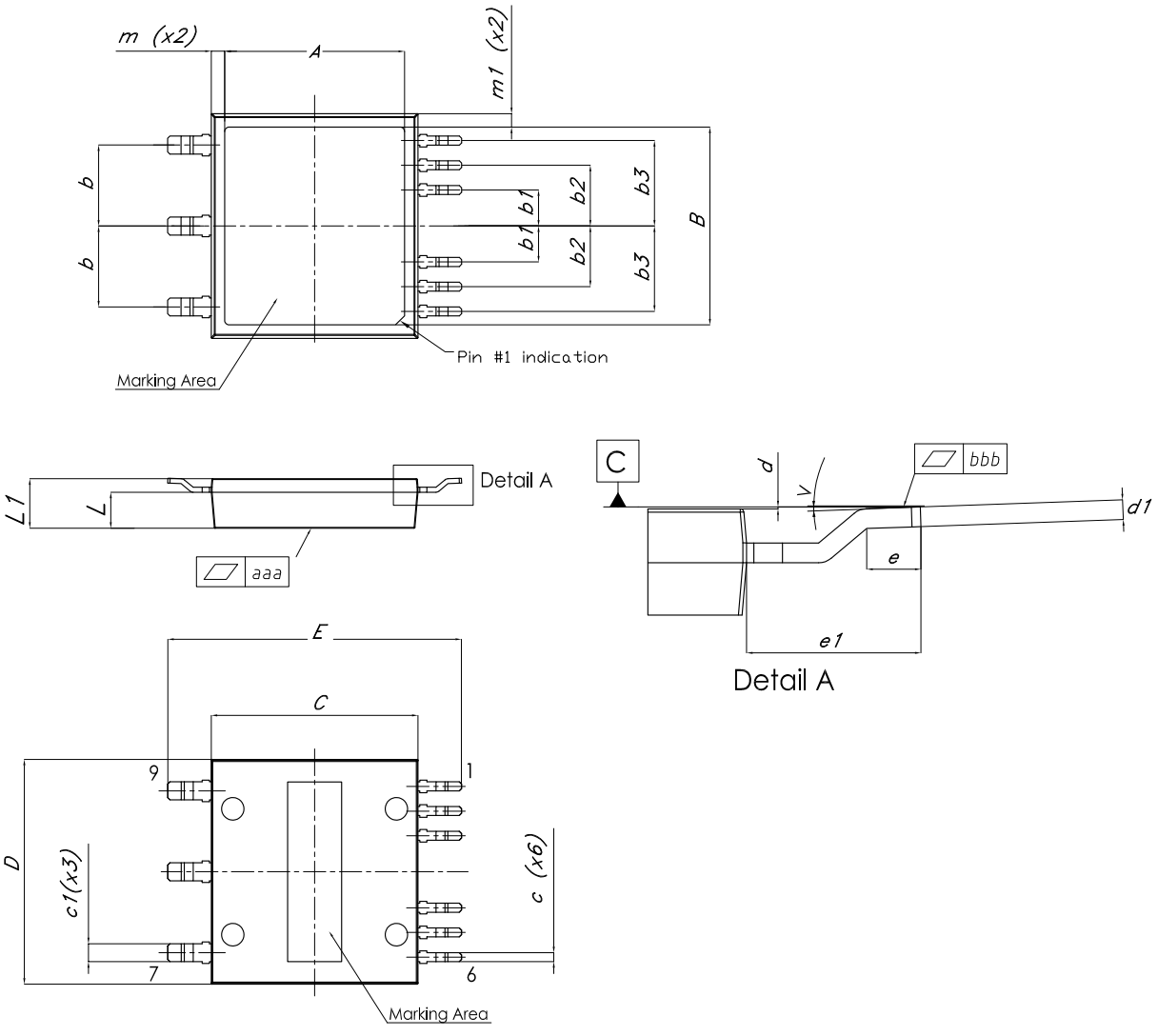


4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 ACEPACK SMIT package information

Figure 20. ACEPACK SMIT package outline

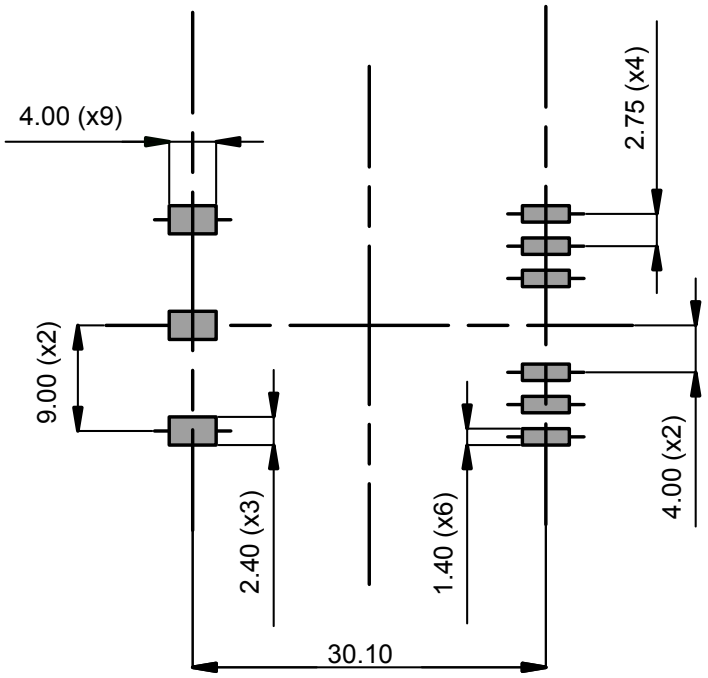


DM00447519_Rev.6

Table 9. **ACEPACK SMIT package mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	19.50	20.00	20.50
B	21.50	22.00	22.50
C	22.80	23.00	23.20
D	24.80	25.00	25.20
E	32.20	32.70	33.20
b		9.00	
b1		4.00	
b2		6.75	
b3		9.50	
c	0.95	1.00	1.10
c1	1.95	2.00	2.10
d	0.00		0.15
d1	0.45	0.55	0.65
e	1.30	1.50	1.70
e1	4.65	4.85	5.05
L	3.95	4.00	4.05
L1	5.40	5.50	5.60
m	1.30	1.50	1.80
m1	1.30	1.50	1.80
V	0°	2°	4°
aaa	0.01		0.05
bbb	0.00		0.10

Figure 21. **ACEPACK SMIT recommended footprint**



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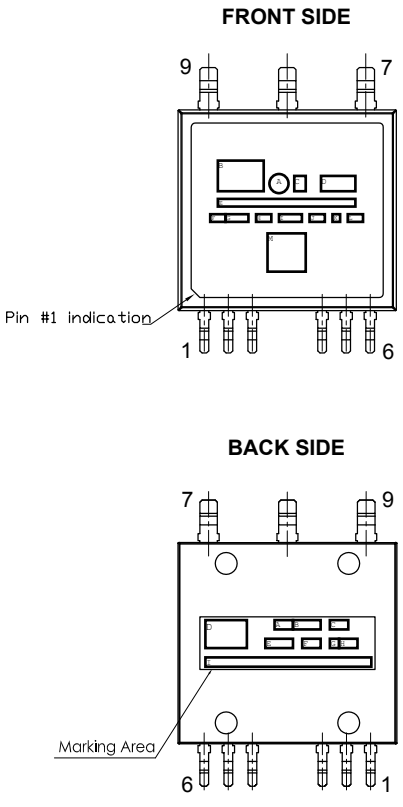
Note: Dimensions in mm.

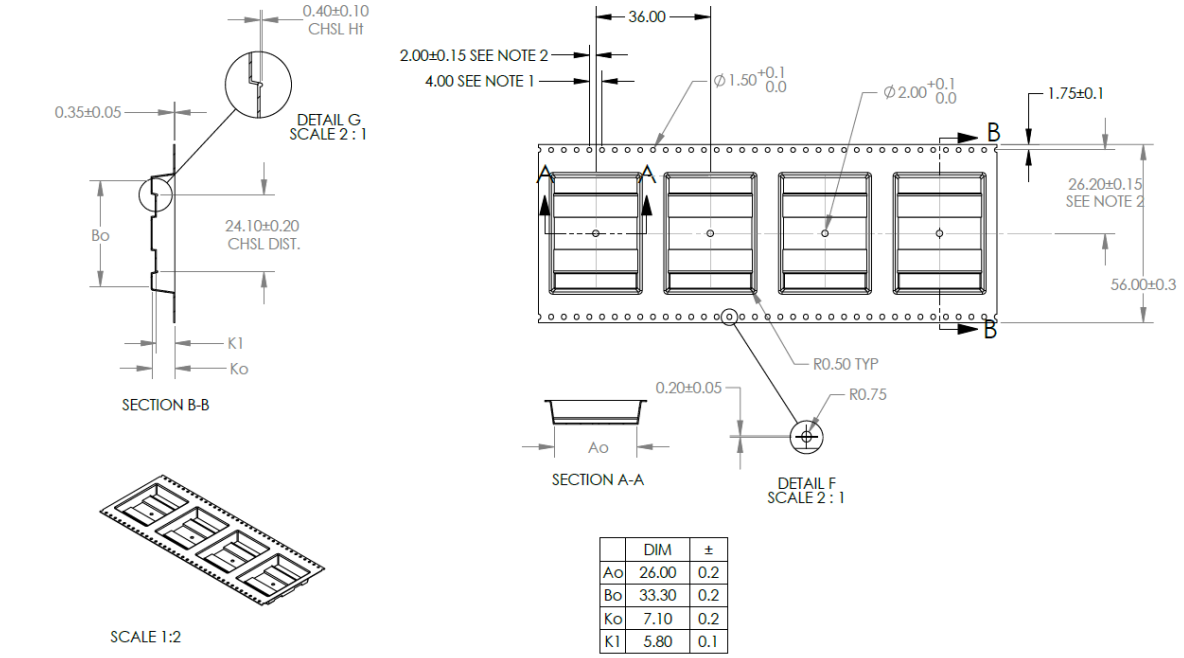
Figure 22. **ACEPACK SMIT marking orientation vs pinout**



DM00447519_MO_Rev.6

4.2 ACEPACK SMIT packing information

Figure 23. ACEPACK SMIT tape outline



	DIM	±
Ao	26.00	0.2
Bo	33.30	0.2
Ko	7.10	0.2
K1	5.80	0.1

NOTES:
1. 10 SPROCKET HOLE PITCH CUMULATIVE TOLERANCE ±0.2
2. POCKET POSITION RELATIVE TO SPROCKET HOLE MEASURED AS TRUE POSITION OF POCKET, NOT POCKET HOLE.
3. Ao AND Bo ARE MEASURED ON A PLANE AT A DISTANCE "R" ABOVE THE BOTTOM OF THE POCKET.

DM00631393_Tape_Rev.1

Note: Dimensions in mm.

Revision history

Table 10. **Document revision history**

Date	Revision	Changes
25-Jul-2022	1	First release.

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