# Stereo 2-W Audio Power Amplifier (with DC_Volume Control)

## Features

- **Low Operating Current with 14mA**
- **Improved Depop Circuitry to Eliminate Turn-on and Turn-off Transients in Outputs**
- **High PSRR**
- **32 Steps Volume Adjustable by DC Voltage with Hysteresis**
- **2W Per Channel Output Power into 4Ω Load at 5V, BTL Mode**
- **Two Output Modes Allowable with BTL and SE Modes Selected by SE/$\overline{\text{BTL}}$ Pin**
- **Low Current Consumption in Shutdown Mode (50μA)**
- **Short Circuit Protection**
- **Power off Depop Circuit Integration**
- **TSSOP-24P with or without Thermal Pad Package**
- **Lead Free and Green Devices Available (RoHS Compliant)**

## General Description

APA2120/1 is a monolithic integrated circuit, which provides precise DC volume control, and a stereo bridged audio power amplifiers is capable of producing 2.7W(2.0W) into 3Ω with less than 10% (1.0%)THD+N. The attenuator range of the volume control in APA2120/1 is from 20dB (DC_Vol=0V) to -80dB (DC_Vol=3.54V) with 32 steps. The advantage of internal gain setting can be less components and PCB area. Both of the depop circuitry and the thermal shutdown protection circuitry are integrated in APA2120/1 and reduce pops and clicks noise during power up or shutdown mode operation. It also improves the power off pop noise and protects the chip from being destroyed by over temperature and short current failure. To simplify the audio system design, APA2120/1 combines a stereo bridge-tied loads (BTL) mode for speaker drive and a stereo single-end (SE) mode for headphone drive into a single chip, where both modes are easily switched by the SE/$\overline{\text{BTL}}$ input control pin signal. Besides, the multiple input selection is used for portable audio system.

## Applications

- **NoteBook PC**
- **LCD Monitor or TV**

## Ordering and Marking Information

APA2120/1 □□-□□□

- Assembly Material
- Handling Code
- Temperature Range
- Package Code

Package Code
R : TSSOP-24P
Operating Ambient Temperature Range
I : - 40 to 85 °C
Handling Code
TR : Tape & Reel
Assembly Material
G : Halogen and Lead Free Device

APA2120/1 R : APA2120/1 XXXXX

XXXXX - Date Code

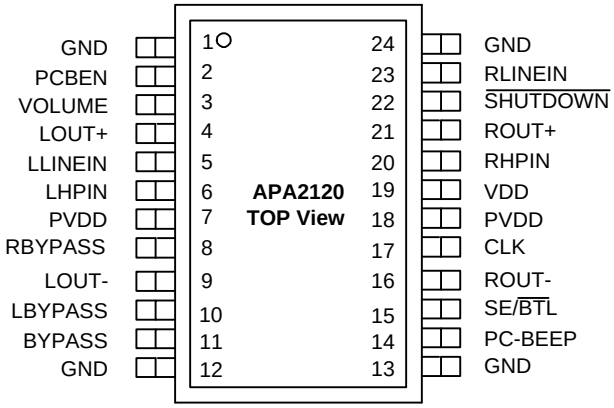
Note: ANPEC lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS. ANPEC lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J-STD-020D for MSL classification at lead-free peak reflow temperature. ANPEC defines “Green” to mean lead-free (RoHS compliant) and halogen free (Br or Cl does not exceed 900ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500ppm by weight).

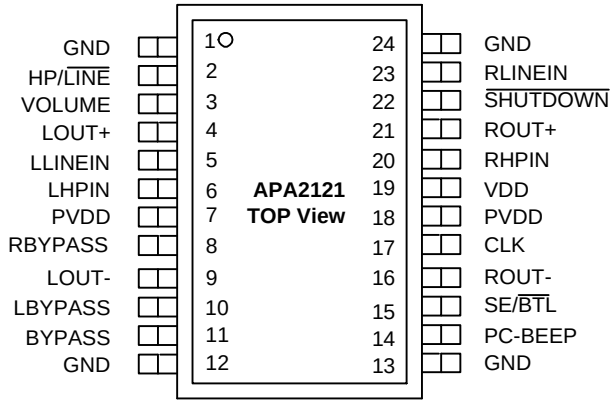
ANPEC reserves the right to make changes to improve reliability or manufacturability without notice, and advise customers to obtain the latest version of relevant information to verify before placing orders.

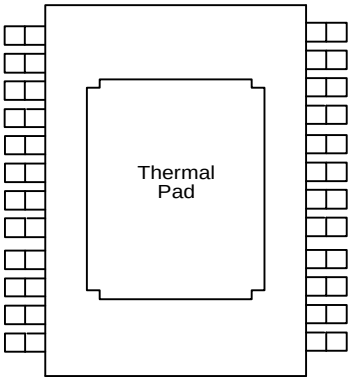
Copyright © ANPEC Electronics Corp.


Rev. A.4 - Jul., 2013

## Pin Configuration




APA2120/1
Bottom View

| | Multiple Input Selection | PCBEEP Control Input |
|---|---|---|
| APA2120 | SE/$\overline{\text{BTL}}$ | PCBEN |
| APA2121 | HP/$\overline{\text{LINE}}$ | - |

## Absolute Maximum Ratings (Note 1)

(Over operating free-air temperature range unless otherwise noted.)

| Symbol | Parameter | Rating | Unit |
|---|---|---|---|
| $V_{DD}$ | Supply Voltage Range | -0.3 to 6 | V |
| $V_{IN}$ | Input Voltage Range, SE/$\overline{\text{BTL}}$, HP/$\overline{\text{LINE}}$, $\overline{\text{SHUTDOWN}}$, PCBEN | -0.3 to $V_{DD}$+0.3 | V |
| $T_A$ | Operating Ambient Temperature Range | -40 to 85 | °C |
| $T_J$ | Maximum Junction Temperature | Intermal Limited(Note 2) | °C |
| $T_{STG}$ | Storage Temperature Range | -65 to +150 | °C |
| $T_S$ | Maximum Lead Soldering Temperature,10 Seconds | 260 | °C |
| $P_D$ | Power Dissipation | Intermal Limited | W |

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: APA2120/1 integrated internal thermal shutdown protection when junction temperature ramp up to 150°C

Copyright © ANPEC Electronics Corp.

## Thermal Characteristics

| Symbol | Parameter | Typical Value | Unit |
|---|---|---|---|
| $\theta_{JA}$ | Thermal Resistance from Junction to Ambient in Free Air (Note 3) TSSOP-24P | 45 | °C/W |

Note 3 : 5 in$^2$ printed circuit board with 2oz trace and copper pad through 9 25mil diameter vias. The thermal pad on the TSSOP_P package with solder on the printed circuit board.

## Recommended Operating Conditions

| Symbol | Parameter | | Range | Unit |
|---|---|---|---|---|
| $V_{DD}$ | Supply Voltage | | 4.5 ~ 5.5 | V |
| $V_{IH}$ | High Level Threshold Voltage | $\overline{SHUTDOWN}$, PCBEN | 2 ~ | V |
| | | SE/$\overline{BTL}$ , HP/$\overline{LINE}$ | 4 ~ | |
| $V_{IL}$ | Low Level Threshold Voltage | $\overline{SHUTDOWN}$, PCBEN | ~ 1.0 | V |
| | | SE/$\overline{BTL}$ , HP/$\overline{LINE}$ | ~ 3 | |
| $V_{ICM}$ | Common Mode Input Voltage | | $V_{DD}$-1.0 ~ | V |

## Electrical Characteristics

$V_{DD}$=5V, -20°C<$T_A$<85°C (unless otherwise noted)

| Symbol | Parameter | Test Conditions | APA2120/1 | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| $V_{DD}$ | Supply Voltage | | 4.5 | - | 5.5 | V |
| $I_{DD}$ | Supply Current | SE/$\overline{BTL}$=0V | - | 14 | 25 | mA |
| | | SE/$\overline{BTL}$=5V | - | 8.0 | 15 | |
| $I_{SD}$ | Supply Current in Shutdown Mode | SE/$\overline{BTL}$=5V, $\overline{SHUTDOWN}$=0V | - | 50 | - | µA |
| $I_{IH}$ | High input Current | | - | 900 | - | nA |
| $I_{IL}$ | Low Input Current | | - | 900 | - | nA |
| $V_{OS}$ | Output Differential Voltage | | - | 5 | - | mV |

Operating Characteristics, BTL mode

$V_{DD}$=5V,$T_A$=25°C, $R_L$=4Ω, $A_V$=2V/V (unless otherwise noted)

| Symbol | Parameter | Test Conditions | APA2120/1 | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| $P_O$ | Maximum Output Power | THD+N=10%, $R_L$=3Ω, $f_{in}$=1kHz | - | 2.7 | - | W |
| | | THD+N=10%, $R_L$=4Ω, $f_{in}$=1kHz | - | 2.3 | - | |
| | | THD+N=10%, $R_L$=8Ω, $f_{in}$=1kHz | - | 1.5 | - | |
| | | THD+N=1%, $R_L$=3Ω, $f_{in}$=1kHz | - | 2.0 | - | |
| | | THD+N=1%, $R_L$=4Ω, $f_{in}$=1kHz | - | 1.9 | - | |
| | | THD+N=0.5%, $R_L$=8Ω, $f_{in}$=1kHz | 1 | 1.1 | - | |
| THD+N | Total Harmonic Distortion Plus Noise | $P_O$=1.5W, $R_L$=4Ω, $f_{in}$=1kHz | - | 0.05 | - | % |
| | | $P_O$=1W, $R_L$=8Ω, $f_{in}$=1kHz | - | 0.07 | - | |
| PSRR | Power Ripple Rejection Ratio | $V_{IN}$=0.1Vrms, $R_L$=8Ω, $C_B$=1µF, $f_{in}$=120Hz | - | 60 | - | dB |

Copyright © ANPEC Electronics Corp.

## Electrical Characteristics (Cont.)

Operating Characteristics, BTL mode

$V_{DD}$=5V,$T_A$=25°C, $R_L$=4Ω, $A_V$=2V/V (unless otherwise noted)

| Symbol | Parameter | Test Conditions | APA2120/1 | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| Xtalk | Channel Separation | $C_B$=1μF, $R_L$=8Ω, $f_{in}$=1kHz | - | 90 | - | dB |
| S/N | Signal to Noise Ratio | $P_O$=1.1mW, $R_L$=8Ω, A_weighting | - | 95 | - | dB |

Operating Characteristics, SE mode

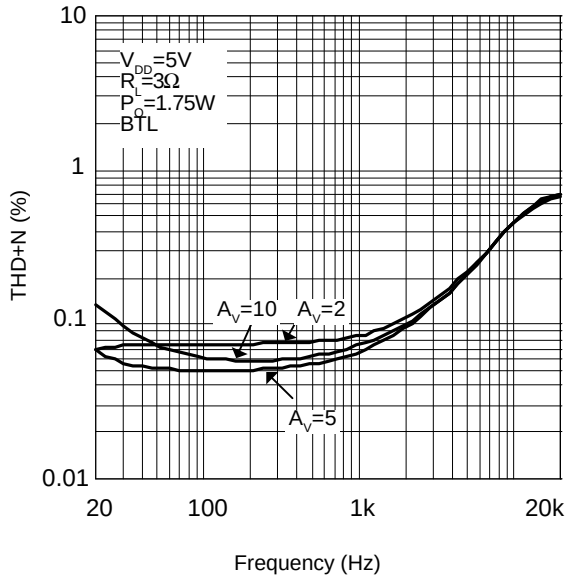
$V_{DD}$=5V,$T_A$=25°C, $R_L$=4Ω, Gain=1V/V (unless otherwise noted)

| Symbol | Parameter | Test Conditions | APA2120/1 | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| $P_O$ | Maximum Output Power | THD+N=10%, $R_L$=8Ω, $f_{in}$=1kHz | - | 400 | - | mW |
| | | THD+N=10%, $R_L$=32Ω, $f_{in}$=1kHz | - | 110 | - | |
| | | THD+N=1%, $R_L$=8Ω, $f_{in}$=1kHz | - | 320 | - | |
| | | THD+N=1%, $R_L$=32Ω, $f_{in}$=1kHz | - | 90 | - | |
| THD+N | Total Harmonic Distortion Plus Noise | $P_O$=250mW, $R_L$=8Ω, $f_{in}$=1kHz | - | 0.08 | - | % |
| | | $P_O$=75mW, $R_L$=32Ω, $f_{in}$=1kHz | - | 0.08 | - | |
| PSRR | Power Ripple Rejection Ratio | $V_{IN}$=0.1Vrms, $R_L$=8Ω, $C_B$=1μF, $f_{in}$=120Hz | - | 48 | - | dB |
| Xtalk | Channel Separation | $C_B$=1μF, $R_L$=32Ω, $f_{in}$=1kHz | - | 100 | - | dB |
| S/N | Signal to Noise Ratio | $P_O$=75mW, SE, $R_L$=32Ω, A_weighting | - | 100 | - | dB |

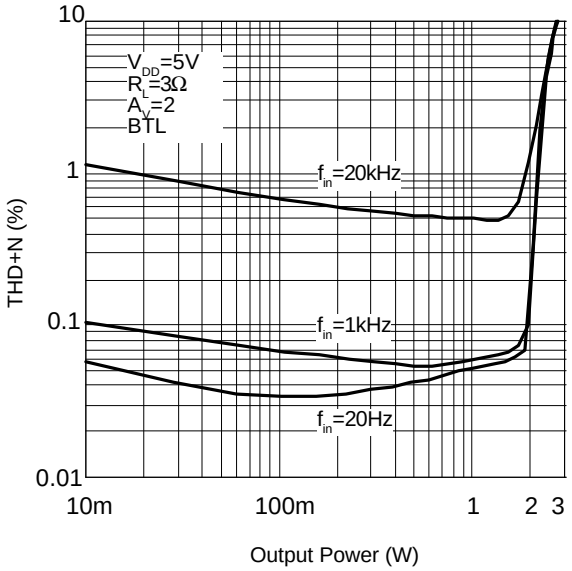
Copyright © ANPEC Electronics Corp.

## Typical Operating Characteristics

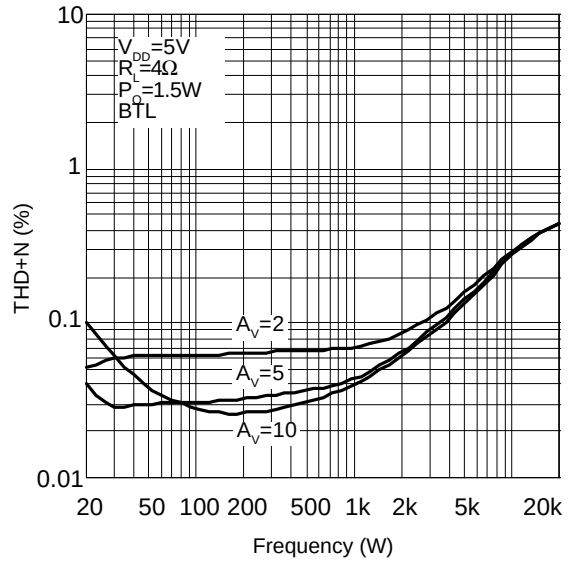
**THD+N vs. Frequency**



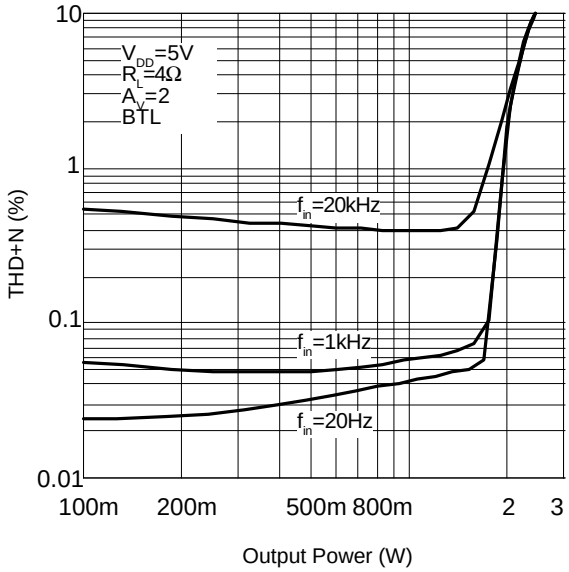

**THD+N vs. Output Power**




**THD+N vs. Frequency**

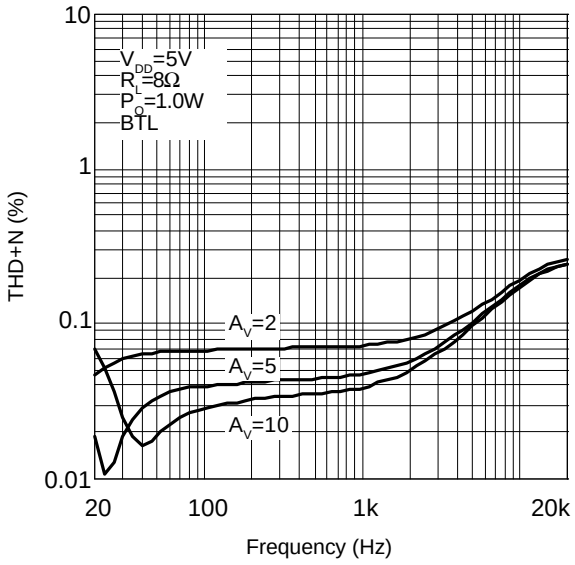



**THD+N vs. Output Power**

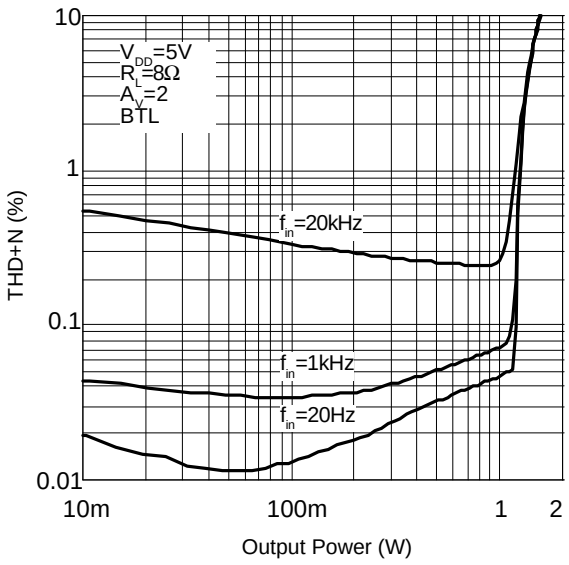


## Typical Operating Characteristics (Cont.)

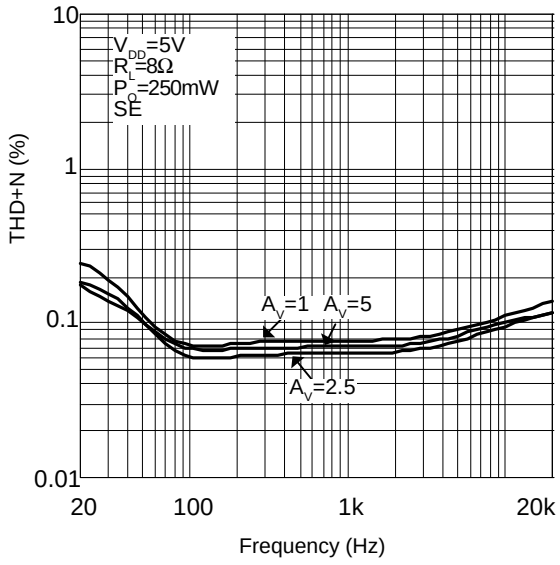
**THD+N vs. Frequency**



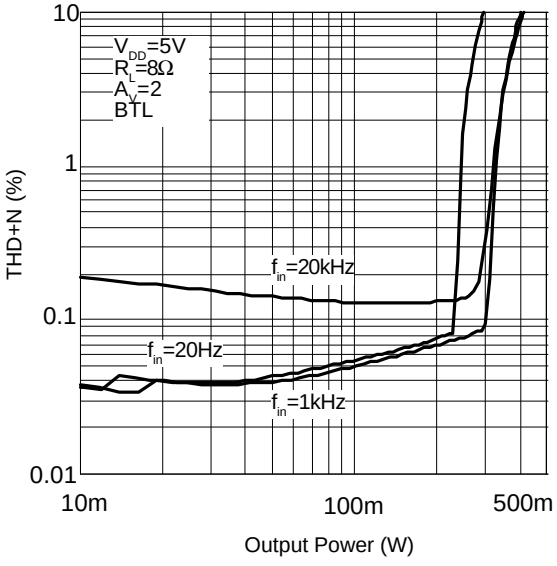

**THD+N vs. Output Power**




**THD+N vs. Frequency**

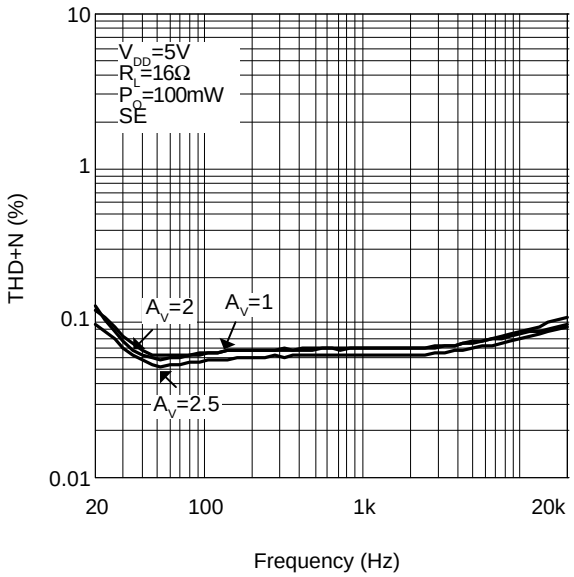



**THD+N vs. Output Power**

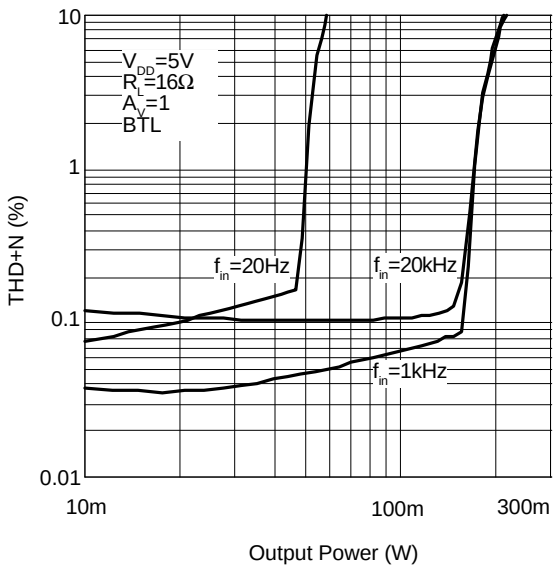


## Typical Operating Characteristics (Cont.)

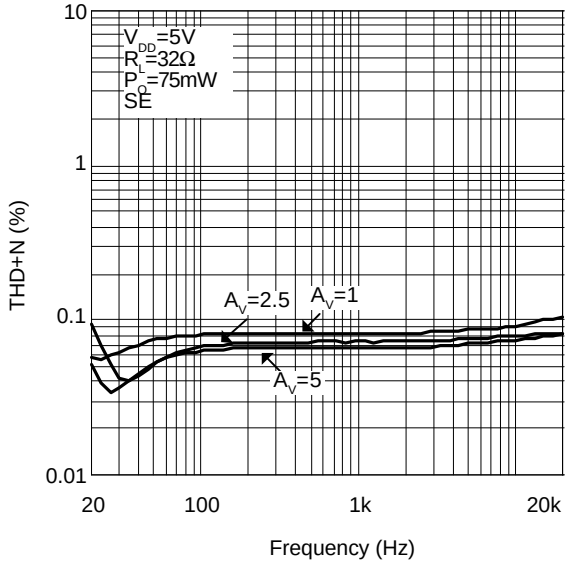
**THD+N vs. Frequency**



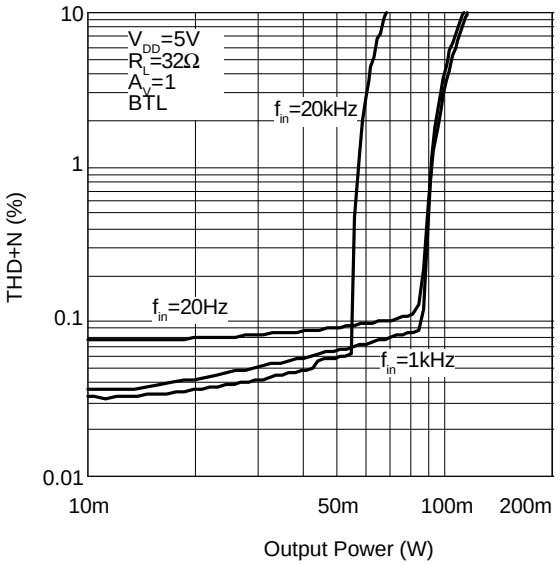

**THD+N vs. Output Power**




**THD+N vs. Frequency**



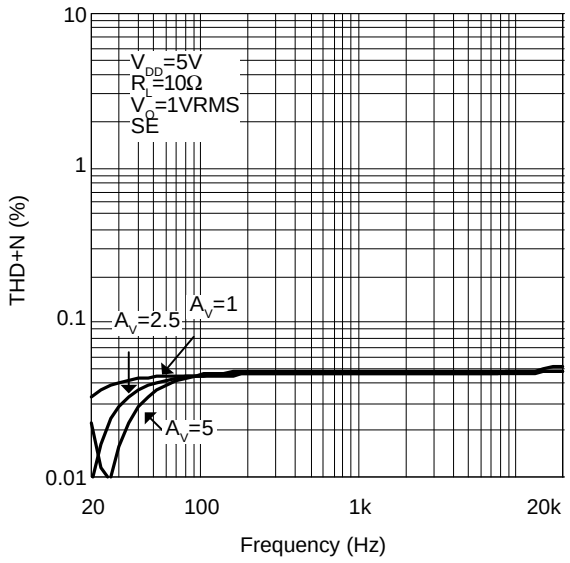

**THD+N vs. Output Power**



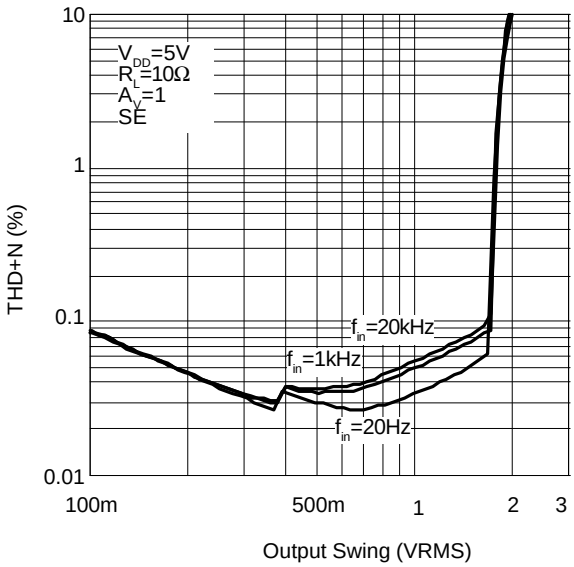

Copyright © ANPEC Electronics Corp.

## Typical Operating Characteristics (Cont.)

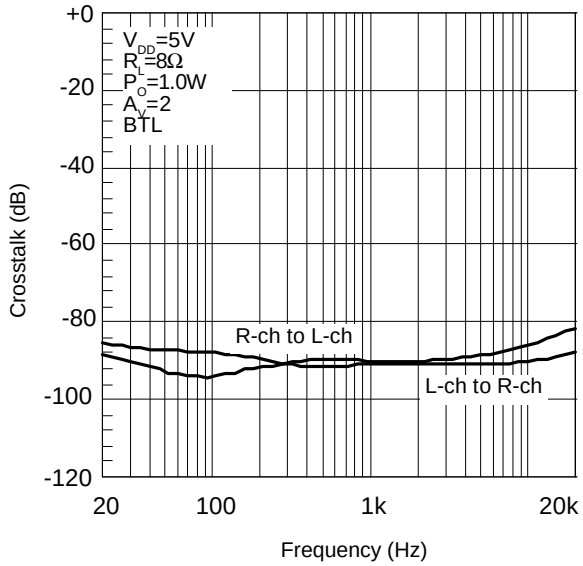
**THD+N vs. Frequency**



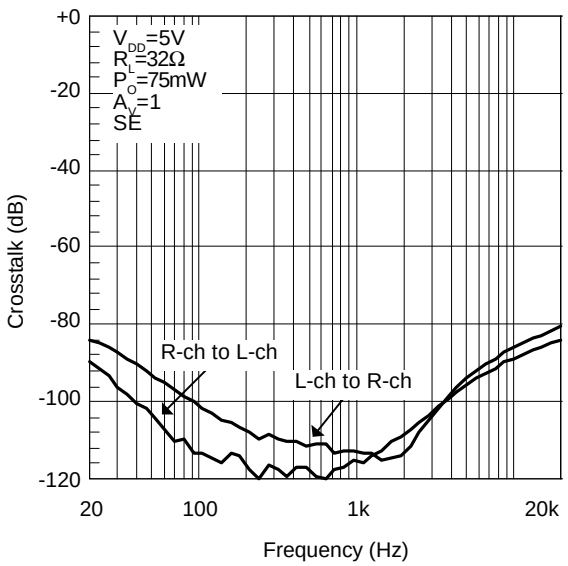

**THD+N vs. Output Swing**




**Crosstalk vs. Frequency**



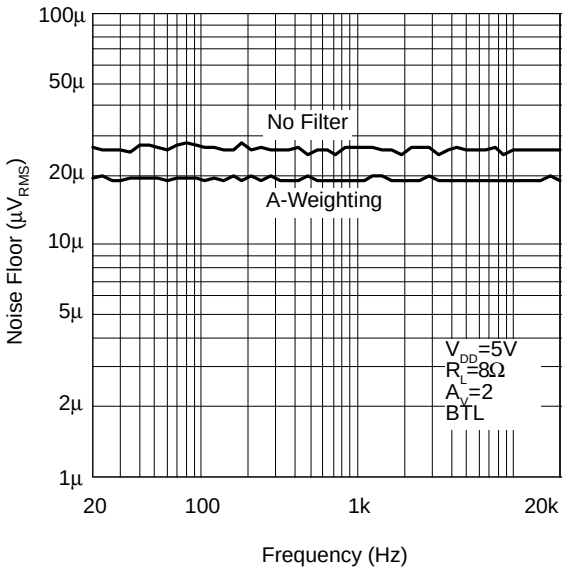

**Crosstalk vs. Frequency**



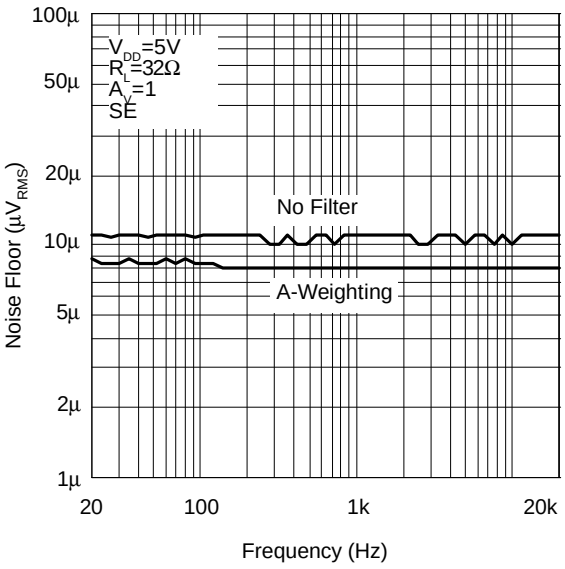

Copyright © ANPEC Electronics Corp.

## Typical Operating Characteristics (Cont.)

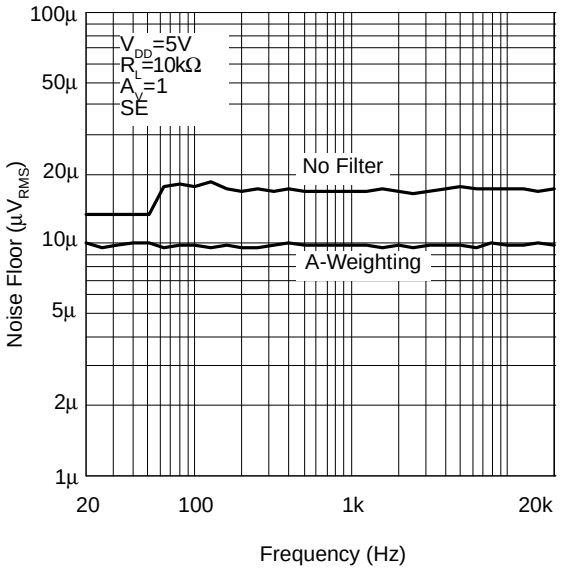
**Noise Floor vs. Frequency**



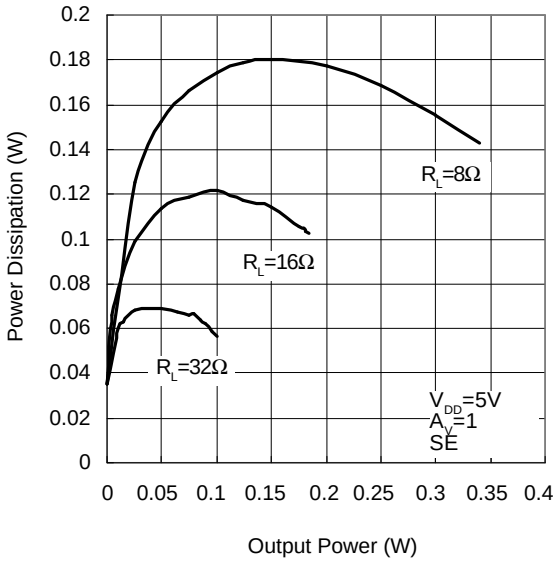

**Noise Floor vs. Frequency**




**Noise Floor vs. Frequency**



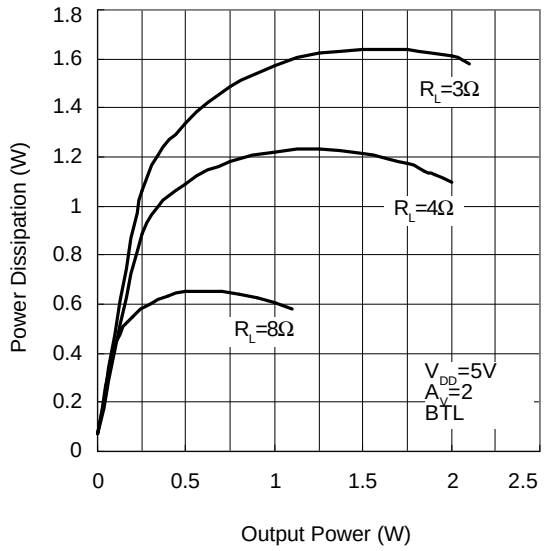

**Power Dissipation vs. Output Power**



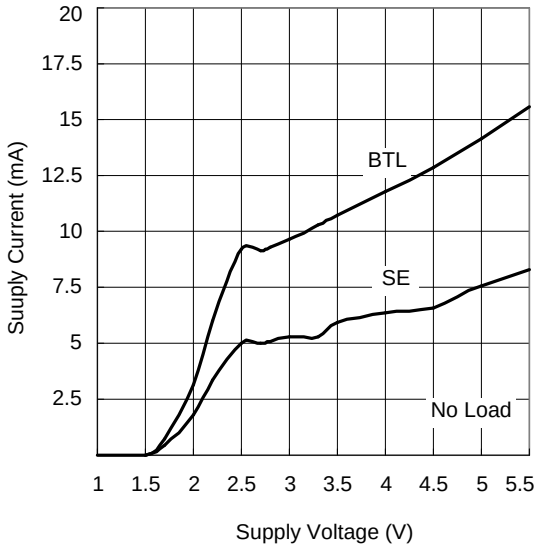

Copyright © ANPEC Electronics Corp.

## Typical Operating Characteristics (Cont.)

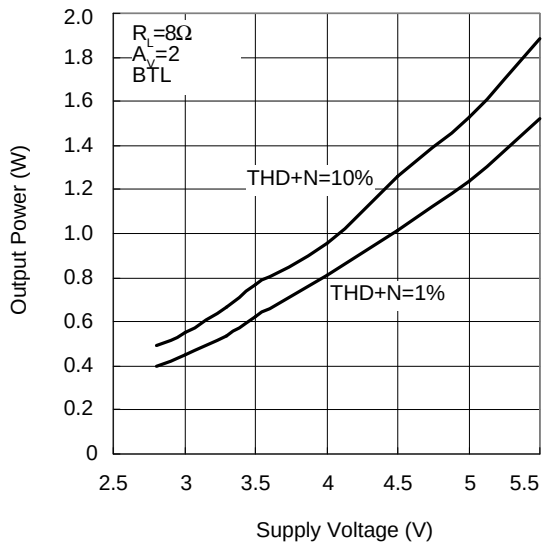
**Power Dissipation vs. Output Power**



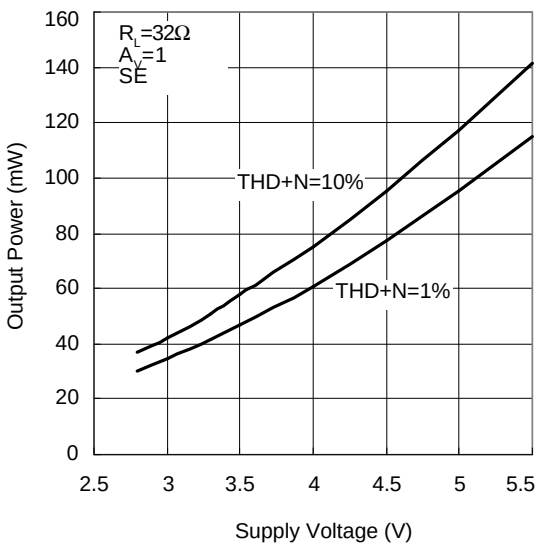

**Supply Current vs. Supply Voltage**




**Output Power vs. Supply Voltage**

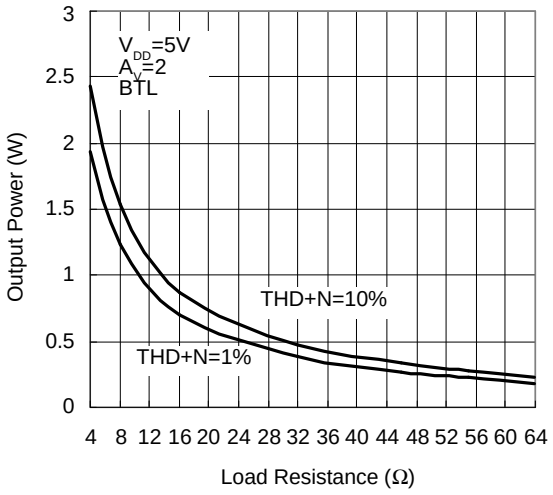



**Output Power vs. Supply Voltage**

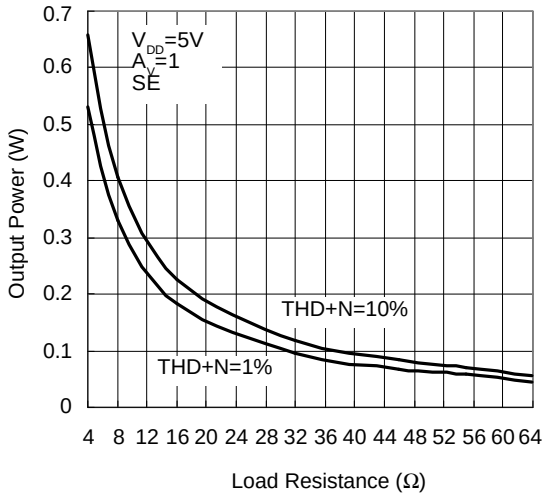


## Typical Operating Characteristics (Cont.)

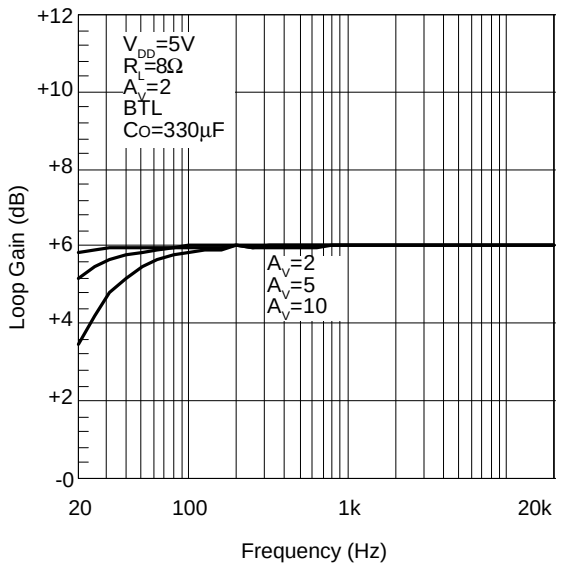
**Output Power vs. Load Resistance**



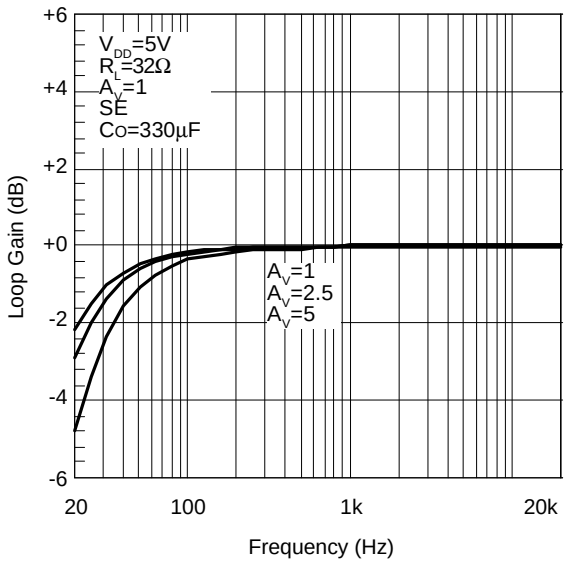

**Output Power vs. Load Resistance**



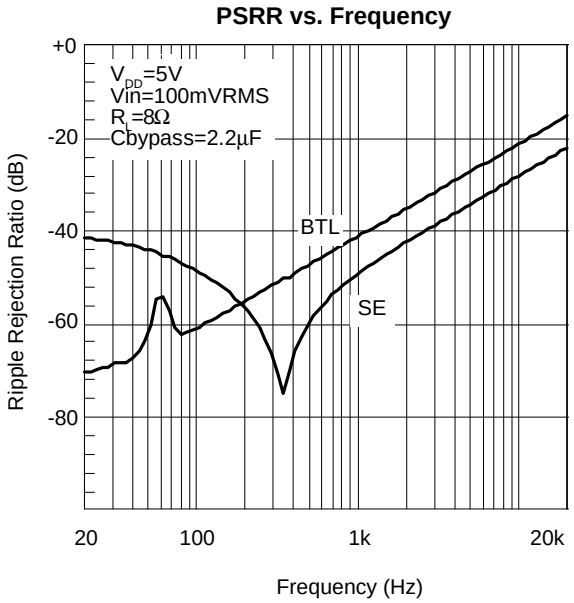

**Close Loop Response**




**Close Loop Response**



## Typical Operating Characteristics (Cont.)




## Pin Description

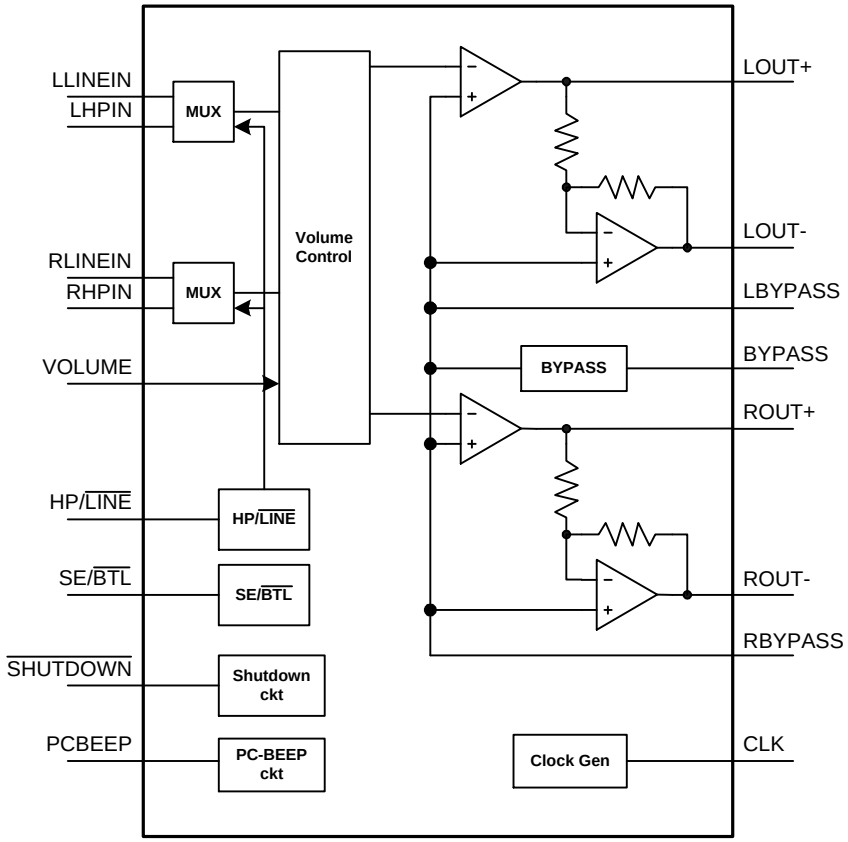
| PIN | | I/O/P | FUNCTION |
|---|---|---|---|
| NAME | NO. | | |
| GND | 1,12,13,24 | | Ground connection, Connected to the thermal pad. |
| PCBEN | 2 | I/P | BEEP mode control input, active H, for APA2120 only |
| HP/$\overline{\text{LINE}}$ | 2 | I/P | Multi-input selection input, headphone mode when held high, line-in mode when held low for APA2121 only. |
| VOLUME | 3 | | Input signal for internal volume gain setting. |
| LOUT+ | 4 | O/P | Left channel positive output in BTL mode and SE mode. |
| LLINEIN | 5 | I/P | Left channel line input terminal, selected when HP/$\overline{\text{LINE}}$ is held low. |
| LHPIN | 6 | O/P | Left channel headphone input terminal, selected when HP/$\overline{\text{LINE}}$ is held high. |
| PVDD | 7,18 | | Supply voltage only for power amplifier. |
| RBYPASS | 8 | I/P | Right channel bypass voltage. |
| LOUT- | 9 | O/P | Left channel negative output in BTL mode and high impedance in SE mode. |
| LBYPASS | 10 | I/P | Left channel bias voltage generator. |
| BYPASS | 11 | | Bias voltage generator |
| PC_BEEP | 14 | I/P | PCBEP signal input |
| SE/$\overline{\text{BTL}}$ | 15 | I/P | Output mode control input, high for SE output mode and low for BTL mode. |
| ROUT- | 16 | O/P | Right channel negative output in BTL mode and high impedance in SE mode. |
| CLK | 17 | | Clock signal generator |
| VDD | 19 | | Supply voltage for internal circuit excepting power amplifier. |

Copyright © ANPEC Electronics Corp.

## Pin Description (Cont.)

| PIN | | I/O/P | FUNCTION |
|---|---|---|---|
| NAME | NO. | | |
| RHPIN | 20 | I/P | Right channel headphone input terminal, selected when HP/$\overline{\text{LINE}}$ is held high. |
| ROUT+ | 21 | O/P | Right channel positive output in BTL mode and SE mode. |
| $\overline{\text{SHUTDOWN}}$ | 22 | I/P | It will be into shutdown mode when pull low. |
| RLINEIN | 23 | I/P | Right channel line input terminal, selected when HP/$\overline{\text{LINE}}$ is held low. |

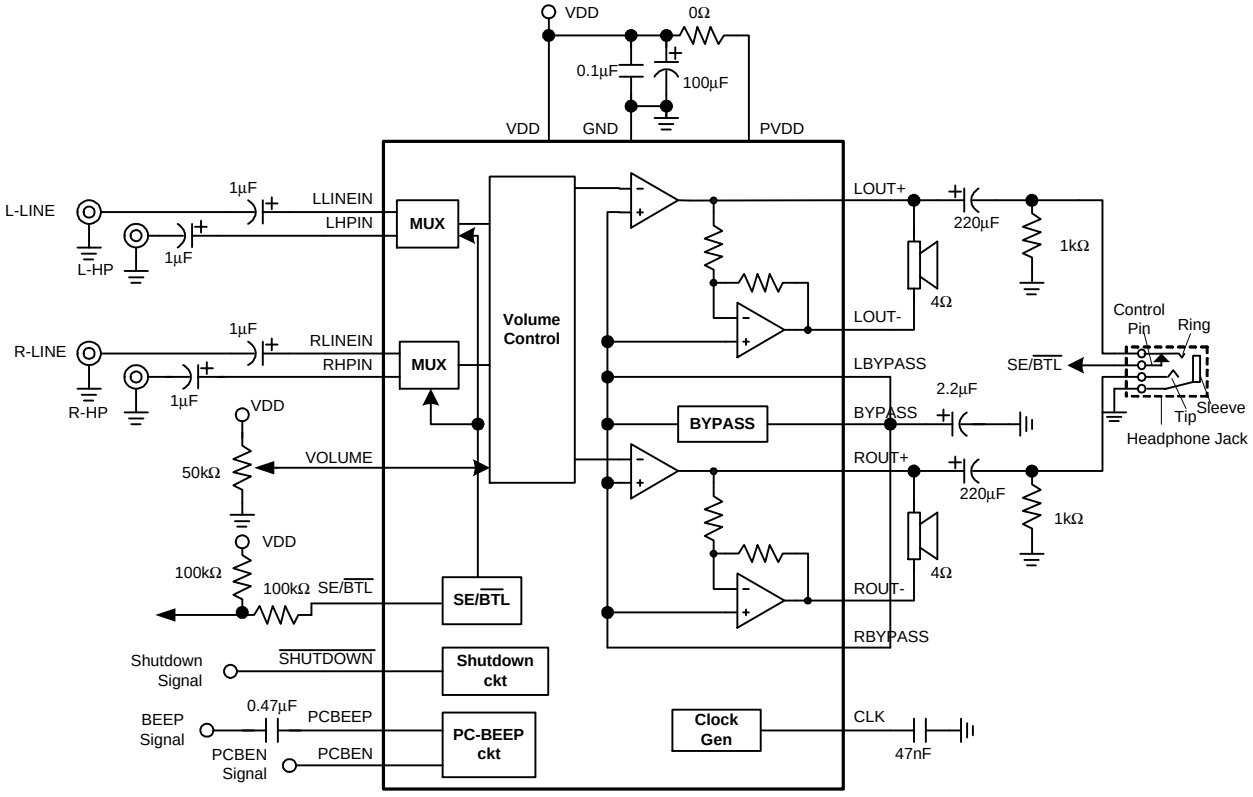
## Block Diagram




For APA2121

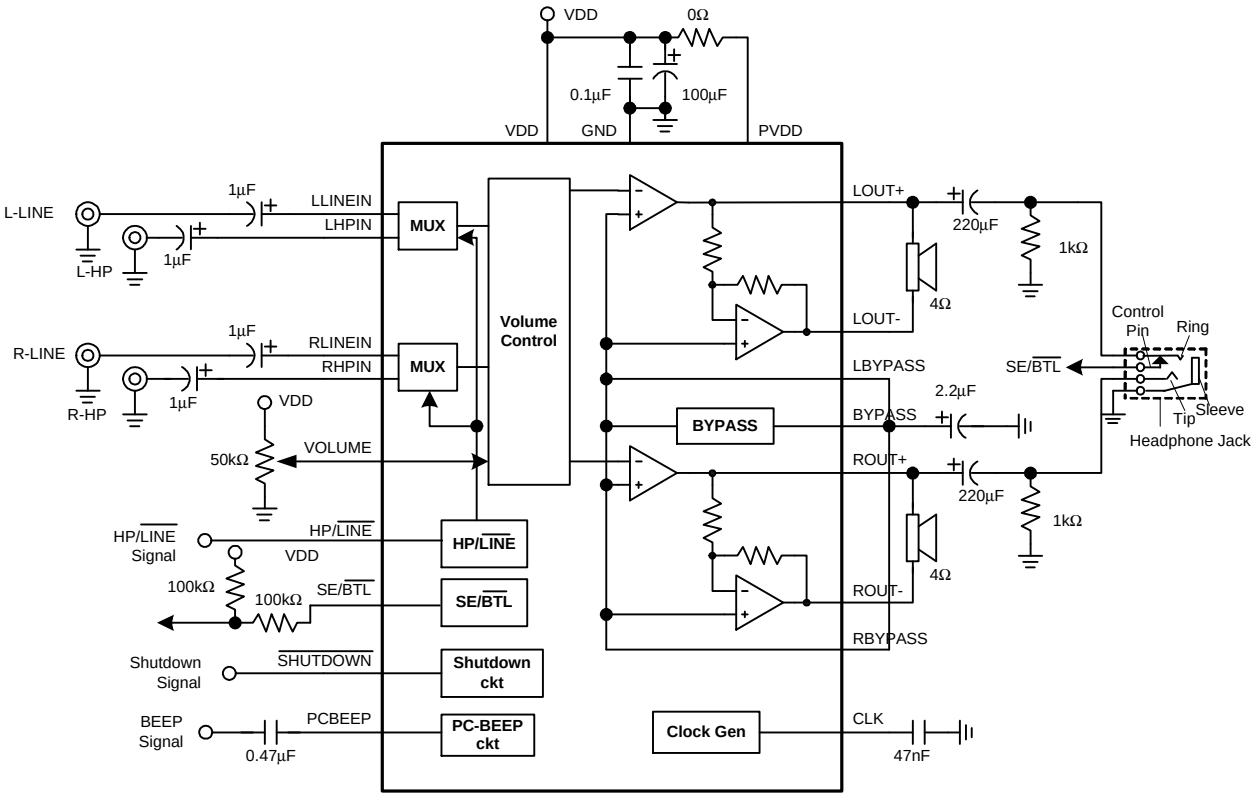
## Typical Application Circuits

APA2120



## Typical Application Circuits (Cont.)

APA2121




## Control Input Table

For APA2120

| $\overline{\text{SE/BTL}}$ | $\overline{\text{SHUTDOWN}}$ | PC-BEEP | Operating Mode |
|---|---|---|---|
| X | L | Disable | Shutdown mode |
| L | H | Disable | Line input, BTL out |
| H | H | Disable | HP input, SE out |
| X | X | Enable | PCBEEP input, BTL out |

For APA2121

| $\overline{\text{SE/BTL}}$ | $\overline{\text{HP/LINE}}$ | $\overline{\text{SHUTDOWN}}$ | PC-BEEP | Operating Mode |
|---|---|---|---|---|
| X | X | L | Disable | Shutdown mode |
| L | L | H | Disable | Line input, BTL out |
| L | H | H | Disable | HP input, BTL out |
| H | L | H | Disable | Line input, SE out |
| H | H | H | Disable | HP input, BTL out |
| X | X | X | Enable | PCBEEP input, BTL out |

## Volume Control Table_BTL Mode

Supply Voltage Vdd=5V

| Gain(dB) | High(V) | Low(V) | Hysteresis(mV) | Recommended Voltage(V) |
|---|---|---|---|---|
| 20 | 0.12 | 0.00 | | 0 |
| 18 | 0.23 | 0.17 | 52 | 0.20 |
| 16 | 0.34 | 0.28 | 51 | 0.31 |
| 14 | 0.46 | 0.39 | 50 | 0.43 |
| 12 | 0.57 | 0.51 | 49 | 0.54 |
| 10 | 0.69 | 0.62 | 47 | 0.65 |
| 8 | 0.80 | 0.73 | 46 | 0.77 |
| 6 | 0.91 | 0.84 | 45 | 0.88 |
| 4 | 1.03 | 0.96 | 44 | 0.99 |
| 2 | 1.14 | 1.07 | 43 | 1.10 |
| 0 | 1.25 | 1.18 | 41 | 1.22 |
| -2 | 1.37 | 1.29 | 40 | 1.33 |
| -4 | 1.48 | 1.41 | 39 | 1.44 |
| -6 | 1.59 | 1.52 | 38 | 1.56 |
| -8 | 1.71 | 1.63 | 37 | 1.67 |
| -10 | 1.82 | 1.74 | 35 | 1.78 |
| -12 | 1.93 | 1.85 | 34 | 1.89 |
| -14 | 2.05 | 1.97 | 33 | 2.01 |
| -16 | 2.16 | 2.08 | 32 | 2.12 |
| -18 | 2.28 | 2.19 | 30 | 2.23 |
| -20 | 2.39 | 2.30 | 29 | 2.35 |
| -22 | 2.50 | 2.42 | 28 | 2.46 |
| -24 | 2.62 | 2.53 | 27 | 2.57 |
| -26 | 2.73 | 2.64 | 26 | 2.69 |
| -28 | 2.84 | 2.75 | 24 | 2.80 |
| -30 | 2.96 | 2.87 | 23 | 2.91 |
| -32 | 3.07 | 2.98 | 22 | 3.02 |
| -34 | 3.18 | 3.09 | 21 | 3.14 |
| -36 | 3.30 | 3.20 | 20 | 3.25 |
| -38 | 3.41 | 3.32 | 18 | 3.36 |
| -40 | 3.52 | 3.43 | 17 | 3.48 |
| -80 | 5.00 | 3.54 | 16 | 5 |

Copyright © ANPEC Electronics Corp.

## Application Information

### BTL Operation

The APA2120/1 output stage (power amplifier) has two pairs of operational amplifiers internally, allowed for different amplifier configurations.

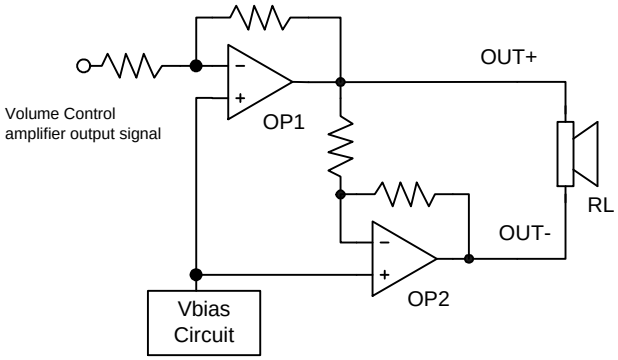



Figure 1 : APA2120/1 Internal Configuration.
(each channel)

The power amplifier's OP1 gain is setting by internal unity-gain and the input audio signal comes from the internal volume control amplifier while the second amplifier OP2 is internally fixed in a unity-gain, inverting configuration. Figure 1 shows that the output of OP1 is connected to the input to OP2, which results in the output signals of both amplifiers with identical in magnitude, but out of phase 180°. Consequently, the differential gain for each channel is 2 x (Gain of SE mode).

By driving the load differentially through outputs OUT+ and OUT-, an amplifier configuration commonly referred to bridged mode is established. The BTL mode operation is different from the classical single-ended SE amplifier configuration where one side of its load is connected to the ground.

A BTL amplifier design has a few distinct advantages over the SE configuration, as it provides differential drive to the load, thus doubling the output swing for a specified supply voltage.

When placed under the same conditions, a BTL amplifier has four times the output power of a SE amplifier. A BTL configuration, such as the one used in APA2120/1, also creates a second advantage over SE amplifiers. Since the differential outputs, ROUT+, ROUT-, LOUT+, and LOUT-, are biased at half-supply, it's not necessary for DC voltage to be across the load. This eliminates the need for an output coupling capacitor which is required in a single supply, SE configuration.

### Single-Ended Operation

Consider the single-supply SE configuration shown Application Circuit. A coupling capacitor is required to block the DC offset voltage from reaching the load. These capacitors can be quite large (approximately 33µF to 1000µF) so they tend to be expensive, occupied valuable PCB area, and have the additional drawback of limiting low-frequency performance of the system (refer to the Output Coupling Capacitor).The rules described still hold with the addition of the following relationship:

$$\frac{1}{Cbypass \times 125k\Omega} \leq \frac{1}{RiCi} << \frac{1}{R_L C_C} \qquad (1)$$

### Output $\overline{SE/BTL}$ Operation

The best cost saving feature of APA2120/1 is that they can be switched easily between BTL and SE modes. This feature eliminates the requirement for an additional headphone amplifier in applications where internal stereo speakers are driven in the BTL mode but external headphone or speakers must be accommodated.

Internal to the APA2120/1, two separate amplifiers drive OUT+ and OUT- (see Figure 1). The $\overline{SE/BTL}$ input controls the operation of the follower amplifier that drives LOUT- and ROUT-.

- When $\overline{SE/BTL}$ is held low, the OP2 is turned on and the APA2120/1 is in the BTL mode.
- When $\overline{SE/BTL}$ is held high, the OP2 is in a high output impedance state, which configures the APA2120/1 as SE driver from OUT+. $I_{DD}$ is reduced by approximately one-half in SE mode.

The control of the $\overline{SE/BTL}$ input can be a logic-level TTL source, a resistor divider network, or the stereo headphone jack with switch pin as shown in the Application Circuit.

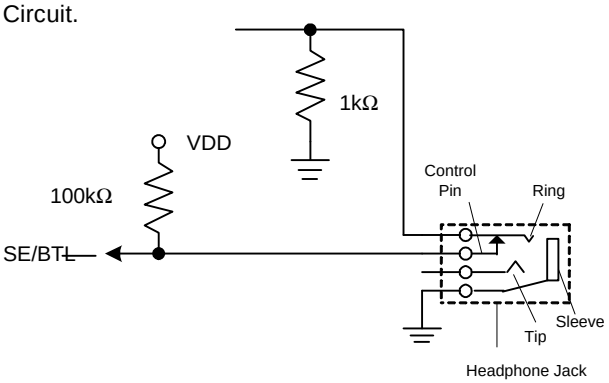



Figure 2 : SE/BTL Input Selection by Phonejack Plug.

## Application Information (Cont.)

**Output SE/$\overline{BTL}$ Operation (Cont.)**

In Figure 2, input SE/$\overline{BTL}$ operates as below :

When the phonejack plug is inserted, the 1kΩ resistor is disconnected and the SE/$\overline{BTL}$ input is pulled high and enables the SE mode. When the input goes to a high level, the OUT- amplifier is shutdown which causes the speaker to mute. Then, the OUT+ amplifier drives through the output capacitor ($C_C$) into the headphone jack. When there is no headphone plugged into the system, the contact pin of the headphone jack is connected from the signal pin, and the voltage divider set up by resistors 100kΩ and 1kΩ. Resistor 1kΩ then pulls low the SE/$\overline{BTL}$ pin, enabling the BTL function.

**Volume Control Function**

APA2120/1 have an internal stereo volume control that setting is the function of the DC voltage applied to the VOLUME input pin. The APA2120/1 volume control consists of 32 steps that are individually selected by a variable DC voltage level on the VOLUME control pin. The range of the steps, controlled by the DC voltage, are from 20dB to -80dB. Each gain step corresponds to a specific input voltage range as shown in table. To minimize the effect of noise on the volume control pin, which can affect the selected gain level, hysteresis and clock delay are implemented. The amount of hysteresis corresponds to half of the step width is shown in the volume control graph.

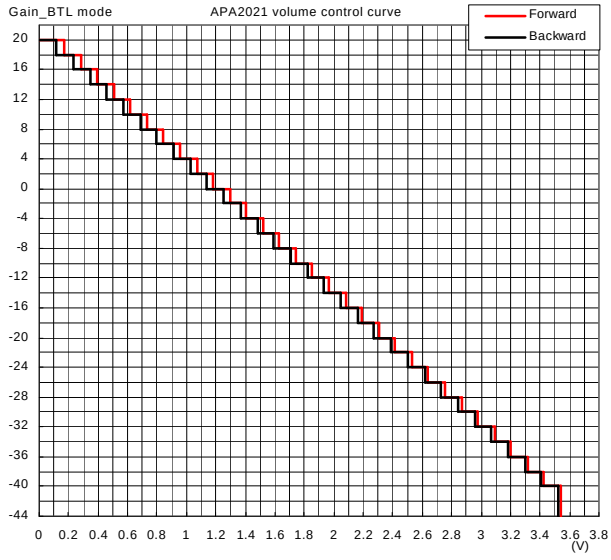



Figure 3 : Gain setting vs VOLUME Pin Voltage.

For the highest accuracy, the voltage is shown in the 'recommended voltage' column of the table and used to select a desired gain. This recommended voltage is exactly halfway between the two nearest transitions. The gain levels are 2dB/step from 20dB to -40dB in BTL mode, and the last step at -80dB as mute mode.

**Input Resistance, Ri**

The gain for each audio input of the APA2120/1 is set by the internal resistors (Ri and Rf) of volume control amplifier in inverting configuration.

$$\text{SE Gain} = A_V = -\frac{R_F}{Ri} \quad (2)$$

$$\text{BTL Gain} = -2 \times \frac{R_F}{Ri} \quad (3)$$

BTL mode operation brings the factor of 2 in the gain equation due to the inverting amplifier mirroring the voltage swing across the load. For the varying gain setting, APA2120/1 generate each input resistance on the figure 4. The input resistance will affect the low frequency performance of audio signal. The minmum input resistance is 10kΩ when gain setting is 20dB, and the resistance will ramp up when close loop gain below 20dB. The input resistance has wide variation (+/-10%) caused by the process variation.

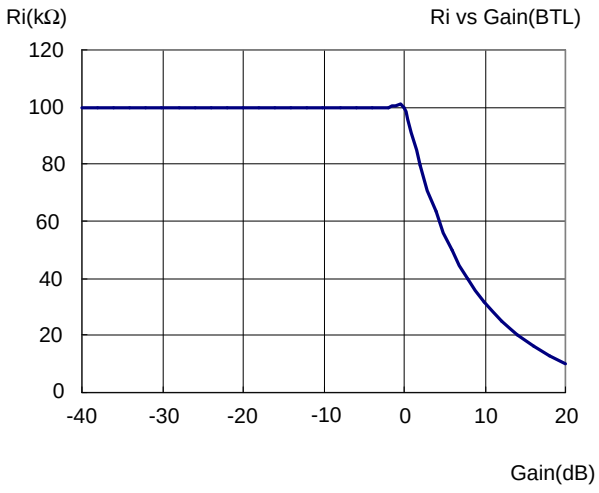



Figure 4: Input Resistance vs Gain Setting.

## Application Information (Cont.)

**Input Capacitor, Ci**

In the typical application, an input capacitor, Ci, is required to allow the amplifier to bias the input signal to the proper DC level for optimum operation. In this case, Ci and the minimum input impedance Ri (10kΩ) form a high-pass filter with the corner frequency determined in the following equation :

$$F_C(\text{highpass}) = \frac{1}{2\pi x 10k\Omega x Ci} \quad (4)$$

The value of Ci is important to consider as it directly affects the low frequency performance of the circuit. Consider the example where Ri is 10kΩ and the specification calls for a flat bass response down to 100Hz. Equation is reconfigured as below :

$$Ci = \frac{1}{2\pi x 10k\Omega x f_C} \quad (5)$$

When the input resistance variation is considered, the Ci is 0.16μF. Therefore, a value in the range of 0.22μF to 1.0μF would be chosen.

A further consideration for this capacitor is the leakage path from the input source through the input network (Ri+Rf, Ci) to the load. This leakage current creates a DC offset voltage at the input to the amplifier that reduces useful headroom, especially in high gain applications. For this reason, a low-leakage tantalum or ceramic capacitor is the best choice. When polarized capacitors are used, the positive side of the capacitor should face the amplifier input in most applications as the DC level there is held at $V_{DD}/2$, which is likely higher than the source DC level. Please note that it is important to confirm the capacitor polarity in the application.

**Effective Bypass Capacitor, Cbypass**

As other power amplifiers, proper supply bypassing is critical for low noise performance and high power supply rejection.

The capacitors located on both the bypass and power supply pins should be as close to the device as possible. The effect of a larger bypass capacitor will improve PSRR due to increased supply stability. Typical applications employ a 5V regulator with 1.0μF and a 0.1μF bypass capacitor as supply filtering. This does not eliminate the need for bypassing the supply nodes of the APA2120/1. The selection of bypass capacitors, especially Cbypass, is thus dependent upon desired PSRR requirements, click and pop performance.

On the chip, there are three bypass pins for used, and they are tied together in the internal circuit.

The effective capacitance is the Cbypass=(Cb//CLbyasss/ /CRbypass). When absolute minimum cost and/or component space is required, one bypass capacitor can be used.

To avoid the start-up pop noise, the bypass voltage should rise slower than the input bias voltage and the relationship shown in equation (6) should be maintained.

$$\frac{1}{Cbypass \times 125k\Omega} << \frac{1}{100k\Omega \times Ci} \quad (6)$$

The bypass capacitor is fed from a 125kΩ resistor inside the amplifier and the 100kΩ is maximum input resistance of (Ri+ Rf). Bypass capacitor, Cb, values of 3.3μF to 10μF ceramic or tantalum low-ESR capacitors are recommended for the best THD and noise performance.

The bypass capacitance also effects to the start up time. It is determined in the following equation :

$$Tstart\ up = 5 \times (Cbypass \times 125k\Omega) \quad (7)$$

**Output Coupling Capacitor, Cc**

In the typical single-supply SE configuration, an output coupling capacitor (Cc) is required to block the DC bias at the output of the amplifier thus preventing DC currents in the load. As with the input coupling capacitor, the output coupling capacitor and impedance of the load form a high-pass filter governed by the following equation:

$$F_C(\text{highpass}) = \frac{1}{2\pi R_L C_C} \quad (8)$$

For example, a 330μF capacitor with an 8Ω speaker would attenuate low frequencies below 60.6Hz. The main disadvantage of performance is that the load impedance is typically small, which drives the low-frequency corner higher degrading the bass response. Large values of $C_C$ are required to pass low frequencies into the load.

Copyright © ANPEC Electronics Corp.

## Application Information (Cont.)

**Power Supply Decoupling, Cs**

The APA2120/1 provide $PV_{DD}$ and $V_{DD}$ two independent power inputs for used. $PV_{DD}$ is used for power amplifier only and $V_{DD}$ is used for volume control amplifier and internal circuit excepting power amplifier. The APA2120/1 are high-performance CMOS audio amplifiers that requires adequate power supply decoupling to ensure the output total harmonic distortion (THD) is as low as possible. Power supply decoupling also prevents the oscillations being caused by long lead length between the amplifier and the speaker. The optimum decoupling is achieved by using two different types of capacitors that target on different noise on the power supply leads.

For higher frequency transients, spikes, or digital hash on the line, a good low equivalent-series-resistance(ESR) ceramic capacitor, typically 0.1µF placed as close as possible to the device $V_{DD}$ and $PV_{DD}$ lead works the best. For filtering lower-frequency noise signals, a large aluminum electrolytic capacitor of 10µF or greater placed near the audio power amplifier is recommended.

**Optimizing Depop Circuitry**

Circuitry has been included in the APA2120/1 to minimize the amount of popping noise at power-up and when coming out of shutdown mode. Popping occurs whenever a voltage step is applied to the speaker. In order to eliminate clicks and pops, all capacitors must be fully discharged before turn-on. Rapid on/off switching of the device or the shutdown function will cause the click and pop circuitry.

The value of Ci will also affect turn-on pops. (Refer to Effective Bypass Capacitance) The bypass voltage should rises slower than input bias voltage. Although the bypass pin current source cannot be modified, the size of Cbypass can be changed to alter the device turn-on time and the amount of clicks and pops. By increasing the value of Cbypass, turn-on pop can be reduced. However, the tradeoff for using a larger bypass capacitor is to increase the turn-on time for this device. There is a linear relationship between the size of Cbypass and the turn-on time. In a SE configuration, the output coupling capacitor, $C_C$, is of particular concern.

This capacitor discharges through the internal 10kΩ resistors. Depending on the size of $C_C$, the time constant can be relatively large. To reduce transients in SE mode, an external 1kΩ resistor can be placed in parallel with the internal 10kΩ resistor. The tradeoff for using this resistor is an increase in quiescent current. In most cases, choosing a small value of Ci in the range of 0.33µF to 1µF, Cb being equal to 4.7µF and an external 1kΩ resistor should be placed in parallel, and the internal 10kΩ resistor should produce a virtually clickless and popless turn-on.

A high gain amplifier intensifies the problem as the small delta in voltage is multiplied by the gain. So it is advantageous to use low-gain configurations.

**Shutdown Function**

In order to reduce power consumption while not in use, the APA2120/1 contain a shutdown pin to externally turn off the amplifier bias circuitry. This shutdown feature turns the amplifier off when a logic low is placed on the $\overline{\text{SHUTDOWN}}$ pin. The trigger point between a logic high and logic low level is typically 2.0V. It is best to switch between the ground and the supply $V_{DD}$ to provide maximum device performance.

By switching the $\overline{\text{SHUTDOWN}}$ pin to low, the amplifier enters a low-current state, $I_{DD}$<50µA. APA2120/1 is in shutdown mode, except PC-BEEP detect circuit. Under normal operation, $\overline{\text{SHUTDOWN}}$ pin pulls to high level to keep the IC out of the shutdown mode. The $\overline{\text{SHUTDOWN}}$ pin should be tied to a definite voltage to avoid unwanted state changing.

**Input HP/$\overline{\text{LINE}}$ Operation**

APA2120/1 amplifiers have two separate inputs for each of the left and right stereo channels. The APA2120 and APA2121 have different control input by SE/$\overline{\text{BTL}}$ and HP/$\overline{\text{LINE}}$, respectively.

APA2120 internal multiplexor is selected by SE/$\overline{\text{BTL}}$ control input. Refer to the 'Output SE/$\overline{\text{BTL}}$ Operation', the voltage divider of 100kΩ and 1kΩ sets the voltage at the SE/$\overline{\text{BTL}}$ pin to be approximately 50mV when no phonejack plugged into the system.

Copyright © ANPEC Electronics Corp.

## Application Information (Cont.)

**Input HP/$\overline{\text{LINE}}$ Operation (Cont.)**

This logic-low voltage at the SE/$\overline{\text{BTL}}$ pin makes APA2120 into LINE input mode operation. It becomes HP input mode when phonejack plugged.

An internal multiplexor selects the input to connect to the amplifier based on the state of the HP/$\overline{\text{LINE}}$ pin of the APA2121.

- To select the LINE inputs, set HP/$\overline{\text{LINE}}$ pin to a low level.
- To enable the HP(headphone) inputs, set HP/$\overline{\text{LINE}}$ pin to a high level.

As APA2121, HP/$\overline{\text{LINE}}$ input multiplexor and SE/$\overline{\text{BTL}}$ output operating mode have independent control paths, which can be used for multiple audio input system. This function will be the same as APA2120 when HP/$\overline{\text{LINE}}$ and SE/$\overline{\text{BTL}}$ are tied together.

**PC-BEEP Detection**

APA2120/1 integrate a BEEP detect circuit for NOTEBOOK PC. When BEEP signal is provided on the PCBEEP input pin, the BEEP mode is active. APA2120/1 will force to BTL mode and the internal gain is fixed at -10dB. The PCBEEP signal becomes the amplifier input signal and plays on the speaker without coupling capacitor. It will be out of shutdown mode whenever BEEP mode is enabled. APA2120/1 will return to previous setting when it is out of BEEP mode. The input impedance is 100kΩ on the PCBEEP input pin.

APA2120 provide extra PCBEN control input signal to force IC into BEEP mode. The BEEP mode will be enabled when PCBEN goes to a high level. When the BEEP mode is overridden, the signal from the PCBEEP will pass to speaker directly.

**Clock Generator**

APA2120/1 integrate a clock block to avoid volume control function abnormal when VOLUME control signal with spike or noise. APA2120/1 change each step of volume gain after four clock cycles make sure control signal ready. It provides 130kHz frequency if no capacitor is placed on CLK pin to the ground. The larger capacitance will slow down the and clock frequency. A capacitor 33nF between CLK to the ground and will generate 147Hz frequency on the CLK pin.

**BTL Amplifier Efficiency**

An easy-to-use equation to calculate efficiency starts out as being equal to the ratio of power from the power supply to the power delivered to the load.

The following equations are the basis for calculating amplifier efficiency.

$$\text{Efficiency} = \frac{P_O}{P_{SUP}} \quad (9)$$

Where :

$$P_O = \frac{V_{ORMS} \times V_{ORMS}}{RL} = \frac{V_P \times V_P}{2RL}$$

$$V_{ORMS} = \frac{V_P}{\sqrt{2}} \quad (10)$$

$$P_{SUP} = V_{DD} \times I_{DDAVG} = V_{DD} \times \frac{2V_P}{\pi R_L} \quad (11)$$

Table 1 Calculates Efficiencies for Four Different Output Power Levels.

Note that the efficiency of the amplifier is quite low for lower power levels and rises sharply as power to the load is increased resulting in a nearly flat internal power dissipation over the normal operating range. Note that the internal dissipation at full output power is less than the dissipation in the half power range. Calculating the efficiency for a specific system is the key to proper power supply design. For a stereo 1W audio system with 8Ω loads and a 5V supply, the maximum draw on the power supply is almost 3W.

A final point to remember about linear amplifiers (either SE or BTL) is how to manipulate the terms in the efficiency equation to an utmost advantage when possible. Note that in equation, $V_{DD}$ is in the denominator. This indicates that as $V_{DD}$ goes down, efficiency goes up. In other words, use the efficiency analysis to choose the correct supply voltage and speaker impedance for the application.

| Po (W) | Efficiency (%) | $I_{DD}$(A) | $V_{PP}$(V) | $P_D$ (W) |
|---|---|---|---|---|
| 0.25 | 31.25 | 0.16 | 2.00 | 0.55 |
| 0.50 | 47.62 | 0.21 | 2.83 | 0.55 |
| 1.00 | 66.67 | 0.30 | 4.00 | 0.5 |
| 1.25 | 78.13 | 0.32 | 4.47 | 0.35 |

**High peak voltages cause the THD to increase.

Table 1. Efficiency Vs Output Power in 5-V/8Ω BTL Systems

## Application Information (Cont.)

**Power Dissipation**

Whether the power amplifier is operated in BTL or SE modes, power dissipation is a major concern. Equation13 states the maximum power dissipation point for a SE mode operating at a given supply voltage and driving a specified load.

$$\text{SE mode : } P_{D,MAX}=\frac{V_{DD}^2}{2\pi^2 R_L} \quad (13)$$

In BTL mode operation, the output voltage swing is doubled as in SE mode. Thus, the maximum power dissipation point for a BTL mode operating at the same given conditions is 4 times as in SE mode.

$$\text{BTL mode : } P_{D,MAX}=\frac{4V_{DD}^2}{2\pi^2 R_L} \quad (14)$$

Since the APA2120/1 are dual channel power amplifiers, the maximum internal power dissipation is 2 times that both of equations depend on the mode of operation. Even this substantial increase in power dissipation, the APA2120/1 do not require extra heatsink. The power dissipation from equation14, assuming a 5V-power supply and an 8Ω load, must not be greater than the power dissipation that results from the equation15 :

$$P_{D,MAX}=\frac{T_{J,MAX}-T_A}{\theta_{JA}} \quad (15)$$

For TSSOP-24 package with thermal pad, the thermal resistance ($\theta_{JA}$) is equal to 45°C/W.

Since the maximum junction temperature ($T_{J,MAX}$) of APA2120/1 are 150°C and the ambient temperature ($T_A$) are defined by the power system design, the maximum power dissipation which the IC package is able to handle can be obtained from equation16.

Once the power dissipation is greater than the maximum limit ($P_{D,MAX}$), either the supply voltage ($V_{DD}$) must be decreased, the load impedance ($R_L$) must be increased or the ambient temperature should be reduced.

**Thermal Pad Consideration**

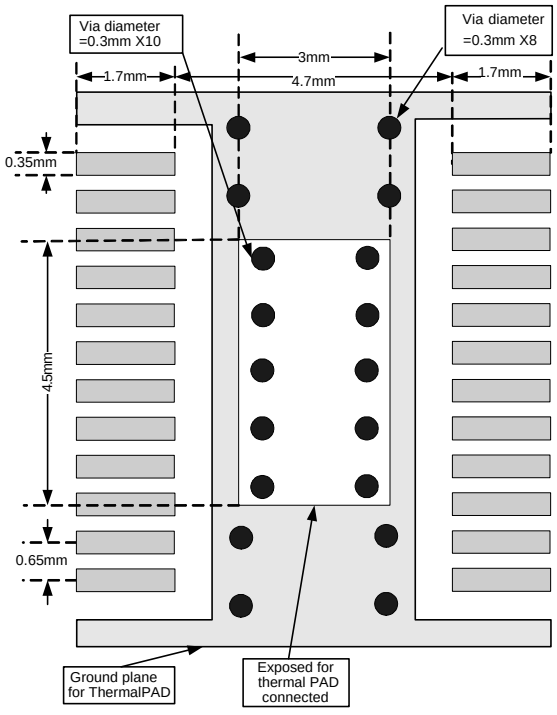
The thermal pad must be connected to the ground. The package with thermal pad of the APA2120/1 require special attention on thermal design. If the thermal design issues are not properly addressed, the APA2120/1 4Ω will go into thermal shutdown when driving a 4Ω load.

The thermal pad on the bottom of the APA2120/1 should be soldered down to a copper pad on the circuit board. Heat can be conducted away from the thermal pad through the copper plane to ambient. If the copper plane is not on the top surface of the circuit board, 8 to 10 vias of 13 mil or smaller in diameter should be used to thermally couple the thermal pad to the bottom plane.

For good thermal conduction, the vias must be plated through and solder filled. The copper plane used to conduct heat away from the thermal pad should be as large as practical.

If the ambient temperature is higher than 25°C, a larger copper plane or forced-air cooling will be required to keep the APA2120/1 junction temperature below the thermal shutdown temperature (150°C). In higher ambient temperature, higher airflow rate and/or larger copper area will be required to keep the IC out of the thermal shutdown.

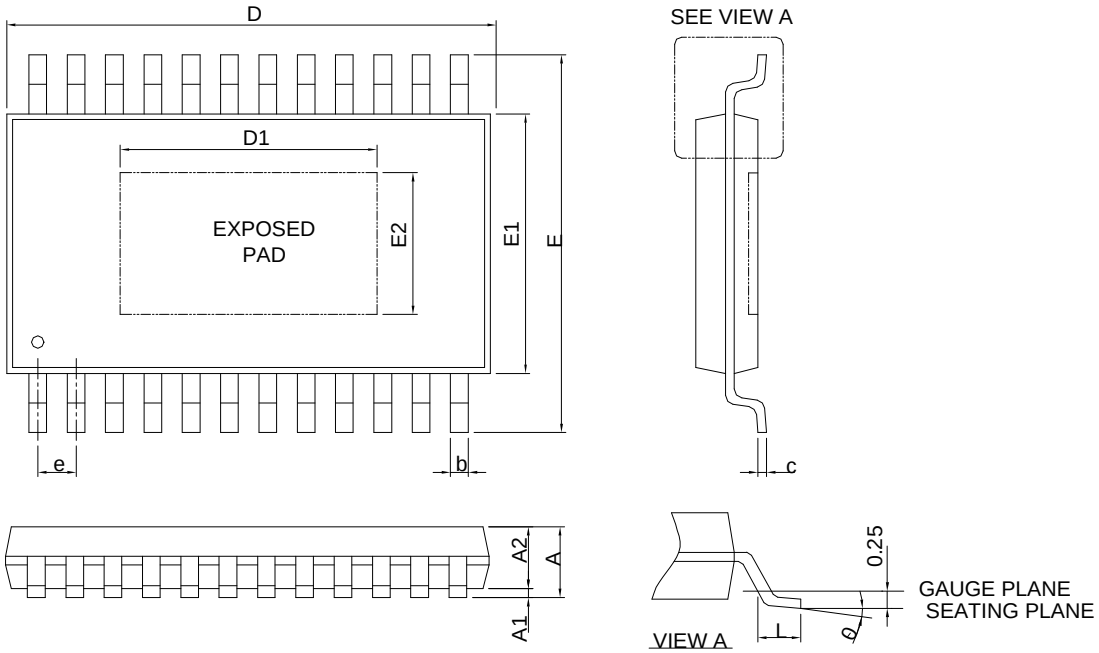
**Recommended Minmum Footprint**




TSSOP-24P

## Package Information

**TSSOP-24P**

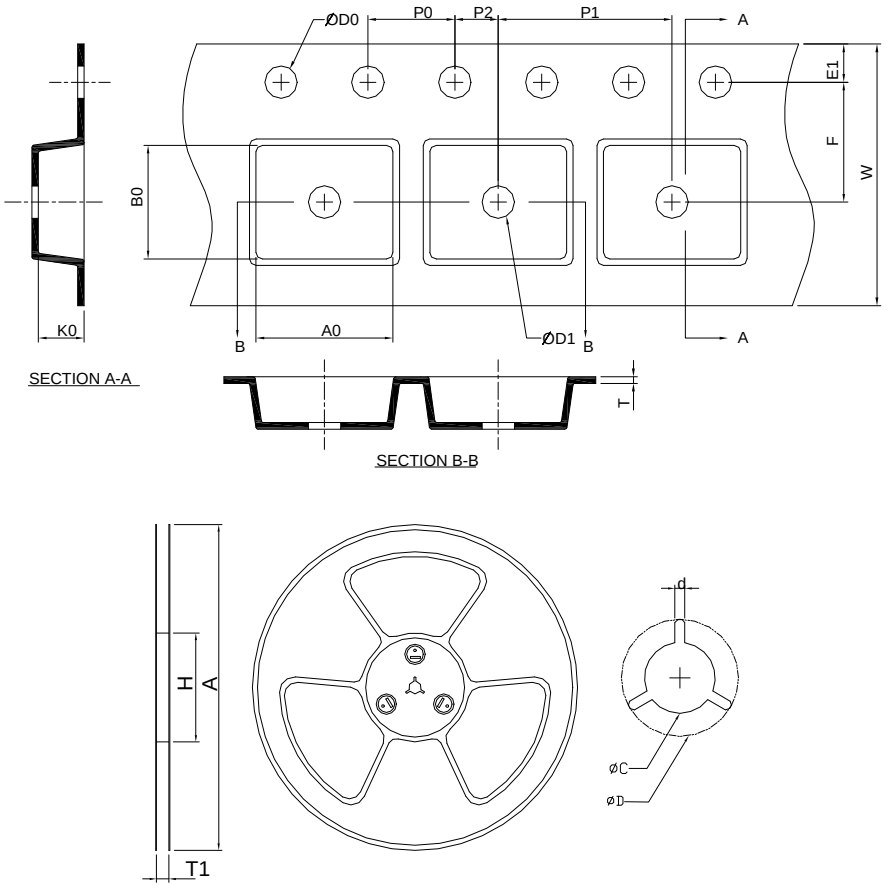



| SYMBOL | TSSOP-24P | | | |
|---|---|---|---|---|
| | MILLIMETERS | | INCHES | |
| | MIN. | MAX. | MIN. | MAX. |
| A | | 1.20 | | 0.047 |
| A1 | 0.05 | 0.15 | 0.002 | 0.006 |
| A2 | 0.80 | 1.05 | 0.031 | 0.041 |
| b | 0.19 | 0.30 | 0.007 | 0.012 |
| c | 0.09 | 0.20 | 0.004 | 0.008 |
| D | 7.70 | 7.90 | 0.303 | 0.311 |
| D1 | 3.50 | 5.00 | 0.138 | 0.197 |
| E | 6.20 | 6.60 | 0.244 | 0.260 |
| E1 | 4.30 | 4.50 | 0.169 | 0.177 |
| E2 | 2.50 | 3.50 | 0.098 | 0.138 |
| e | 0.65 BSC | | 0.026 BSC | |
| L | 0.45 | 0.75 | 0.018 | 0.030 |
| θ | 0° | 8° | 0° | 8° |

Note : 1. Followed from JEDEC MO-153 ADT.
2. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion or gate burrs shall not exceed 6 mil per side.
3. Dimension "E1" does not include inter-lead flash or protrusions. Inter-lead flash and protrusions shall not exceed 10 mil per side.

Copyright © ANPEC Electronics Corp.

## Carrier Tape & Reel Dimensions




| Application | A | H | T1 | C | d | D | W | E1 | F |
|---|---|---|---|---|---|---|---|---|---|
| TSSOP-24P | 330.0±2.00 | 50 MIN. | 16.4+2.00 -0.00 | 13.0+0.50 -0.20 | 1.5 MIN. | 20.2 MIN. | 16.0±0.30 | 1.75±0.10 | 7.50±0.10 |
| | **P0** | **P1** | **P2** | **D0** | **D1** | **T** | **A0** | **B0** | **K0** |
| | 4.00±0.10 | 8.00±0.10 | 2.00±0.10 | 1.5+0.10 -0.00 | 1.5 MIN. | 0.6+0.00 -0.40 | 6.9±0.20 | 8.30.±0.20 | 1.50±0.20 |

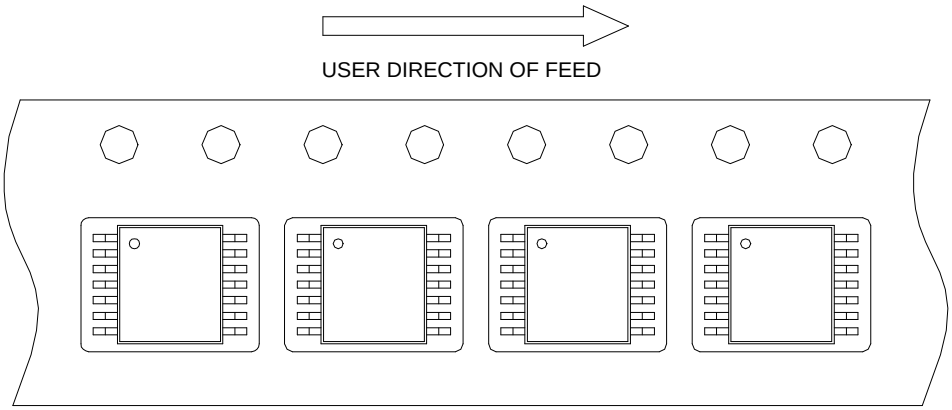
(mm)

## Devices Per Unit

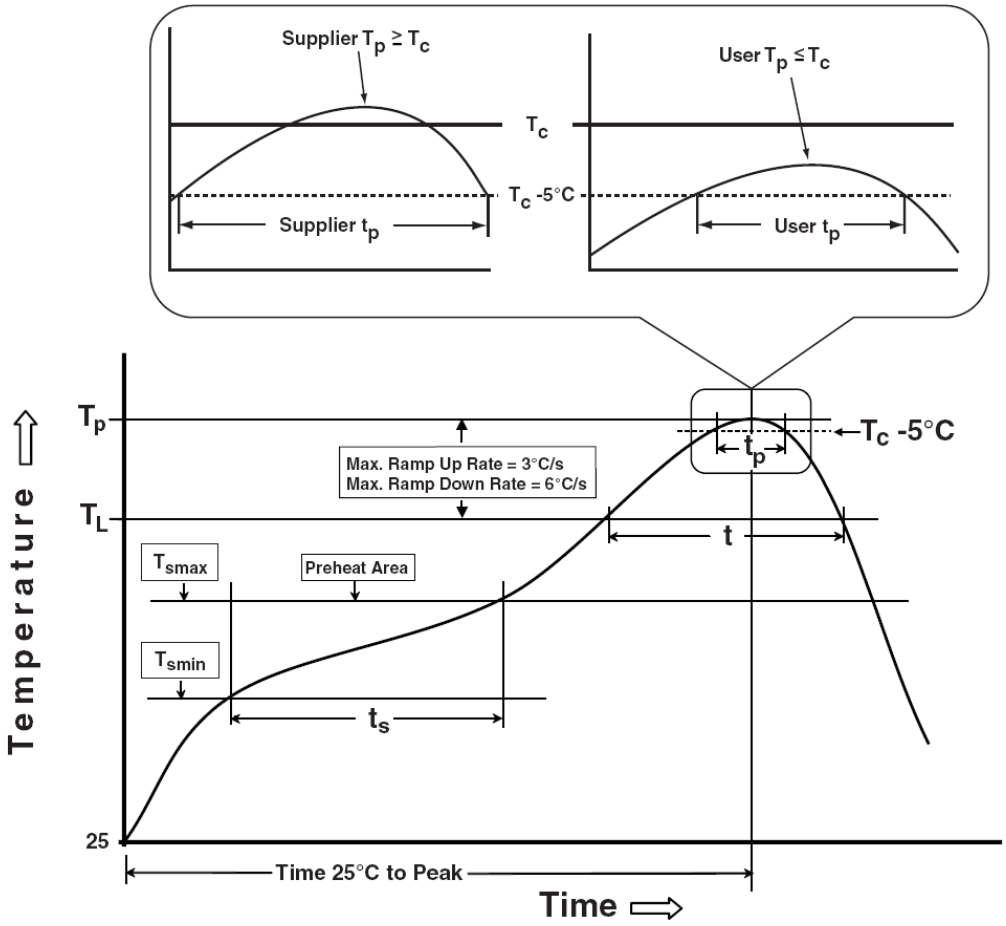
| Package Type | Unit | Quantity |
|---|---|---|
| **TSSOP-24P** | Tape & Reel | 2000 |

## Taping Direction Information

**TSSOP-24P**




## Classification Profile



## Classification Reflow Profiles

| Profile Feature | Sn-Pb Eutectic Assembly | Pb-Free Assembly |
|---|---|---|
| **Preheat & Soak**<br>Temperature min ($T_{smin}$)<br>Temperature max ($T_{smax}$)<br>Time ($T_{smin}$ to $T_{smax}$) ($t_s$) | <br>100 °C<br>150 °C<br>60-120 seconds | <br>150 °C<br>200 °C<br>60-120 seconds |
| Average ramp-up rate ($T_{smax}$ to $T_P$) | 3 °C/second max. | 3°C/second max. |
| Liquidous temperature ($T_L$)<br>Time at liquidous ($t_L$) | 183 °C<br>60-150 seconds | 217 °C<br>60-150 seconds |
| Peak package body Temperature ($T_p$)* | See Classification Temp in table 1 | See Classification Temp in table 2 |
| Time ($t_P$)** within 5°C of the specified classification temperature ($T_c$) | 20** seconds | 30** seconds |
| Average ramp-down rate ($T_p$ to $T_{smax}$) | 6 °C/second max. | 6 °C/second max. |
| Time 25°C to peak temperature | 6 minutes max. | 8 minutes max. |
| * Tolerance for peak profile Temperature ($T_p$) is defined as a supplier minimum and a user maximum.<br>** Tolerance for time at peak profile temperature ($t_p$) is defined as a supplier minimum and a user maximum. | | |

Table 1. SnPb Eutectic Process – Classification Temperatures (Tc)

| Package Thickness | Volume $mm^3$ <350 | Volume $mm^3$ ³350 |
|---|---|---|
| <2.5 mm | 235 °C | 220 °C |
| ≥2.5 mm | 220 °C | 220 °C |

Table 2. Pb-free Process – Classification Temperatures (Tc)

| Package Thickness | Volume $mm^3$ <350 | Volume $mm^3$ 350-2000 | Volume $mm^3$ >2000 |
|---|---|---|---|
| <1.6 mm | 260 °C | 260 °C | 260 °C |
| 1.6 mm – 2.5 mm | 260 °C | 250 °C | 245 °C |
| ≥2.5 mm | 250 °C | 245 °C | 245 °C |

## Reliability Test Program

| Test item | Method | Description |
|---|---|---|
| SOLDERABILITY | JESD-22, B102 | 5 Sec, 245°C |
| HOLT | JESD-22, A108 | 1000 Hrs, Bias @ 125°C |
| PCT | JESD-22, A102 | 168 Hrs, 100%RH, 2atm, 121°C |
| TCT | JESD-22, A104 | 500 Cycles, -65°C~150°C |
| HBM | MIL-STD-883-3015.7 | VHBM≧2KV |
| MM | JESD-22, A115 | VMM≧200V |
| Latch-Up | JESD 78 | 10ms, $1_{tr}$≧100mA |

Copyright © ANPEC Electronics Corp.

## Customer Service

**Anpec Electronics Corp.**
Head Office :
No.6, Dusing 1st Road, SBIP,
Hsin-Chu, Taiwan
Tel : 886-3-5642000
Fax : 886-3-5642050

Taipei Branch :
2F, No. 11, Lane 218, Sec 2 Jhongsing Rd.,
Sindian City, Taipei County 23146, Taiwan
Tel : 886-2-2910-3838
Fax : 886-2-2917-3838